TGA2599-SM

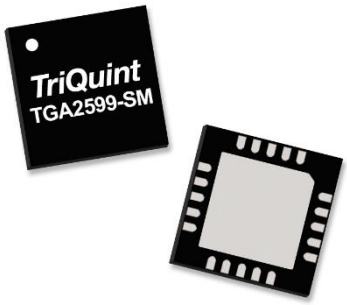
5 – 8 GHz 2W GaN Driver Amplifier

Product Description

Qorvo's TGA2599-SM is a packaged driver amplifier fabricated on Qorvo's QGaN25 0.25um GaN on SiC production process. The TGA2599-SM operates from 5.0 to 8.0GHz and provides 33 dBm of output power with 15 dB of large signal gain and 34 % power-added efficiency.

Using GaN MMIC technology and plastic packaging, the TGA2599-SM provides a low cost driver solution that provides the added benefit of operating on the same voltage rail as the corresponding GaN HPA. It can also serve as the primary amplifier on lower power architectures.

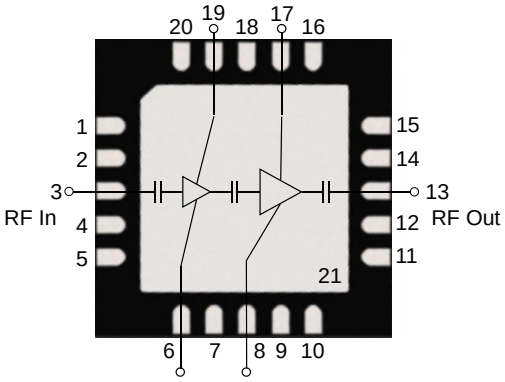
The TGA2599 is offered in a small 4 x 4 mm plastic overmold QFN, fully matched to 50 ohms and includes integrated DC blocking caps on both RF ports allowing for simple system integration.



Product Features

- Frequency Range: 5.0-8.0 GHz
- Small Signal Gain: 23 dB
- Saturated Power (CW): 33 dBm
- PAE (CW, @Pin = 18 dBm): 34%
- IM3: -25 dBc @ 26 dBm Pout
- Bias: V_D = 25 V, I_{DQ} = 50 mA
- Package Dimensions: 4.0 x 4.0 x 0.85 mm

Functional Block Diagram



Top View

Applications

- Commercial and military radar
- Communications
- Electronic Warfare (EW)

Ordering Information

Part No.	Description
TGA2599-SM	5 – 8 GHz 2W GaN Driver Amplifier
TGA2599-SMEVB01	TGA2599-SM Evaluation Board

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (V_D)		25		V
Drain Current (I_{DQ})		50		mA
Drain Current Under RF Drive (I_{D_DRIVE})		See plots		mA
Gate Voltage (V_G)		−2.5		V
Gate Current Under RF Drive (I_{G_DRIVE})		See plots		mA
Temperature (T_{BASE})	−40		+85	°C

Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Min	Typ	Max	Units
Operational Frequency Range	5		8	GHz
Small Signal Gain		23		dB
Input Return Loss		17		dB
Output Return Loss		5		dB
Output Power (at Pin = 18 dBm)		33		dBm
Power Added Efficiency (at Pin = 18 dBm)		34		%

Test conditions unless otherwise noted: T_{BASE} = +25 °C, V_D = +25 V, IDQ= 50 mA, VG = -2.5V typical, CW Mode
Data de-embedded to reference planes

Absolute Maximum Ratings

Parameter	Range / Value	Units
Drain Voltage (V_D)	40	V
Gate Voltage Range (V_G)	-8 to 0	V
Drain Current (I_{D1})	128	mA
Drain Current (I_{D2})	260	mA
Gate Current (I_{G1}) at Tch = 200 °C	1.4	mA
Gate Current (I_{G2}) at Tch = 200 °C	2.8	mA
Power Dissipation (P_{DISS}), 85 °C	5.5	W
Input Power (P_{IN}), CW, 50 Ω	30	dBm
Input Power (P_{IN}), CW, VSWR 10:1	25	dBm
Mounting Temperature (30 Seconds)	260	°C
Storage Temperature	-55 to 150	°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Thermal and Reliability Information

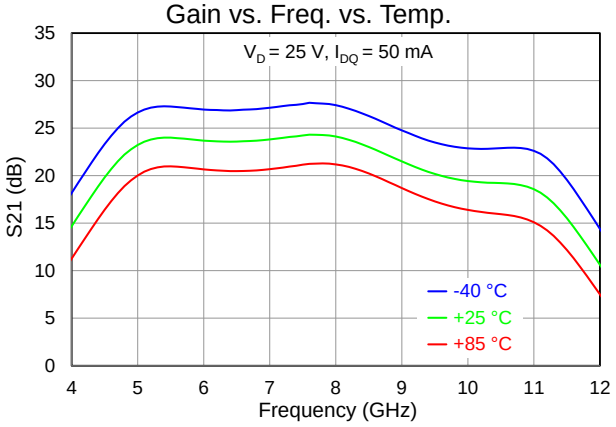
Parameter	Values	Units	Conditions
Under Drive, Thermal Resistance (θ_{JC}) (1,2,3)	16.3	°C/W	T_{BASE} = 85 °C, V_D = +25 V, CW Freq = 8 GHz, I_{D_DRIVE} = 250 mA P_{IN} = +18 dBm, P_{OUT} = +33 dBm, P_{DISS} = 4.2 W
Channel Temperature (T_{CH})	153.48	°C	

Notes:
1. Thermal resistance is measured to package backside
2. Base or ambient temperature is 85 °C
3. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

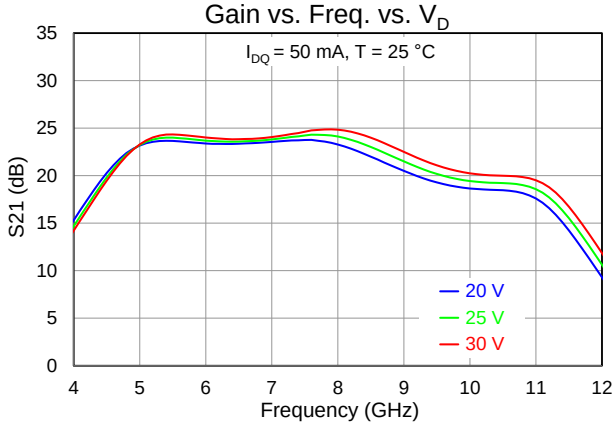
Performance Plots – Small Signal

Test conditions unless otherwise specified: V_D = 25 V, I_{DQ} = 50 mA, V_G = -2.5 V Typical, CW, 25 °C

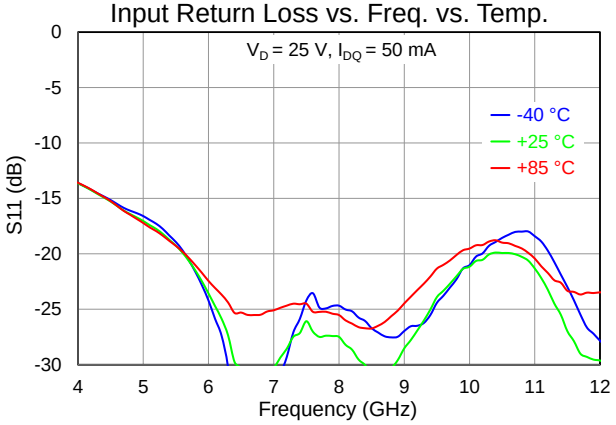
Gain vs. Freq. vs. Temp.



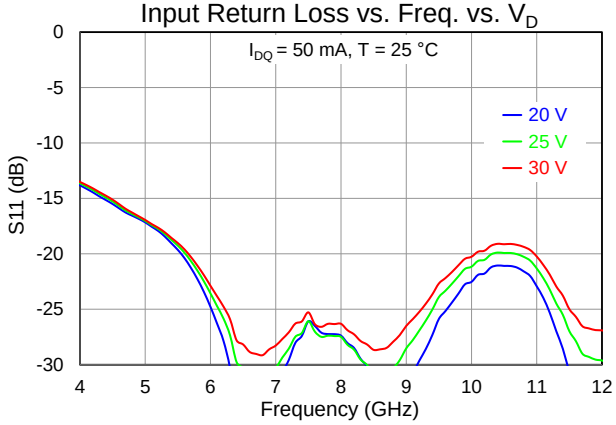
Gain vs. Freq. vs. V_D



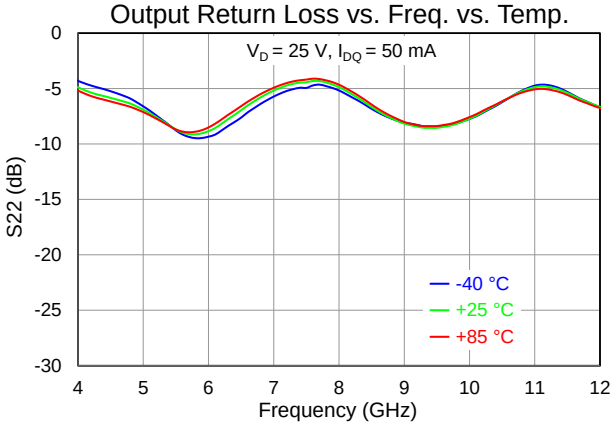
Input Return Loss vs. Freq. vs. Temp.



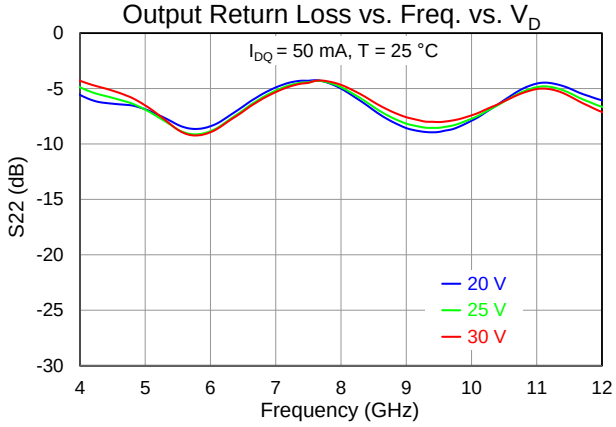
Input Return Loss vs. Freq. vs. V_D



Output Return Loss vs. Freq. vs. Temp.



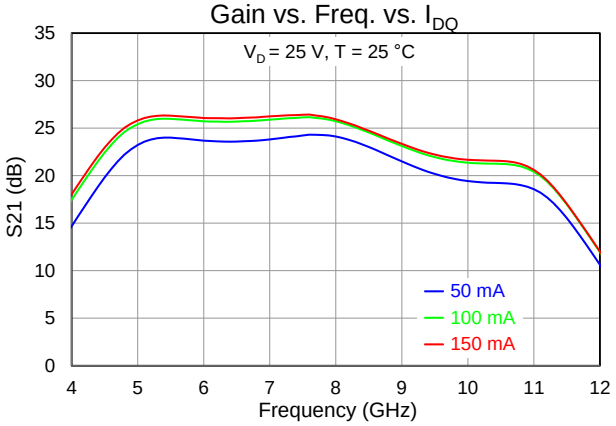
Output Return Loss vs. Freq. vs. V_D



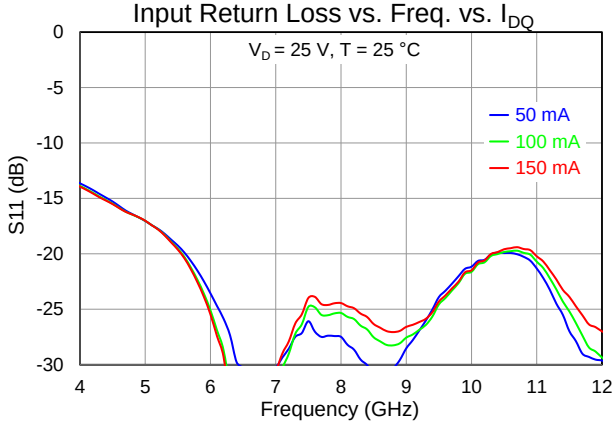
Performance Plots – Small Signal

Test conditions unless otherwise specified: V_D = 25 V, I_{DQ} = 50 mA, V_G = -2.5 V Typical, CW, 25 °C

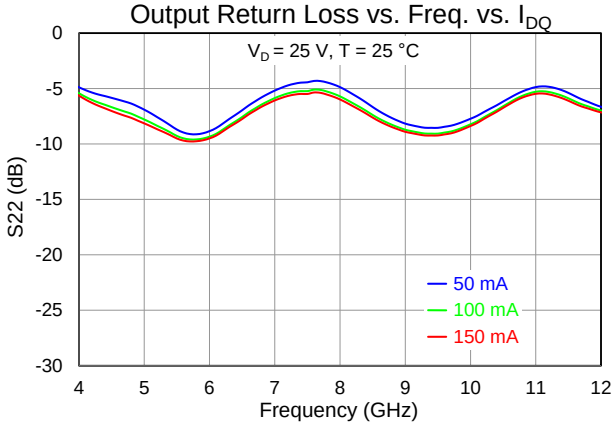
Gain vs. Freq. vs. I_{DQ}



Input Return Loss vs. Freq. vs. I_{DQ}



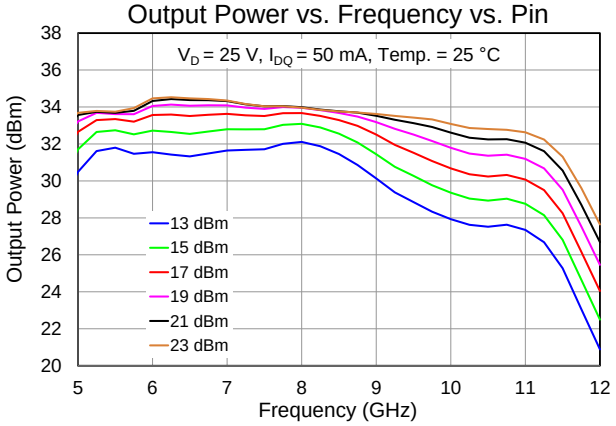
Output Return Loss vs. Freq. vs. I_{DQ}



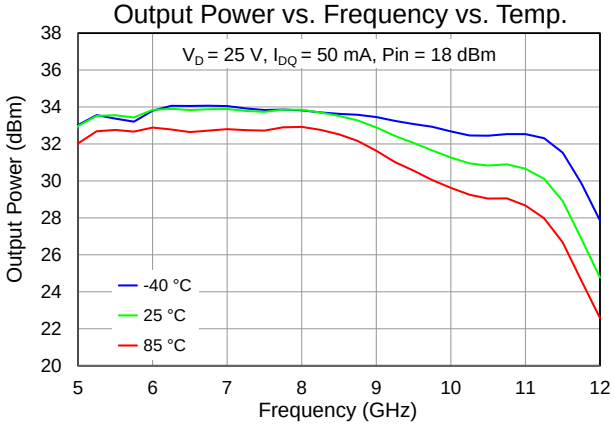
Performance Plots – Large Signal

Test conditions unless otherwise specified: V_D = 25 V, I_{DQ} = 50 mA, V_G = -2.5 V Typical, CW, 25 °C

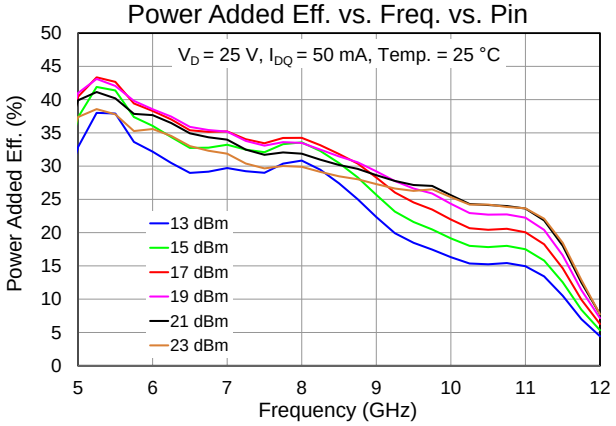
Output Power vs. Frequency vs. Pin



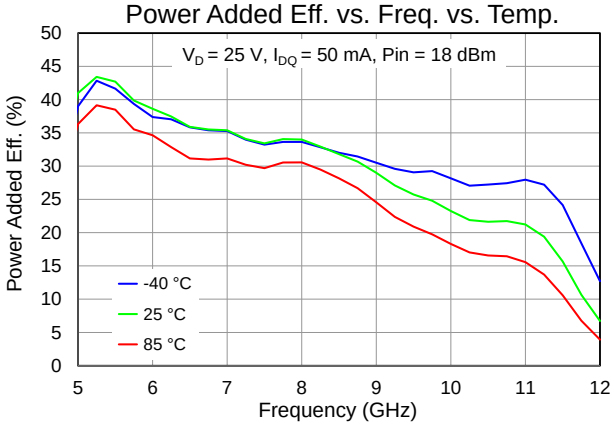
Output Power vs. Frequency vs. Temp.



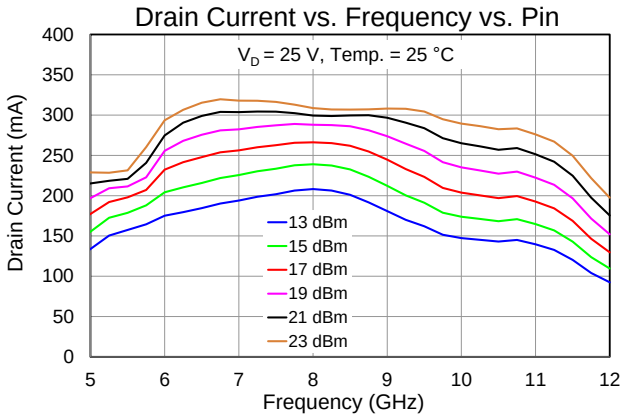
Power Added Eff. vs. Freq. vs. Pin



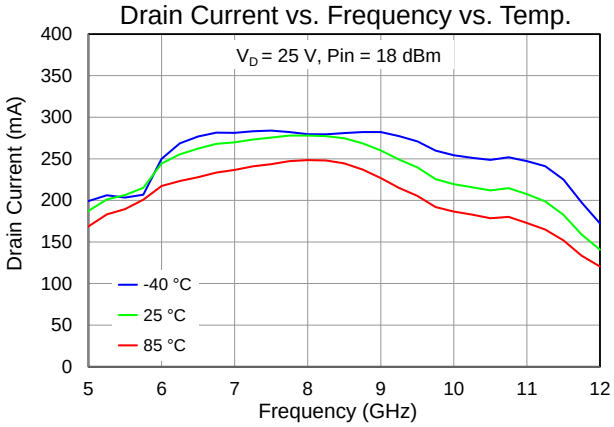
Power Added Eff. vs. Freq. vs. Temp.



Drain Current vs. Frequency vs. Pin



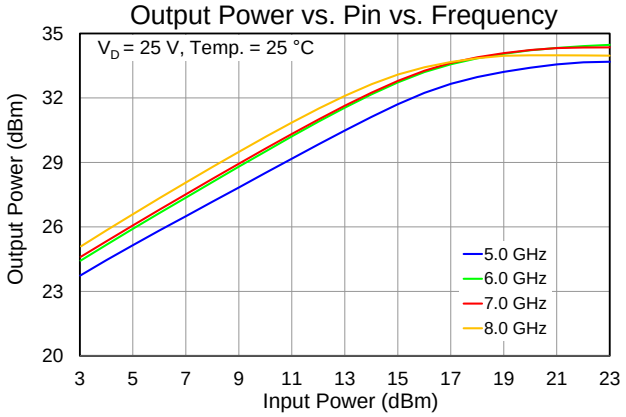
Drain Current vs. Frequency vs. Temp.



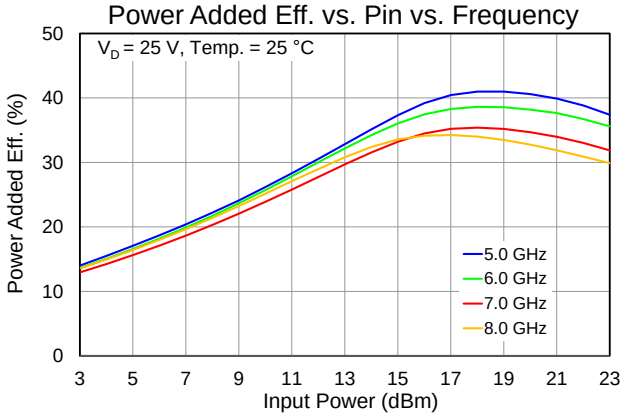
Performance Plots – Large Signal

Test conditions unless otherwise specified: V_D = 25 V, I_{DQ} = 50 mA, V_G = -2.5 V Typical, CW, 25 °C

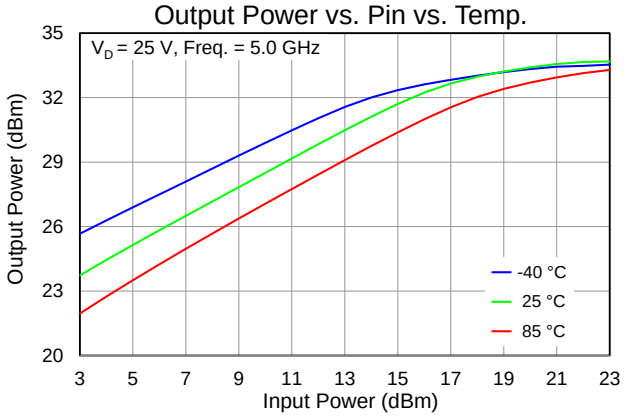
Output Power vs. Pin vs. Frequency



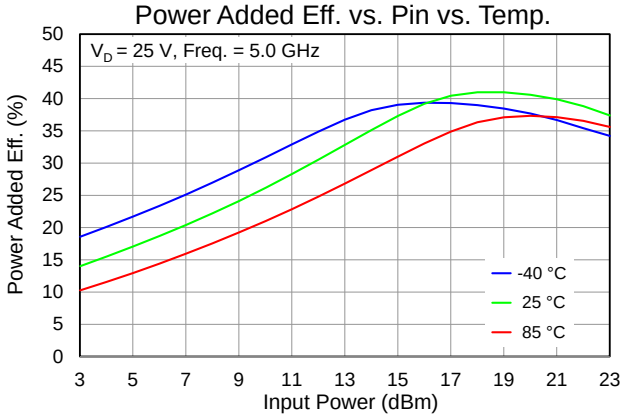
Power Added Eff. vs. Pin vs. Frequency



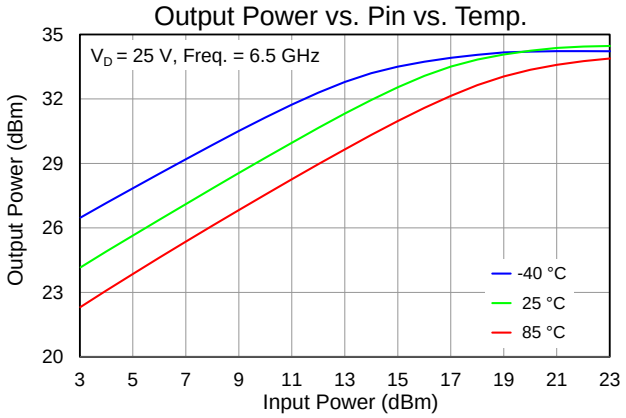
Output Power vs. Pin vs. Temp.



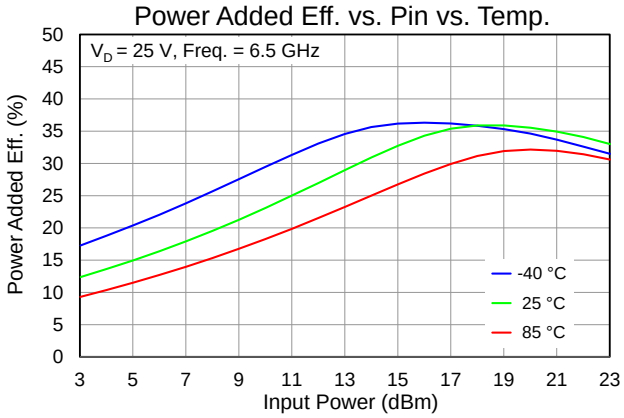
Power Added Eff. vs. Pin vs. Temp.



Output Power vs. Pin vs. Temp.



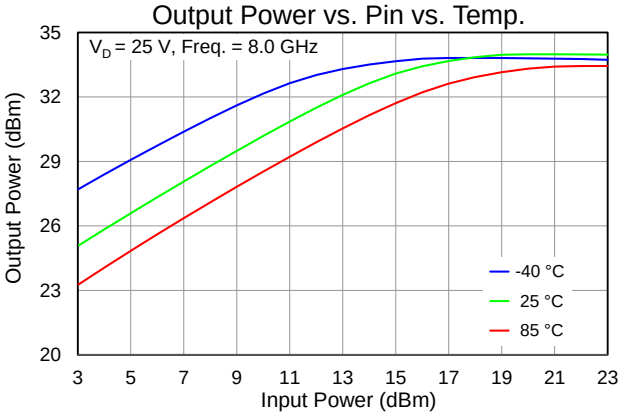
Power Added Eff. vs. Pin vs. Temp.



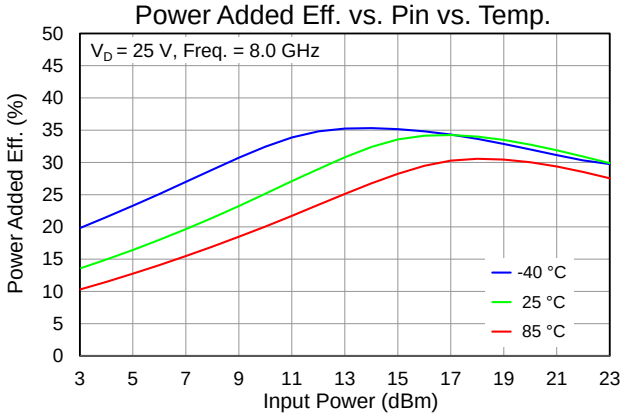
Performance Plots – Large Signals

Test conditions unless otherwise specified: V_D = 25 V, I_{DQ} = 50 mA, V_G = -2.5 V Typical, CW, 25 °C

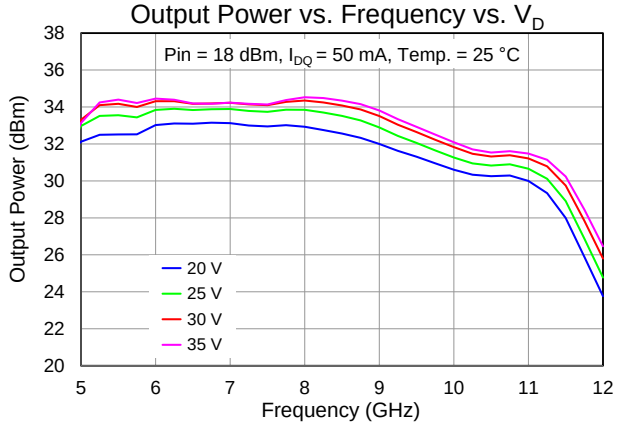
Output Power vs. Pin vs. Temp.



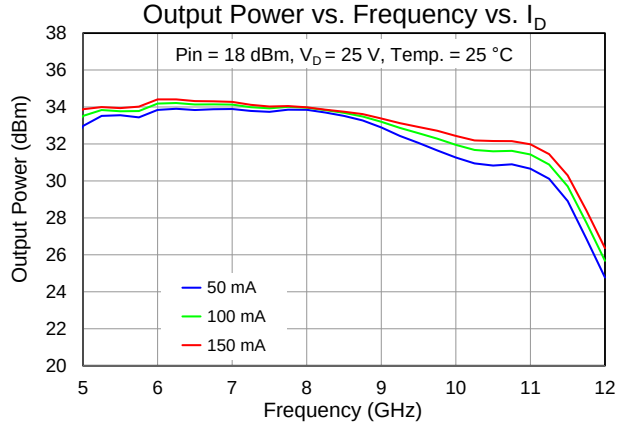
Power Added Eff. vs. Pin vs. Temp.



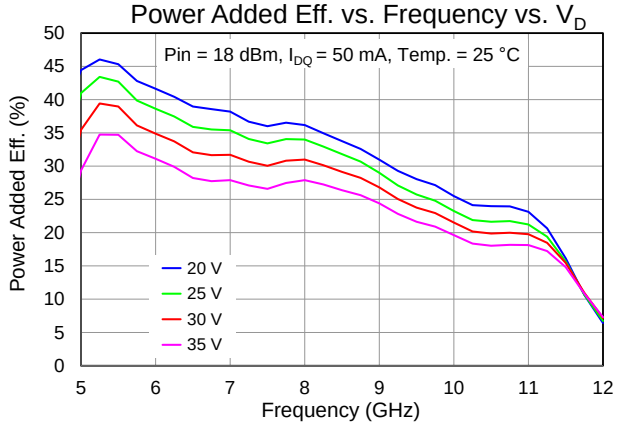
Output Power vs. Frequency vs. V_D



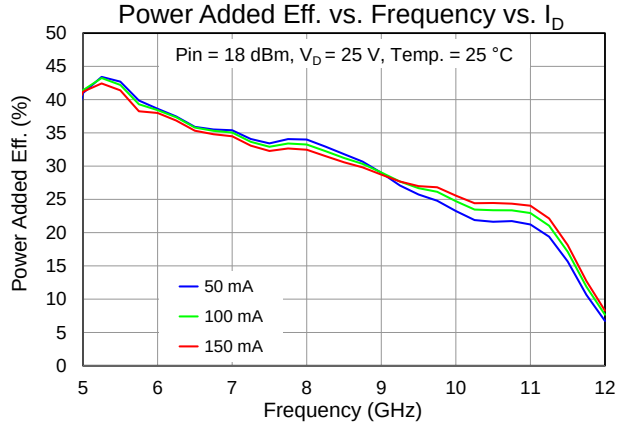
Output Power vs. Frequency vs. I_D



Power Added Eff. vs. Frequency vs. V_D

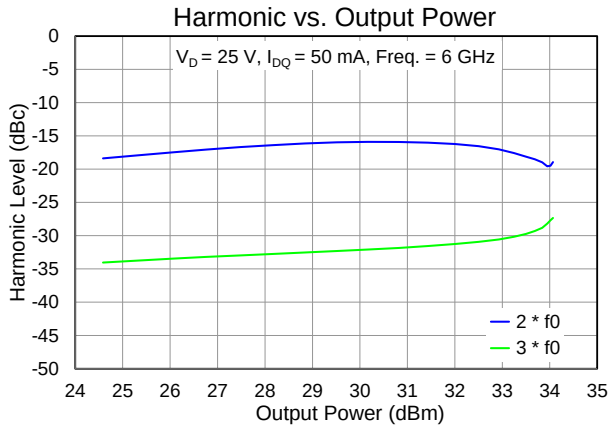


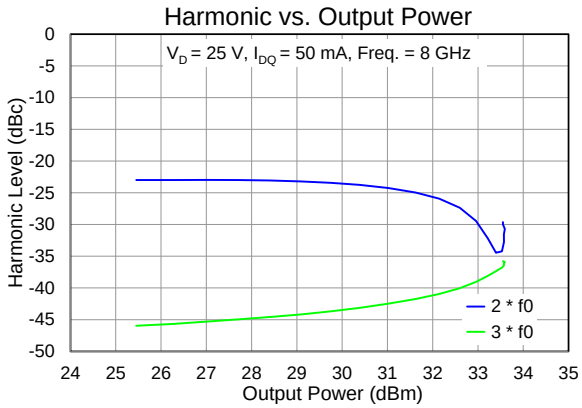
Power Added Eff. vs. Frequency vs. I_D

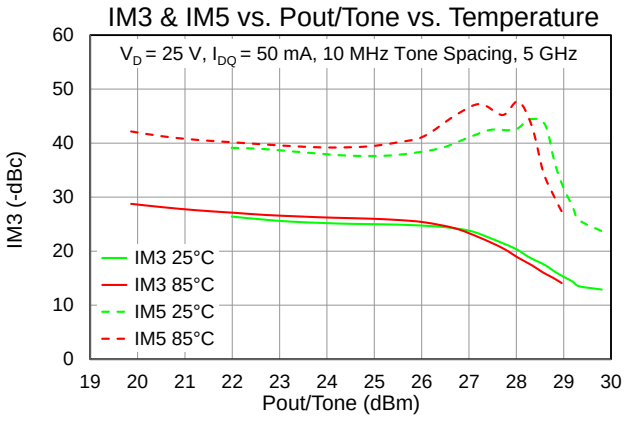


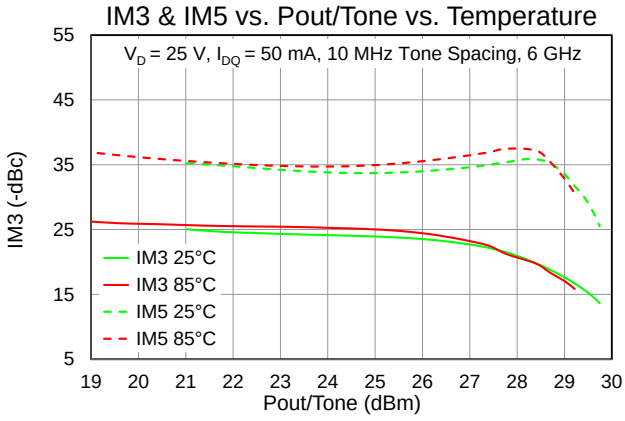
Performance Plots – Linearity and Harmonics

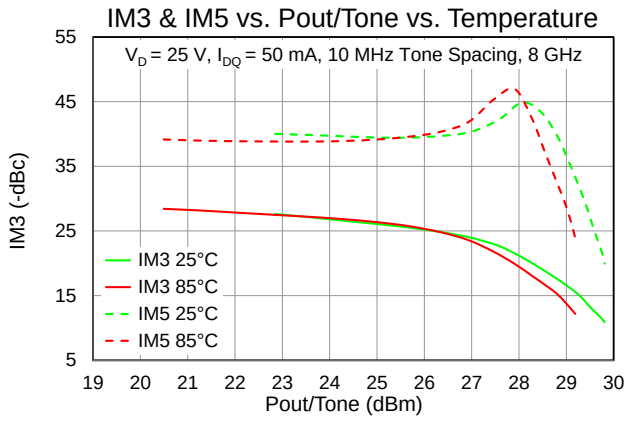
Test conditions unless otherwise specified: V_D = 25 V, I_{DQ} = 50 mA, V_G = -2.5 V Typical, CW, 25 °C



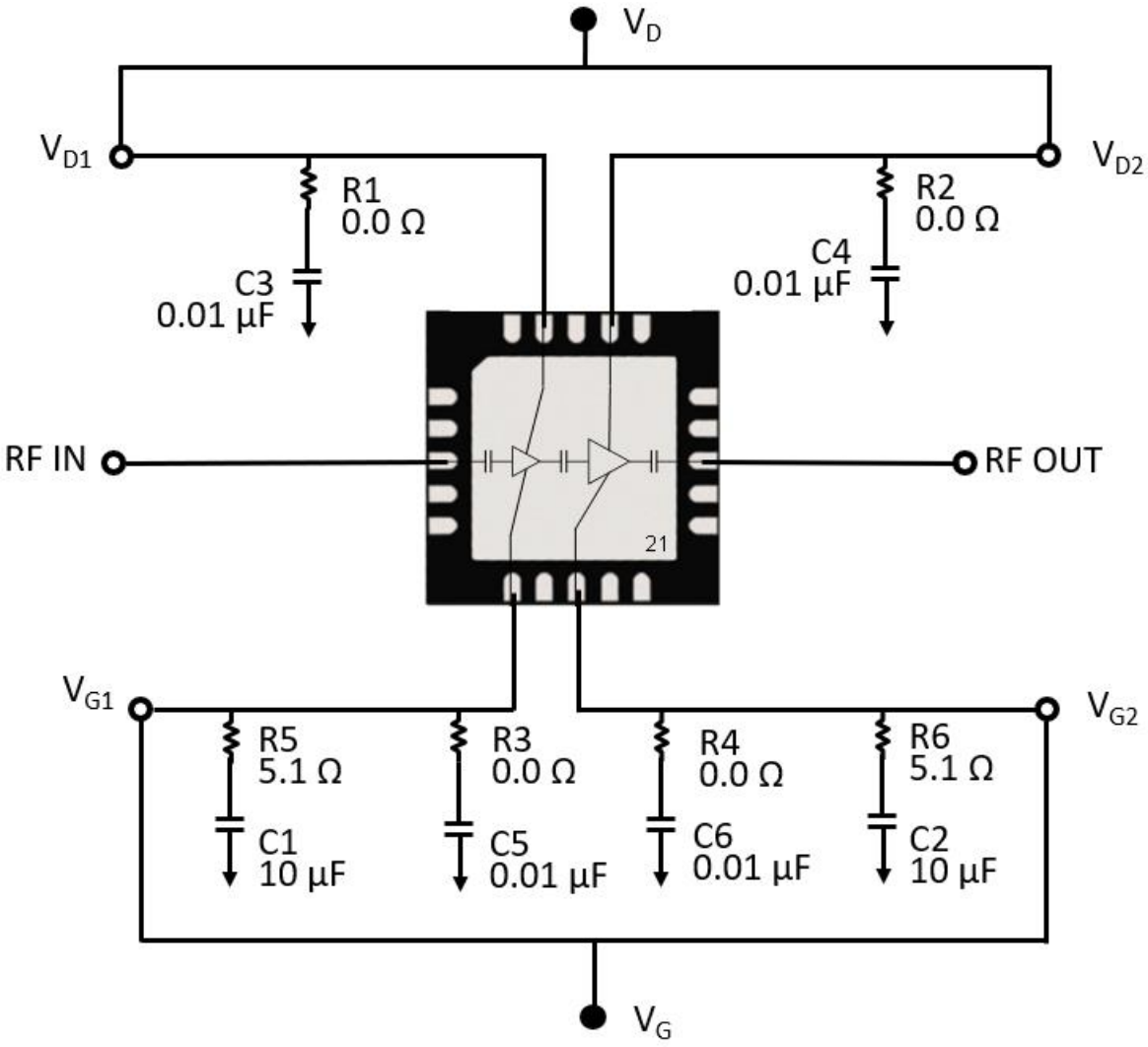








Application Circuit



Note: Device shown is top view, V_{D1} / V_{D2}, and V_{G1} / V_{G2} can be gied together

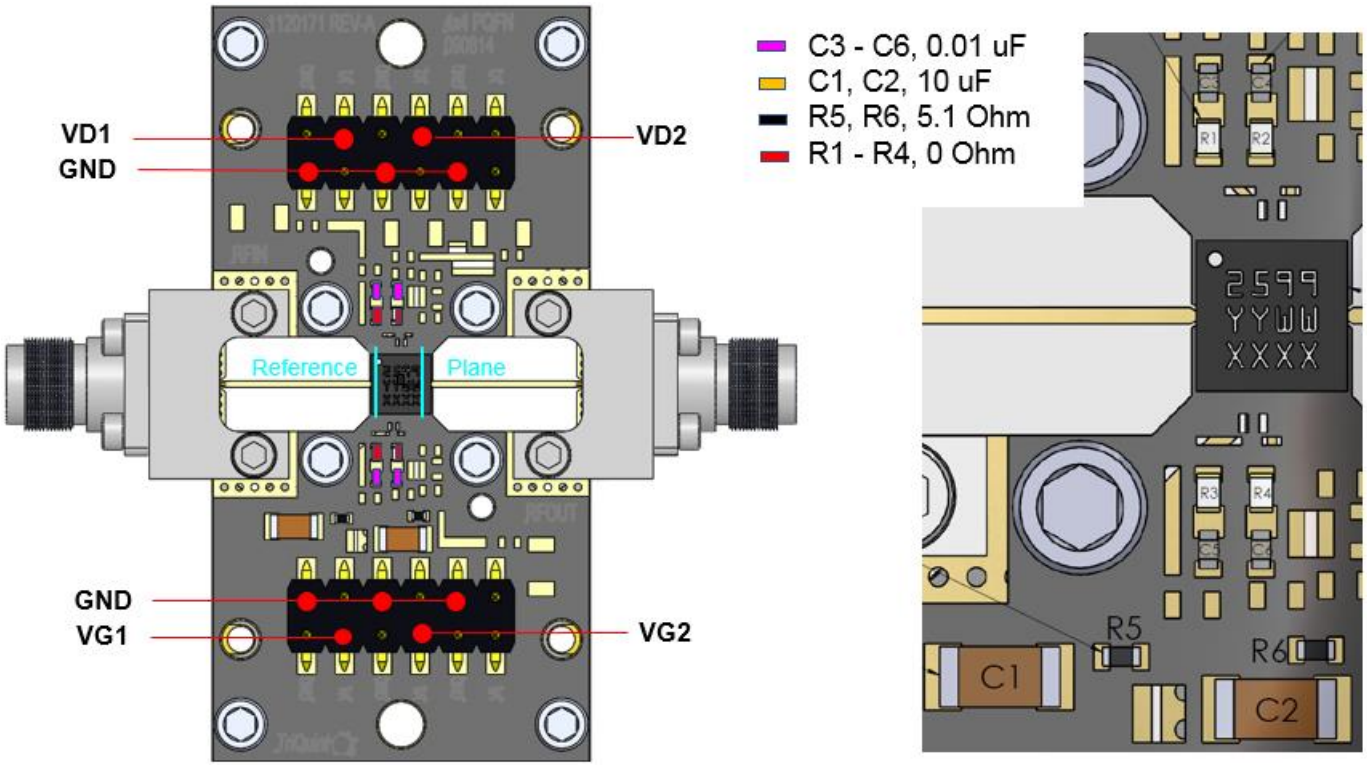
Bias Up Procedure

1. Set I_D limit to 400 mA, I_G limit to 4.5 mA
2. Set V_{G1}/V_{G2} to -5.0V
3. Set V_{D1}/V_{D2} +25V
4. Adjust V_{G1}/V_{G2} more positive until I_{DQ} = 50 mA
5. Apply RF signal

Bias Down Procedure

1. Turn off RF signal
2. Set V_{G1}/V_{G2} to -5.0V. Ensure I_{DQ} ~ 0mA
3. Set V_{D1}/V_{D2} to 0V
4. Turn off V_{D1}/V_{D2} supply
5. Turn off V_{G1}/V_{G2} supply

EVB and BOM



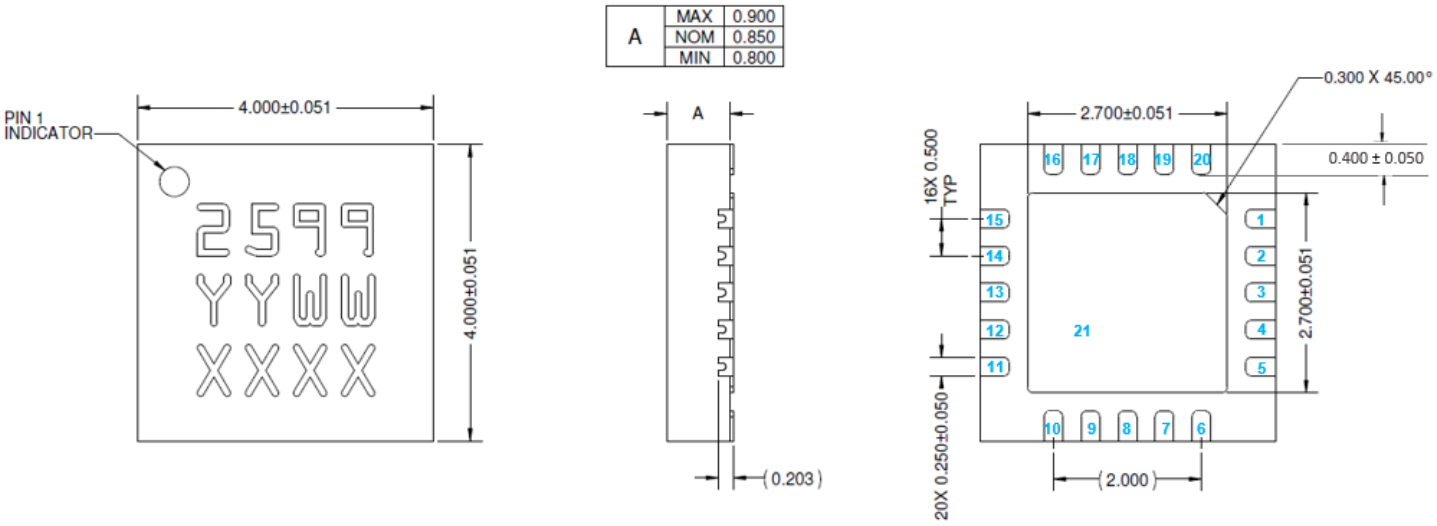
RF Layer is 0.008" thick Rogers Corp. RO4003C, ε_r = 3.38. Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-01A-5.

The trace pattern shown has been developed and tested for optimized assembly at Qorvo Semiconductor. The PCB land pattern has been developed to accommodate lead tolerances. Since processes vary from company to company, careful process development is recommended

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C3 – C6	0.01 uF	Cap., 50V, 10% X7R, 0402 case	Various	
C1 - C2	10 uF	Cap., 50V, 10% X5R, 1206 case	Various	
R1 – R4	0.0 Ohms	Resistor, 0402 case	Various	
R5 – R6	5.1 Ohms	Resistor, 0402 case	Various	

Pin Configuration and Description



Dimensions in mm. Tolerance unless otherwise stated is +/- 0.127 um.
Package lead finish: Ni / Au plating with minimum gold thickness of 0.1 um
Materials: Base: Ceramic, Lid: Plastic, Part is epoxy sealed
Part Marking: 2599: Part Number, YY = Part Assembly Year, WW = Part Assembly Week, MXXX = Batch ID

Pin No.	Label	Description
1-2,4-5,7,9-12,14-16,18, 20	GND	Connected to ground paddle (21); must be grounded to PCB to improve isolation.
3	RF Input	RF input, matched to 50 Ω, DC blocked
6	V_{G1}	First stage gate voltage. Bias network required. V_{G1} and V_{G2} can be tied together in application.
8	V_{G2}	Second stage gate voltage. Bias network required. V_{G1} and V_{G2} can be tied together in application.
13	RF Output	RF output, matched to 50 Ω, DC blocked
17	V_{D2}	Second stage drain voltage. Bias network required. V_{D1} and V_{D2} can be tied together in application.
19	V_{D1}	First stage drain voltage. Bias network required. V_{D1} and V_{D2} can be tied together in application.
21	GND	Backside paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

Solderability

1. Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C.
2. The use of no-clean solder to avoid washing after soldering is recommended.

Recommended Soldering Temperature Profile