TGA2976-SM

0.1 – 3.0 GHz 10W GaN Power Amplifier

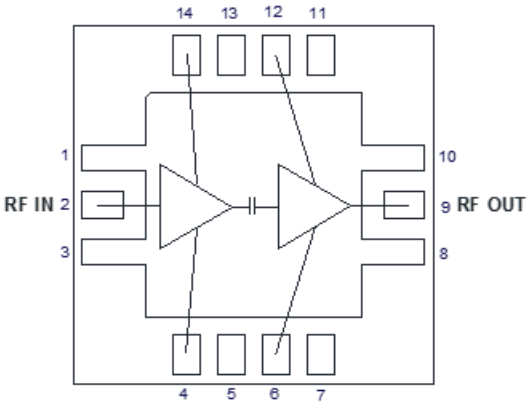
Product Overview

Qorvo's TGA2976-SM is a wideband cascode amplifier fabricated on Qorvo's production 0.25um GaN on SiC process. The cascode configuration offers exceptional wideband performance as well as supporting 40 V operation. The TGA2976-SM operates from 0.1 - 3.0 GHz and provides greater than 10 W of saturated output power with greater than 13 dB of large signal gain and greater than 38% power-added efficiency.

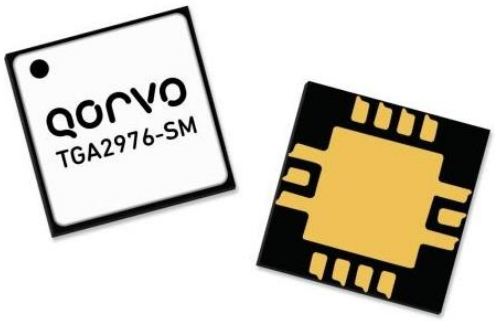
The TGA2976-SM is available in a low-cost, surface mount 14 lead 4x4 Air Cavity laminate package. It is ideally suited to support both radar and communication applications across defense and commercial markets as well as electronic warfare. The TGA2976-SM is fully matched to 50 Ω at both RF ports allowing for simple system integration. DC blocks are required on both RF ports and the drain voltage must be injected through an off chip bias-tee on the RF output port.

Lead-free and RoHS compliant.

Functional Block Diagram



Top View



AC-QFN 4x4 mm 14L

Key Features

- Frequency Range: 0.1 – 3.0 GHz
- PSAT: >40 dBm at P_{IN} = 27 dBm
- PAE: 48% @ mid-band
- Large Signal Gain: >13 dB
- Small Signal Gain: >20 dB
- Bias: V_D = 40 V, I_{DQ} = 360 mA
- Wideband Flat Gain and Power
- Package Dimensions: 4.0 x 4.0 x 1.64 mm

Applications

- Commercial and military radar
- Communications
- Electronic Warfare

Ordering Information

Part No.	Description
TGA2976-SM	0.1-3.0 GHz 10 W GaN Power Amplifier
TGA2976-SM EVB	TGA2976-SM Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage (V_D)	80 V
Gate Voltage Range (V_{G1})	-8 to 0 V
Gate Voltage Range (V_{G2})	0 to 40 V
Drain Current (I_D)	760 mA
Gate Current (I_{G1})	See plot on pg. 3
Gate Current (I_{G2})	See plot on pg. 3
Power Dissipation (P_{DISS}), 85°C	28 W
Input Power (P_{IN}), CW, 50 Ω, 85°C,	33 dBm
Input Power (P_{IN}), CW, VSWR 3:1, V_D = 40V, 85°C	33 dBm
Mounting Temperature	260°C
Storage Temperature	-55 to 150°C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	40 V
Drain Current (I_{DQ})	360 mA
Gate Voltage Range (V_{G1})	−2.8 to −2.0 V
Gate Voltage (V_{G2})	+17.7 V (Typ.)

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions [1]	Min	Typ	Max	Units
Operational Frequency Range		0.1		3.0	GHz
Small Signal Gain			> 20		dB
Input Return Loss			> 5		dB
Output Return Loss			> 9		dB
Output Power	P_{IN} = 27 dBm		> 40		dBm
Power Added Efficiency	P_{IN} = 27 dBm, mid-band		48		%
3rd Order Intermodulation	120 mA, P_{OUT}/tone = 28 dBm		-30		dBc
5th Order Intermodulation	120 mA, P_{OUT}/tone = 28 dBm		-38		dBc
Small Signal Gain Temperature Coefficient			-0.03		dB/°C
Output Power Temperature Coefficient			-0.009		dBm/°C
Recommended Operating Voltage			40	50	V

Notes:

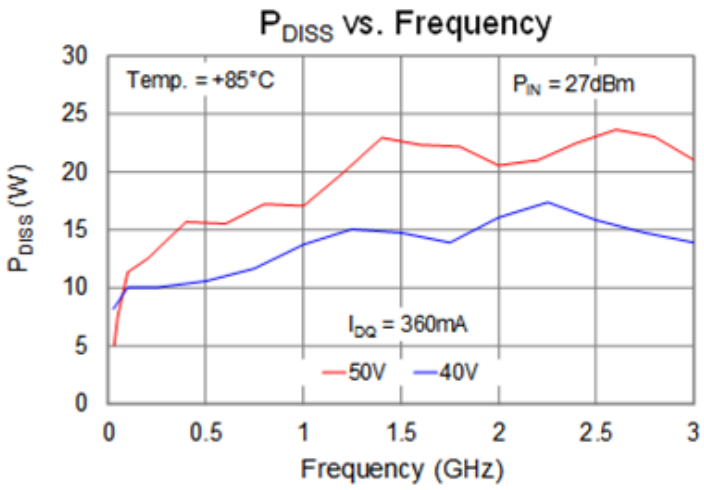
1. Test conditions unless otherwise noted: 25°C , V_D = 40 V, I_{DQ} = 360 mA, V_{G1} = -2.4 V, V_{G2} = +17.7 V

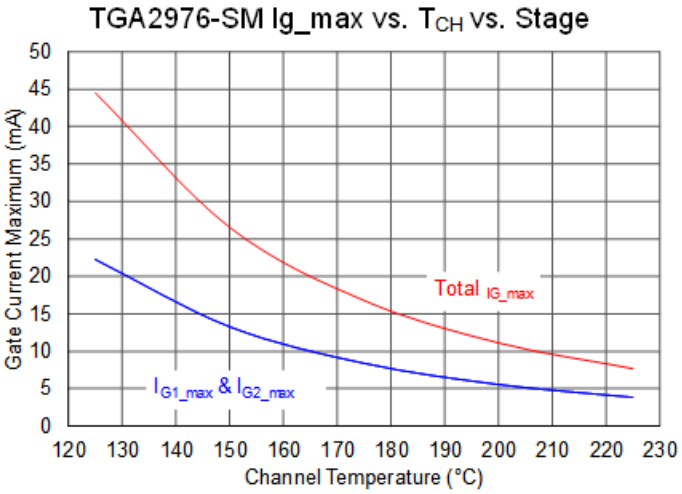
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D(2) = 40 V (CW), I_{DQ} = 360 mA, I_{D_Drive} = 655 mA, P_{IN} = 27 dBm, P_{OUT} = 40 dBm, P_{DISS} = 17.4 W	3.55	ºC/W
Channel Temperature, T_{CH} (Under RF) 3		146.8	°C
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D(2) = 50 V (CW), I_{DQ} = 360 mA, I_{D_Drive} = 655 mA, P_{IN} = 27 dBm, P_{OUT} = 40 dBm, P_{DISS} = 23.6 W	3.70	ºC/W
Channel Temperature, T_{CH} (Under RF) 3		172.3	°C

Notes:
1. Thermal resistance measured at back of package.
2. The drain voltage for Cascode amplifier transistor is ½ of V_D
3. IR scan equivalent. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

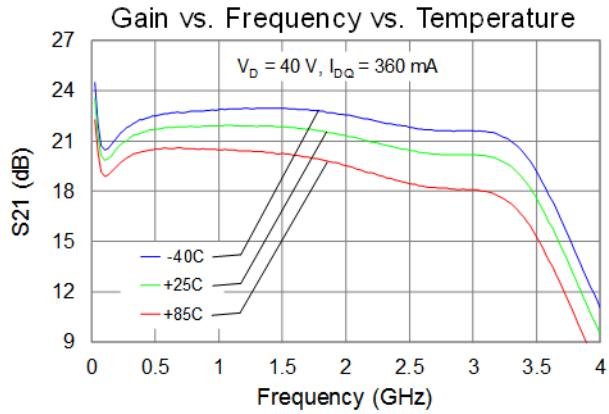
Power Dissipation and Maximum Gate Current

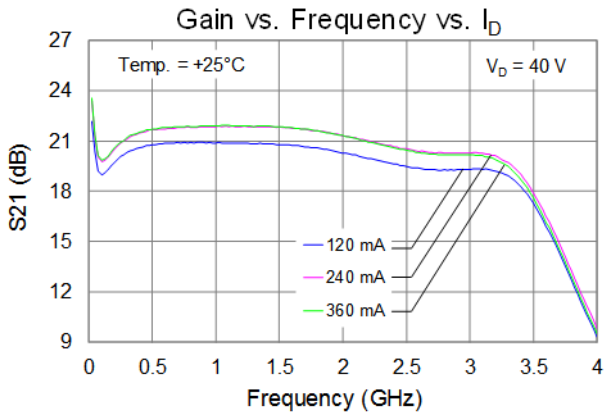


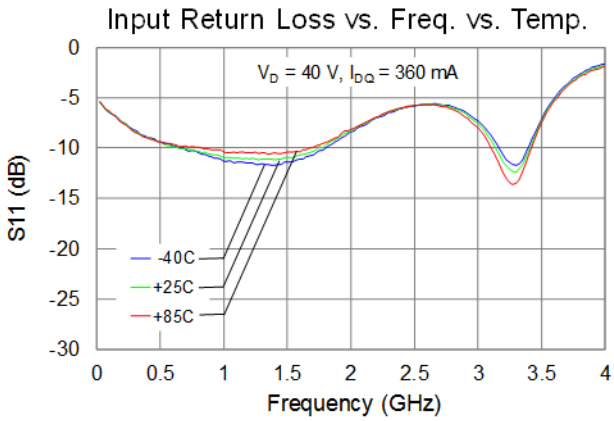


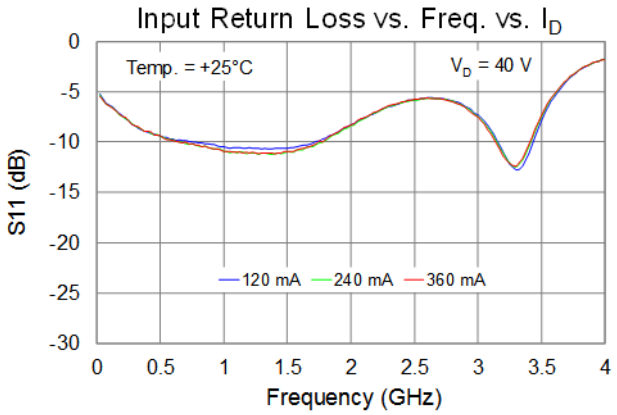
Performance Plots – Small Signal

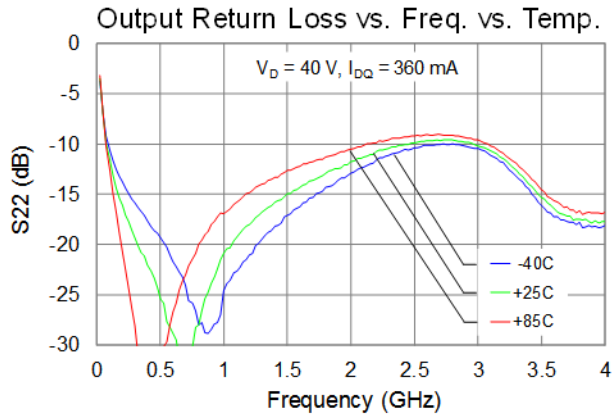
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 12)

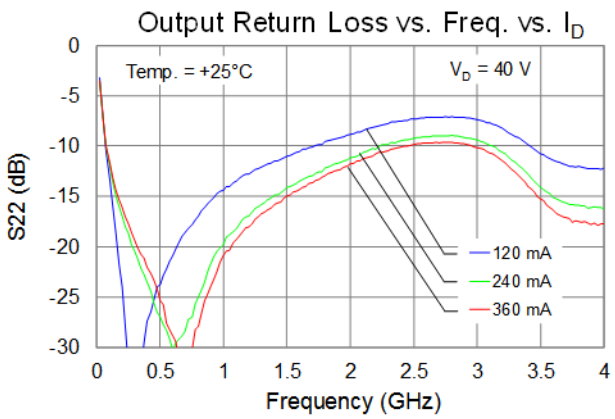












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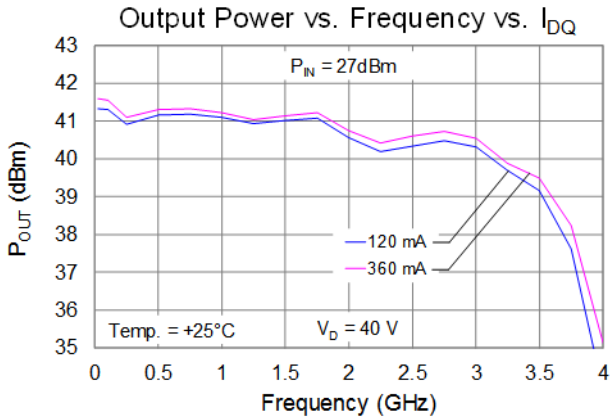
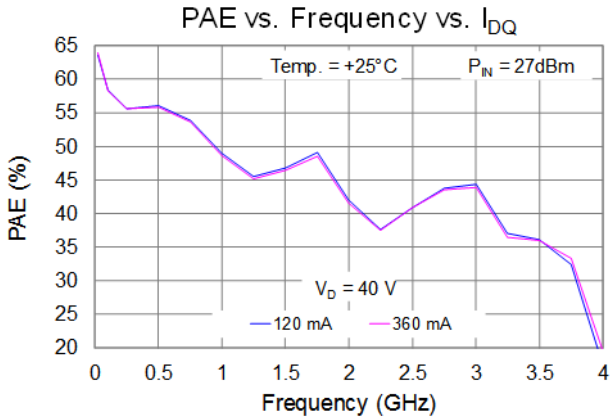
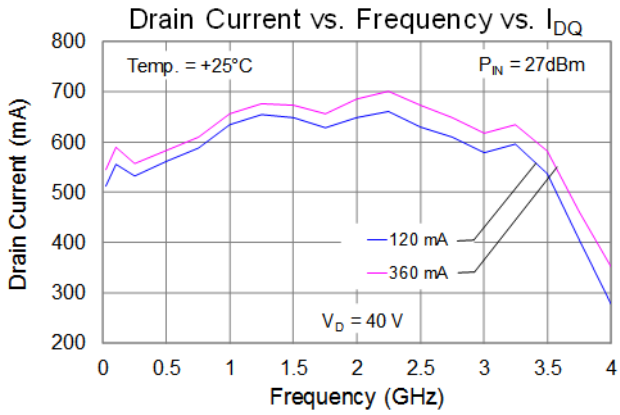
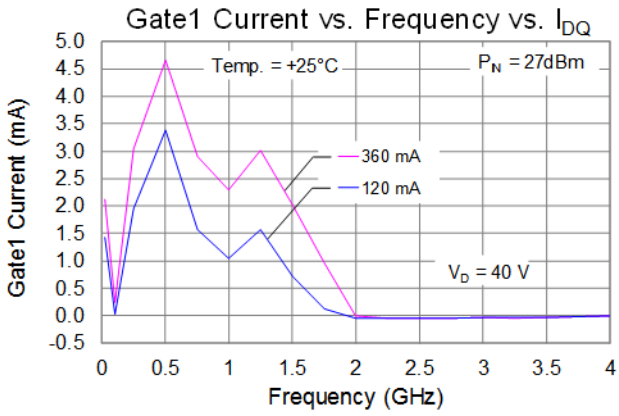
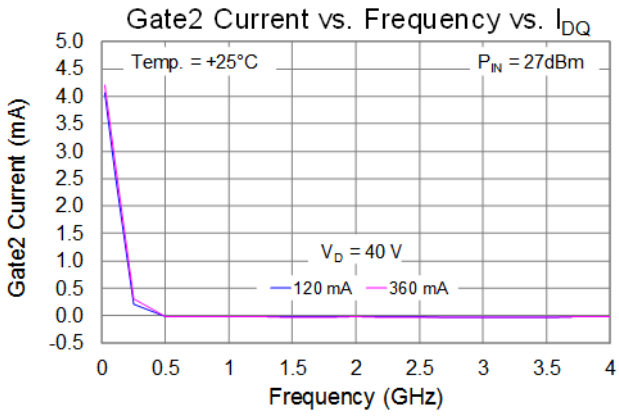




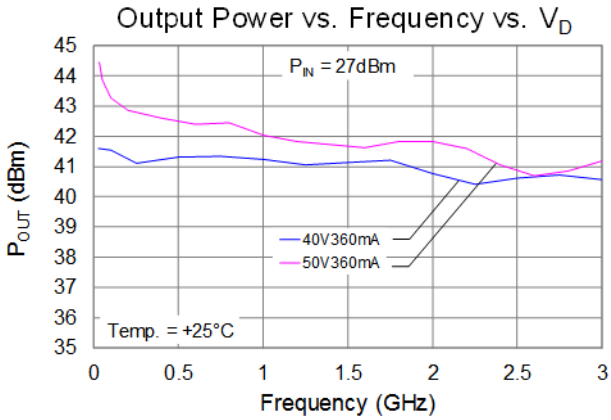


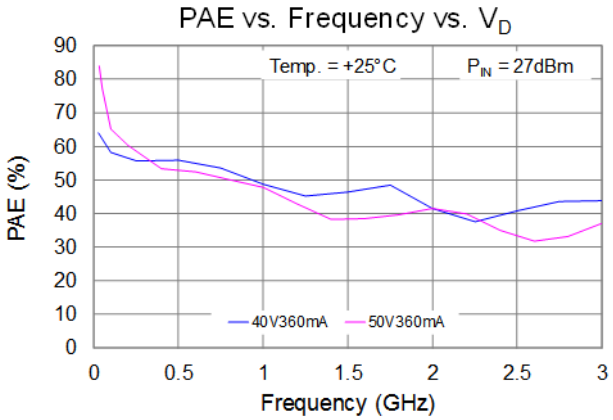


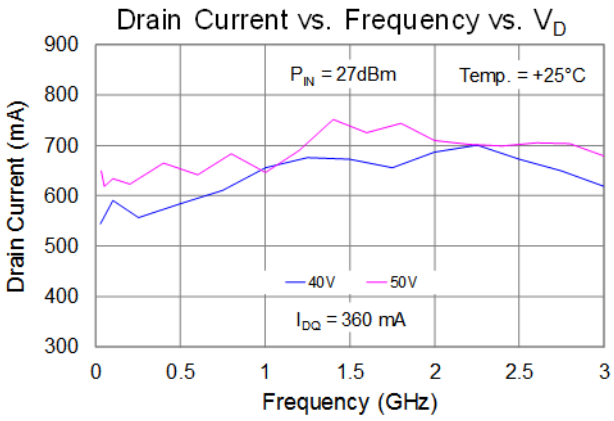


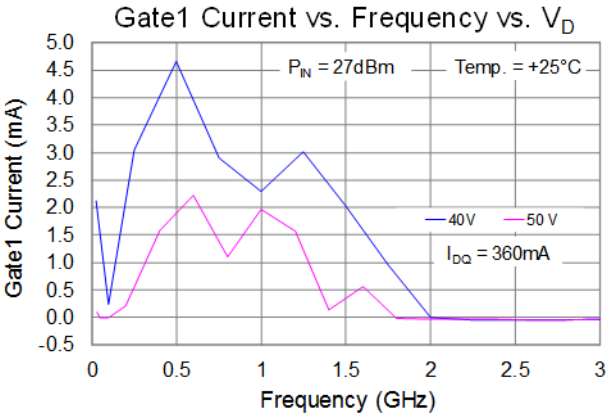
Performance Plots – Large Signal (CW)

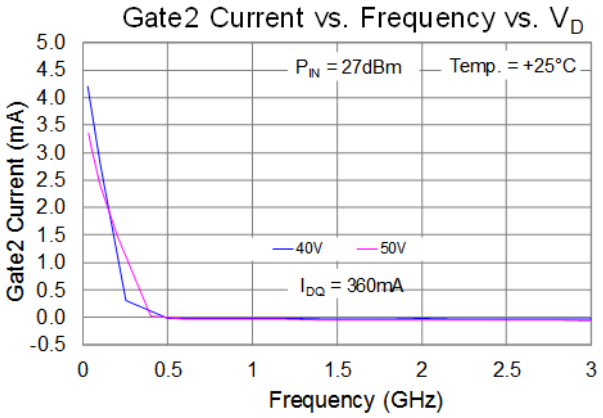
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 12)











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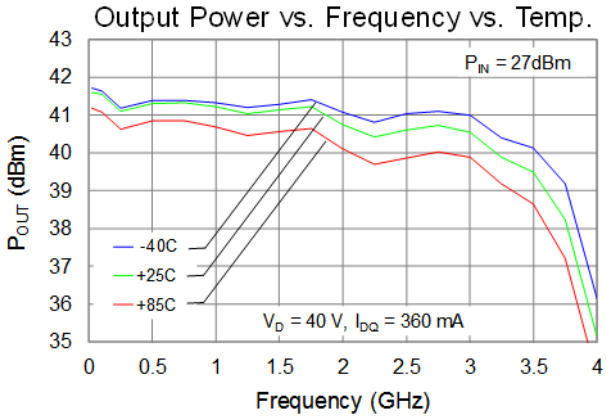

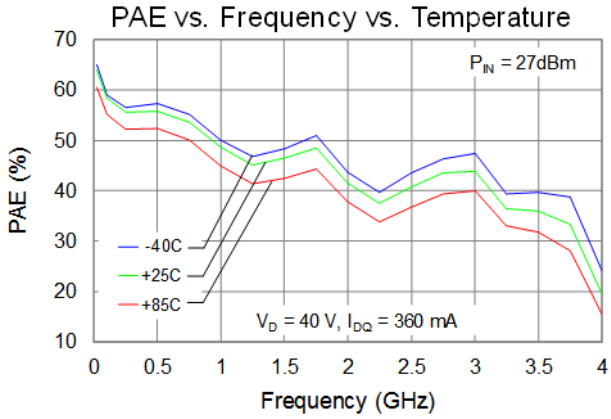

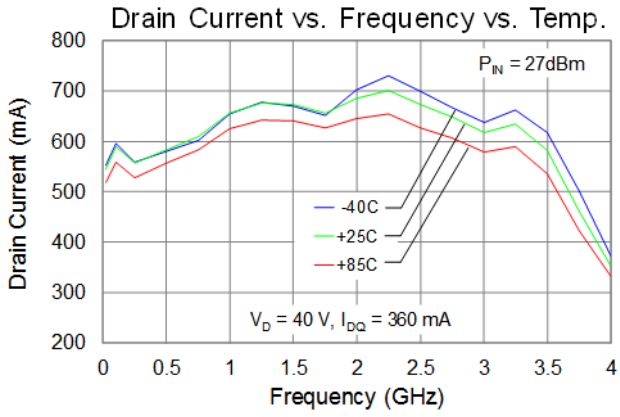

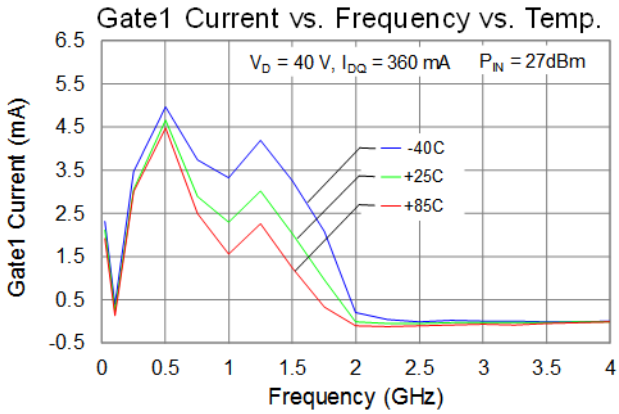

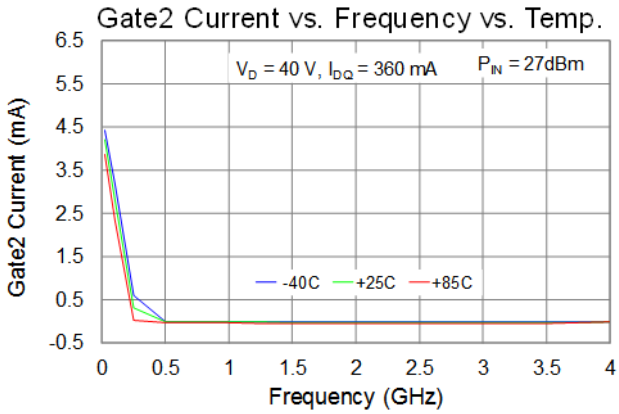

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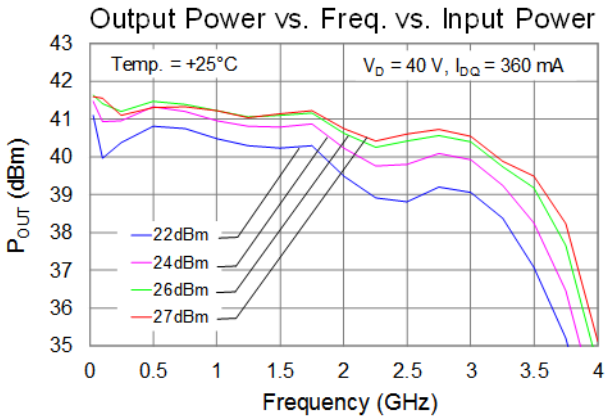
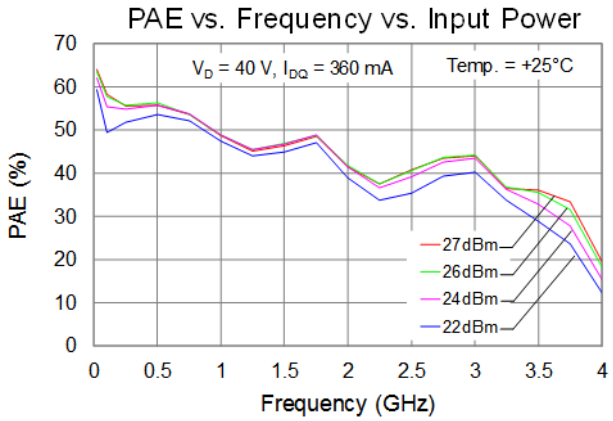
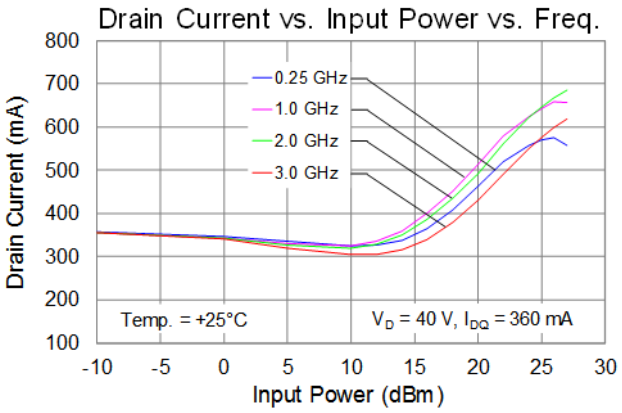
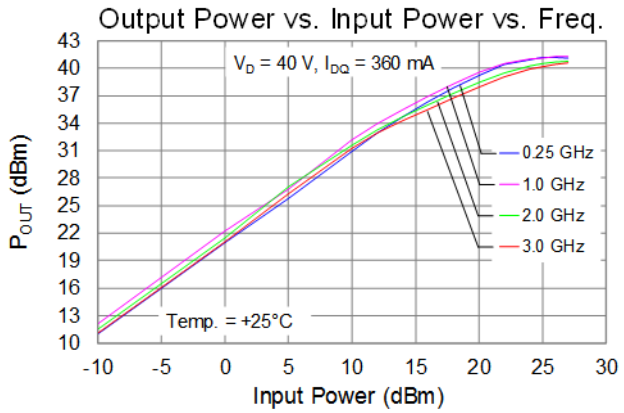
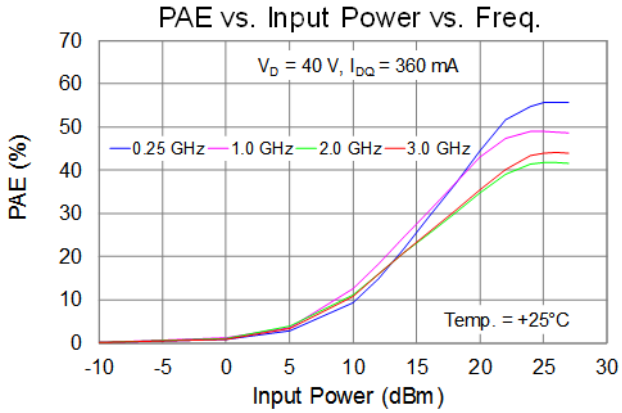




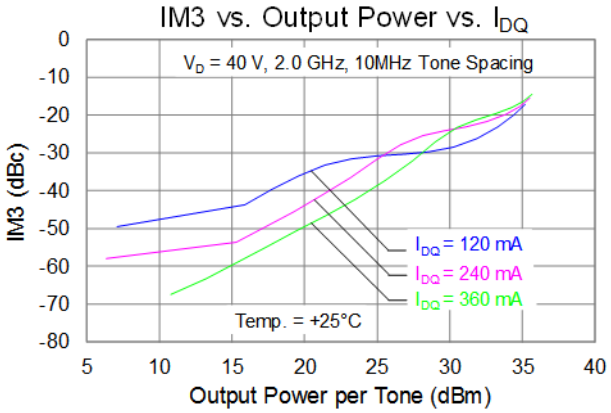


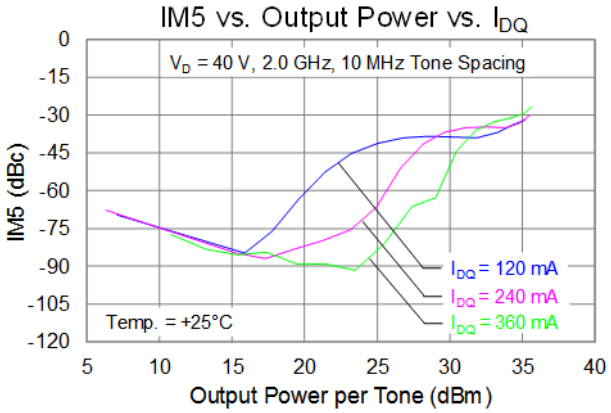


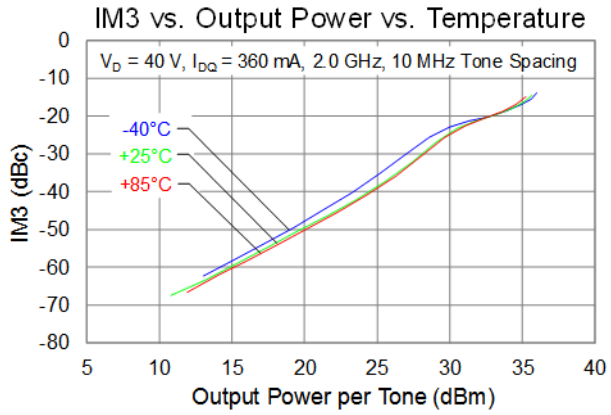


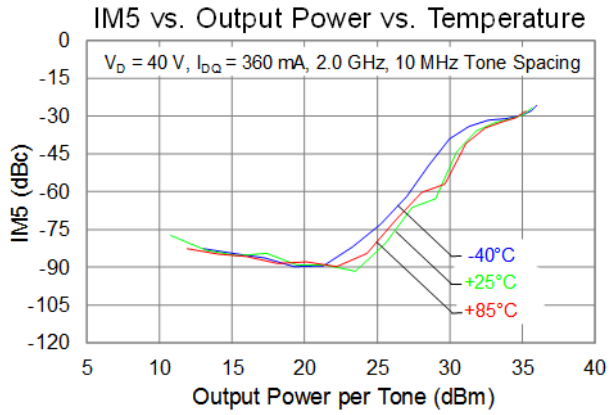
Performance Plots – Linearity

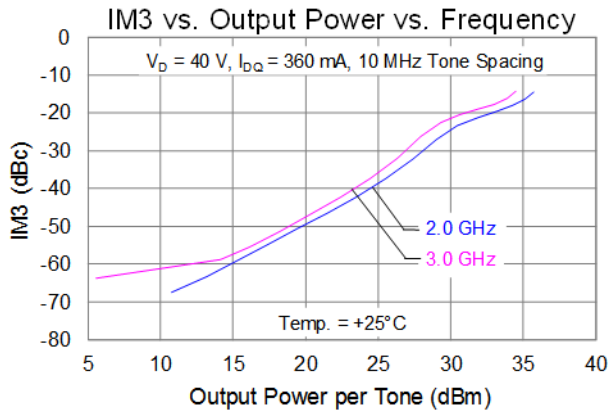
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 12)

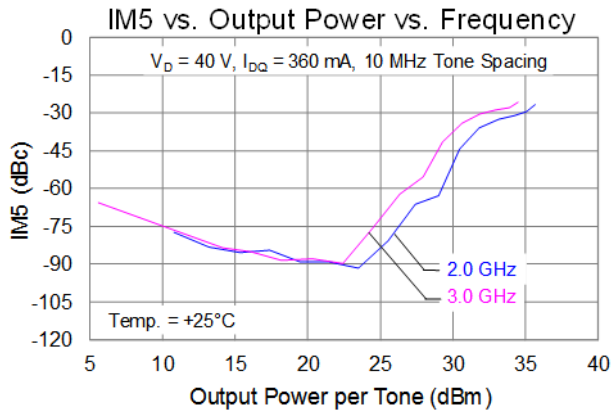






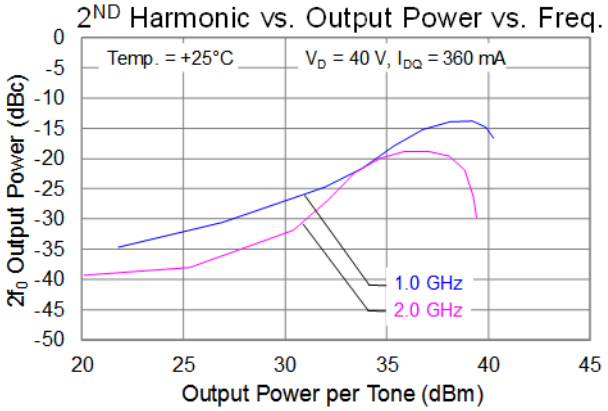


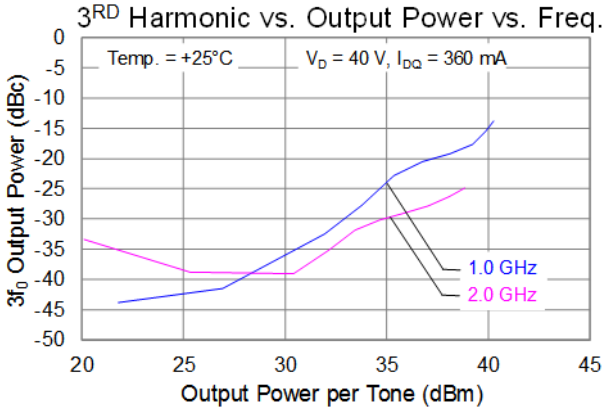


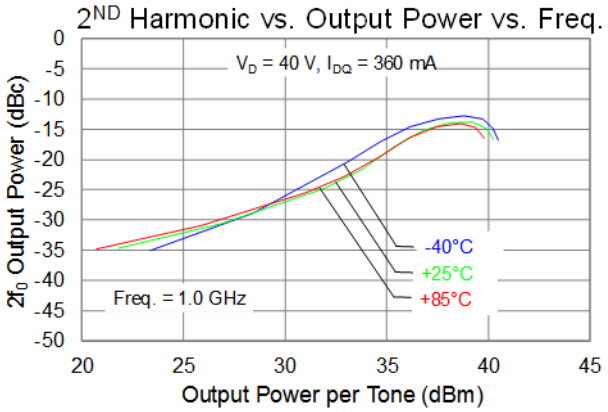


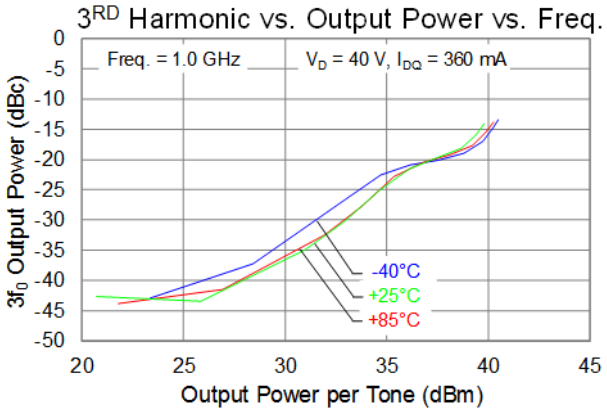
Performance Plots – Linearity

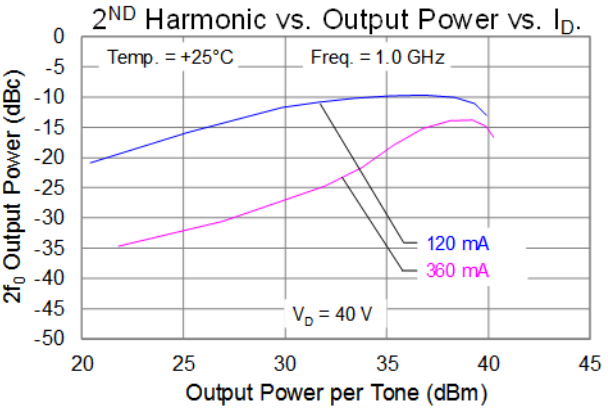
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 12)

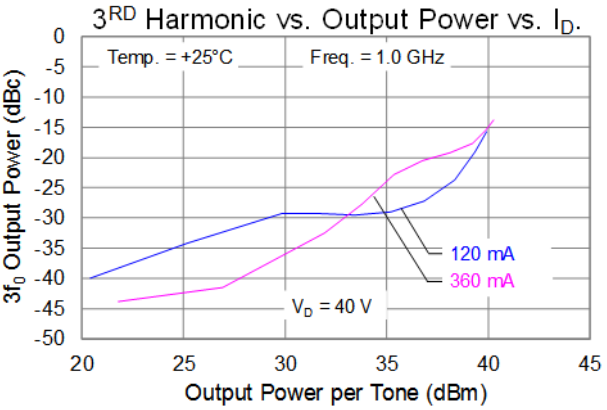






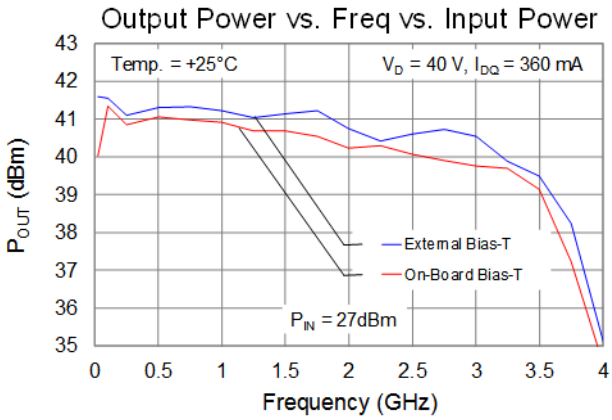


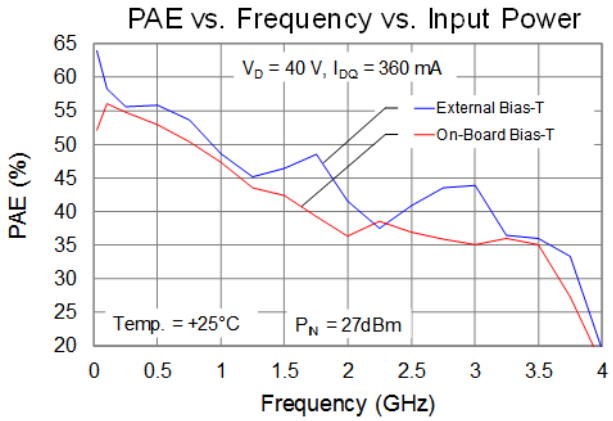




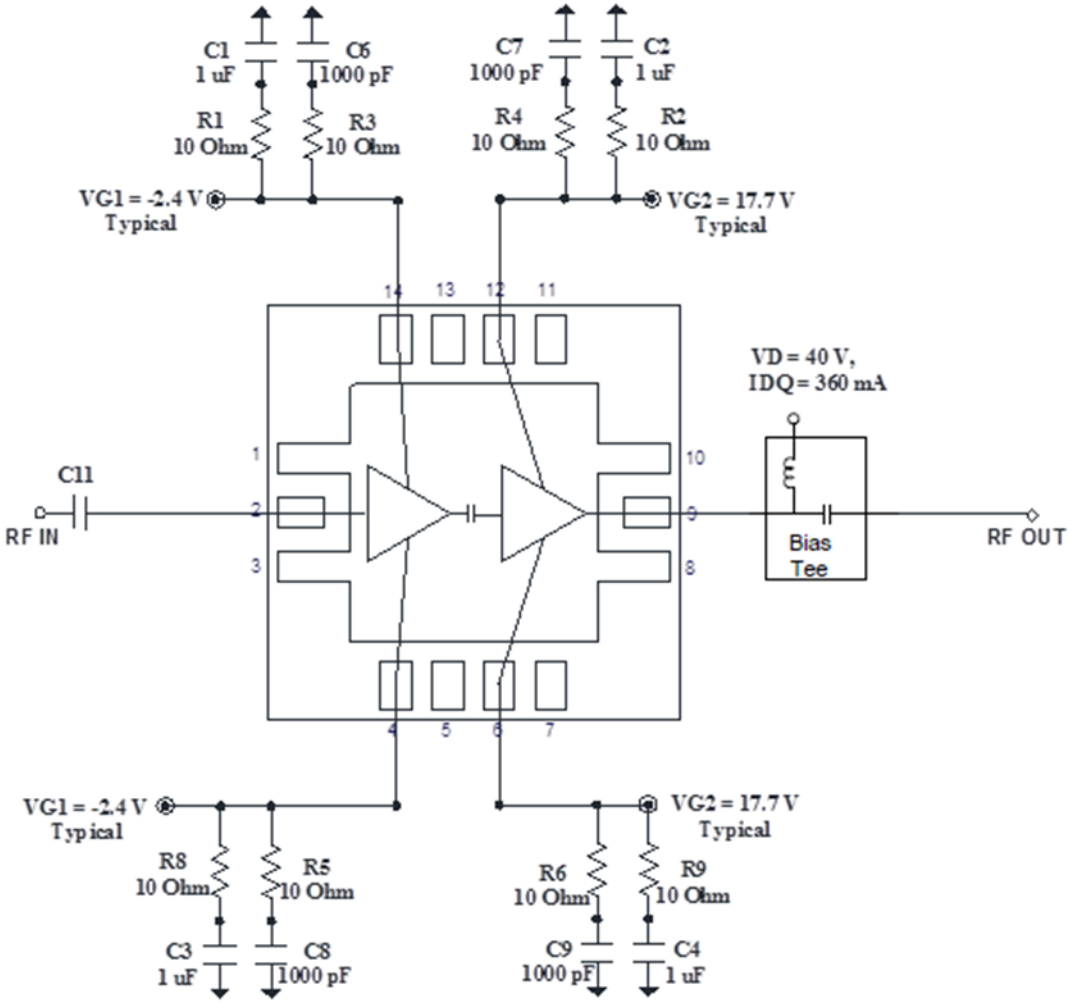
Performance Plots – Large Signal (CW), On–board vs. External Bias–T

The plots below reflect performance measured between external bias tee and on-board bias tee
(See application circuit on page 12 and 14)





Application Circuit (Coaxial Input DC Block and Coaxial Output Bias–T)



Notes:

1. V_{G1} & V_{G2} can be biased from either side (Top or Bottom.)
2. Coaxial input DC block (C11) is used for input port (RF In.)
3. External wide bandwidth Bias-Tee is used for output port (RF Out). V_D is applied through the output Bias-Tee.

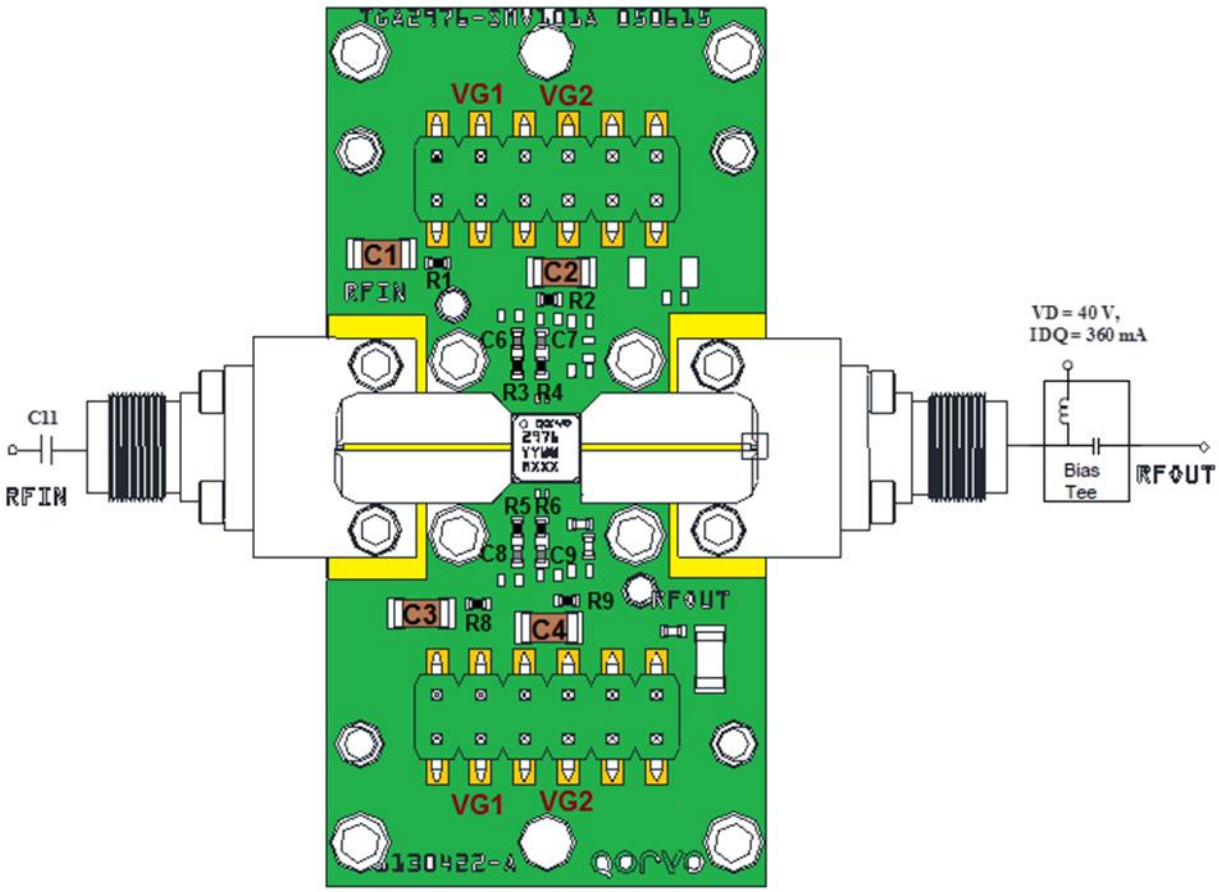
Bias-Up Procedure

1. Set I_D limit to 755 mA, I_{G1} & I_{G2} limit to 5 mA
2. Set V_{G1} to -5.0 V
3. Set V_{G2} to (V_D/2) - 2.7 V or (40 V/2) - 2.7 V = 17.3 V
4. Set V_D +40 V
5. Adjust V_{G1} more positive until I_{DQ} = 360 mA
6. Adjust V_{G2} to (V_D/2) + V_{G1}; (V_{G2} ~ +17.7 V Typical)
7. Apply RF signal

Bias-Up Procedure

1. Turn off RF signal
2. Reduce V_{G1} to -5.0 V. Ensure I_{DQ} ~ 0mA
3. Reduce V_{G2} to 0 V.
4. Set V_D to 0 V
5. Turn off V_D supply
6. Turn off V_{G2} supply
7. Turn off V_{G1} supply

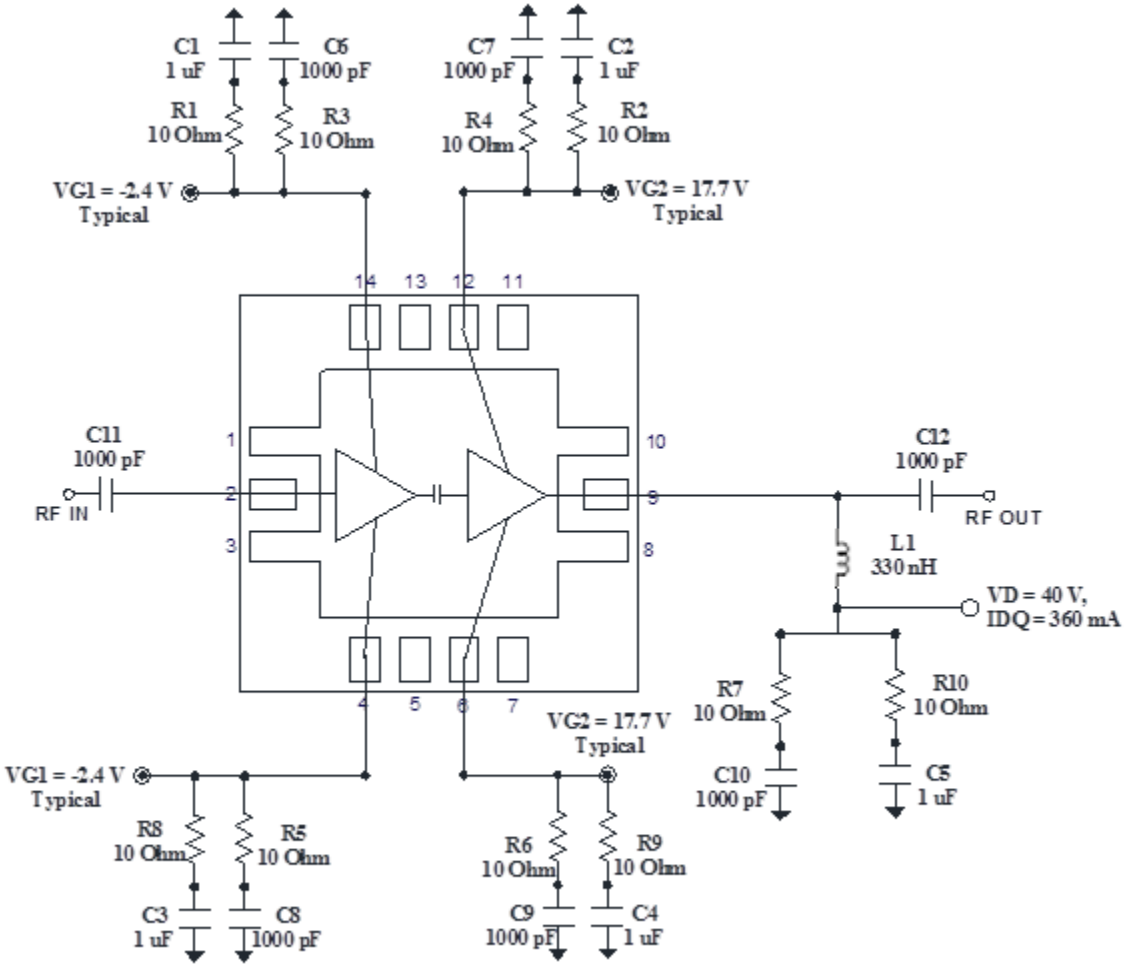
EVB Assembly Drawing (Coaxial Input DC Block and Coaxial Output Bias–T)



Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1 – C4	1uF	Cap, 1206, 50V, 5%, X7R	Various	
C6 – C9	1000pF	Cap, 0402, 100V, 10%, X7R	Various	
C11		DC Block	Various	
R1 – R6, R8 – R9	10Ω	Res, 0402, 5%	Various	

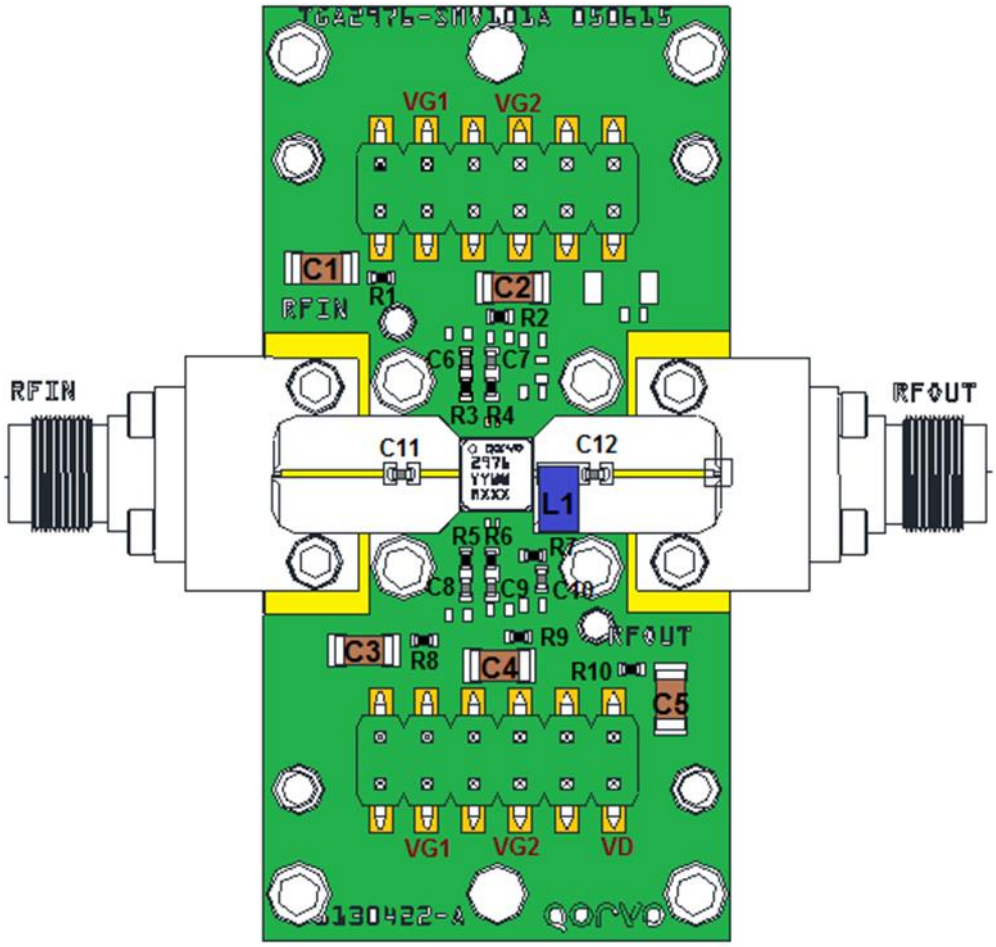
Application Circuit (Option with Board–Level DC Blocks and Output Bias–T)



Notes:

1. Performance of the DUT with surface mount DC blocks and bias tee components may be degraded relative to the coaxial option. These components should be optimized for the desired operational bandwidth.
2. V_{G1} & V_{G2} can be biased from either side (Top or Bottom.)

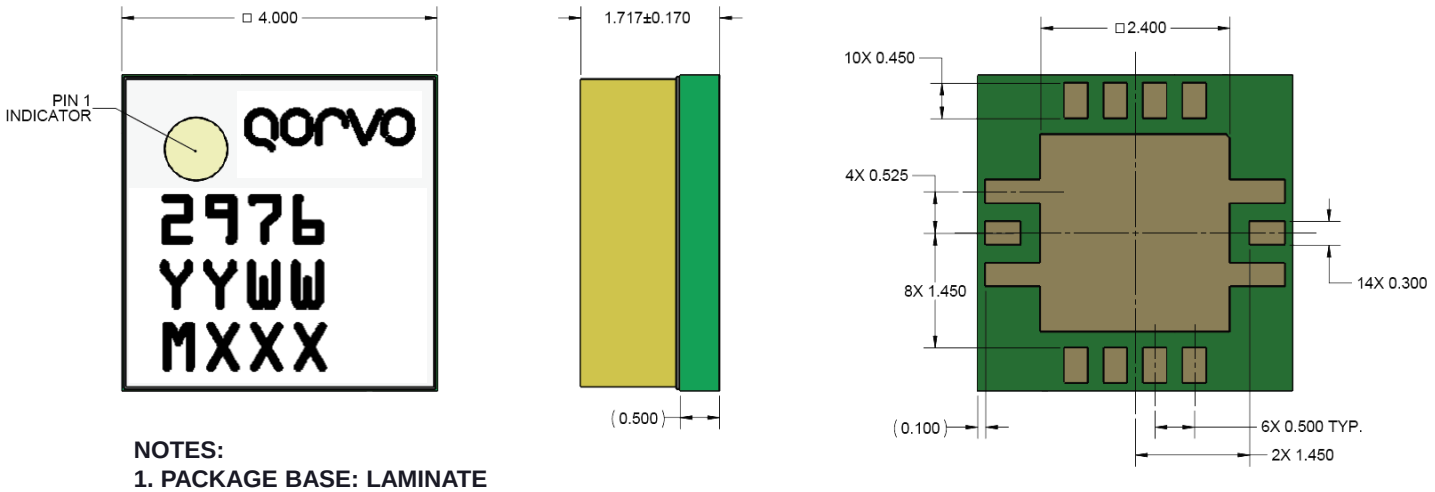
EVB Assembly Drawing (On–Board DC Blocks and Output Bias–T Option)



Bill of Materials for On–Board Bias–T

Reference Des.	Value	Description	Manuf.	Part Number
C1 – C5	1uF	Cap, 1206, 50V, 15%, X7R	Various	
C6 – C12	1000pF	Cap, 0402, 100V, 10%, X7R	Various	
L1	330nH	Inductor, 1206, 850 mA	Various	
R1 – R10	10Ω	Res, 0402, 5%	Various	

Mechanical Drawing and Pad Description



NOTES:
1. PACKAGE BASE: LAMINATE
2. PACKAGE LID: FR4
3. ALL METALIZED FEATURES ARE GOLD PLATED.
4. THE PART IS EPOXY SEALED

Units: millimeters
Tolerances: unless specified
x.xx = ± 0.25
x.xxx = ± 0.100
Marking:
2976: Part Number
YY: Part Assembly Year
WW: Part Assembly Week
MXXX: Batch ID

Pad No.	Symbol	Description
1, 3, 8, 10	GND	Connected to ground paddle (pin 15); must be grounded on PCB.
2	RF IN	Input; matched to 50 Ω.
4, 14	GATE1	Gate voltage1; bias network is required; see recommended Application Information on page 12.
5, 7, 11, 13	N/C	No internal connection; should be connected to PCB ground.
6, 12	GATE2	Gate voltage2; bias network is required; see recommended Application Information on page 12.
9	RF OUT/ DRAIN	Output; matched to 50 Ω.
15	GND	Ground Paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

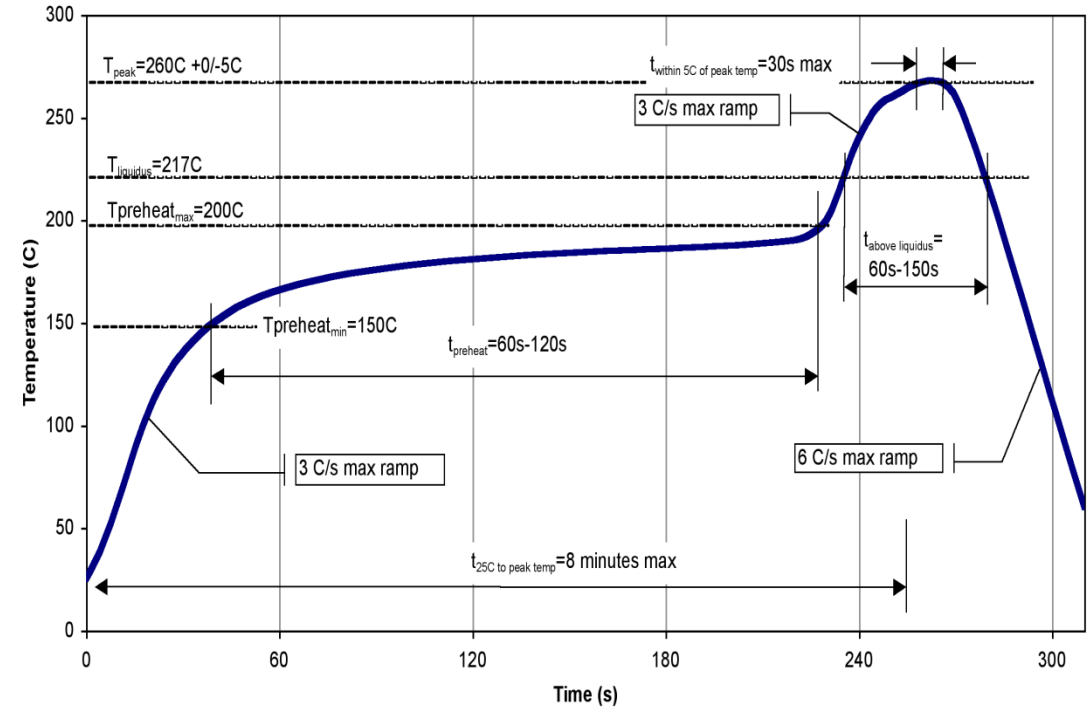
Assembly Notes

Compatible with lead-free soldering processes with 260°C peak reflow temperature.

This package is air-cavity and non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing after soldering is highly recommended.

Contact plating: Ni-Au.

Solder rework not recommended.



Recommended Soldering Temperature Profile