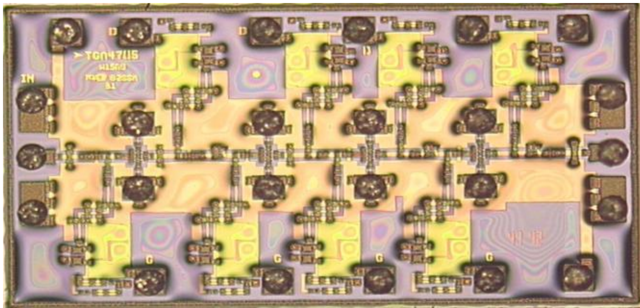
TriQuint SEMICONDUCTOR

TGA4705-FC

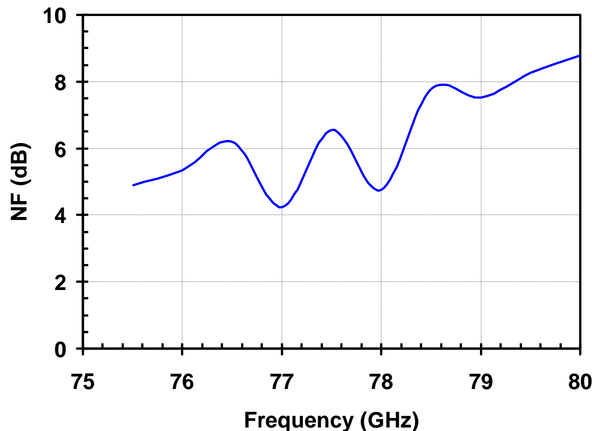
77 GHz Flip-Chip Low Noise Amplifier

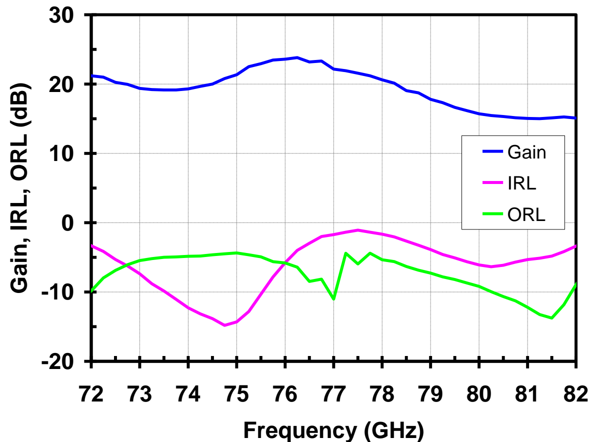


Key Features

- Frequency Range: 72 - 80 GHz
- Noise Figure: 5 dB at 77 GHz
- Gain: 23 dB
- Bias: Vd = 2.5 V, Id = 60 mA, Vg = +0.18 V Typical
- Technology: 0.13 um pHEMT with front-side Cu/Sn pillars
- Chip Dimensions: 2.24 x 1.27 x 0.38 mm

Measured Performance





Primary Applications

- Automotive RADAR

Product Description

The TriQuint TGA4705-FC is a flip-chip low noise amplifier designed to operate at frequencies that target the automotive RADAR market. The TGA4705-FC is designed using TriQuint's proven 0.13 µm pHEMT process and front-side Cu / Sn pillar technology for reduced source inductance and superior noise performance at frequencies of 72 – 80 GHz. Die reliability is enhanced by using TriQuint's BCB polymeric passivation process.

The TGA4705-FC is a low noise amplifier that typically provides 23 dB small signal gain with 5 dB noise figure at 77 GHz. The TGA4705-FC is an excellent choice for applications requiring low noise in receive chain architectures.

Lead-free and RoHS compliant.

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Table I
Absolute Maximum Ratings 1/

Symbol	Parameter	Value	Notes
Vd-Vg	Drain to Gate Voltage	5.5 V	
Vd	Drain Voltage	4 V	2/
Vg	Gate Voltage Range	-1 to + 0.45 V	
Id	Drain Current	108 mA	2/
Ig	Gate Current Range	-0.24 to +0.25 mA	
Pin	Input Continuous Wave Power	10 dBm	2/
Tchannel	Max Channel Temperature	200 C	

1/ These ratings represent the maximum operable values for this device. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device and / or affect device lifetime. These are stress ratings only, and functional operation of the device at these conditions is not implied.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed the maximum power dissipation listed in Table IV.

Table II
Recommended Operating Conditions

Symbol	Parameter 1/	Value
Vd	Drain Voltage	2.5 V
Id	Drain Current	60 mA
Vg	Gate Voltage	+0.18 V Typical

1/ See assembly diagram for bias instructions.

Table III
RF Characterization Table
Bias: Vd = 2.5 V, Id = 60 mA, Vg = 0.18 V, typical

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	NOMINAL	MAX	UNITS
Gain	Small Signal Gain	f = 76 –77 GHz	17	23	26	dB
IRL	Input Return Loss	f = 76 - 77 GHz	3	8	-	dB
ORL	Output Return Loss	f = 76 - 77 GHz	5	10	-	dB
NF	Noise Figure	f = 76 - 77 GHz	-	6	-	dB

Table IV
Power Dissipation and Thermal Properties

Parameter	Test Conditions	Value	Notes
Maximum Power Dissipation	Tbaseplate = 102.5 C	Pd = 0.432 W Tchannel = 150 C Tm = 2.4E+7 Hrs	1/ 2/ 3/
Thermal Resistance, θjc	Vd = 2 V Id = 60 mA Pd = 0.12 W Tbaseplate = 85 C	θjc = 110 C/W Tchannel = 98.2 C Tm = 1.68E+10 Hrs	3/
Mounting Temperature		Refer to Solder Reflow Profiles (pg 11)	
Storage Temperature		-65 to 150 C	

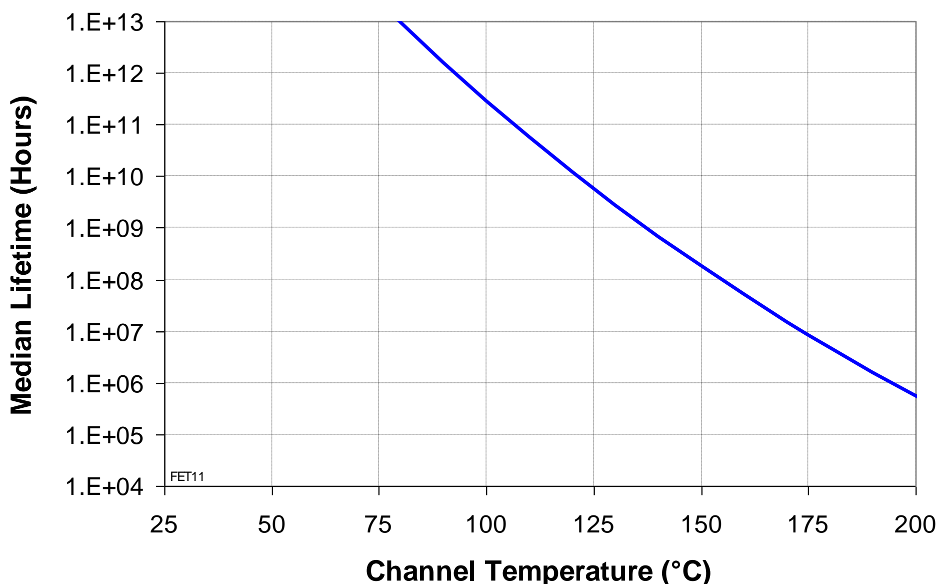
1/ For a median life of 2.4E+7 hours, Power Dissipation is limited to

Pd(max) = (150 °C – Tbase °C)/θjc.

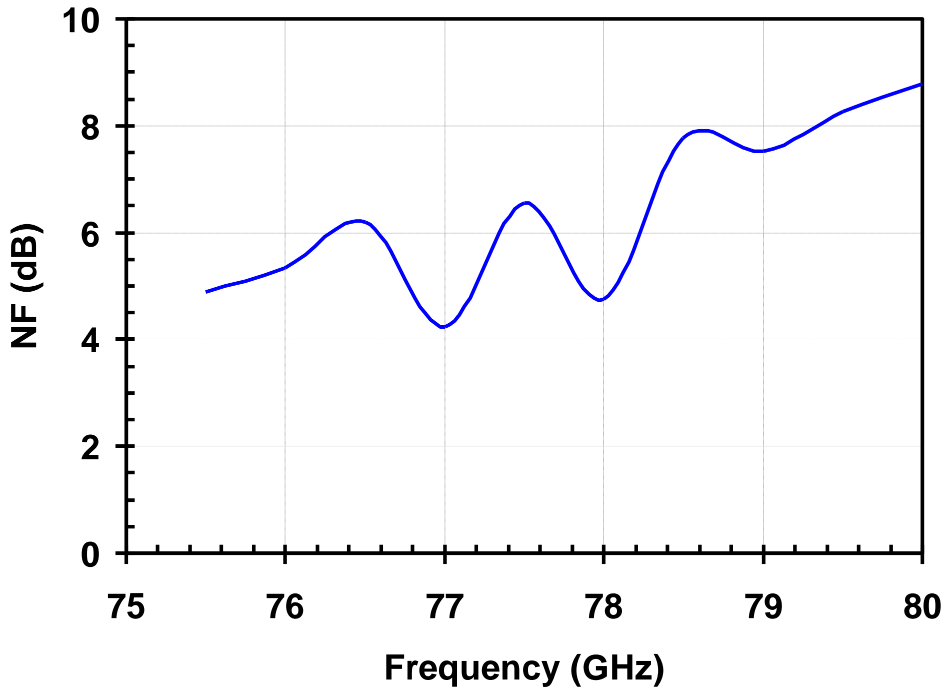
2/ Channel operating temperature will directly affect the device median lifetime (Tm). For maximum life, it is recommended that channel temperatures be maintained at the lowest possible levels.

3/ For this flip-chip die, the baseplate is a plane between the Cu/Sn pillars and the test board. For the TGA4705-FC, the critical pillars for thermal power dissipation are 18 thru 25. (See Mechanical Drawing.)

Median Lifetime (Tm) vs Channel Temperature



Measured Data on Face-down (flipped) Die on Carrier Board



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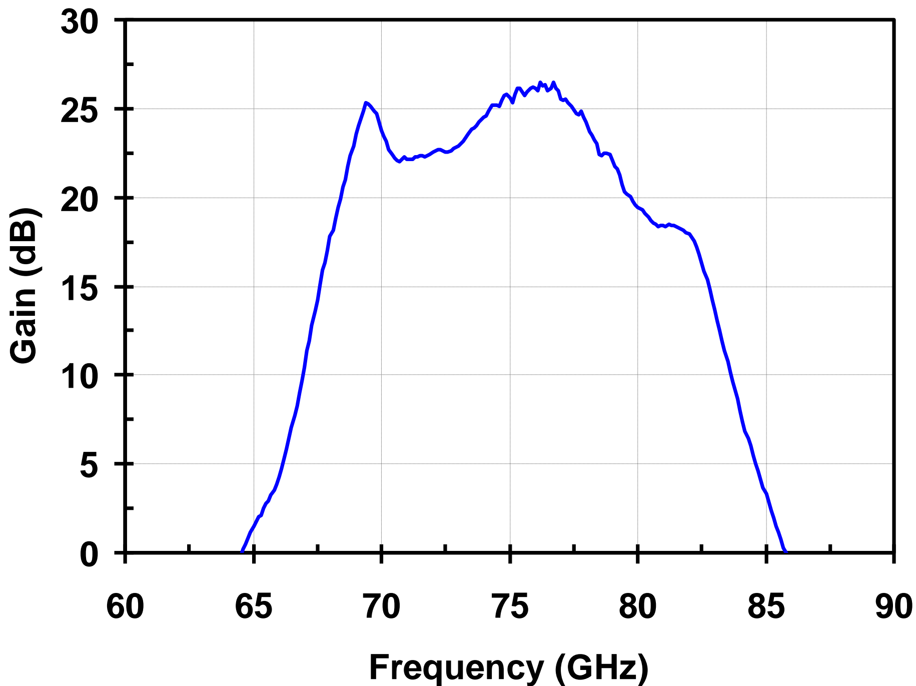
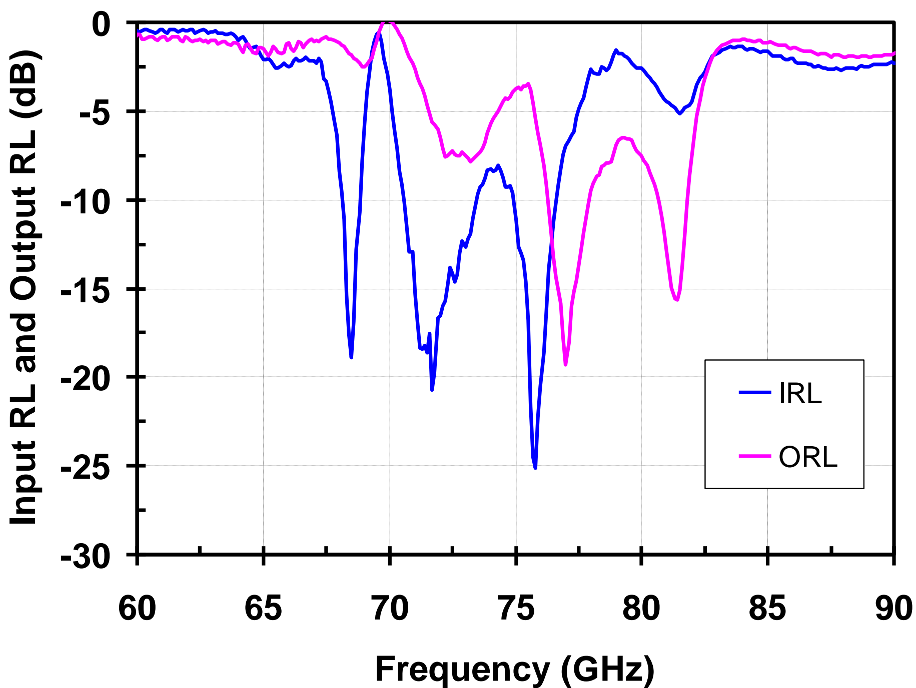
Measured Data on Face-down (flipped) Die on Carrier Board

Bias conditions: Vd = 2 V, Id = 60 mA





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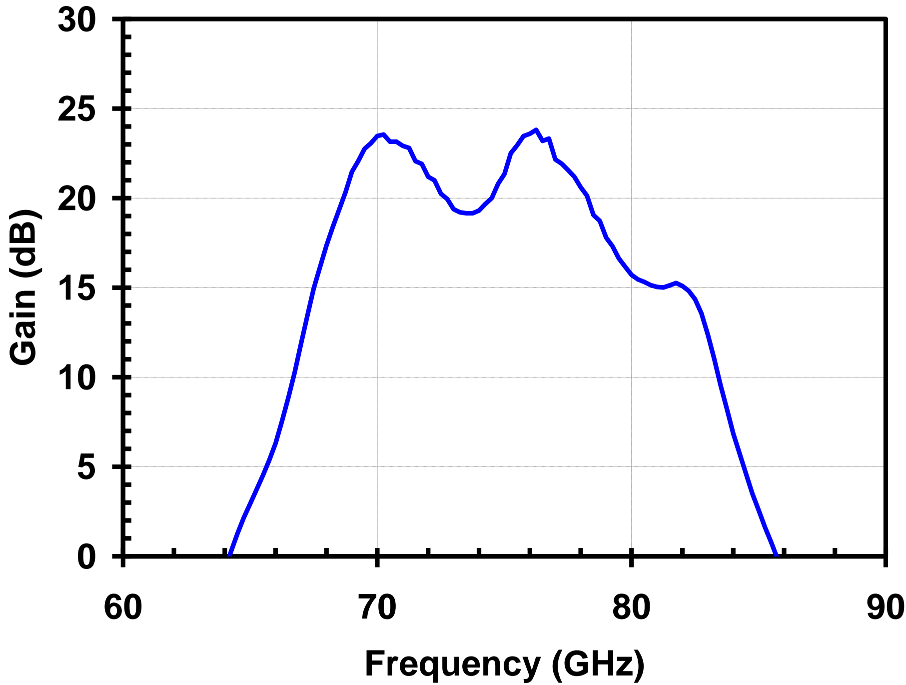
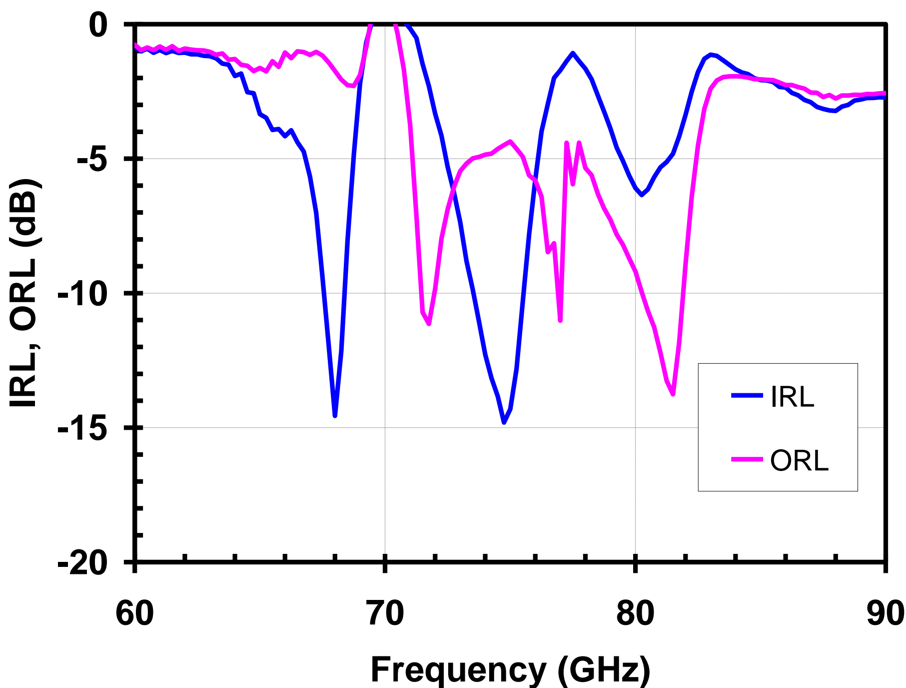
Measured Data on Face-down (flipped) Die on Carrier Board

Bias conditions: Vd = 2.5 V, Id = 60 mA





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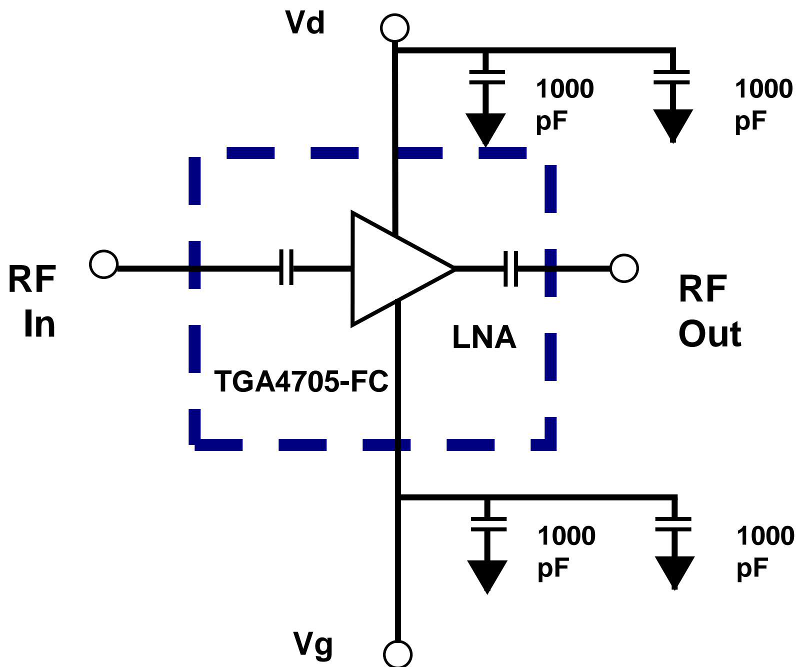
Electrical Schematic



Bias Procedures

Bias-up Procedure

Vg set to -0.5 V

Vd set to +2.5 V

Adjust Vg more positive until Id is 60 mA. This will be Vg ~ +0.18 V

Apply RF signal to input

Bias-down Procedure

Turn off RF supply

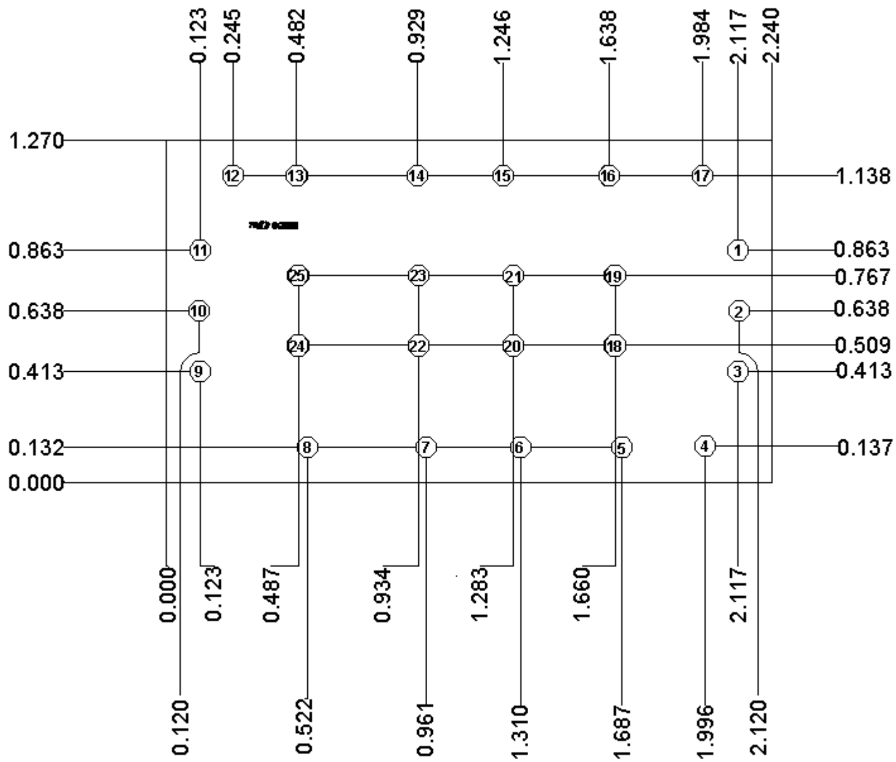
Reduce Vg to -0.5V. Ensure Id ~ 0 mA

Turn Vd to 0 V

Turn Vg to 0 V

Mechanical Drawing

Drawing is for chip face-up



Units: millimeters

Thickness: 0.380

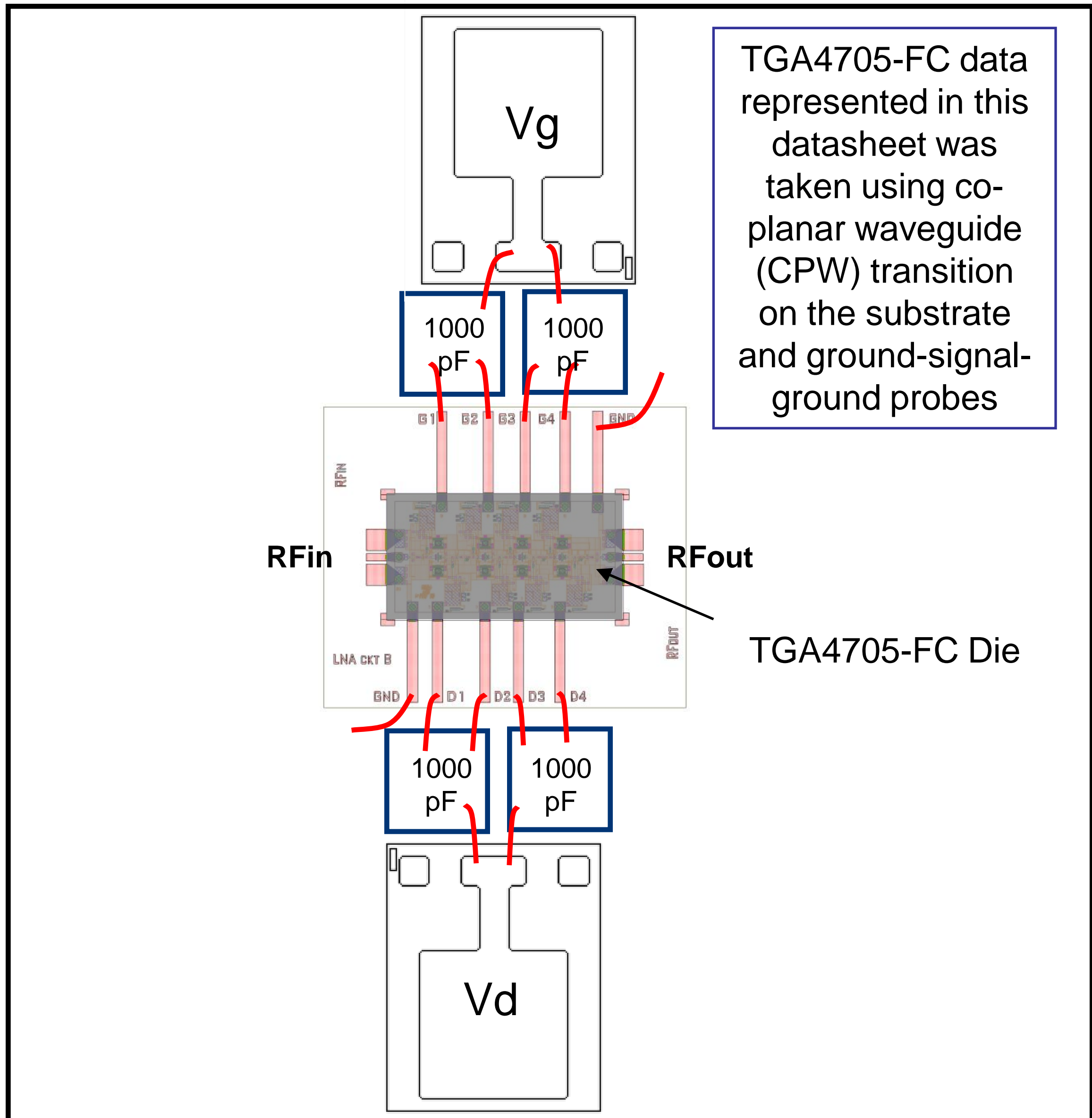
Die x,y size tolerance: +/- 0.050

Chip edge to pillar dimensions are shown to center of pillar

Pillar #4,12,18-25	DC Ground	0.075 Ø	Pillar #5	Vg4	0.075 Ø
Pillar #1, 3, 9, 11	RF CPW Ground	0.075 Ø	Pillar #13	Vd1	0.075 Ø
Pillar #2	RF Out	0.075 Ø	Pillar #14	Vd2	0.075 Ø
Pillar #10	RF In	0.075 Ø	Pillar #15	Vd3	0.075 Ø
Pillar #8	Vg1	0.075 Ø	Pillar #16	Vd4	0.075 Ø
Pillar #7	Vg2	0.075 Ø	Pillar #17	Mech. Support Only	0.075 Ø
Pillar #6	Vg3	0.075 Ø			

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Recommended Assembly Diagram



Die is flip-chip soldered to a 15 mil thick alumina test substrate

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