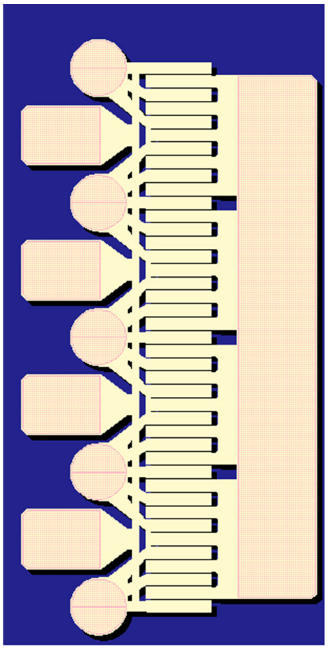
TGF2023-2-05

25 Watt Discrete Power GaN on SiC HEMT

Applications

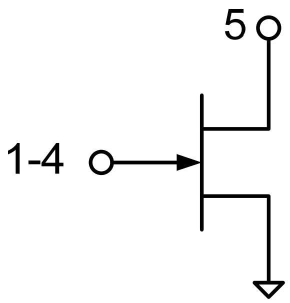
- Defense & Aerospace
- Broadband Wireless



Product Features

- Frequency Range: DC - 18 GHz
- 44.3 dBm Nominal P_{SAT} at 6 GHz
- 64.4% Maximum PAE at 6 GHz
- 17.6 dB Linear Gain at 6 GHz
- Bias: V_D = 12 - 32 V, I_{DQ} = 100 - 250 mA
- Technology: QGaN25 on SiC
- Chip Dimensions: 0.82 x 1.44 x 0.10 mm

Functional Block Diagram



General Description

The Qorvo TGF2023-2-05 is a discrete 5 mm GaN on SiC HEMT which operates from DC-18 GHz. The TGF2023-2-05 is designed using Qorvo's proven QGaN25 production process. This process features advanced field plate techniques to optimize microwave power and efficiency at high drain bias operating conditions.

The TGF2023-2-05 typically provides 44.3 dBm of saturated output power with power gain of 14.6 dB at 6 GHz. The maximum power added efficiency is 64.4 % which makes the TGF2023-2-05 appropriate for high efficiency applications.

Lead-free and RoHS compliant

Pad Configuration

Pad No.	Symbol
1-4	V_G / RF IN
5	V_D / RF OUT
Backside	Source / Ground

Ordering Information

Part	ECCN	Description
TGF2023-2-05	3A001b.3.b	25 Watt GaN HEMT

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Absolute Maximum Ratings

Parameter	Value
Drain to Gate Voltage (V_{DG})	100 V
Gate Voltage Range (V_G)	–10 to 0 V
Drain Current (I_D)	5 A
Gate Current (I_G)	–5 to 14 mA
Power Dissipation, CW (P_D)	See graph on pg.5.
CW Input Power (P_{IN})	+37 dBm
Channel Temperature (T_{CH})	275 °C
Mounting Temperature	320 °C
Storage Temperature	–65 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions[1]

Parameter	Value
Drain Voltage Range (V_D)	12 - 40 V
Drain Quiescent Current (I_{DQ})	250 mA
Drain Current Under RF Drive (I_D)[2]	0.5 A (Typ.)
Gate Voltage (V_G)	–3.0 V (Typ.)
Channel Temperature (T_{CH})	225 °C (Max.)
Dissipation Power, CW (P_D)	16 W
Dissipation Power, Pulsed (P_D)[2,3]	17.5 W

1. Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.
2. 2.66 mS Pulse Width, 10% Duty Cycle
3. Carrier plate temperature is at 85 °C.

Model RF Characterization – Optimum Power Tune

Simulation conditions: T = 25 °C, Signal Duty Cycle = 10%

Parameter	Typical Value								Units
Frequency (F)	3		6		8		10		GHz
Drain Voltage (V_D)	28	28	28	28	28	28	28	28	V
Bias Current (I_{DQ})	100	250	100	250	100	250	100	250	mA
Output P3dB (P_{3dB})	44.2	44.1	44.4	44.3	44.4	44.3	44.4	44.3	dBm
PAE @ P_{3dB} (PAE_{3dB})	61.7	60.9	60	59.2	57.4	57.5	55.3	55.4	%
Gain @ P3dB (G_{3dB})	19.1	20	13.8	14.6	11.5	12.2	9.7	10.4	dB
Parallel Resistance (1) (R_p)	63.5	63.6	61.4	60.6	57.9	58	53.1	52.6	Ω·mm
Parallel Capacitance (1) (C_p)	0.268	0.275	0.297	0.303	0.297	0.303	0.320	0.325	pF/mm
Load Reflection Coefficient (2) (Γ_L)	0.44∠17°	0.44∠17°	0.46∠37°	0.45∠37°	0.46∠48°	0.46∠49°	0.47∠62°	0.47∠63°	--

Notes:
1. Large signal equivalent output network (normalized).
2. Characteristic Impedance (Zo) = 5 Ω.

Model RF Characterization – Optimum Efficiency Tune

Simulation conditions: T = 25 °C, Signal Duty Cycle = 10%

Parameter	Typical Value								Units
Frequency (F)	3		6		8		10		GHz
Drain Voltage (V_D)	28	28	28	28	28	28	28	28	V
Bias Current (I_{DQ})	100	250	100	250	100	250	100	250	mA
Output P3dB (P_{3dB})	42.7	42.7	43.1	43.1	43.1	43.1	43.3	43.3	dBm
PAE @ P_{3dB} (PAE_{3dB})	67.1	65.9	65.1	64.4	63	62.7	60.3	60.4	%
Gain @ P3dB (G_{3dB})	20.8	21.5	15.2	15.8	12.8	13.3	10.8	11.5	dB
Parallel Resistance (1) (R_p)	115	112	103	98.6	98.9	93.9	84.5	82.7	Ω·mm
Parallel Capacitance (1) (C_p)	0.347	0.340	0.361	0.359	0.368	0.369	0.368	0.373	pF/mm
Load Reflection Coefficient (2) (Γ_L)	0.65∠19°	0.64∠19°	0.64∠40°	0.63∠40°	0.66∠48°	0.64∠52°	0.64∠63°	0.64∠64°	--

Notes:
1. Large signal equivalent output network (normalized).
2. Characteristic Impedance (Zo) = 5 Ω.

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Thermal and Reliability - CW (1)

Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC}	P_D = 3 W, Tbaseplate = 85°C	9.3	°C/W
Channel Temperature, T_{CH}		113	°C
Median Lifetime, T_M		2.5E11	Hrs
Thermal Resistance, θ_{JC}	P_D = 6W,Tbaseplate = 85°C	10	°C/W
Channel Temperature, T_{CH}		145	°C
Median Lifetime, T_M		4.4E9	Hrs
Thermal Resistance, θ_{JC}	P_D = 9 W, Tbaseplate = 85°C	10.8	°C/W
Channel Temperature, T_{CH}		182	°C
Median Lifetime, T_M		8.6E7	Hrs
Thermal Resistance, θ_{JC}	P_D = 12 W, Tbaseplate = 85°C	11.8	°C/W
Channel Temperature, T_{CH}		226	°C
Median Lifetime, T_M		1.7E6	Hrs
Thermal Resistance, θ_{JC}	P_D = 15 W, Tbaseplate = 85°C	12.9	°C/W
Channel Temperature, T_{CH}		278	°C
Median Lifetime, T_M		3.6E4	Hrs

Notes:
1. Assumes eutectic attach using 1.5 mil thick 80/20 AuSn mounted to a 10 mm x 10 mm x 40 mil CuMo Carrier Plate.

Thermal and Reliability - Pulsed (1)

Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC}	P_D = 17.5 W, Tbaseplate = 85°C Pulse Width = 100 uS Duty Cycle = 5%	4.7	°C/W
Channel Temperature, T_{CH}		168	°C
Median Lifetime, T_M		7.1E9	Hrs
Thermal Resistance, θ_{JC}	P_D = 17.5 W, Tbaseplate = 85°C Pulse Width = 100 uS Duty Cycle = 10%	5.0	°C/W
Channel Temperature, T_{CH}		172	°C
Median Lifetime, T_M		2.3E9	Hrs
Thermal Resistance, θ_{JC}	P_D = 17.5 W, Tbaseplate = 85°C Pulse Width = 100 uS Duty Cycle = 20%	5.3	°C/W
Channel Temperature, T_{CH}		177	°C
Median Lifetime, T_M		6.9E8	Hrs
Thermal Resistance, θ_{JC}	P_D = 17.5 W, Tbaseplate = 85°C Pulse Width = 100 uS Duty Cycle = 50%	6.6	°C/W
Channel Temperature, T_{CH}		200	°C
Median Lifetime, T_M		3.1E7	Hrs

Notes:
1. Assumes eutectic attach using 1.5 mil thick 80/20 AuSn mounted to a 10 mm x 10 mm x 40 mil CuMo Carrier Plate.

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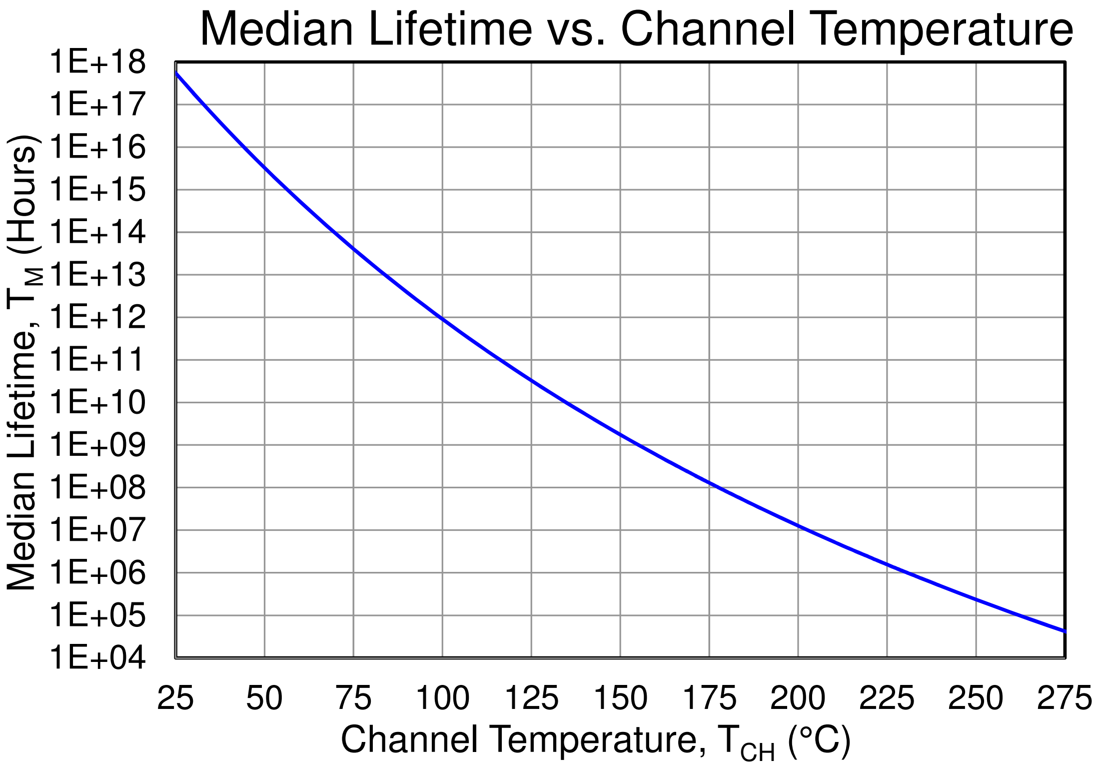
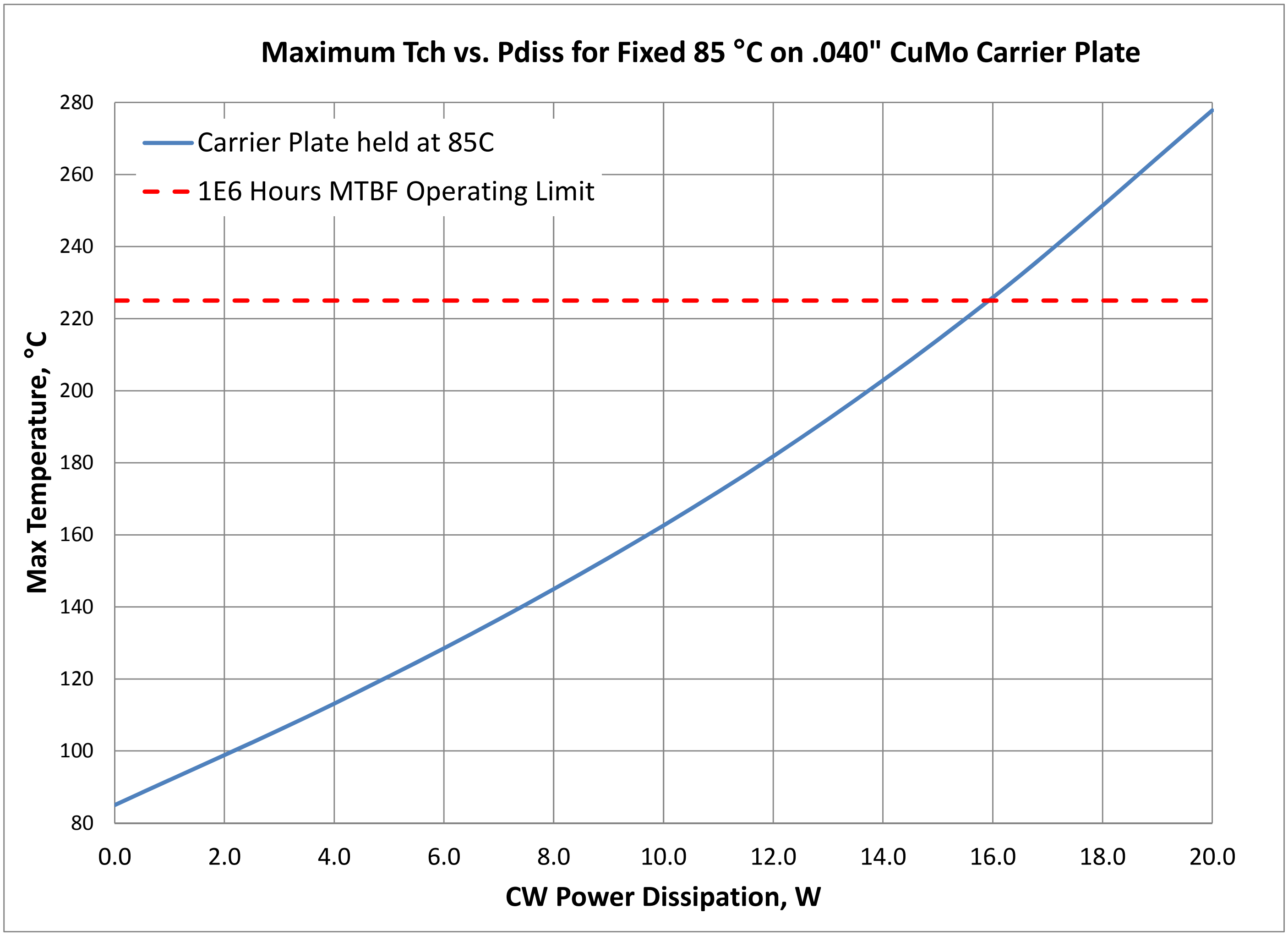
Median Lifetime



Maximum Channel Temperature - CW



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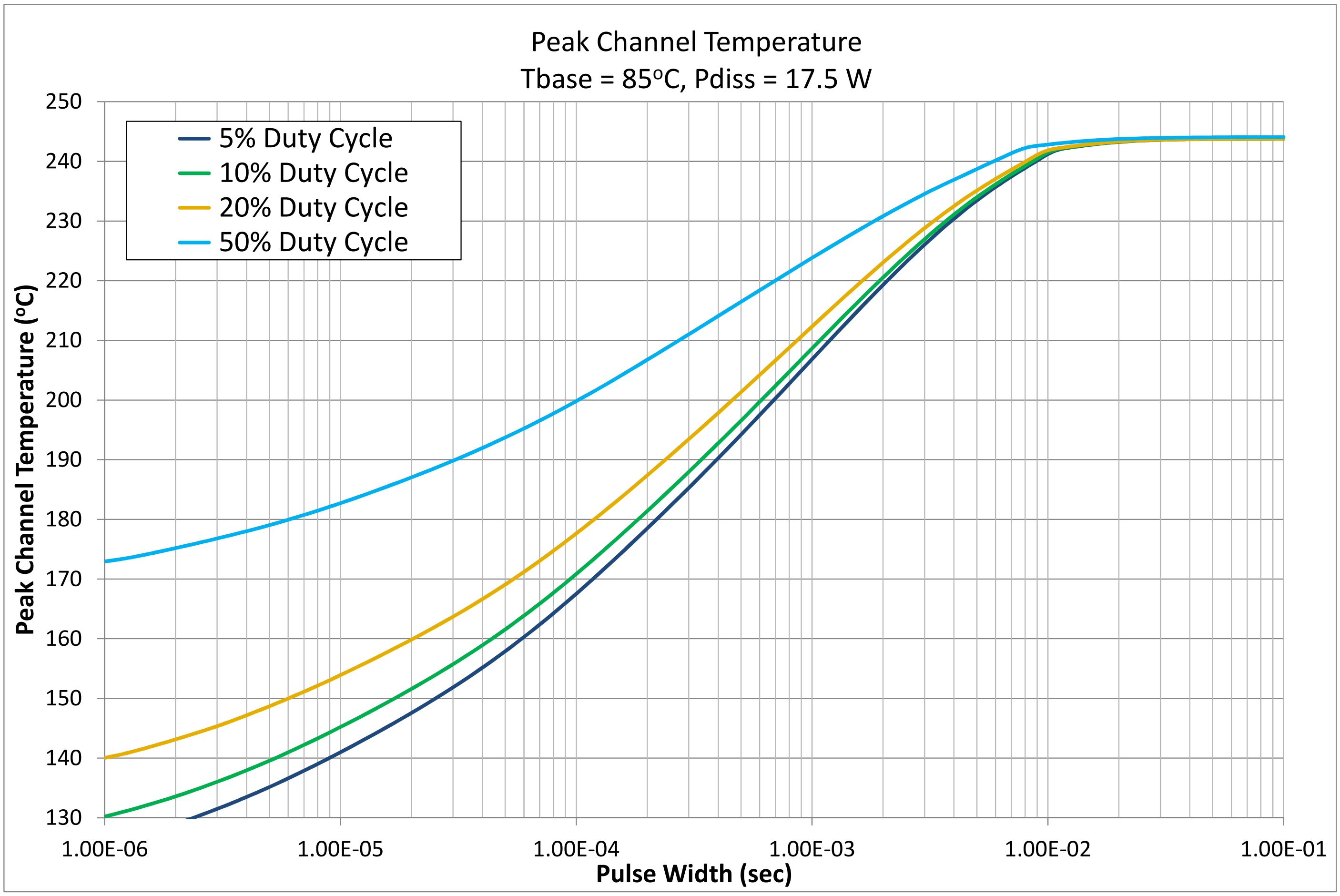
Peak Channel Temperature - Pulsed



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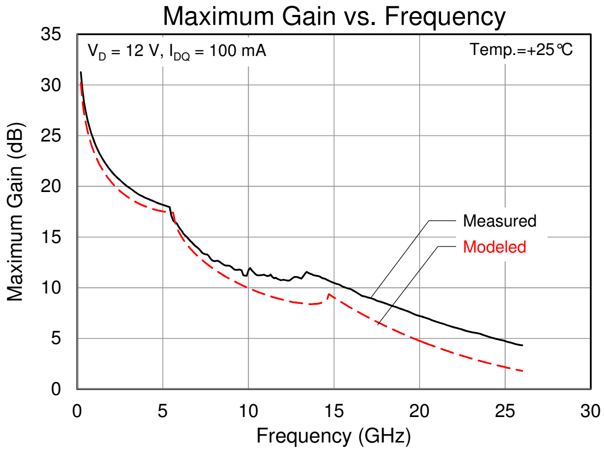
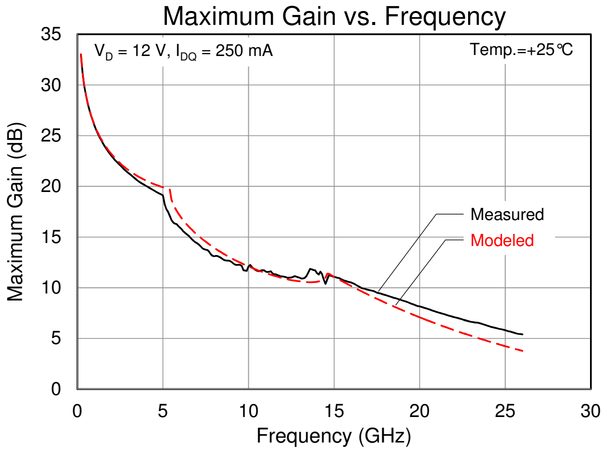
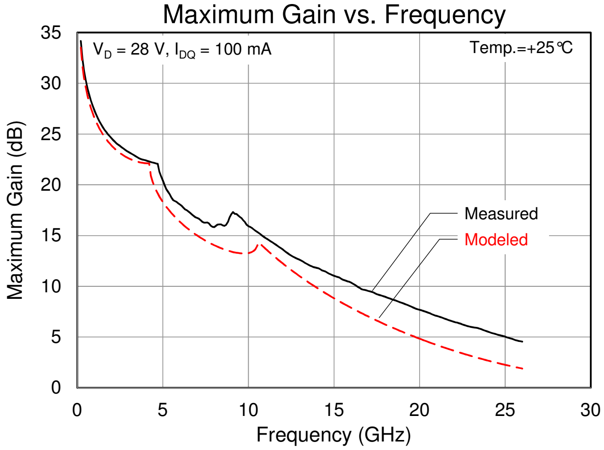
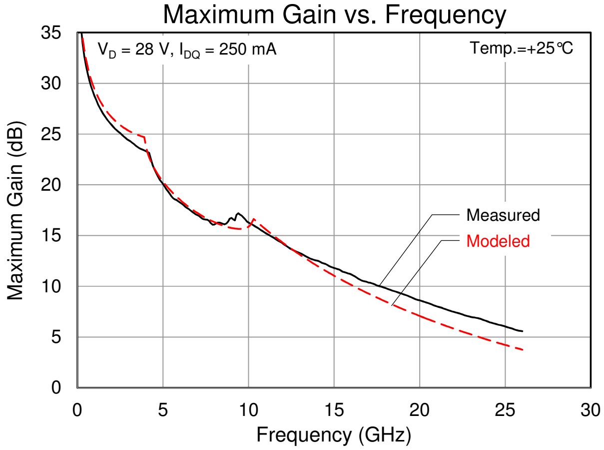
Maximum Gain Performance









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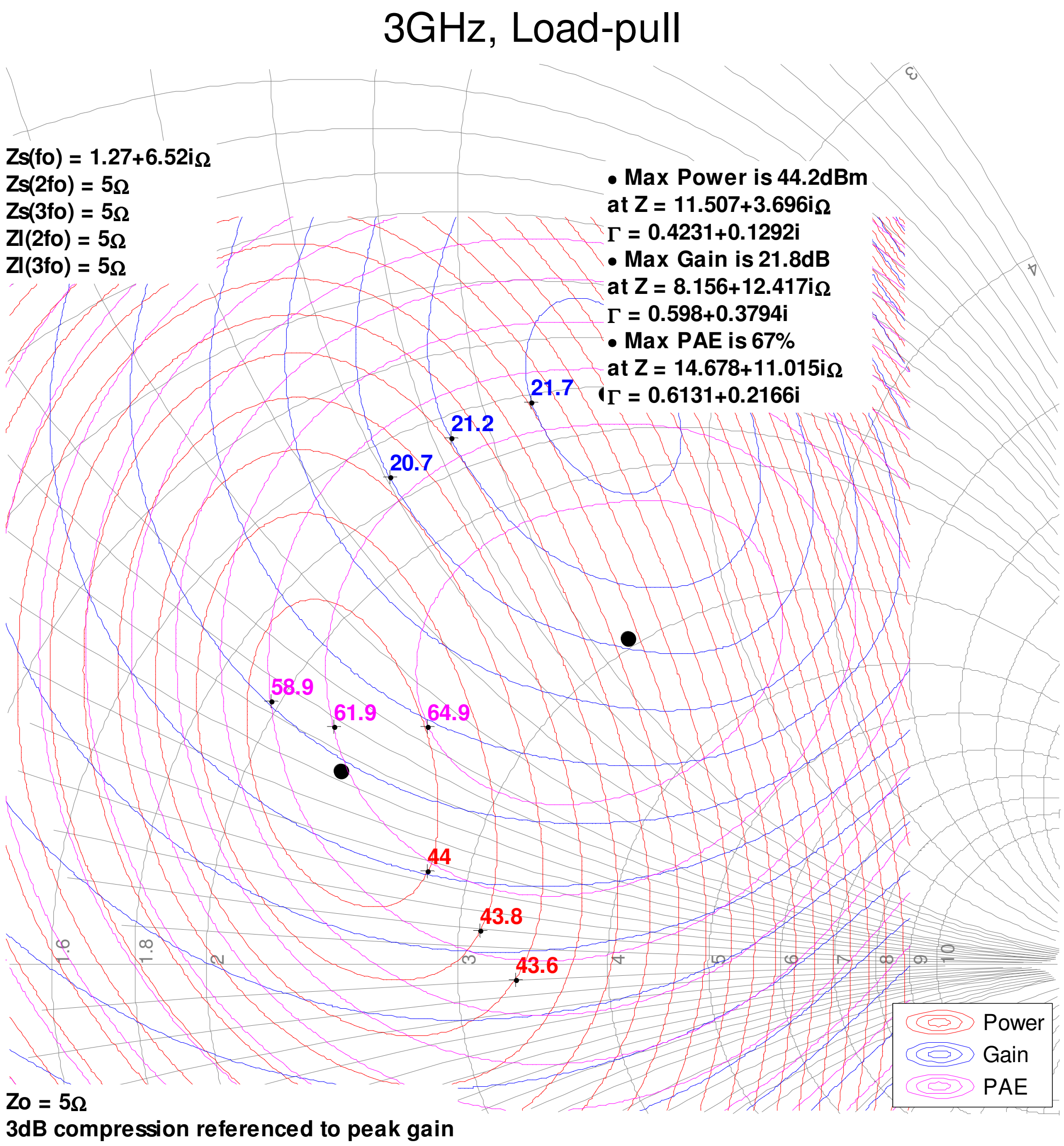
Model Load Pull Contours – 3 GHz

Simulated signal: 10% pulses
Vd = 28 V, Idq = 100 mA



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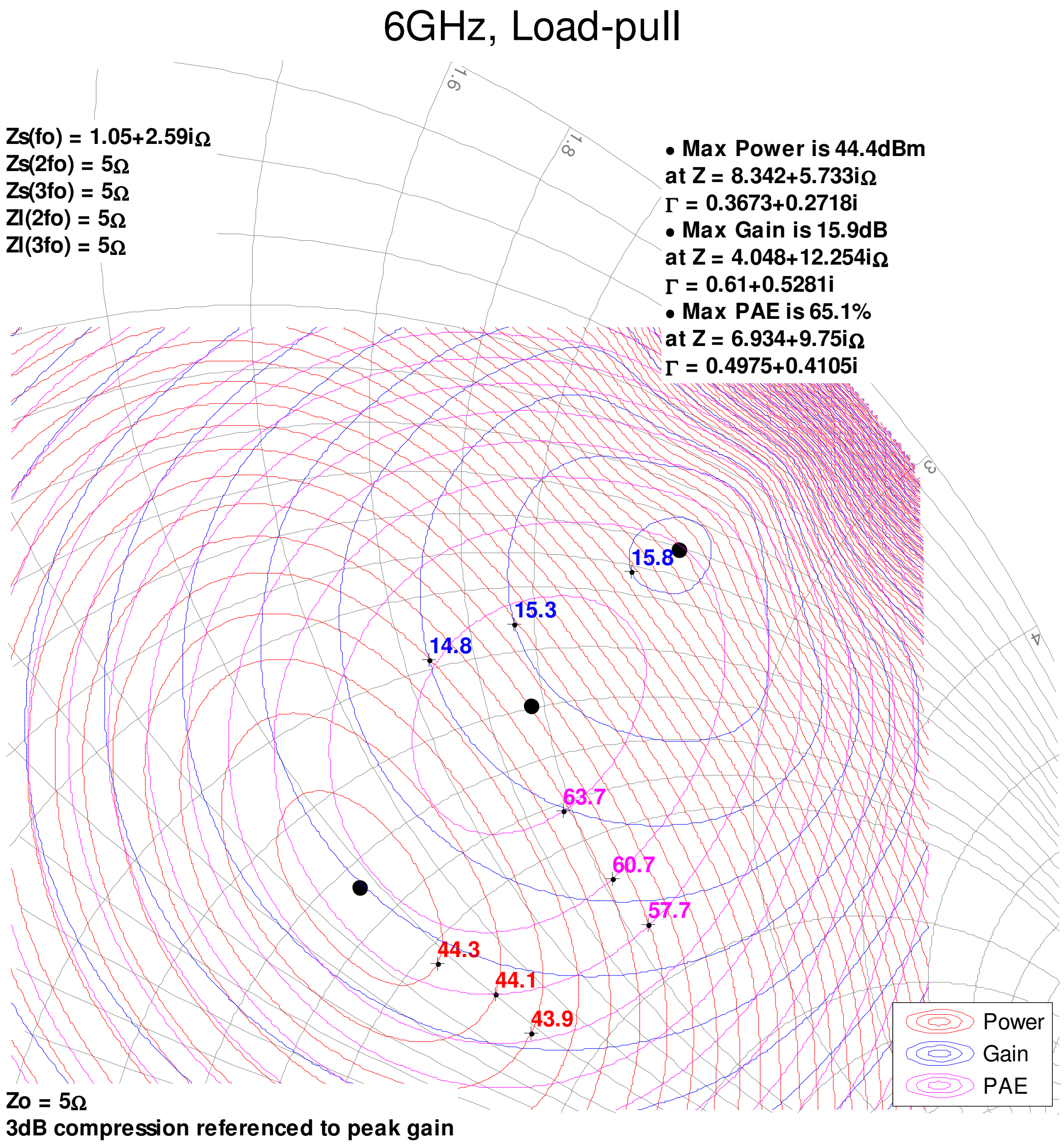
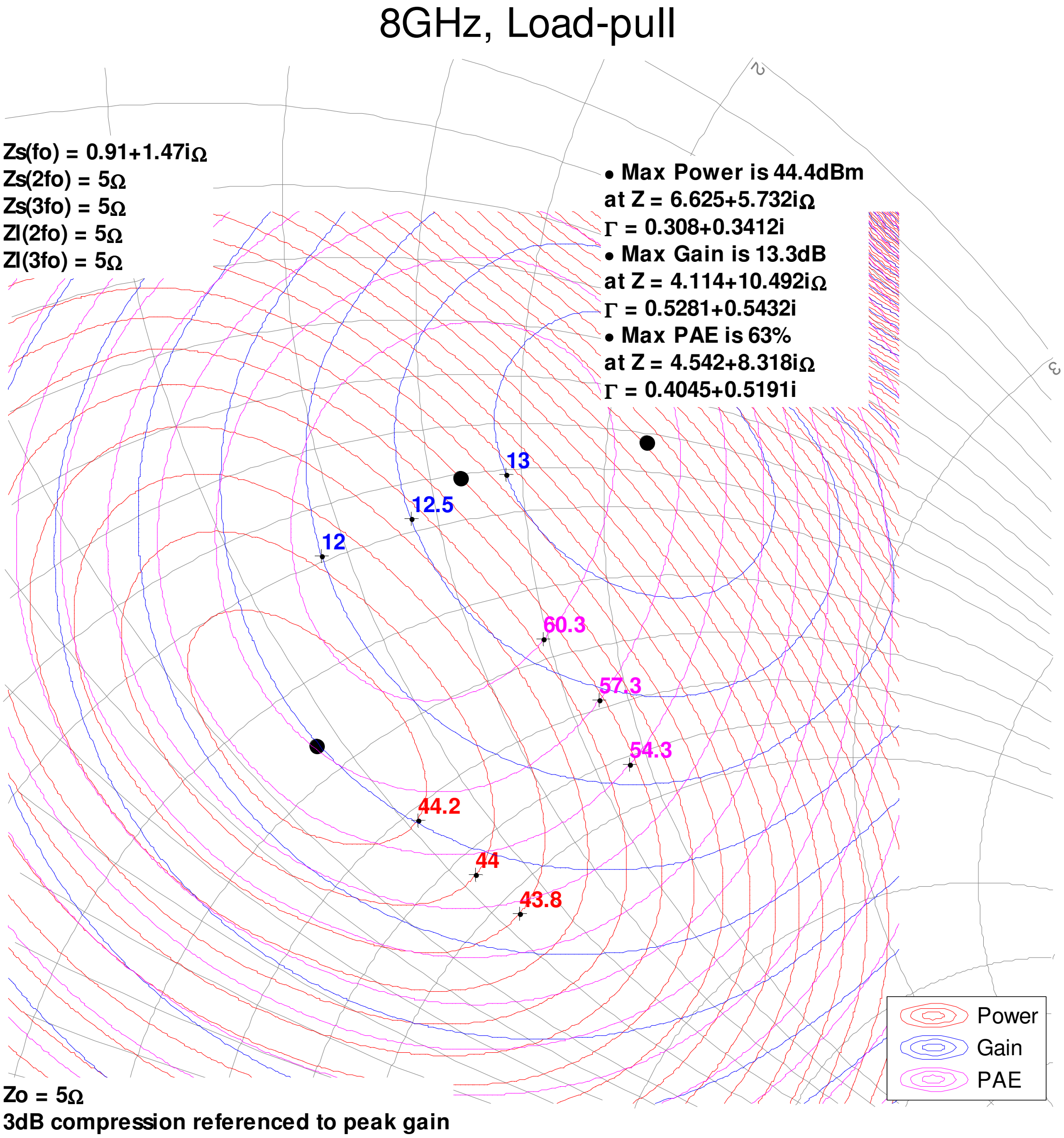
Model Load Pull Contours – 6 GHz

Simulated signal: 10% pulses
Vd = 28 V, Idq = 100 mA



Model Load Pull Contours – 8 GHz

Simulated signal: 10% pulses
Vd = 28 V, Idq = 100 mA



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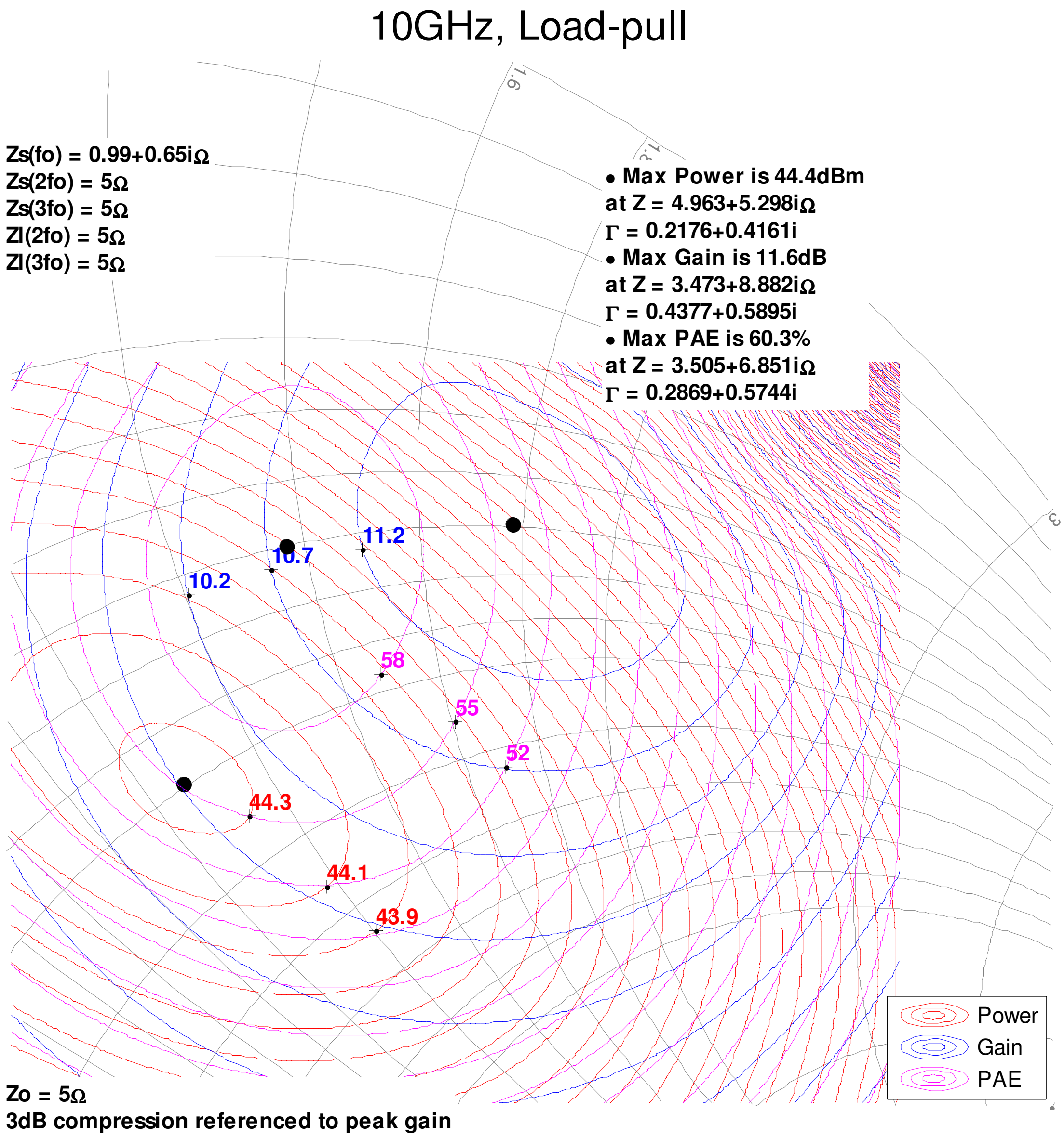
Model Load Pull Contours – 10 GHz

Simulated signal: 10% pulses
Vd = 28 V, Idq = 100 mA



10GHz, Load-pull

Zs(fo) = 0.99+0.65iΩ
Zs(2fo) = 5Ω
Zs(3fo) = 5Ω
Zl(2fo) = 5Ω
Zl(3fo) = 5Ω

- **Max Power is 44.4dBm**

at Z = 4.963+5.298iΩ
Γ = 0.2176+0.4161i

- **Max Gain is 11.6dB**

at Z = 3.473+8.882iΩ
Γ = 0.4377+0.5895i

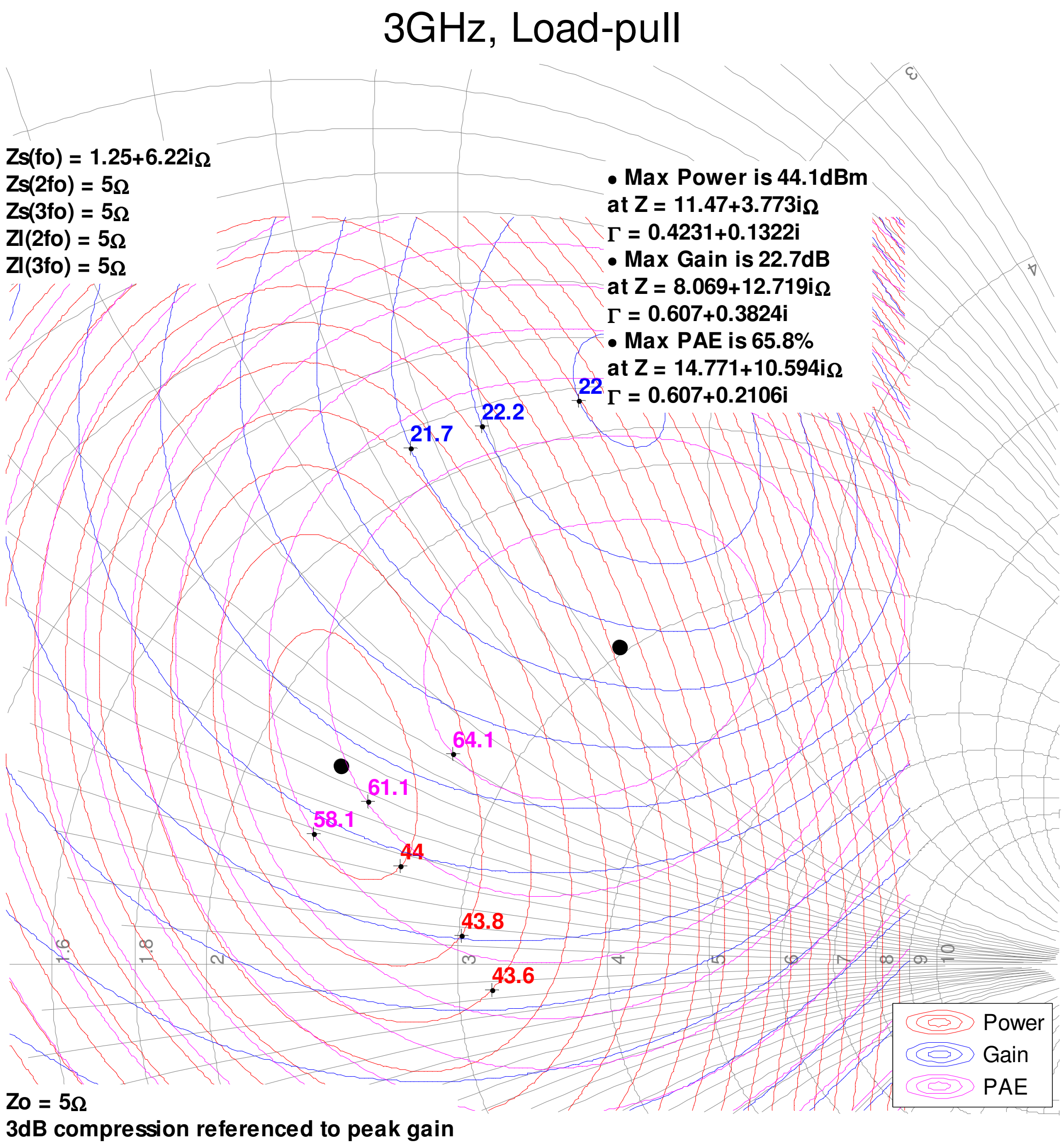
- **Max PAE is 60.3%**

at Z = 3.505+6.851iΩ
Γ = 0.2869+0.5744i

Zo = 5Ω
3dB compression referenced to peak gain

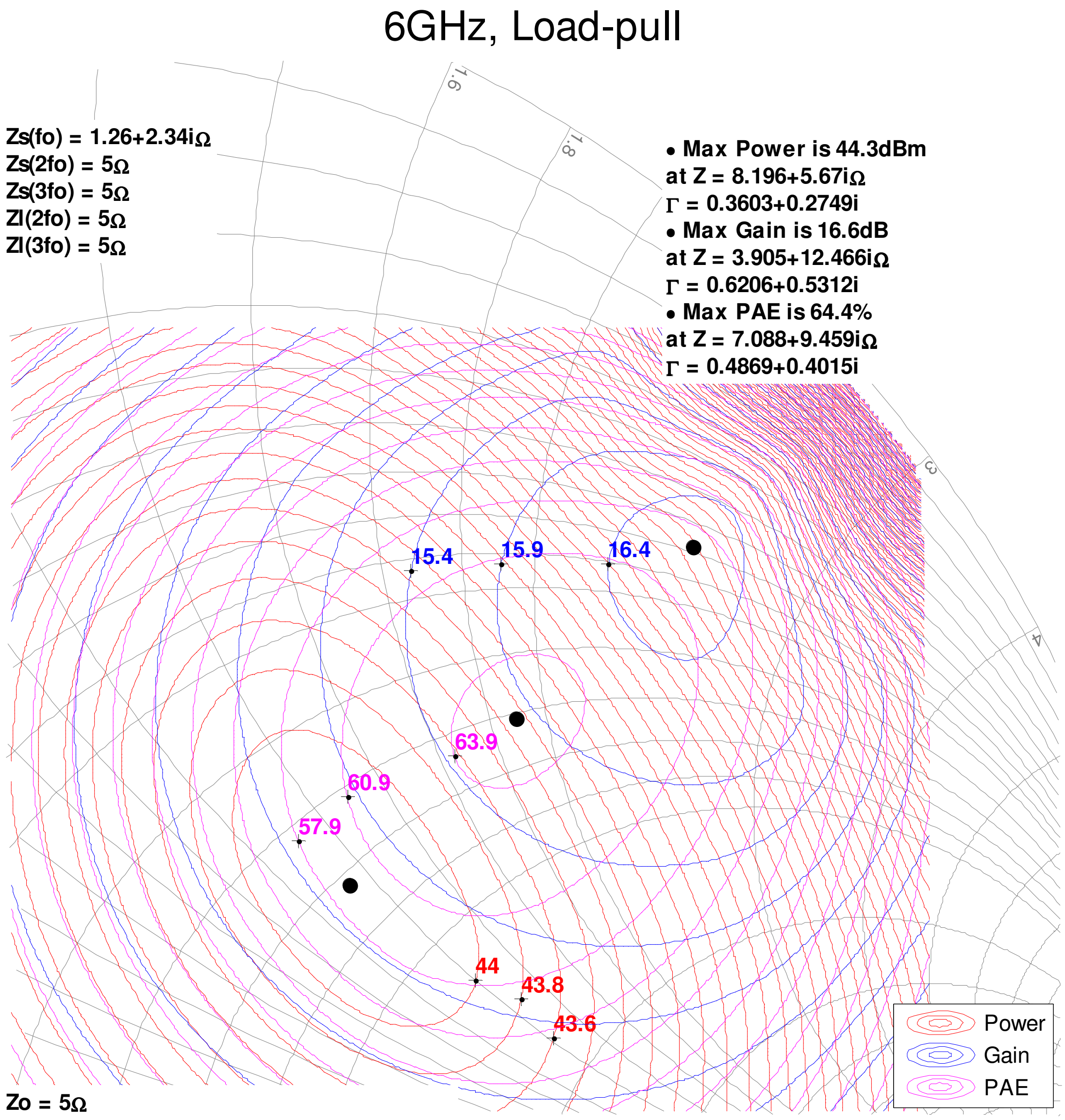
Model Load Pull Contours – 3 GHz

Simulated signal: 10% pulses
Vd = 28 V, Idq = 250 mA



Model Load Pull Contours – 6 GHz

Simulated signal: 10% pulses
Vd = 28 V, Idq = 250 mA



6GHz, Load-pull

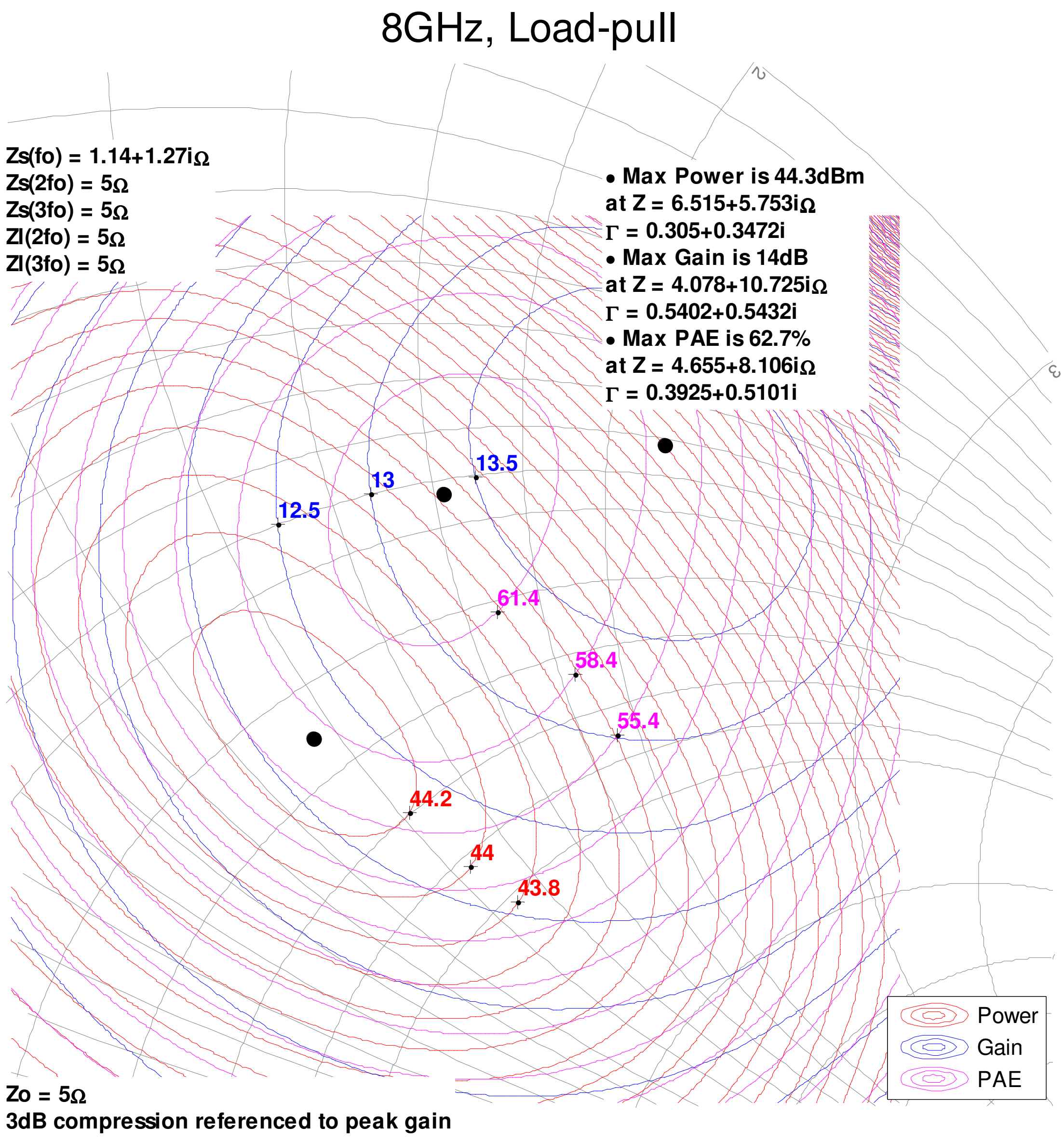
Zs(fo) = 1.26+2.34iΩ
Zs(2fo) = 5Ω
Zs(3fo) = 5Ω
Zl(2fo) = 5Ω
Zl(3fo) = 5Ω

• Max Power is 44.3dBm
at Z = 8.196+5.67iΩ
Γ = 0.3603+0.2749i
• Max Gain is 16.6dB
at Z = 3.905+12.466iΩ
Γ = 0.6206+0.5312i
• Max PAE is 64.4%
at Z = 7.088+9.459iΩ
Γ = 0.4869+0.4015i

Zo = 5Ω
3dB compression referenced to peak gain

Model Load Pull Contours – 8 GHz

Simulated signal: 10% pulses
Vd = 28 V, Idq = 250 mA



Zs(fo) = 1.14+1.27iΩ
Zs(2fo) = 5Ω
Zs(3fo) = 5Ω
Zl(2fo) = 5Ω
Zl(3fo) = 5Ω

• Max Power is 44.3dBm
at Z = 6.515+5.753iΩ
Γ = 0.305+0.3472i
• Max Gain is 14dB
at Z = 4.078+10.725iΩ
Γ = 0.5402+0.5432i
• Max PAE is 62.7%
at Z = 4.655+8.106iΩ
Γ = 0.3925+0.5101i

Zo = 5Ω
3dB compression referenced to peak gain

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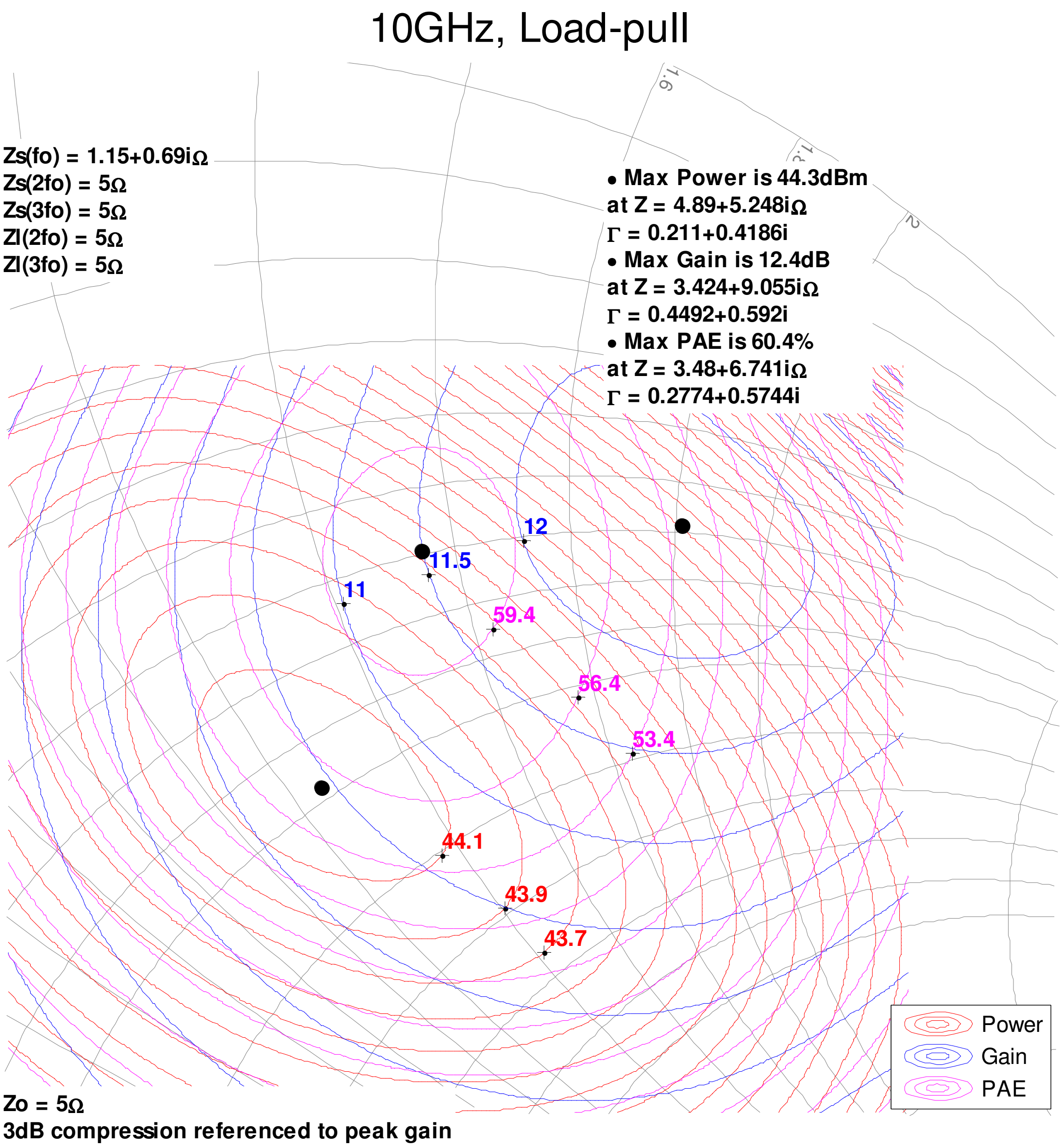
Model Load Pull Contours – 10 GHz

Simulated signal: 10% pulses
Vd = 28 V, Idq = 250 mA



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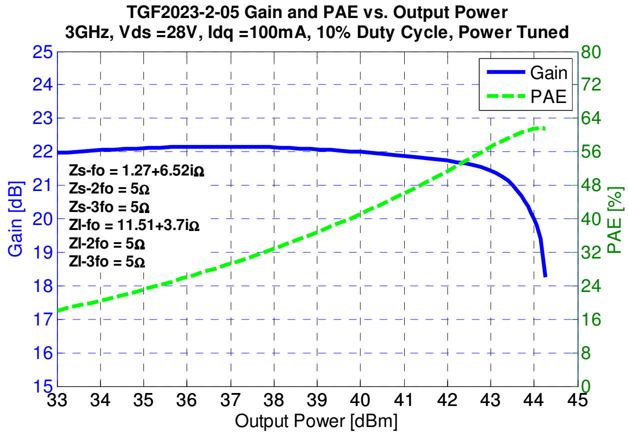
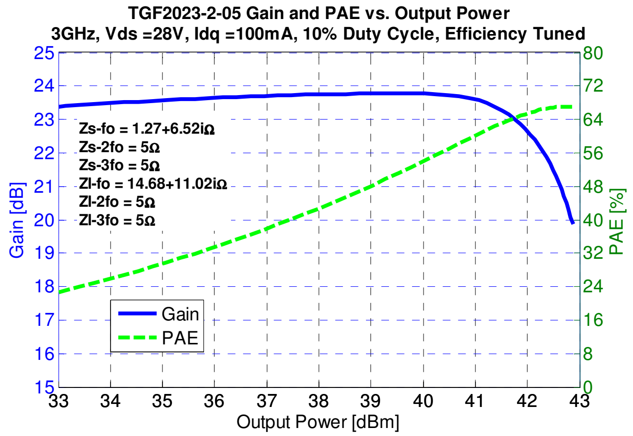
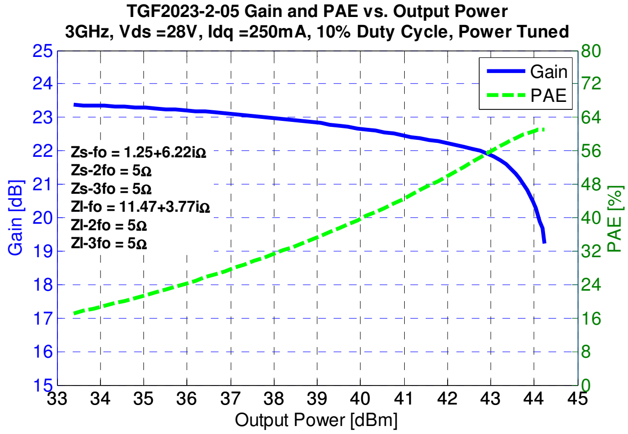
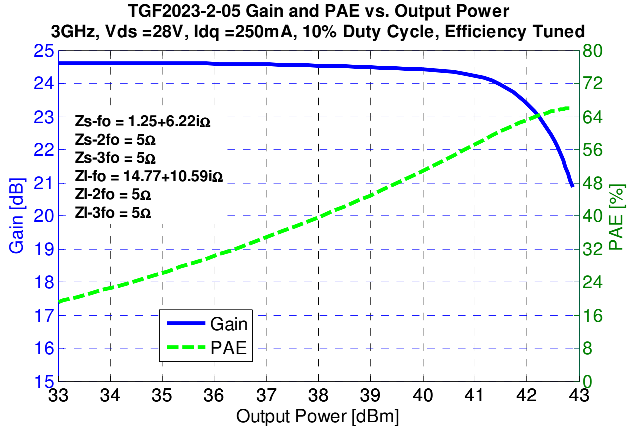
Model Drive-up Data – 3 GHz









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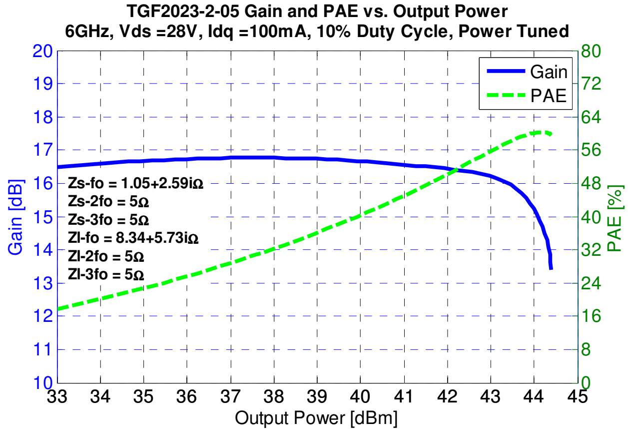
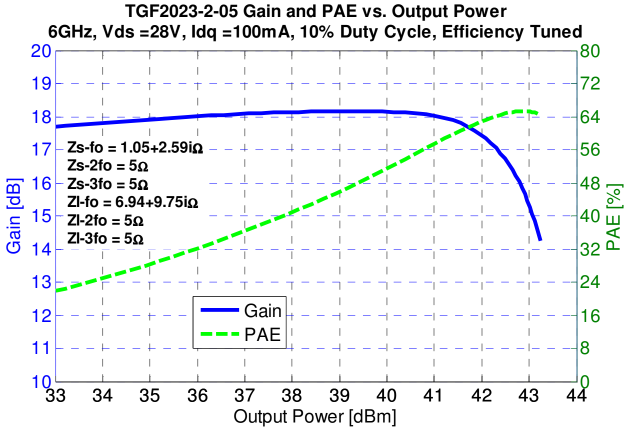
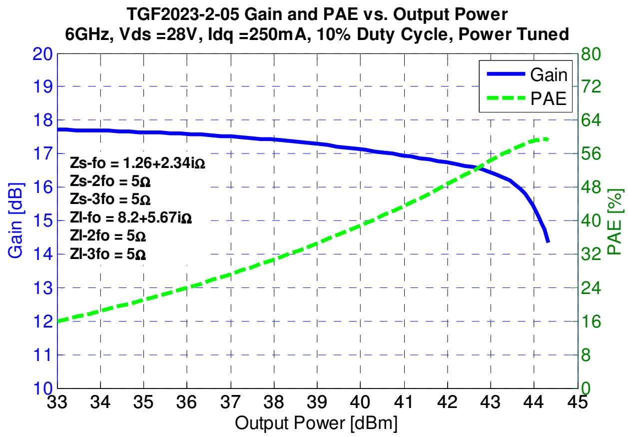
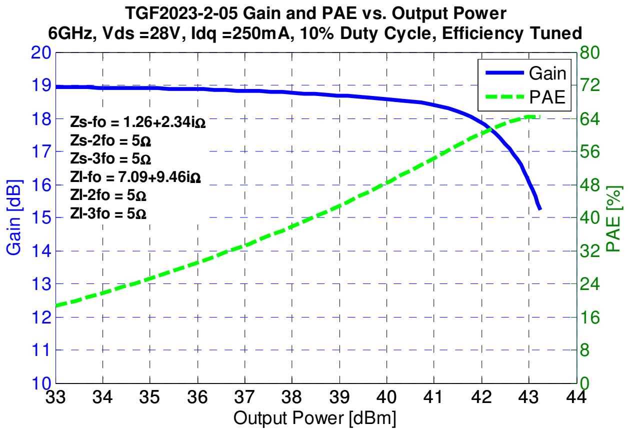
Model Drive-up Data – 6 GHz



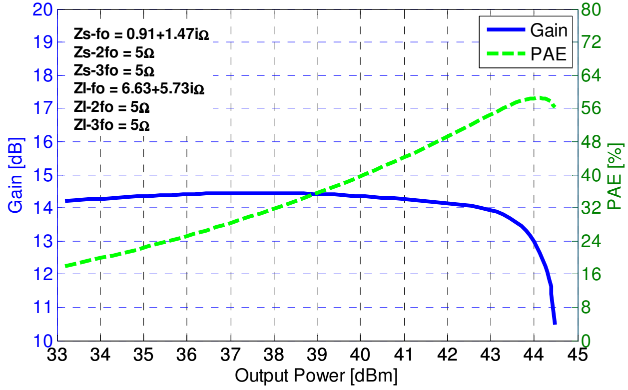




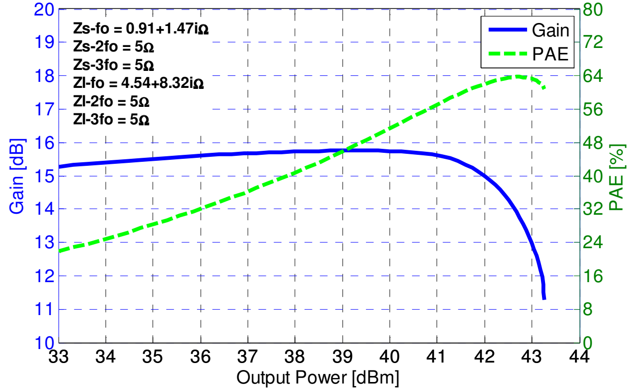


Model Drive-up Data – 8 GHz

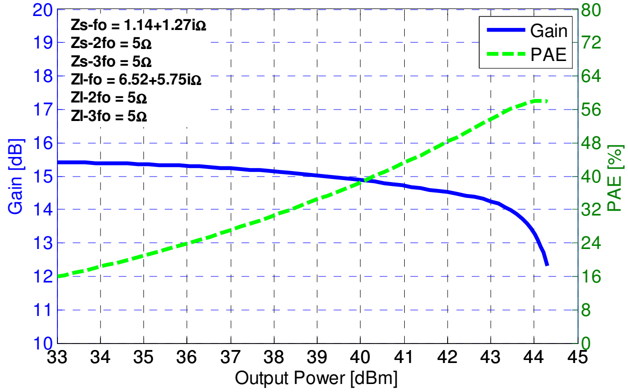
TGF2023-2-05 Gain and PAE vs. Output Power
8GHz, Vds =28V, Idq =100mA, 10% Duty Cycle, Power Tuned



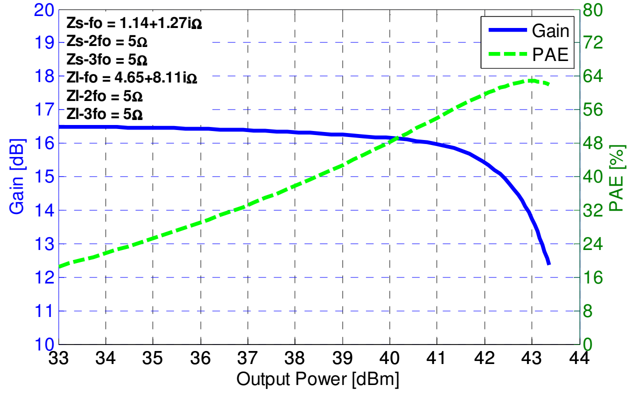
TGF2023-2-05 Gain and PAE vs. Output Power
8GHz, Vds =28V, Idq =100mA, 10% Duty Cycle, Efficiency Tuned



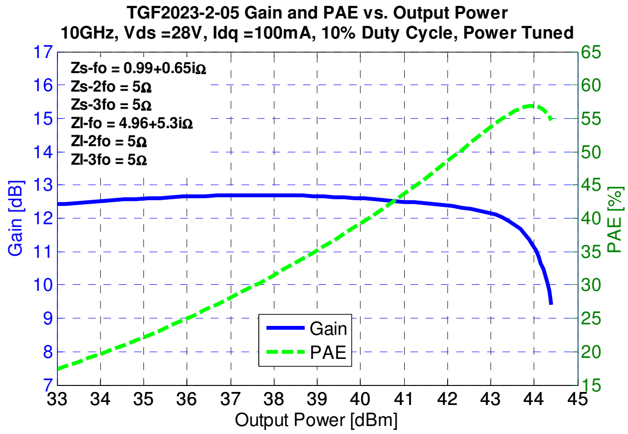
TGF2023-2-05 Gain and PAE vs. Output Power
8GHz, Vds =28V, Idq =250mA, 10% Duty Cycle, Power Tuned

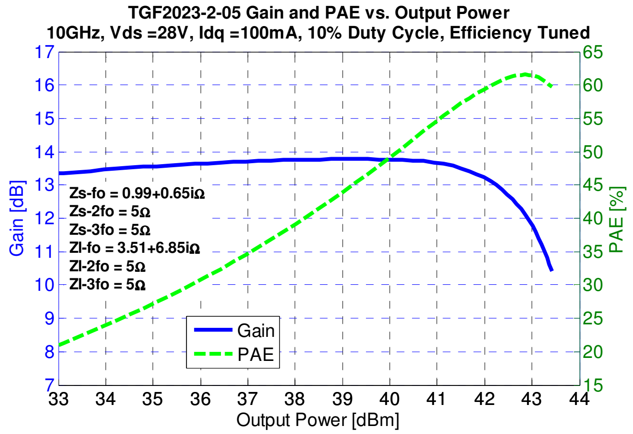


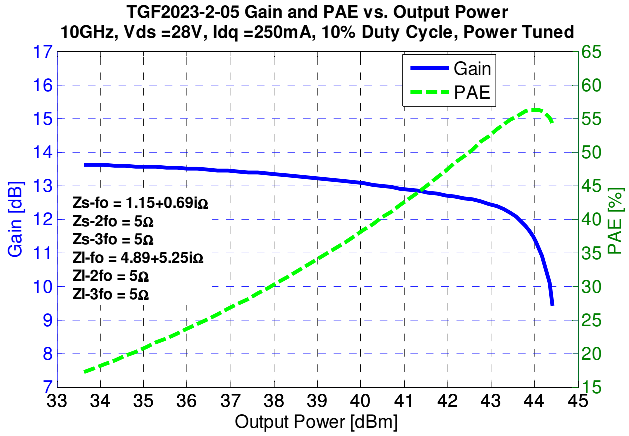
TGF2023-2-05 Gain and PAE vs. Output Power
8GHz, Vds =28V, Idq =250mA, 10% Duty Cycle, Efficiency Tuned

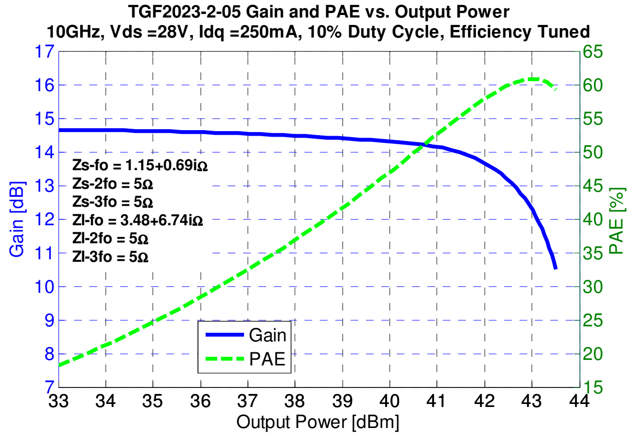


Model Drive-up Data – 10 GHz









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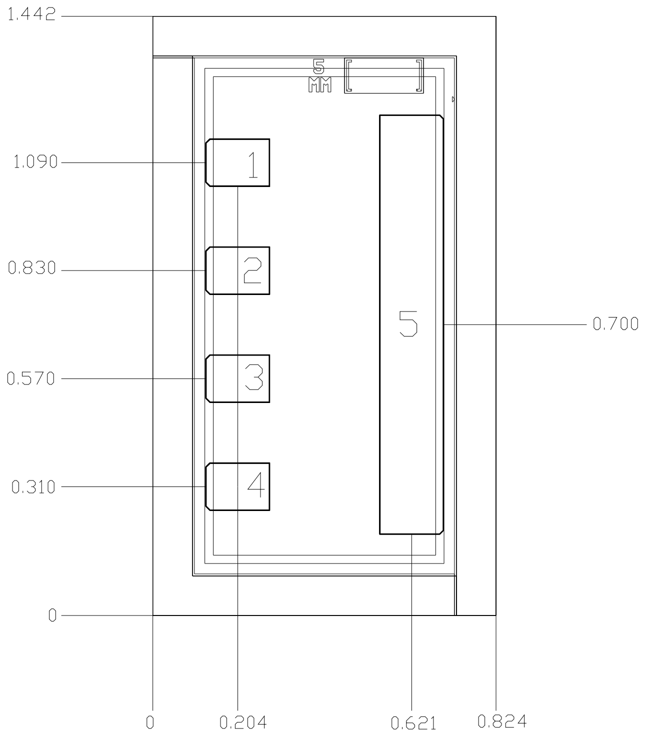
Model

A non-linear model is available for download from Modelithics (at http://www.modelithics.com/mvp/Qorvo&tab=3) by approved Qorvo customers. The model is compatible with the industry's most popular design software including Agilent ADS and National Instruments/AWR applications. Once on the Modelithics web page, the user will need to register for a free license before being granted the download.

Mechanical Drawing



Notes:

1. Units: millimeters
2. Thickness: 0.100 mm
3. Die x,y size tolerance: +/- 0.050 mm

Bond Pads

Pad No.	Description	Dimensions
1-4	Gate	0.154 x 0.115
5	Drain	0.154 x 1.01
Die Backside	Source / Ground	0.824 x 1.442

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Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) not recommended.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Ball bonding is the preferred interconnect technique, except where noted on the assembly diagram.
- Force, time, and ultrasonics are critical bonding parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Disclaimer

GaN/SiC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Bias-up Procedure

1. Set V_G to -5 V.
2. Set I_D limit to 280 mA.
3. Set V_D to 28 V.
4. Adjust V_G more positive until quiescent I_D is 250 mA.
5. Set I_D limit to 2 A.
6. Apply RF signal.

Bias-down Procedure

1. Turn off RF signal.
2. Turn off V_D and wait 1 second to allow drain capacitor dissipation.
3. Turn off V_G.

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