TGF2965-SM

5 W, 32 V, 0.03–3 GHz, GaN RF Input-Matched Transistor

General Description

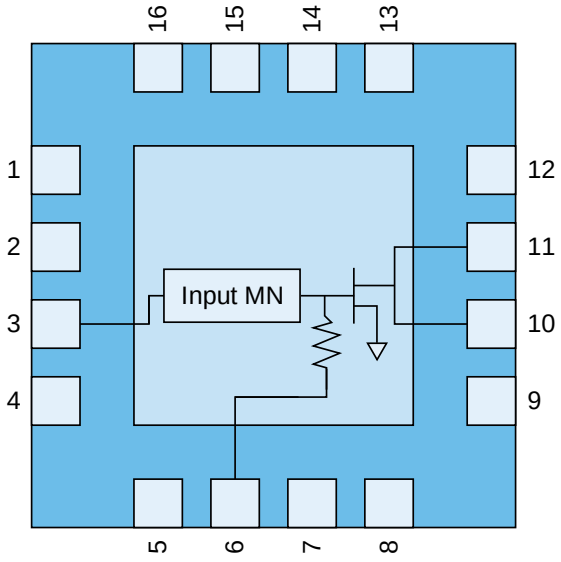
The Qorvo TGF2965-SM is a 6 W (P_{3dB}), 50 Ω-input matched discrete GaN on SiC HEMT which operates from 0.03 to 3.0 GHz. The integrated input matching network enables wideband gain and power performance, while the output can be matched on board to optimize power and efficiency for any region within the band.

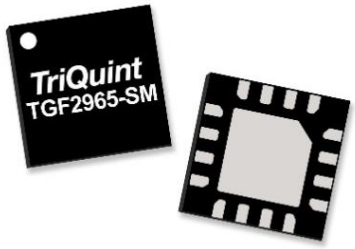
The device is housed in an industry-standard 3 x 3 mm surface mount QFN package.

Lead-free and ROHS compliant

Evaluation boards are available upon request.

Functional Block Diagram





Product Features

- Frequency: 0.03 to 3.0 GHz
- Output Power (P_{3dB})[1]: 6.0 W
- Linear Gain[1]: 18 dB
- Typical $DEFF_{3dB}$[1]: 65%
- Operating Voltage: 32 V
- Low thermal resistance package
- CW and Pulse capable
- 3 x 3 mm package

[1] At 2 GHz

Applications

- Military Radar
- Civilian Radar
- Land Mobile and Military Radio Communications
- Test Instrumentation
- Wideband and Narrowband Amplifiers
- Jammers

Ordering Information

Part	Description
1123170	TGF2965-SM 100 pc MOQ
1123185	TGF2965-SM EVB
TGF2965-SMTR13	TGF2965-SM Tape/Reel 2500 pc MOQ

Absolute Maximum Ratings

Parameter	Value/Range
Breakdown Voltage (BV_{DG})	100 V min.
Gate Voltage Range (V_G)	-7 to +2 V
Drain Current (I_D)	0.6 A
Gate Current (I_G)	See page 4.
Power Dissipation (P_D)	7.5 W
RF Input Power, CW, T = 25 °C (P_{IN})	30 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter[1]	Value/Range
Drain Voltage (V_D)	32 V (Typ.)
Drain Quiescent Current (I_{DQ})	25 mA (Typ.)
Peak Drain Current (I_D)	326 mA (Typ.)
Gate Voltage (V_G)	-2.7 V (Typ.)
Power Dissipation, CW (P_D)	7.05 W (Max)
Power Dissipation, Pulse (P_D)[2]	9.1 W (Max)

[1]Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

[2]100uS Pulse Width, 20% Duty Cycle

RF Characterization–Load Pull Performance

Test conditions unless otherwise noted: T_A = 25 °C, V_D = 32 V, I_{DQ} = 30 mA, Pulse: 100 uS Pulse Width, 20% Duty Cycle

Symbol	Parameter	Typical					Units
F	Frequency	1	1.5	2	2.5	3	GHz
G_{LIN}	Linear Gain, Power Tuned	17.3	17.4	18.2	17.8	16.9	dB
P_{3dB}	Output Power at 3 dB Gain Compression, Power Tuned	37.8	37.7	37.8	38.1	38.3	dBm
$DEFF_{3dB}$	Drain Efficiency at 3 dB Gain Compression, Efficiency Tuned	76.0	62.7	65.2	65.4	71.9	%
G_{3dB}	Gain at 3 dB Compression, Power Tuned	14.3	14.4	15.2	14.8	13.9	dB

RF Characterization–0.03–3 GHz EVB Performance at 2.5 GHz–Pulsed

Test conditions unless otherwise noted: T_A = 25 °C, V_D = 32 V, I_{DQ} = 30 mA, Pulse: 100 uS Pulse Width, 20% Duty Cycle

Symbol	Parameter	Min	Typical	Max	Units
G_{LIN}	Linear Gain		17.1		dB
P_{3dB}	Output Power at 3 dB Gain Compression		5.0		W
DE_{3dB}	Drain Efficiency at 3 dB Gain Compression		50.6		%
G_{3dB}	Gain at 3 dB Compression		14.1		dB

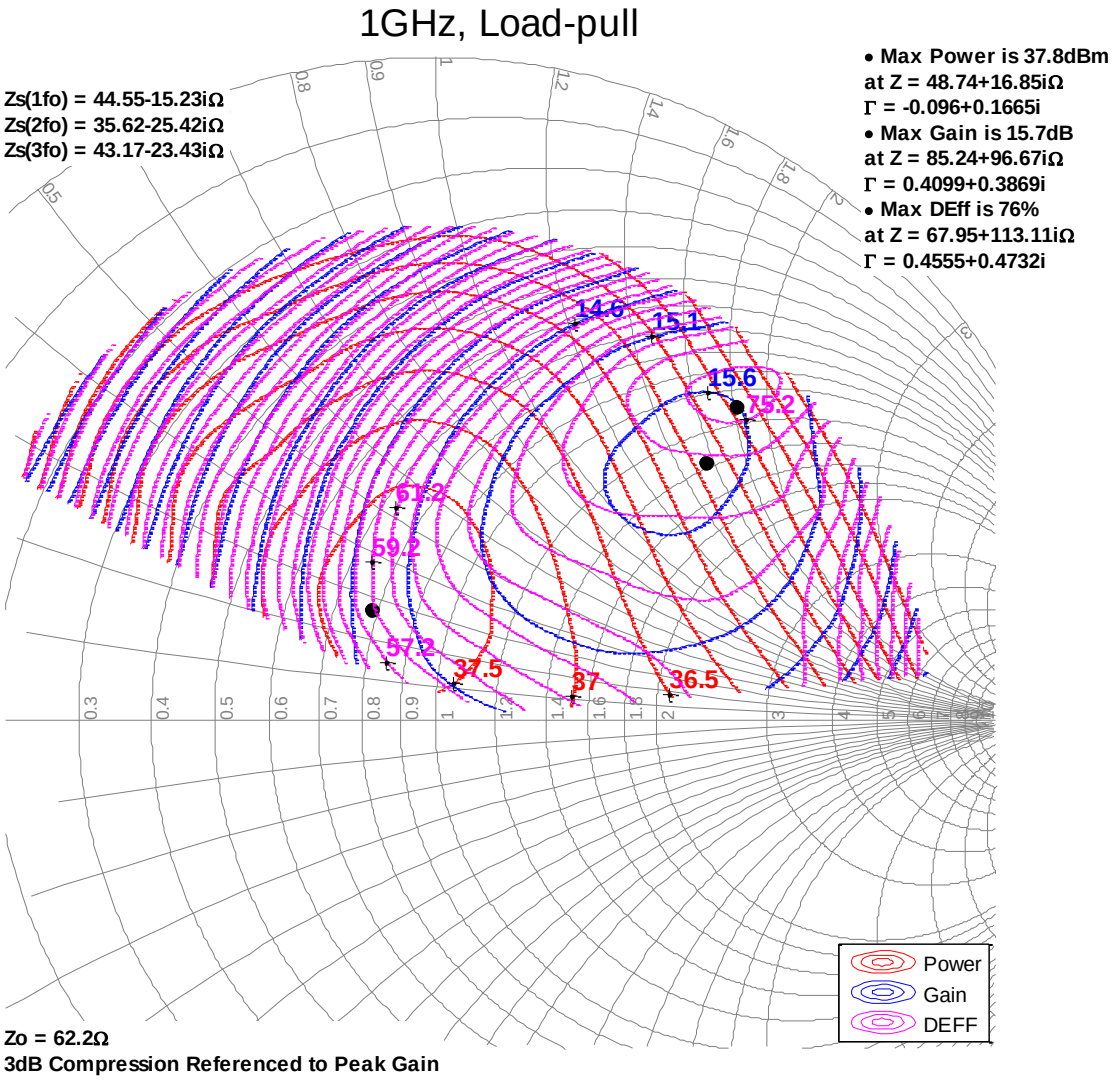
RF Characterization–Mismatch Ruggedness at 1, 2 and 3 GHz

Test conditions unless otherwise noted: T_A = 25 °C, V_D = 28 V, I_{DQ} = 30 mA, Pulse: 100 uS Pulse Width, 20% Duty Cycle
Driving input power is determined at pulsed compression under matched condition at EVB output connector.

Symbol	Parameter	dB Compression	Typical
VSWR	Impedance Mismatch Ruggedness	3	10:1
VSWR	Impedance Mismatch Ruggedness	8	2:1

Load Pull Smith Charts [1, 2]

RF performance that the device typically exhibits when placed in the specified impedance environment. The impedances are not the impedances of the device, they are the impedances presented to the device via an RF circuit or load-pull system. The impedances listed follow an optimized trajectory to maintain high power and high efficiency.



Notes:

1. 32 V, 30 mA, Pulsed signal with 100 uS pulse width and 20% duty cycle. 3 dB compression referenced to peak gain.
2. See page 18 for load pull and source pull reference planes.

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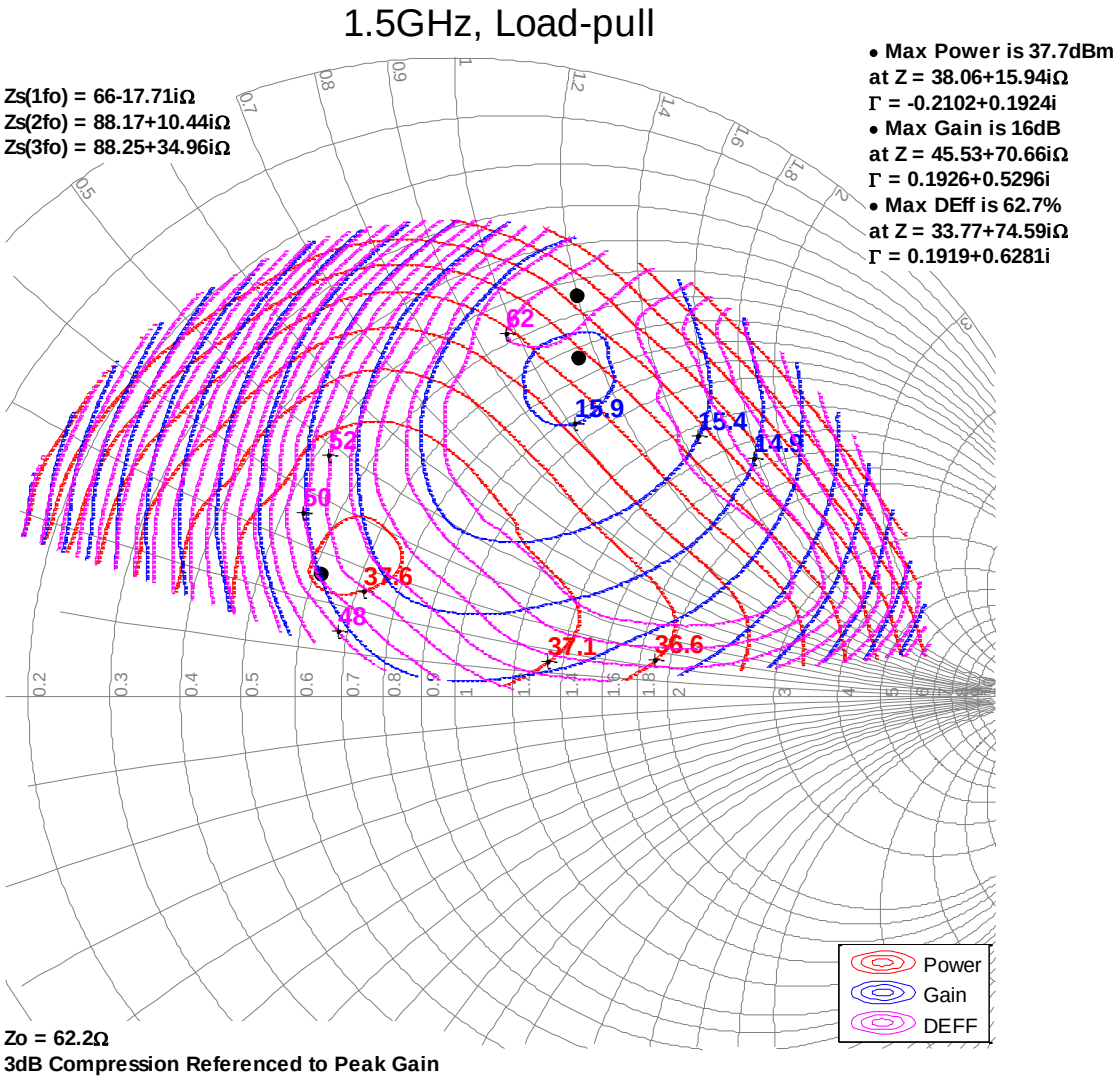

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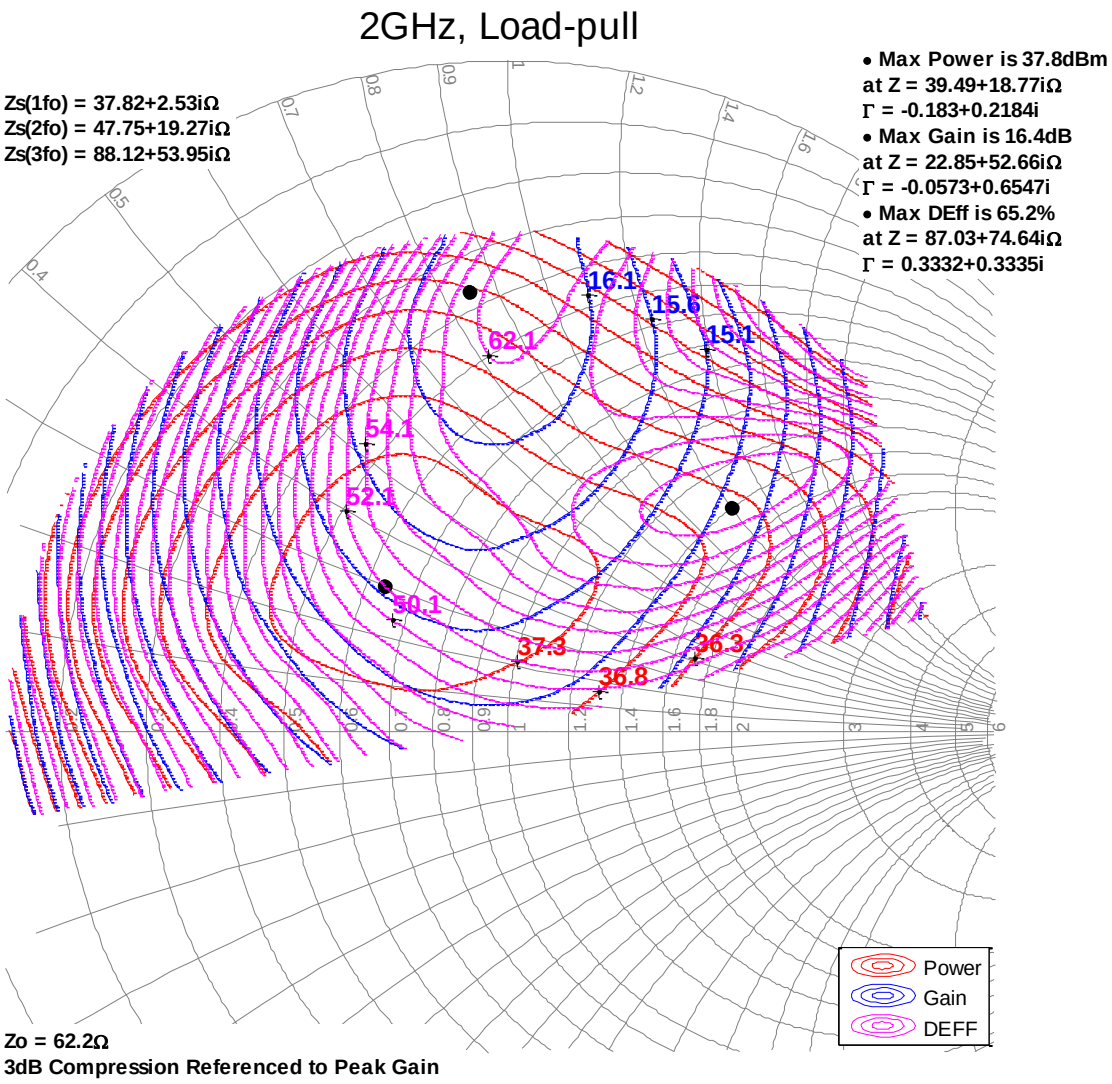

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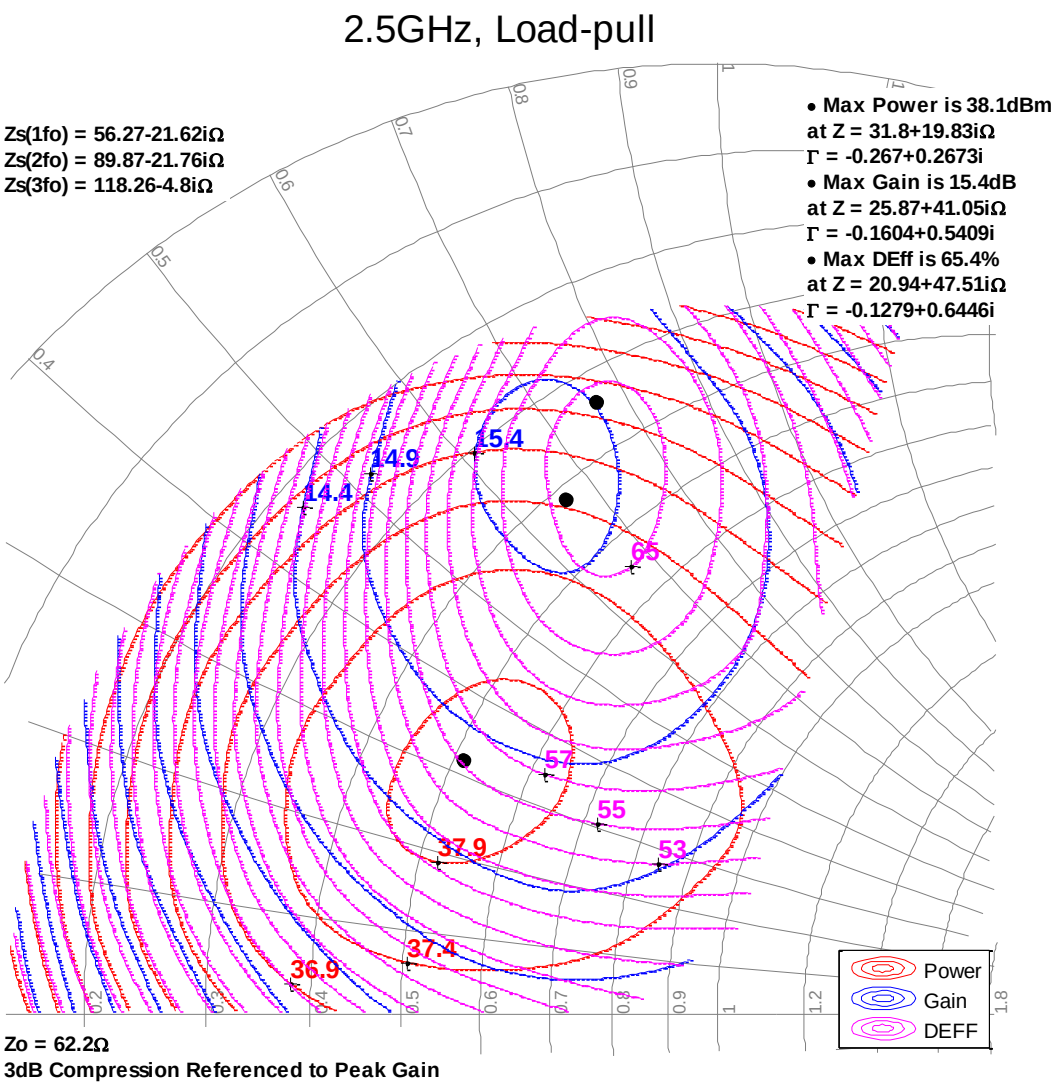

Notes:

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Load Pull Smith Charts [1, 2]

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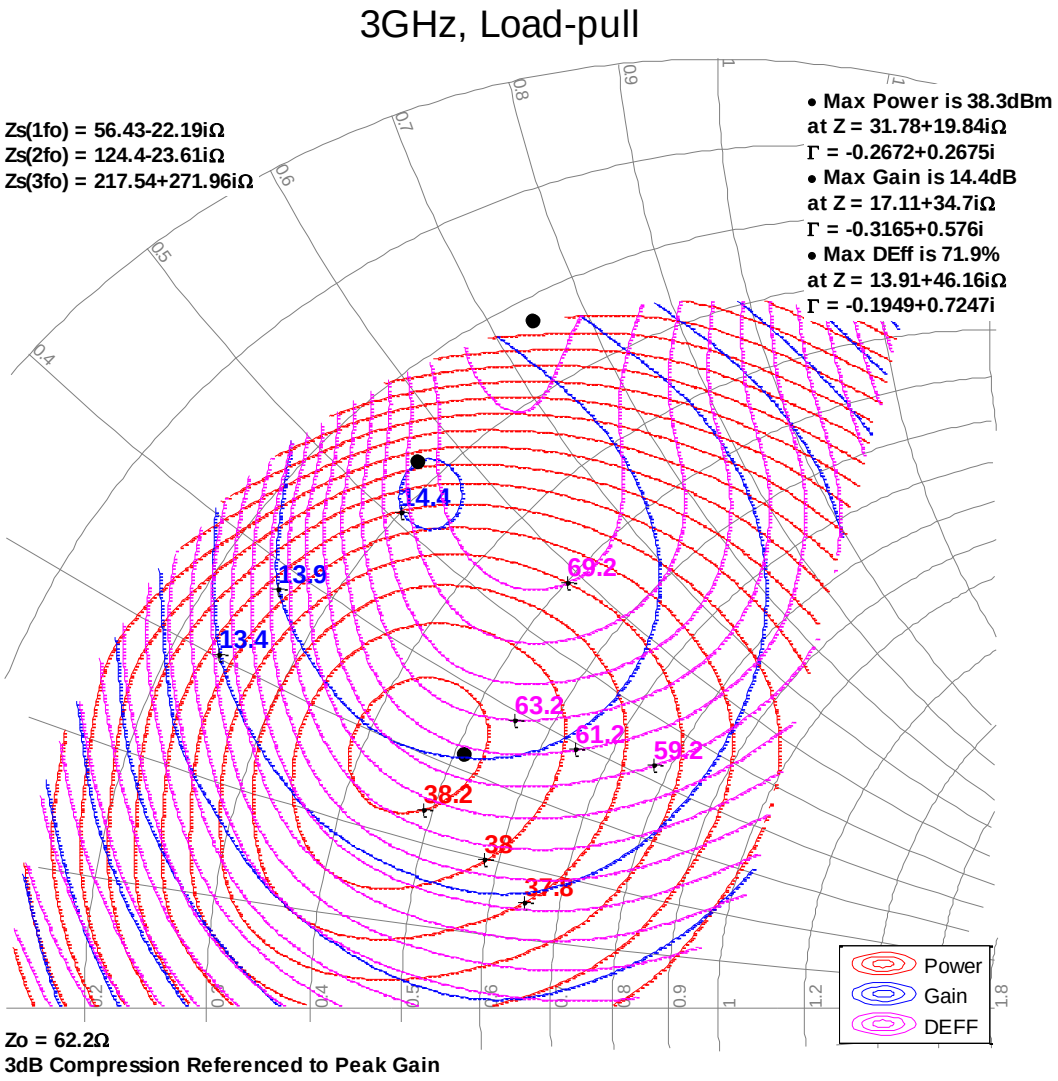
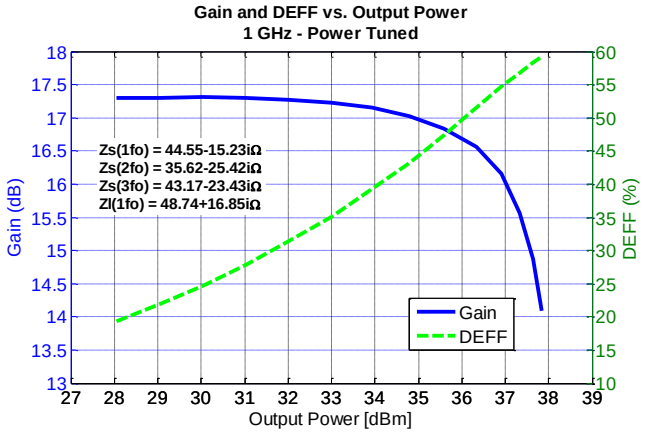
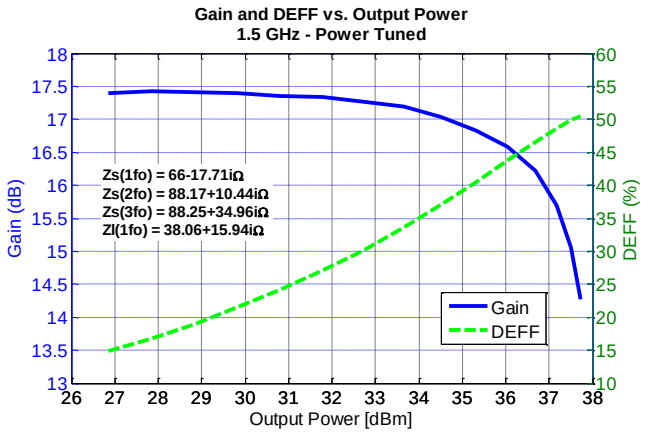


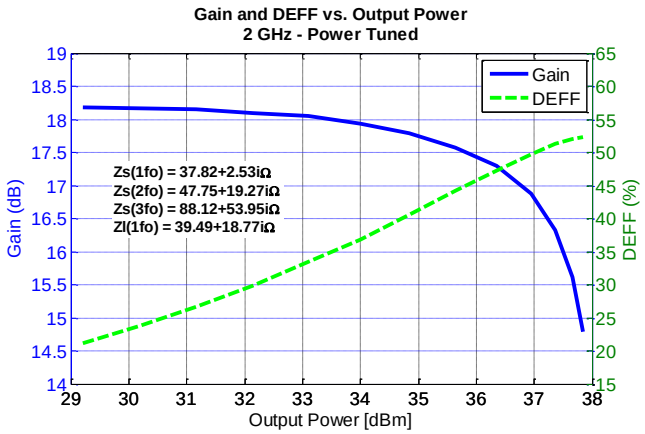
Notes:

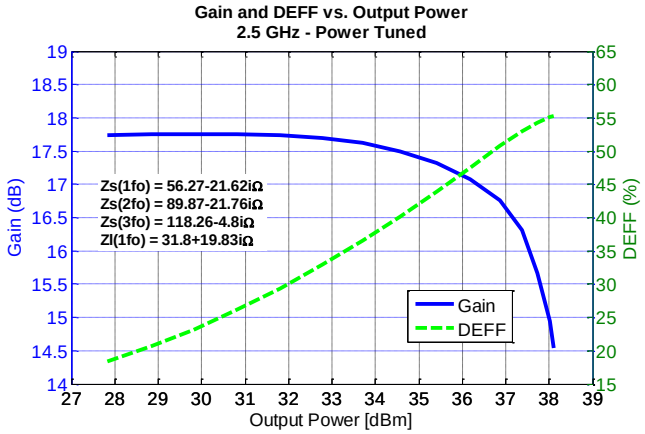
1. 32 V, 30 mA, Pulsed signal with 100 uS pulse width and 20% duty cycle. 3 dB compression referenced to peak gain.
2. See page 18 for load pull and source pull reference planes.

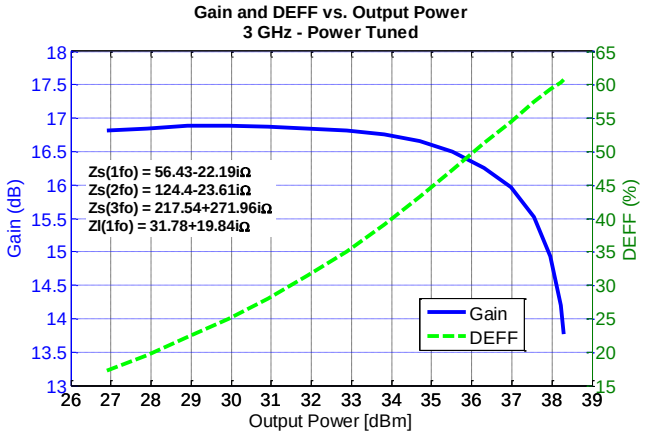
Typical Performance–Power Tuned [1,2]







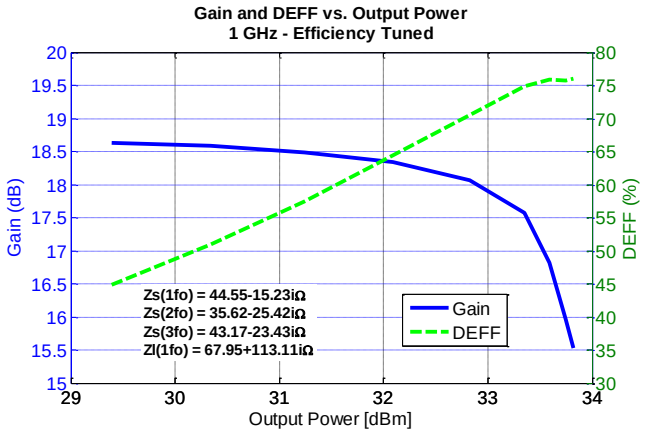


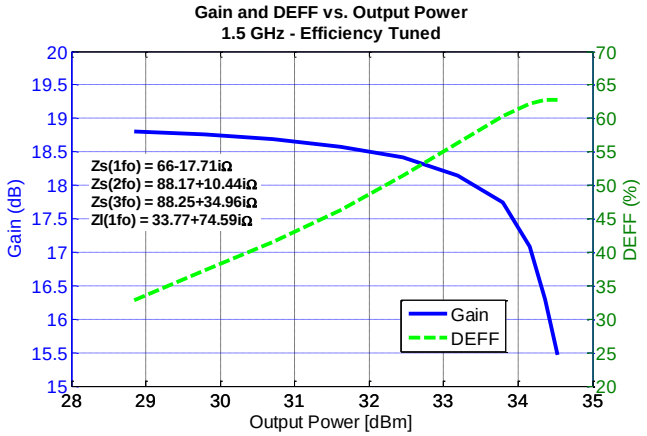


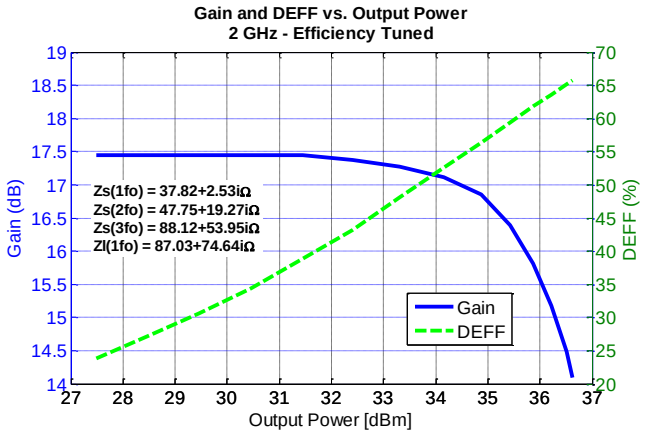
Notes:

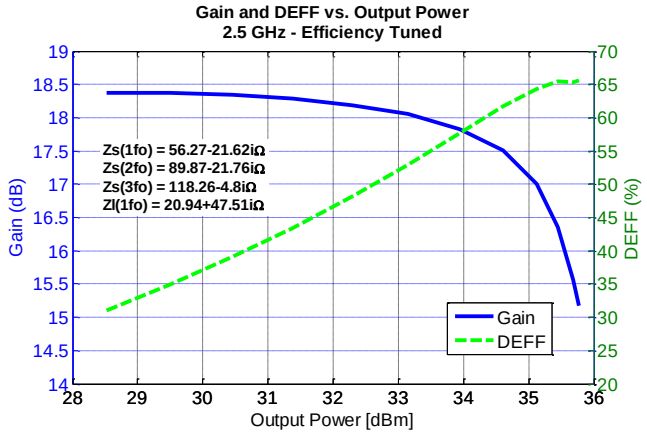
1. Pulsed signal with 100uS pulse width and 20% duty cycle
2. See page 18 for load pull and source pull reference planes where the performance was measured.

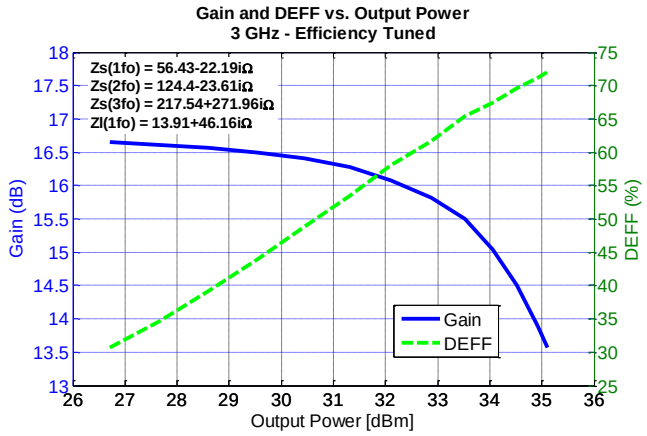
Typical Performance–Efficiency Tuned [1,2]









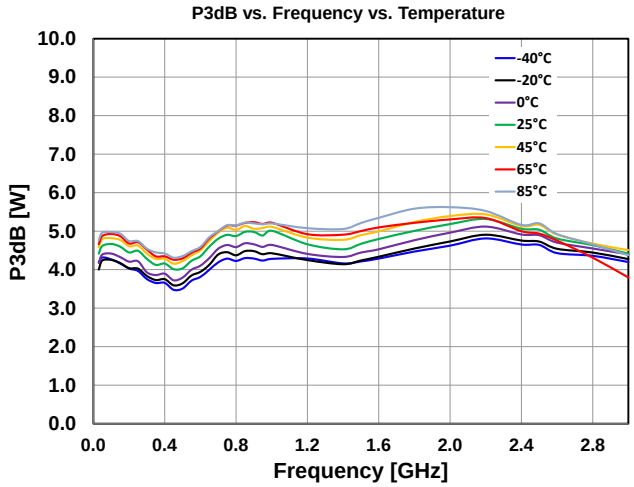


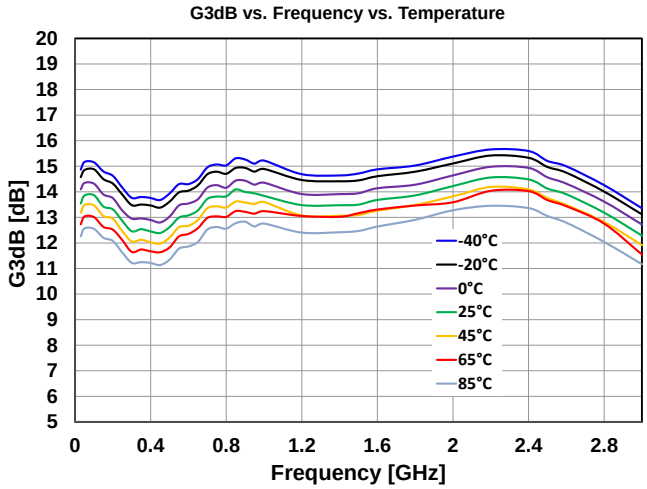
Notes:

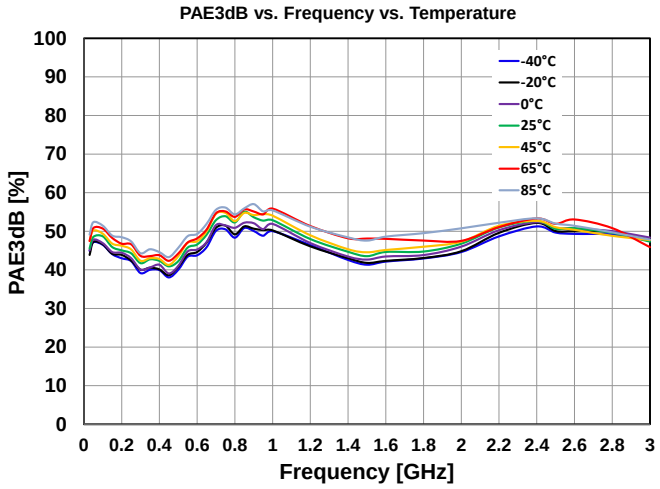
1. Pulsed signal with 100uS pulse width and 20% duty cycle
2. See page 18 for load pull and source pull reference planes where the performance was measured.

0.03–3 GHz Evaluation Board Performance Over Temperature[1, 2]

Performance measured on Qorvo's 0.03 GHz to 3 GHz Evaluation Board.





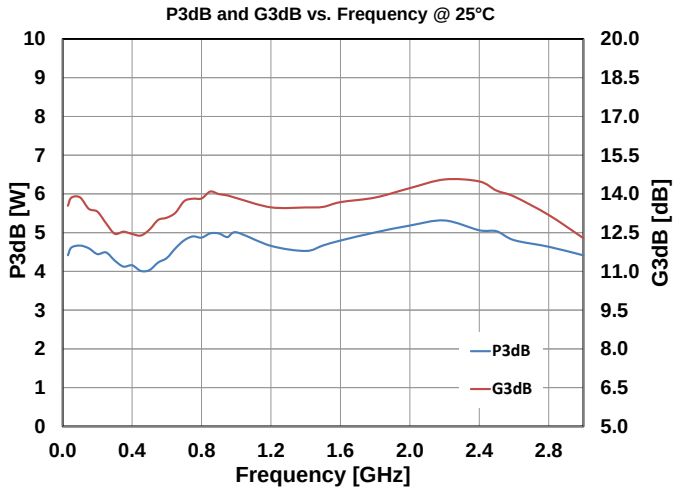


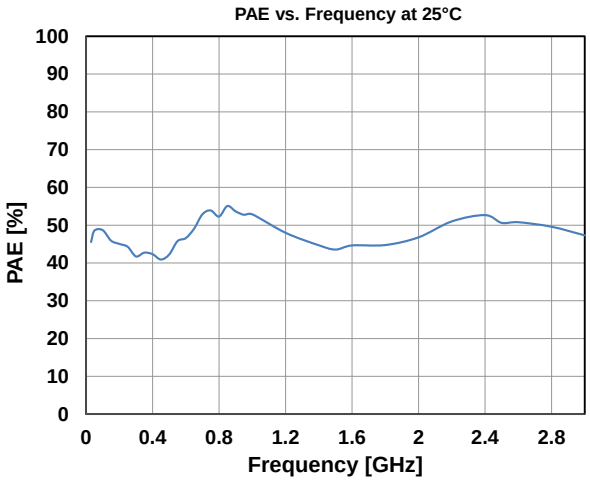
Notes:

1. Test Conditions: V_{DS} = 32 V, I_{DQ} = 30 mA
2. Test Signal: Pulse Width = 100 µs, Duty Cycle = 20%

0.03–3 GHz Evaluation Board Performance At 25 °C[1, 2] – Pulsed

Performance measured on Qorvo's 0.03 GHz to 3 GHz Evaluation Board.



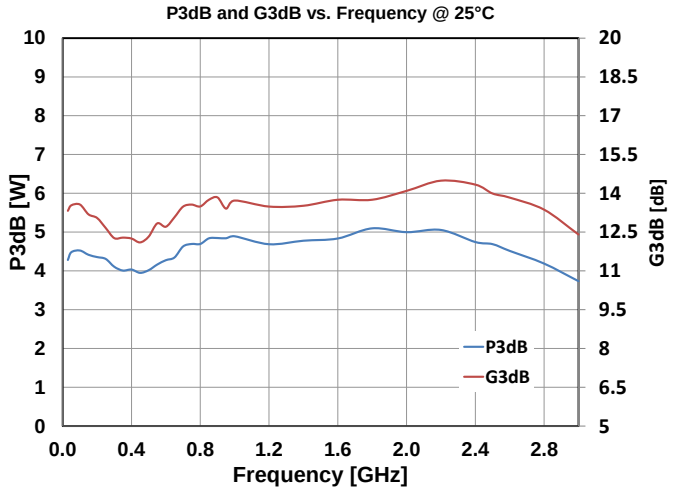


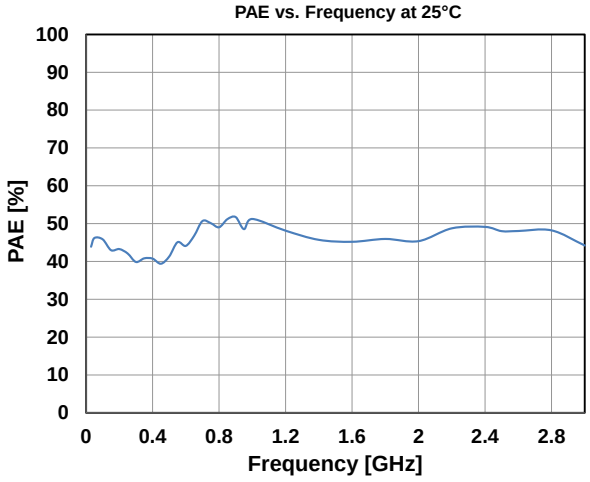
Notes:

1. Test Conditions: V_{DS} = 32 V, I_{DQ} = 30 mA, 25 °C
2. Test Signal: Pulse Width = 100 µs, Duty Cycle = 20%

0.03–3 GHz Evaluation Board Performance At 25 °C[1] – CW

Performance measured on Qorvo's 0.03 GHz to 3 GHz Evaluation Board.

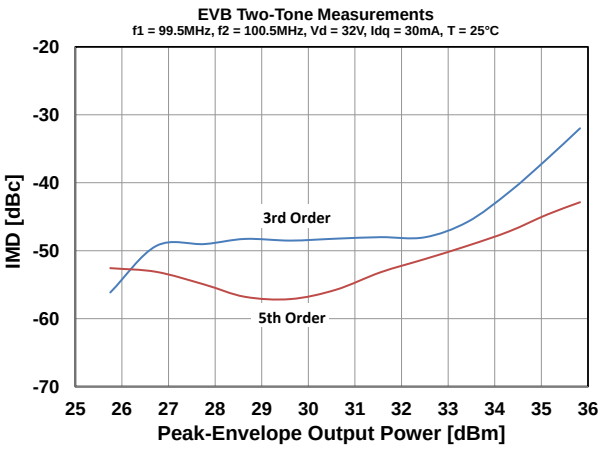


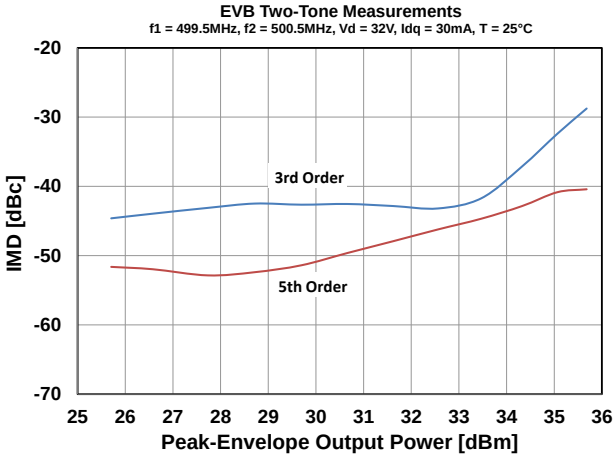


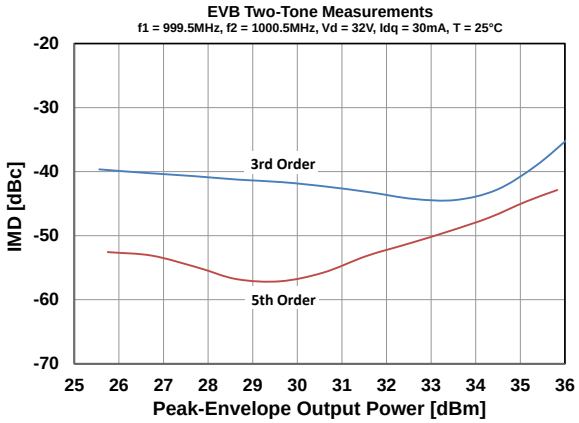
Notes:

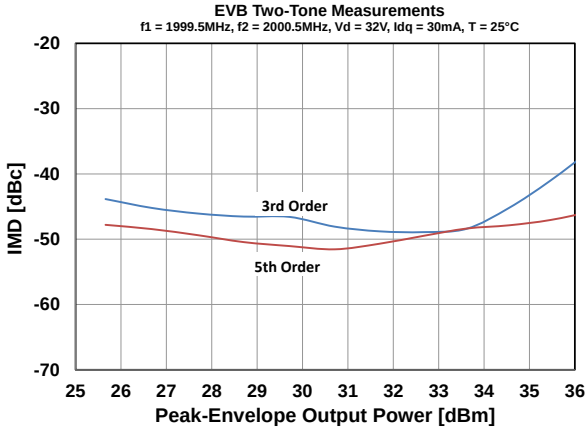
1. Test Conditions: V_{DS} = 32 V, I_{DQ} = 30 mA, 25 °C

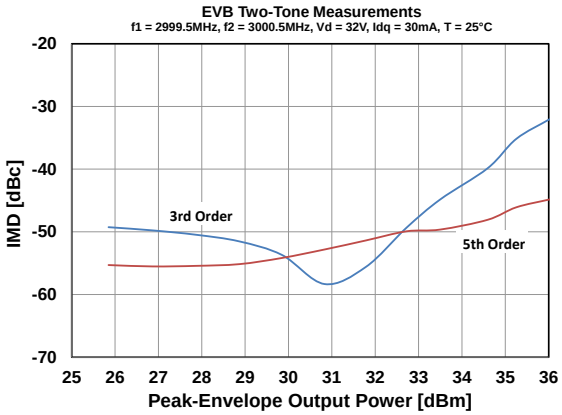
0.03 – 3 GHz Evaluation Board Performance–Two-Tone Measurements [1]







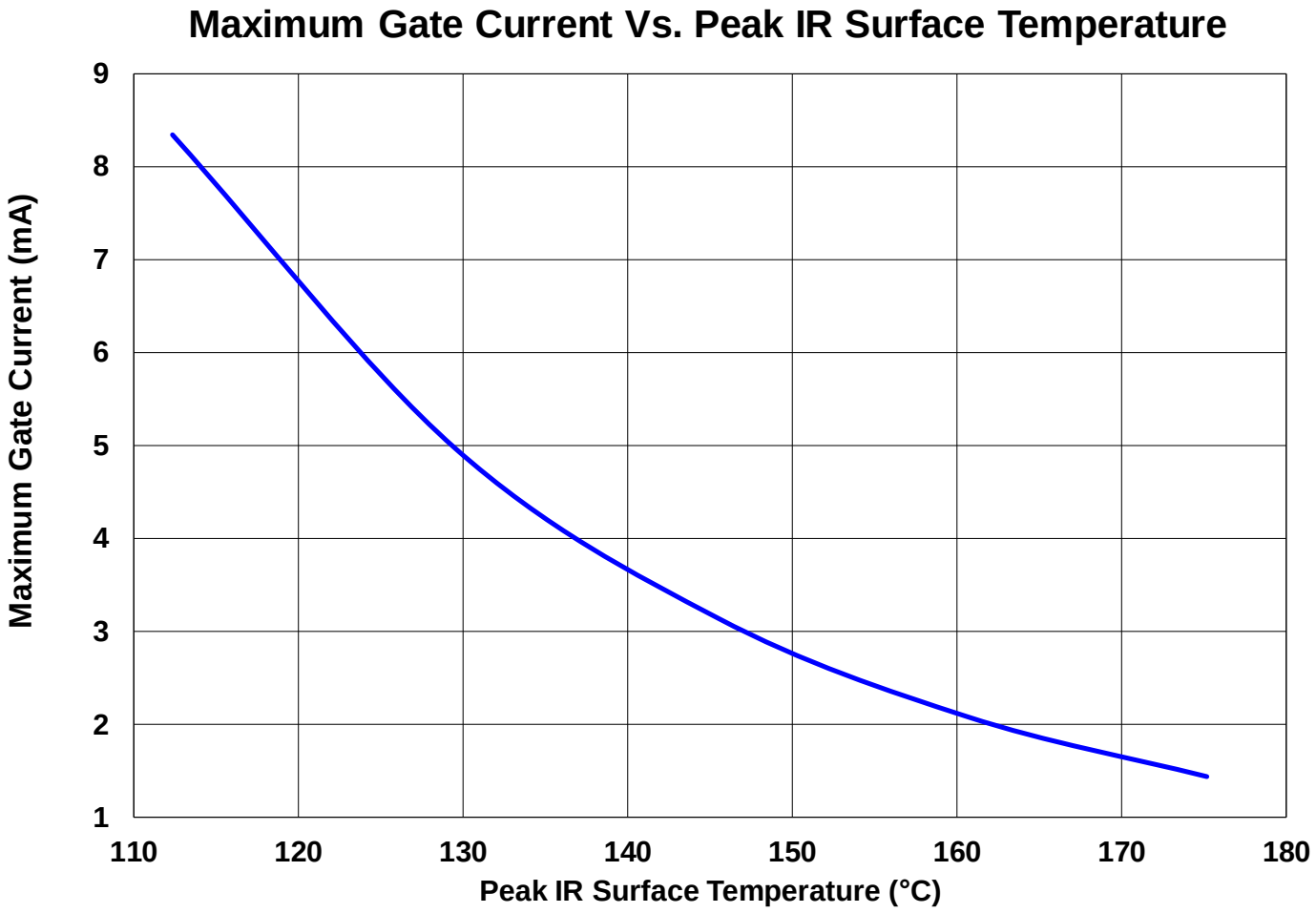




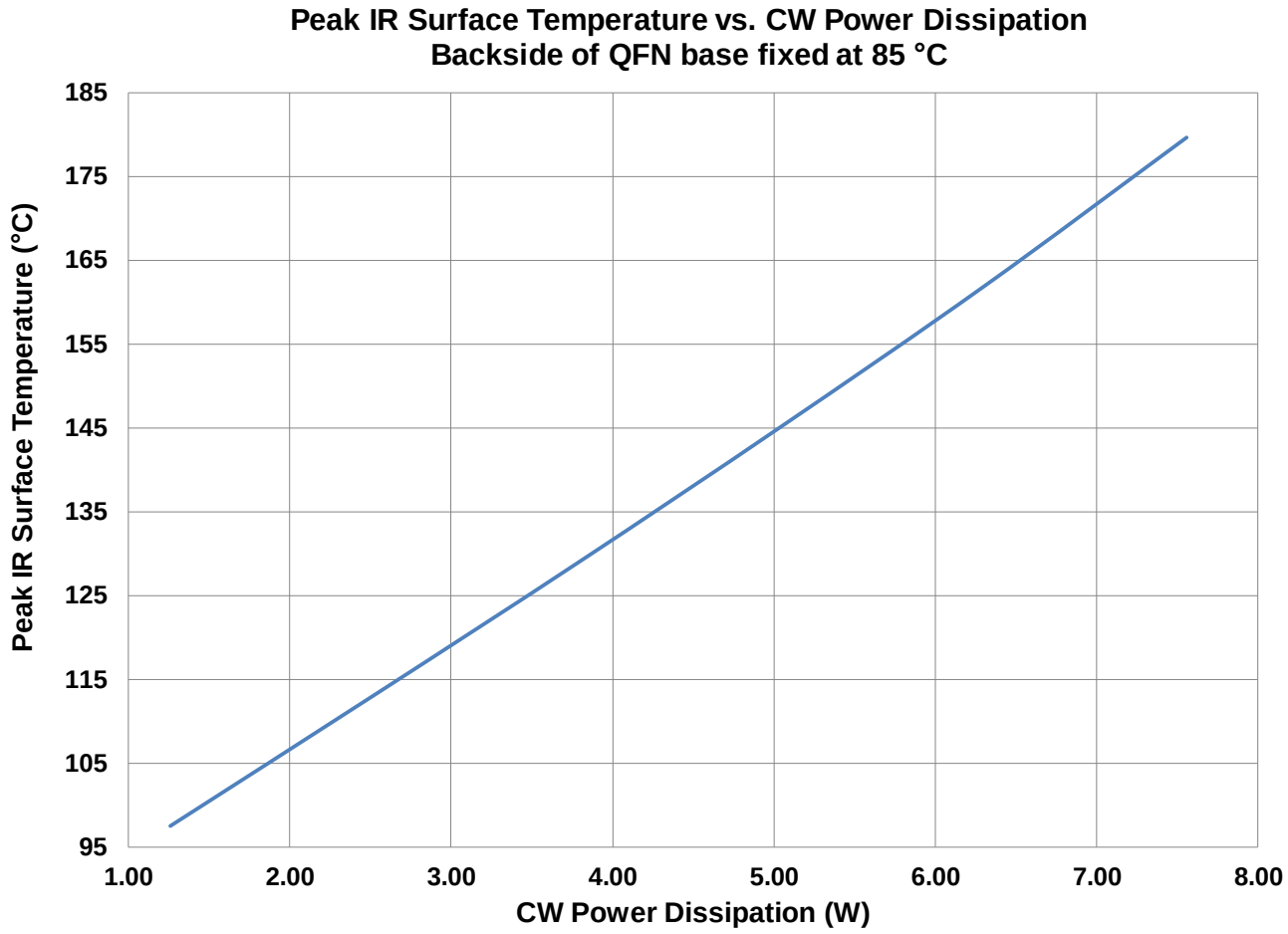
Notes:

1. The Intermodulation Distortion products (IMD) are referenced to peak-envelope output power, which is 6 dB above single-tone output power

Maximum Gate Current



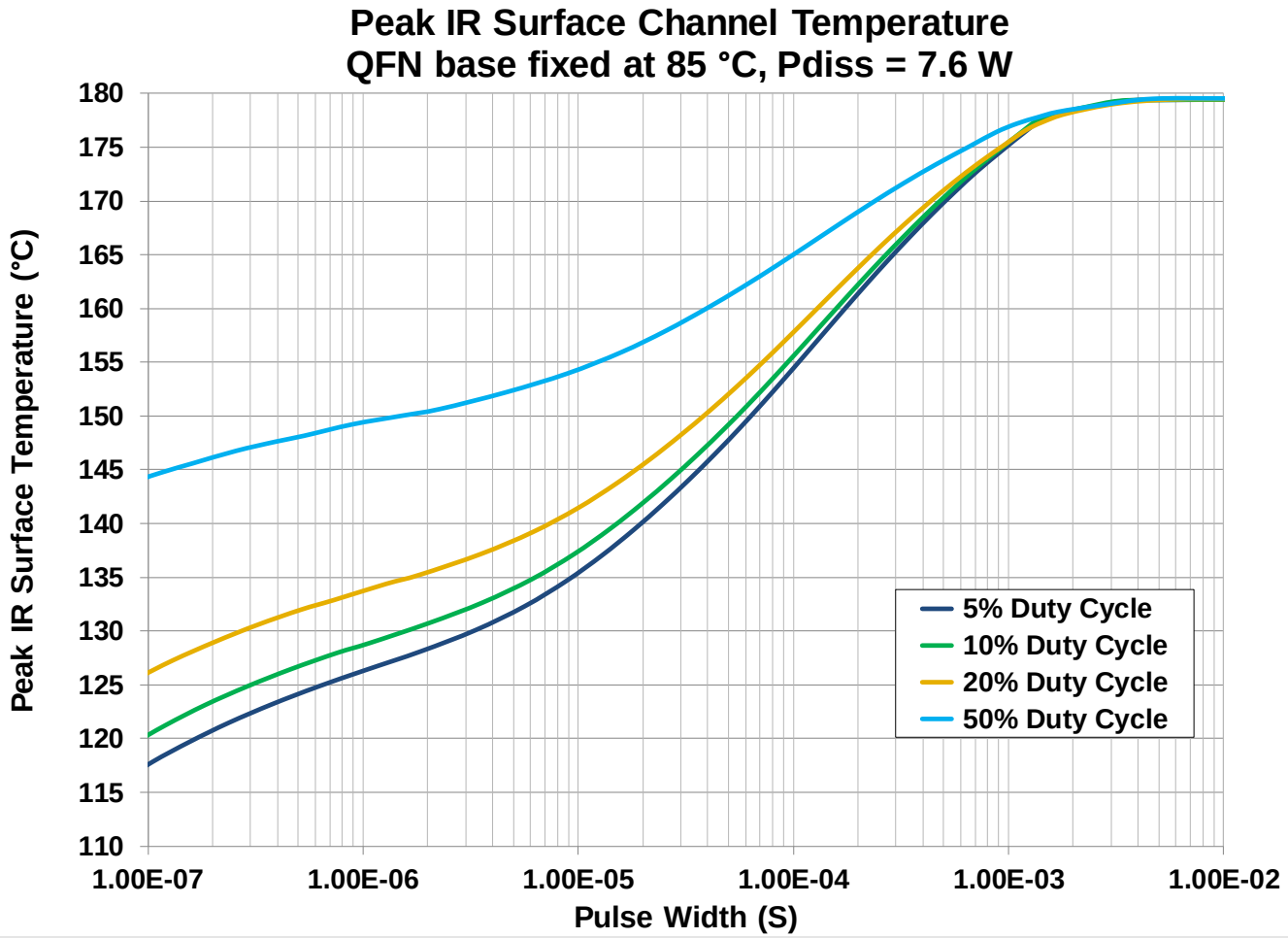
Thermal and Reliability Information - CW



Parameter	Conditions	Values	Units
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 1.26 W Pdiss, CW	9.9	°C/W
Peak IR Surface Temperature[1] (T_{CH})		97.4	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 2.52 W Pdiss, CW	11.1	°C/W
Peak IR Surface Temperature[1] (T_{CH})		113	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 3.78 W Pdiss, CW	11.6	°C/W
Peak IR Surface Temperature[1] (T_{CH})		129	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 5.04 W Pdiss, CW	11.9	°C/W
Peak IR Surface Temperature[1] (T_{CH})		145	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 6.30 W Pdiss, CW	12.2	°C/W
Peak IR Surface Temperature[1] (T_{CH})		162	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 7.56 W Pdiss, CW	12.5	°C/W
Peak IR Surface Temperature[1] (T_{CH})		180	°C

[1]Refer to the following document GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

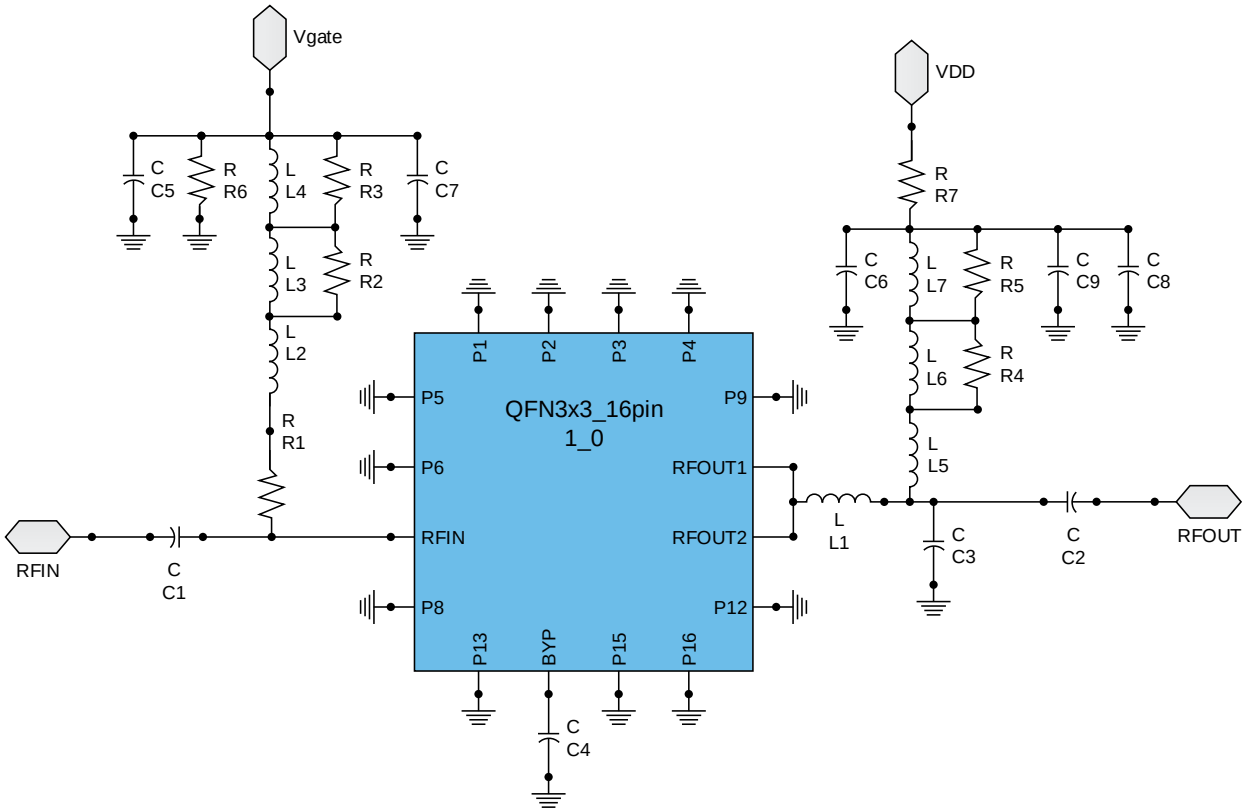
Thermal and Reliability Information - Pulsed



Parameter	Conditions	Values	Units
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 7.6 W Pdiss, 100 uS Pulse Width, 5% DC	9.1	°C/W
Peak IR Surface Temperature[1] (T_{CH})		154	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 7.6 W Pdiss, 100 uS Pulse Width, 10% DC	9.3	°C/W
Peak IR Surface Temperature[1] (T_{CH})		156	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 7.6 W Pdiss, 100 uS Pulse Width, 20% DC	9.6	°C/W
Peak IR Surface Temperature[1] (T_{CH})		158	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 7.6 W Pdiss, 100 uS Pulse Width, 50% DC	10.5	°C/W
Peak IR Surface Temperature[1] (T_{CH})		165	°C

[1]Refer to the following document GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

0.03–3 GHz Application Circuit

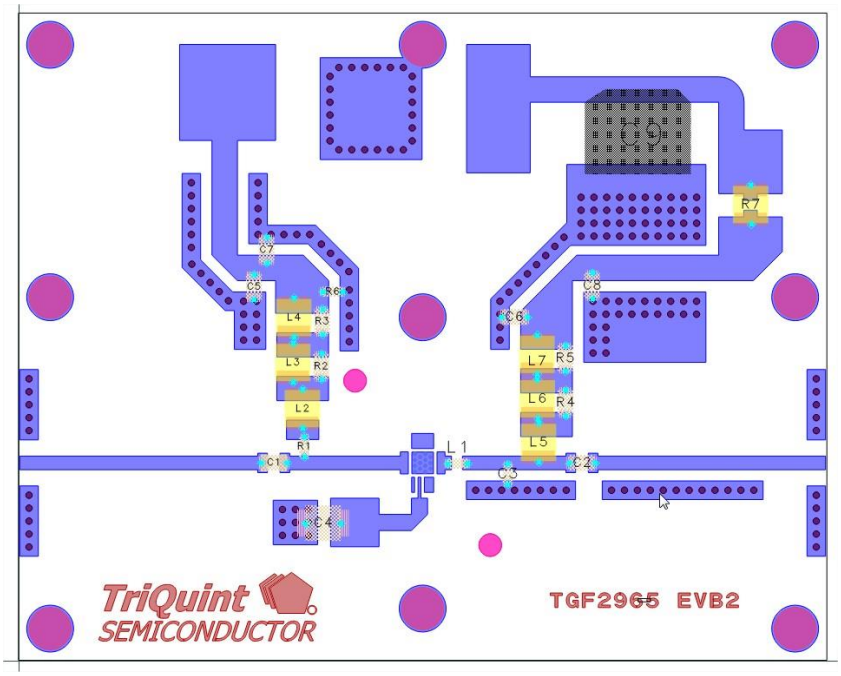


Bias-up Procedure
V_G set to-5 V.
V_D set to 32 V.
Adjust V_G more positive until quiescent I_D is 30 mA.
Apply RF signal.

Bias-down Procedure
Turn off RF signal
Turn off V_D and wait 1 second to allow drain capacitor dissipation
Turn off V_G

0.03–3 GHz Evaluation Board Layout

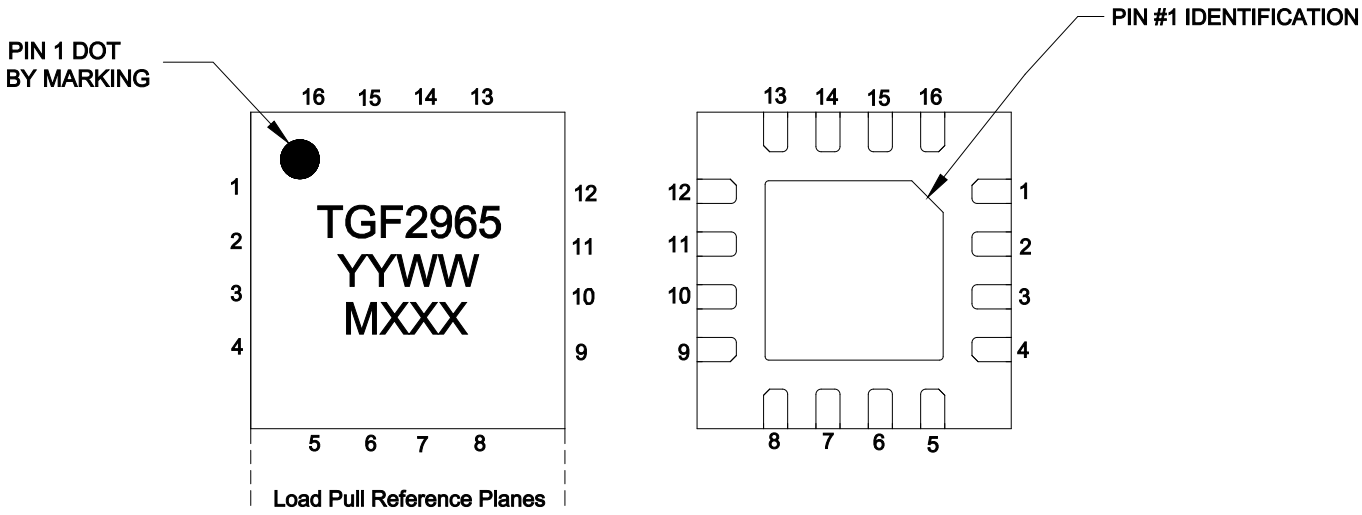
Top RF layer is 0.020” thick Rogers RO4350B, ε_r = 3.48. The pad pattern shown has been developed and tested for optimized assembly at Qorvo Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances.



00.03–3 GHz EVB Bill of Materials

Reference Des.	Value	Qty	Manuf.	Part Number
C1, C2, C5, C6	2400 pF	4	DLI	C08BL102X-1UN-X0T
C3	0.2 pF	1	Murata	GRM1555C1HR20BZ01
C4, C7	10 uF	2	TDK	C1632X5R0J106M130AC
C8	1 uF	1	AVX	18121C105KAT2A
C9	220 uF	1	United Chemicon	EMVY500ADA221MJA0G
L1	2 nH	1	CoilCraft	0603HC-2N0XJLU
L2, L5	82 nH	2	CoilCraft	1008CS-820XGLB
L3, L6	100 nH	2	CoilCraft	1008CS-101XGLB
L4, L7	900 nH	2	CoilCraft	1008AF-901XJLB
R1	499 Ω	1	Venkel	CR0603-10W-4990FT
R2, R3, R4, R5	400 Ω	4	Venkel	CR0805-8W-4020FT
R6	1 kΩ	1	Venkel	CR0603-10W-1001FT
R7	0 Ω	DNP		

Pin Layout



Pin Description

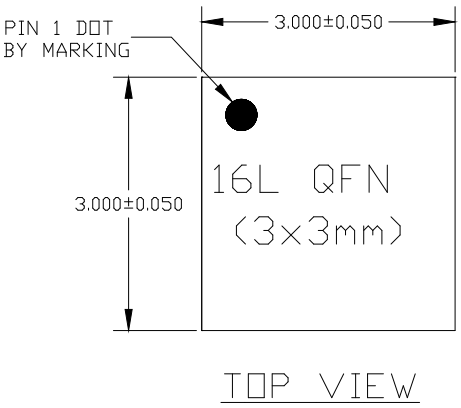
Pin Number	Symbol	Description
10, 11	V_D/RF OUT	Drain voltage / RF Output to be matched to 50 ohms; see EVB Layout on page 19 as an example.
3	V_G/RF IN	Gate voltage / RF Input to be matched to 50 ohms; see EVB Layout on page 19 as an example.
6	Off-chip Cap	Off-chip capacitor to extend low-frequency gain
Back side	Source	Source connected to ground

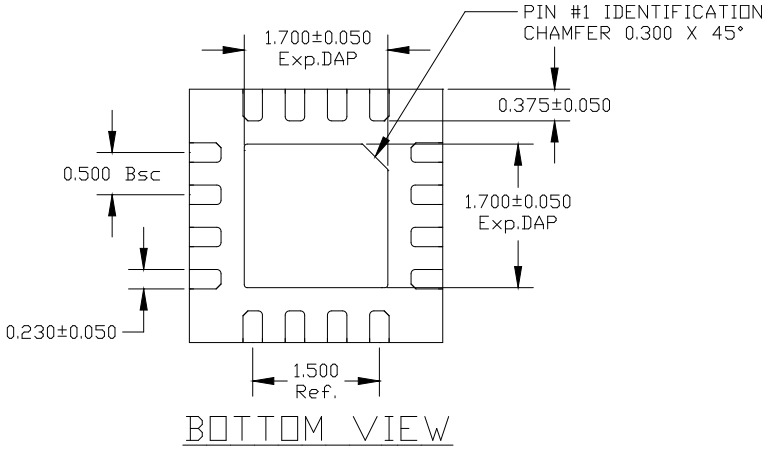
Notes:

1. Thermal resistance measured to back side of package.
2. The TGF2965-SM will be marked with the “TGF2965” designator and a lot code marked below the part designator The “YY” represents the last two digits of the calendar year the part was manufactured, the “WW” is the work week of the assembly lot start, and the “MXXX” is the production lot number.

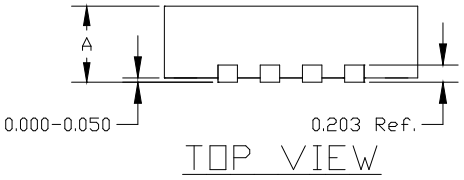
Mechanical Information

All dimensions are in millimeters.





		SLP
A	MAX.	0.900
	NOM.	0.850
	MIN.	0.800



Note:

1. Unless otherwise noted, all dimension tolerances are +/-0.127 mm.
2. This package is lead-free/RoHS-compliant. The plating material on the leads is NiAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and tin-lead (maximum 245 °C reflow temperature) soldering processes

Recommended Soldering Temperature Profile