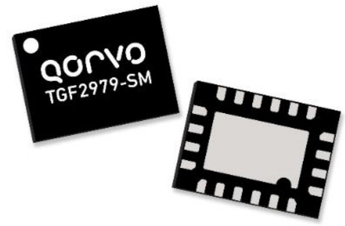
Product Overview

The Qorvo TGF2979-SM is a 25 W (P3dB) discrete GaN on SiC HEMT which operates from DC to 12 GHz. The device is constructed with Qorvo's proven QGaN25 process, which features advanced field plate techniques to optimize power and efficiency at high drain bias operating conditions. This optimization can potentially lower system costs in terms of fewer amplifier line-ups and lower thermal management costs.

The device is housed in an industry-standard 3 x 4 mm surface mount QFN package.

Lead-free and ROHS compliant

Evaluation boards are available upon request



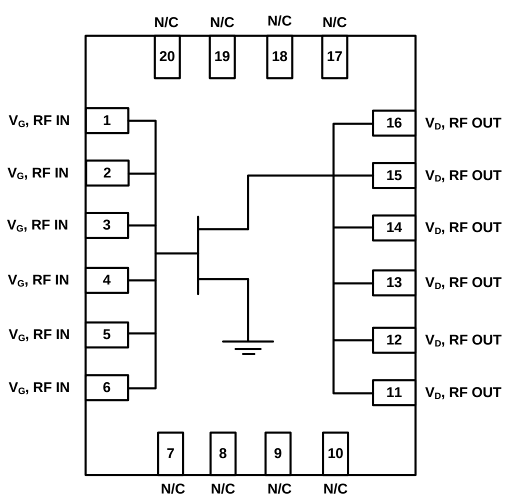
20 Pad 3 x 4 mm Package

Key Features

- Frequency: DC to 12 GHz
- Output Power (P3dB)[1]: 22 W
- Linear Gain[1]: 11 dB
- Typical PAE (3dB)[1]: 45%
- Operating Voltage: 32 V
- Low thermal resistance package
- CW and Pulse capable
- 3 x 4 mm package

Note: @ 9.4 GHz

Functional Block Diagram



Applications

- Military radar
- Commercial radar
    - Avionics
    - Marine
    - Weather

Ordering Information

Part No.	Description
TGF2979-SMEVB01	2.6-3.2 GHz Evaluation Board
TGF2979-SMEVB02	2.8-3.4 GHz Evaluation Board
TGF2979-SMEVB03	3-3.6 GHz Evaluation Board

Absolute Maximum Ratings

Parameter	Value	Units
Breakdown Voltage (BV_{DG})	100	V
Gate Voltage Range (V_G)	−7 to +2	V
Drain Current (I_D)	3.6	A
Gate Current (I_G)	−7.5 to 12.6	mA
Power Dissipation, CW (P_D)	See page 4.	W
RF Input Power, CW, T=25°C (P_{IN})	37.8	dBm
Storage Temperature	−40 to 150	°C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (V_D)		+32		V
Drain Quiescent Current (I_{DQ})		150		mA
Gate Voltage (V_G)[1]		−2.7		V

Electrical specifications are measured at specified test conditions.

Specifications are not guaranteed over all recommended operating conditions.

Note:

1. To be adjusted to desired I_{DQ}

Pulsed RF Characterization – Load Pull Performance

Test conditions unless otherwise noted: T = 25°C, Pulse (20% Duty Cycle, 100 µs Width).

Parameter	Typical Values						Units
Frequency, F	5	8	9	9.4	10	12	GHz
Drain Voltage[1,2], V_D	32	32	32	32	32	32	V
Drain Bias Current[1,2], I_{DQ}	150	150	150	150	150	150	mA
Output Power at 3dB compression[1], P_{3dB}	44.4	43.8	43.2	43.5	43.7	43.4	dBm
Power Added Efficiency at 3dB compression[2], PAE_{3dB}	56.0	51.0	49.2	44.9	40.8	33.00	%
Gain at 3dB compression[1], G_{3dB}	11.5	9.7	8.8	7.9	7.1	6.2	dB

Notes:

1. Power Tuned
2. Efficiency Tuned

Thermal and Reliability Information – CW(1)

Parameter	Simulation Conditions	Value	Units
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 45.4 W, $T_{baseplate}$ = 85 °C	2.53	°C/W
Channel Temperature (T_{CH})		200	°C
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 37.8 W, $T_{baseplate}$ = 85 °C	2.43	°C/W
Channel Temperature (T_{CH})		177	°C
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 30.2 W, $T_{baseplate}$ = 85 °C	2.35	°C/W
Channel Temperature (T_{CH})		156	°C
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 22.7 W, $T_{baseplate}$ = 85 °C	2.28	°C/W
Channel Temperature (T_{CH})		137	°C
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 15.1 W, $T_{baseplate}$ = 85 °C	2.19	°C/W
Channel Temperature (T_{CH})		118	°C
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 7.6 W, $T_{baseplate}$ = 85 °C	1.96	°C/W
Channel Temperature (T_{CH})		100	°C

Note:
1. Thermal resistance measured to bottom of package.
2. Refer to the following document: GaN Device Channel Temperature. Thermal Resistance, and Reliability Estimates

Thermal and Reliability Information – Pulsed(1)

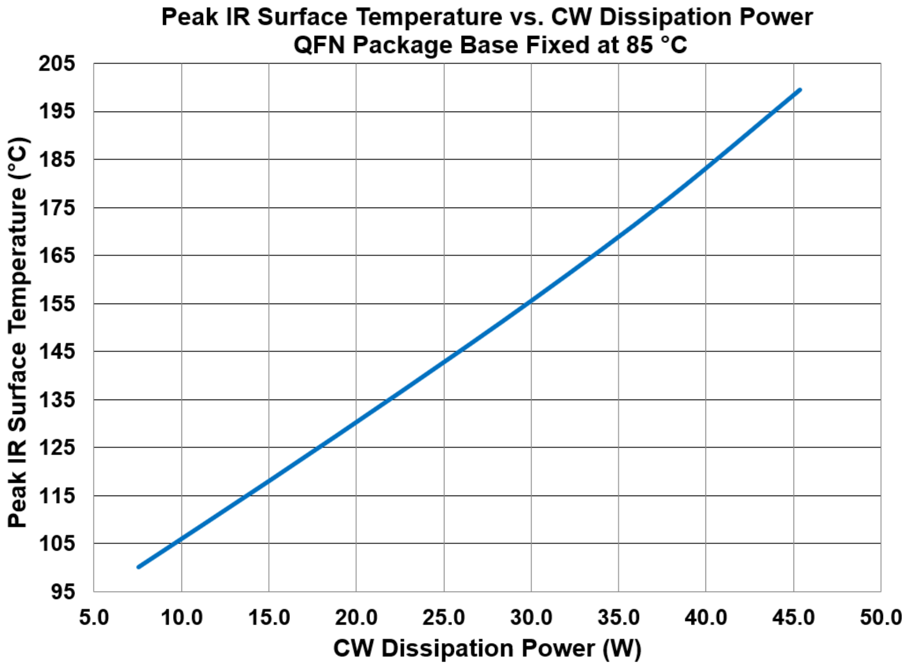
Parameter	Simulation Conditions	Value	Units
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 45.4 W, $T_{baseplate}$ = 85 °C Pulse Width = 500 uS	2.36	°C/W
Channel Temperature (T_{CH})	Duty Cycle = 10%	192	°C
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 37.8 W, $T_{baseplate}$ = 85 °C Pulse Width = 500 uS	2.20	°C/W
Channel Temperature (T_{CH})	Duty Cycle = 10%	168	°C
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 45.4 W, $T_{baseplate}$ = 85 °C Pulse Width = 100 uS	1.82	°C/W
Channel Temperature (T_{CH})	Duty Cycle = 10%	168	°C
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 37.8 W, $T_{baseplate}$ = 85 °C Pulse Width = 100 uS	1.78	°C/W
Channel Temperature (T_{CH})	Duty Cycle = 10%	152	°C

Note:
1. Thermal resistance measured to bottom of package.
2. Refer to the following document: GaN Device Channel Temperature. Thermal Resistance, and Reliability Estimates

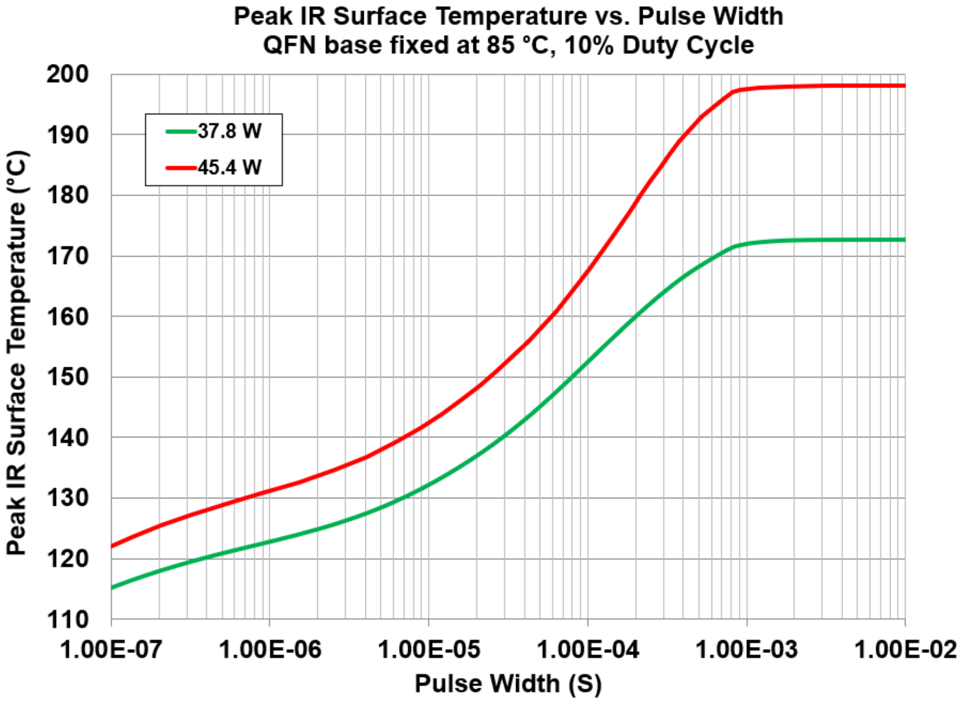
Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Gate Leakage	V_D = +10, V_G = −3.7	−8.25			mA

Maximum Channel Temperature, CW



Maximum Channel Temperature, Pulsed

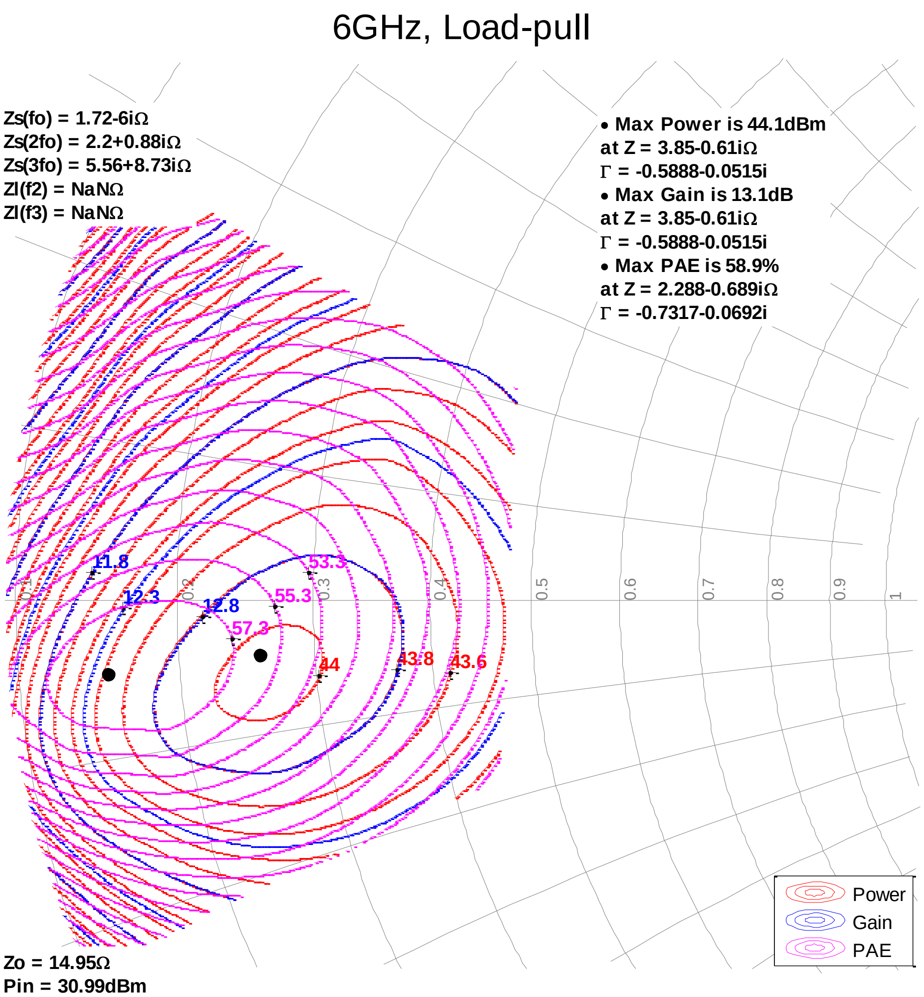


Load Pull Smith Charts – Pulsed(1,2,3)

RF performance that the device typically exhibits when placed in the specified impedance environment. The impedances are not the impedances of the device, they are the impedances presented to the device via an RF circuit or load-pull system. The impedances listed follow an optimized trajectory to maintain high power and high efficiency.

Notes:

1. 32 V, 150 mA, Pulsed signal with 100 uS pulse width and 10 % duty cycle. Performance is at indicated input power.
2. See page 13 for load pull and source pull reference planes. 15-Ω load pull TRL fixtures are built with 10-mil RO4350B material.
3. NaN means the impedances are either undefined or varying in load-pull system.

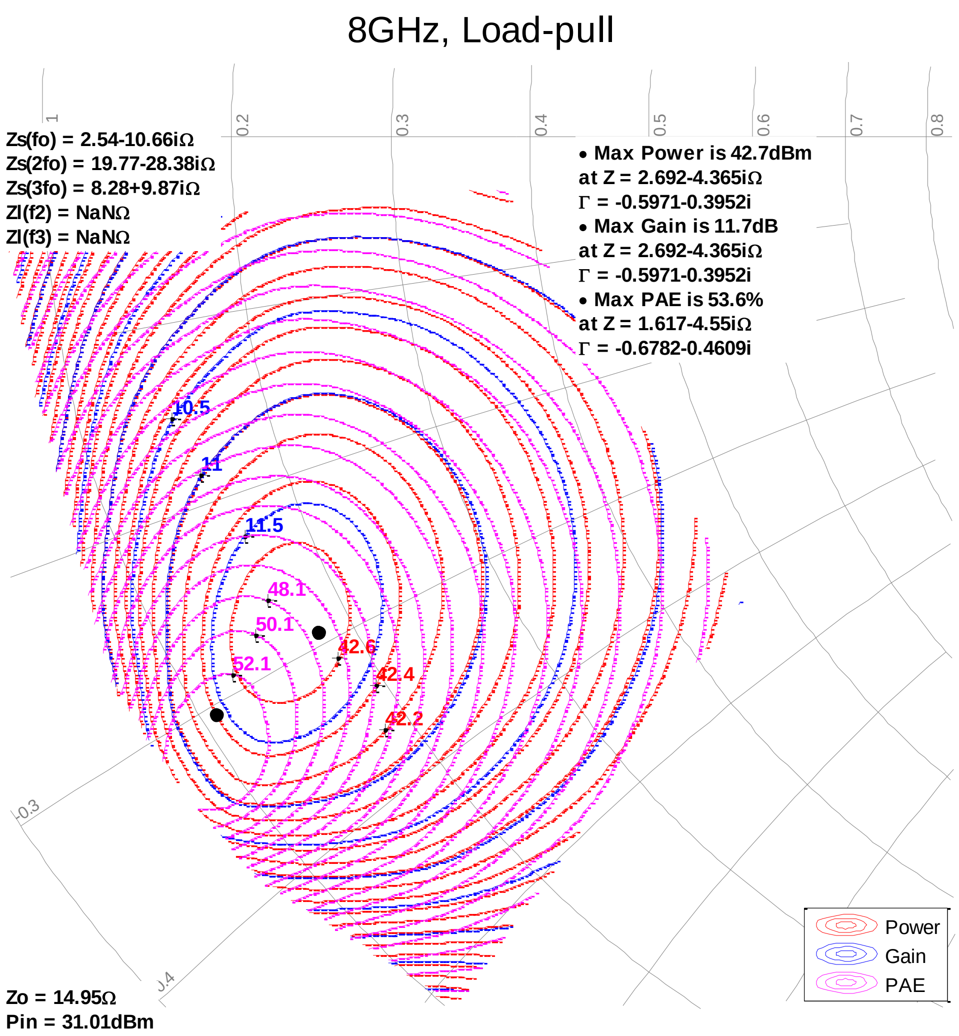


Load Pull Smith Charts – Pulsed[1,2,3]

RF performance that the device typically exhibits when placed in the specified impedance environment. The impedances are not the impedances of the device, they are the impedances presented to the device via an RF circuit or load-pull system. The impedances listed follow an optimized trajectory to maintain high power and high efficiency.

Notes:

1. 32 V, 150 mA, Pulsed signal with 100 uS pulse width and 10 % duty cycle. Performance is at indicated input power.
2. See page 13 for load pull and source pull reference planes. 15-Ω load pull TRL fixtures are built with 10-mil RO4350B material.
3. NaN means the impedances are either undefined or varying in load-pull system.

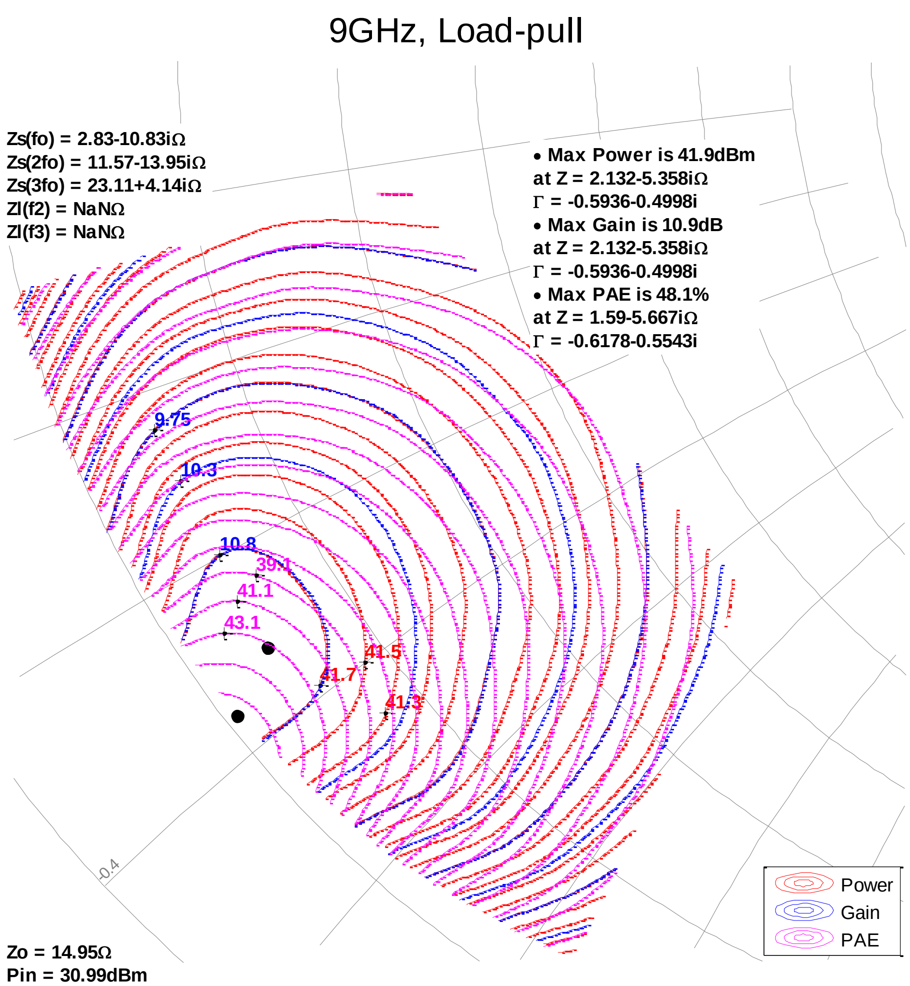


Load Pull Smith Charts – Pulsed(1,2,3)

RF performance that the device typically exhibits when placed in the specified impedance environment. The impedances are not the impedances of the device, they are the impedances presented to the device via an RF circuit or load-pull system. The impedances listed follow an optimized trajectory to maintain high power and high efficiency.

Notes:

1. 32 V, 150 mA, Pulsed signal with 100 uS pulse width and 10 % duty cycle. Performance is at indicated input power.
2. See page 13 for load pull and source pull reference planes. 15-Ω load pull TRL fixtures are built with 10-mil RO4350B material.
3. NaN means the impedances are either undefined or varying in load-pull system.

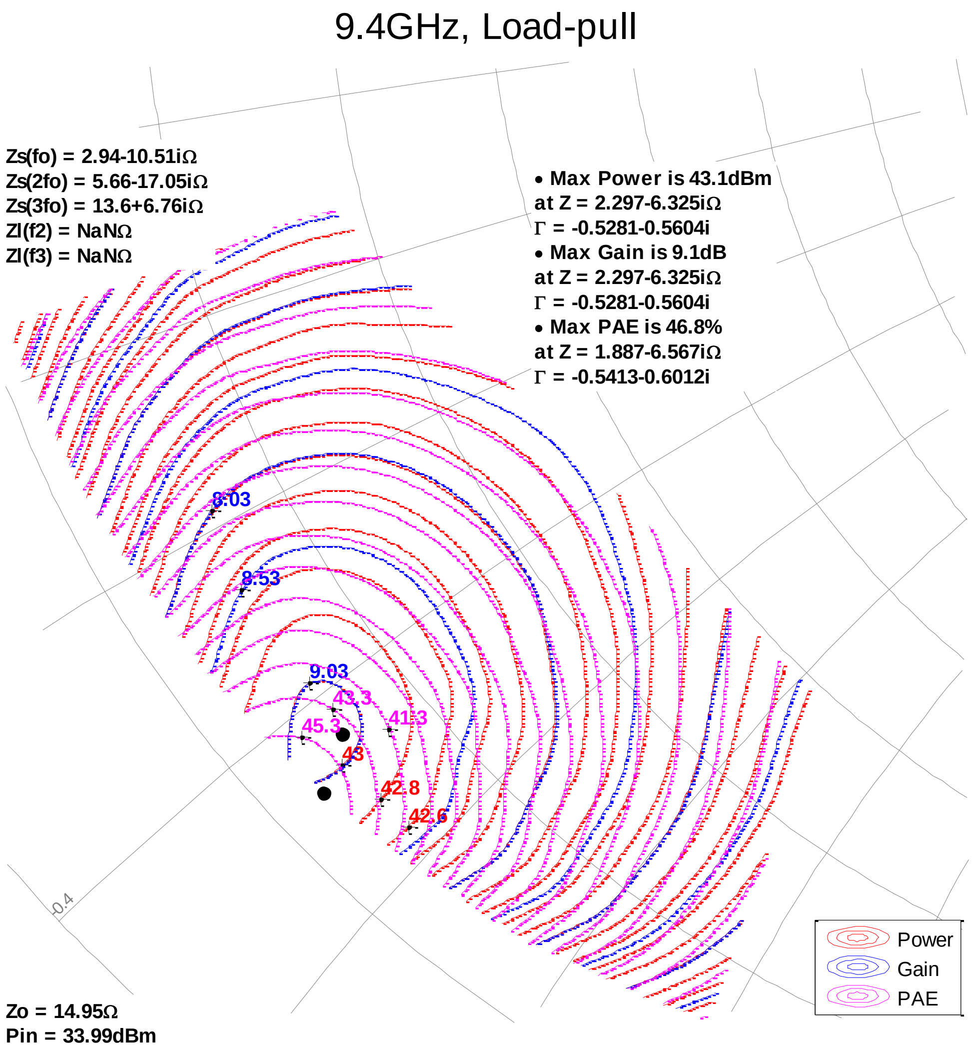


Load Pull Smith Charts – Pulsed(1,2,3)

RF performance that the device typically exhibits when placed in the specified impedance environment. The impedances are not the impedances of the device, they are the impedances presented to the device via an RF circuit or load-pull system. The impedances listed follow an optimized trajectory to maintain high power and high efficiency.

Notes:

1. 32 V, 150 mA, Pulsed signal with 100 uS pulse width and 10 % duty cycle. Performance is at indicated input power.
2. See page 13 for load pull and source pull reference planes. 15-Ω load pull TRL fixtures are built with 10-mil RO4350B material.
3. NaN means the impedances are either undefined or varying in load-pull system.

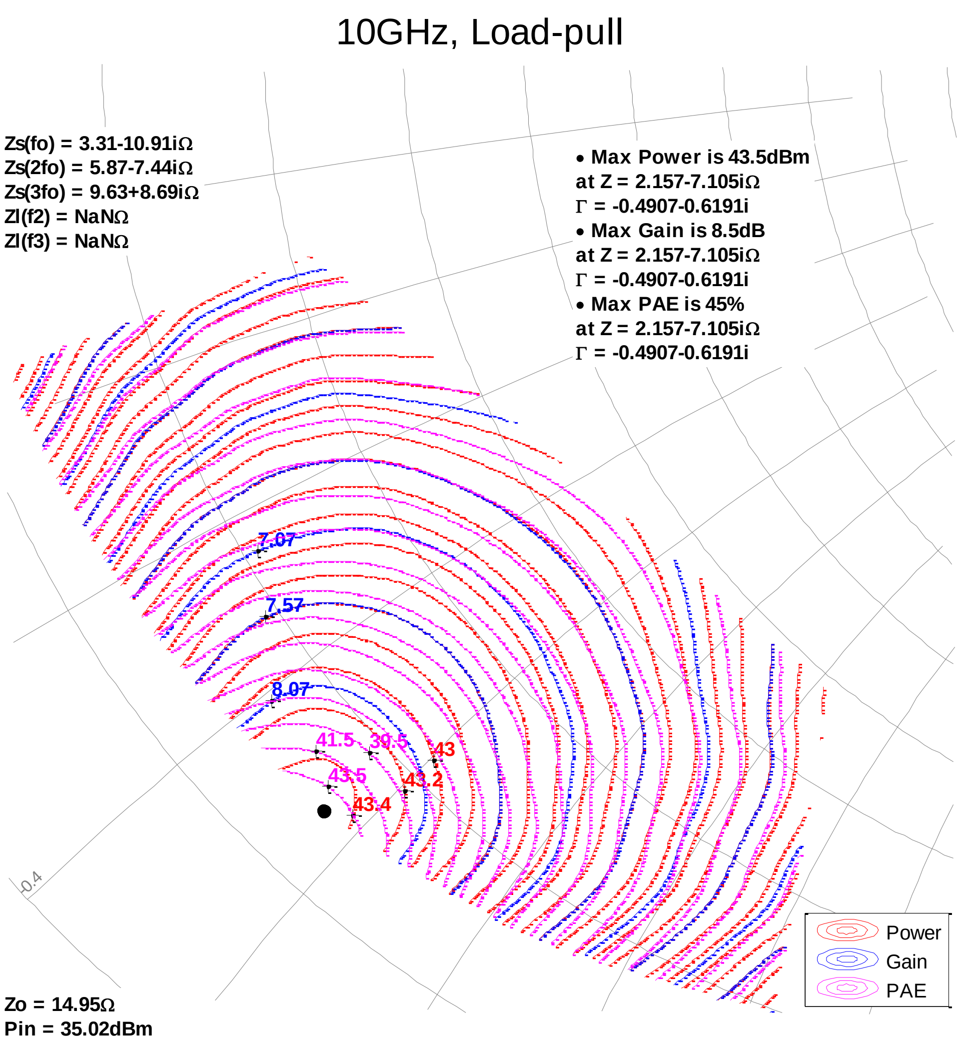


Load Pull Smith Charts – Pulsed(1,2,3)

RF performance that the device typically exhibits when placed in the specified impedance environment. The impedances are not the impedances of the device, they are the impedances presented to the device via an RF circuit or load-pull system. The impedances listed follow an optimized trajectory to maintain high power and high efficiency.

Notes:

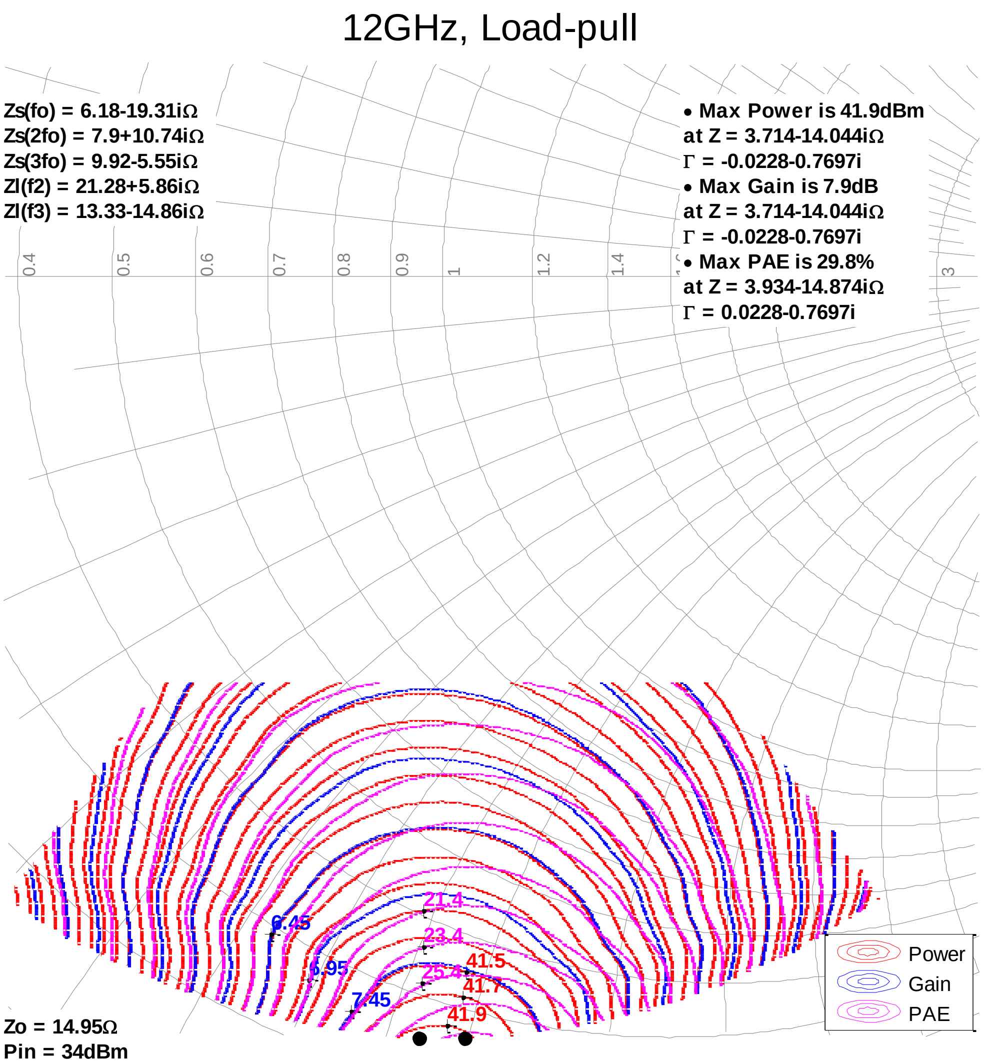
1. 32 V, 150 mA, Pulsed signal with 100 uS pulse width and 10 % duty cycle. Performance is at indicated input power.
2. See page 13 for load pull and source pull reference planes. 15-Ω load pull TRL fixtures are built with 10-mil RO4350B material.
3. NaN means the impedances are either undefined or varying in load-pull system.



Load Pull Smith Charts – Pulsed(1,2,3)

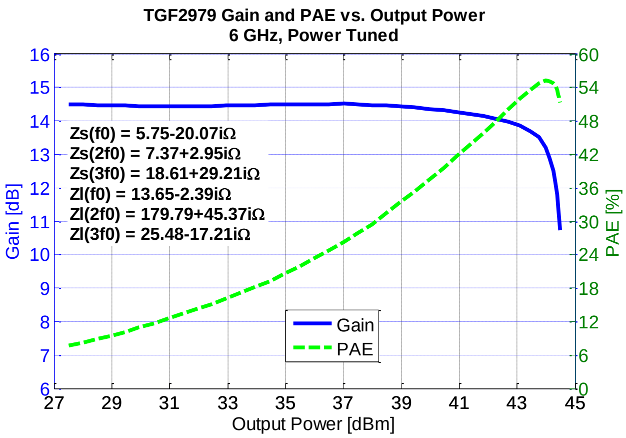
RF performance that the device typically exhibits when placed in the specified impedance environment. The impedances are not the impedances of the device, they are the impedances presented to the device via an RF circuit or load-pull system. The impedances listed follow an optimized trajectory to maintain high power and high efficiency.
Notes:

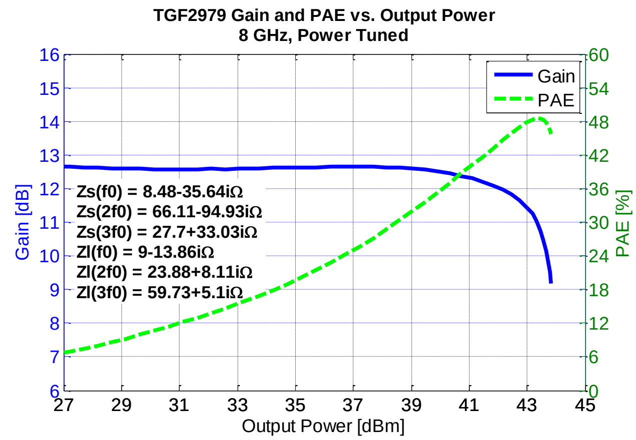
1. 32 V, 150 mA, Pulsed signal with 100 uS pulse width and 10 % duty cycle. Performance is at indicated input power.
2. See page 13 for load pull and source pull reference planes. 15-Ω load pull TRL fixtures are built with 10-mil RO4350B material.
3. NaN means the impedances are either undefined or varying in load-pull system.

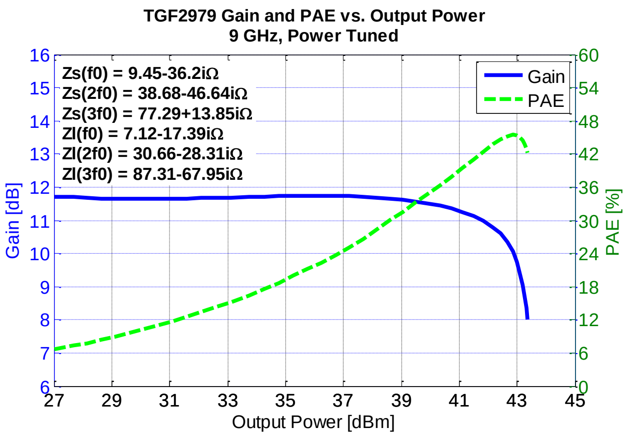


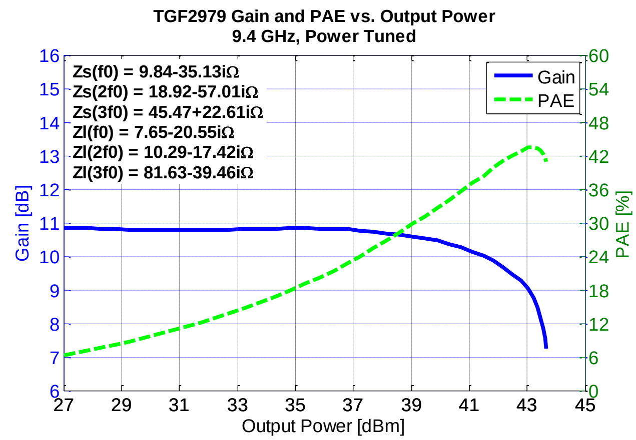
Typical Pulsed Performance – Power Tuned[1,2]

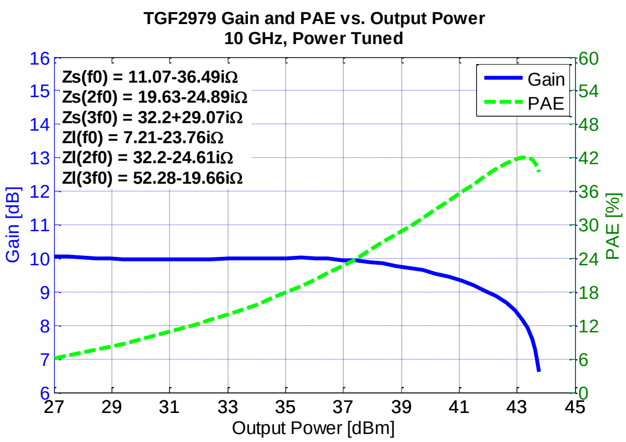
Notes:
1. Pulsed signal with 100uS pulse width and 10% duty cycle
2. See page 13 for load pull and source pull reference planes where the performance was measured.

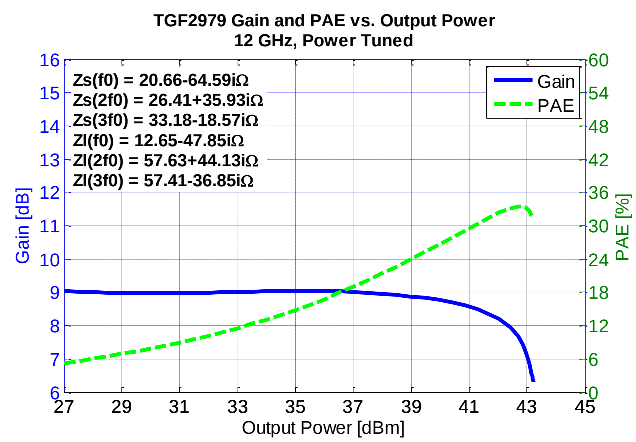






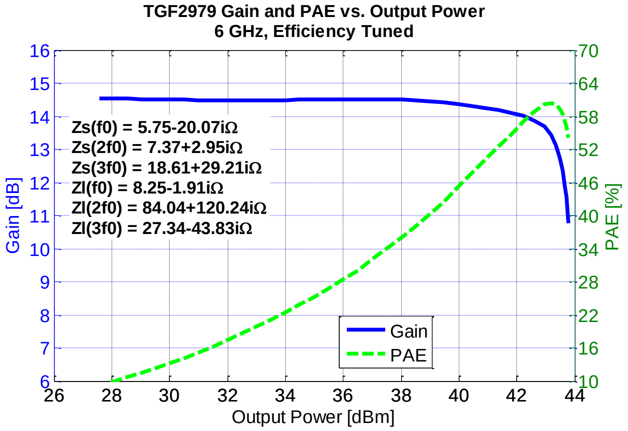


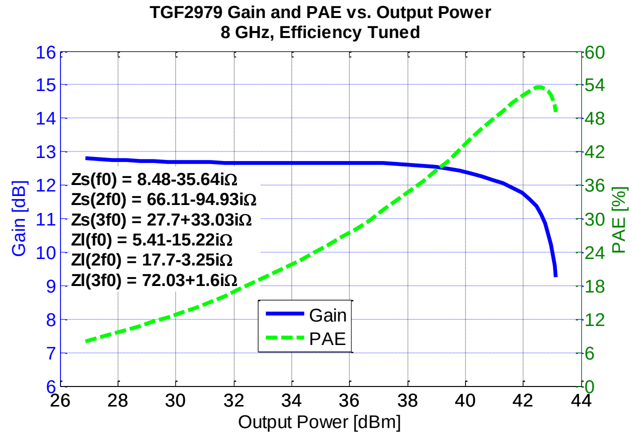


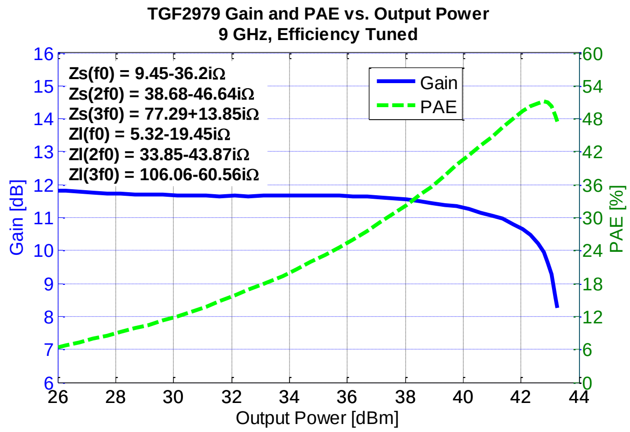


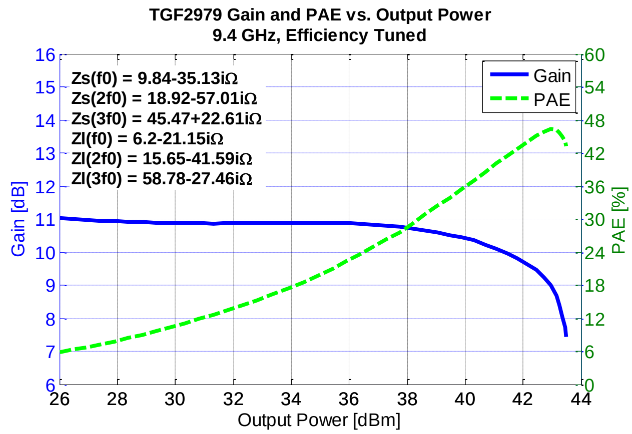
Typical Pulsed Performance – Efficiency Tuned(1,2)

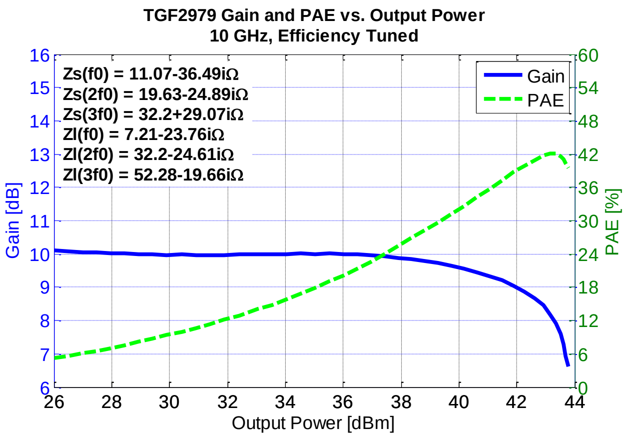
Notes:
1. Pulsed signal with 100uS pulse width and 10% duty cycle
2. See page 13 for load pull and source pull reference planes where the performance was measured.

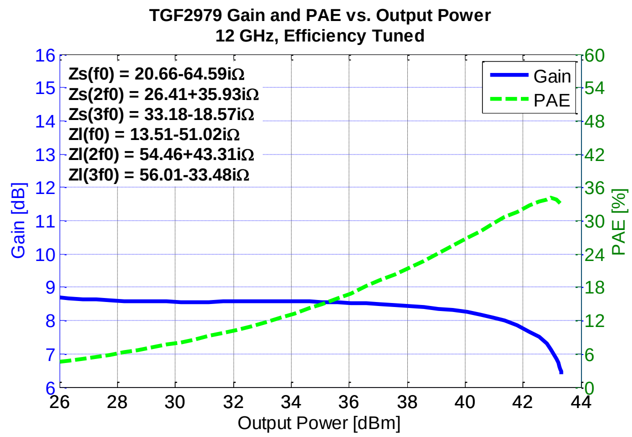






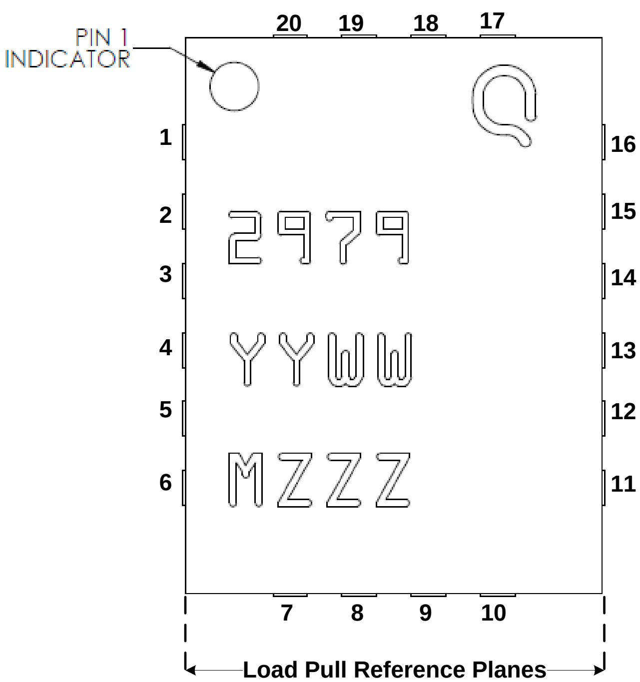






Pin Layout

Marking: Qorvo Logo
Part Number – TGF2979-SM (The TGF2979-SM will be marked with the "2979" designator)
Date Code – YYWW
Lot Code – MZZZ

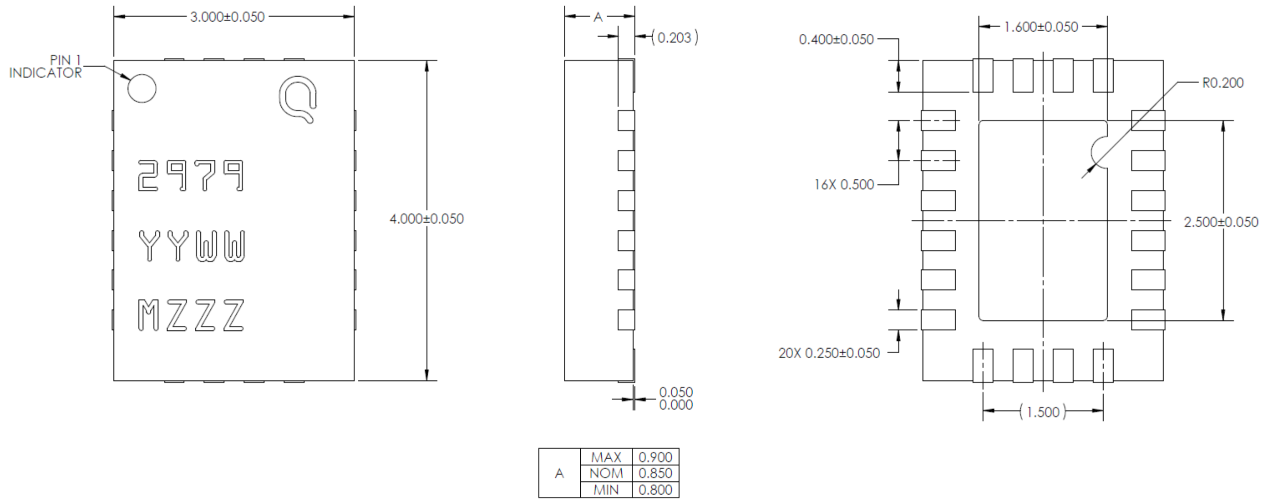


Pin Description

Pin	Symbol	Description
11 – 16	V_D/RF OUT	Drain voltage / RF Output to be matched to 50 ohms;
1 – 6	V_G/RF IN	Gate voltage / RF Input to be matched to 50 ohms; see
7 – 10, 17 – 20	N/C	Not connected
Back side	Source	Source connected to ground

Mechanical Information

All dimensions are in millimeters.



Note:

1. Unless otherwise noted, all dimension tolerances are +/-0.127 mm.
2. This package is lead-free/RoHS-compliant. The plating material on the leads is NiAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and tin-lead (maximum 245°C reflow temperature) soldering processes.

Recommended Solder Temperature Profile