

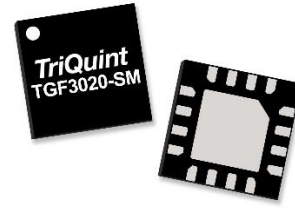
Product Overview

The Qorvo TGF3020-SM is a 5W (P_{3dB}), 50Ω-input matched discrete GaN on SiC HEMT which operates from 4.0 to 6.0GHz. The integrated input matching network enables wideband gain and power performance, while the output can be matched on board to optimize power and efficiency for any region within the band.

The device is housed in an industry-standard 3 x 3 mm surface mount QFN package.

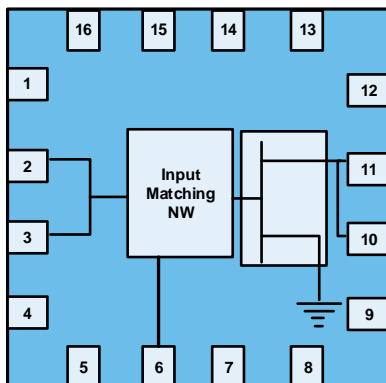
Lead-free and ROHS compliant

Evaluation boards are available upon request.



3 x 3mm QFN package

Functional Block Diagram



Key Features

- Frequency: 4 to 6 GHz
 - Output Power (P_{3dB})¹: 6.8 W
 - Linear Gain¹: 13 dB
 - Typical PAE_{3dB}¹: 60%
 - Operating Voltage: 32 V
 - CW and Pulse capable
- Note 1: @ 5 GHz Load Pull

Applications

- Telemetry
- C-band radar
- Communications
- Test instrumentation
- Wideband amplifiers
- 5.8GHz ISM

Ordering Information

Part No.	Description
TGF3020-SM	QFN Packaged Part
TGF3020-SMEVBP01	5.3 – 5.9 GHz EVB
TGF3020-SMEVBP02	4 – 6 GHz EVB

Absolute Maximum Ratings¹

Parameter	Rating	Units
Breakdown Voltage, V_{BDG}	+100	V
Gate Voltage Range, V_G	-7 to +2	V
Drain Current, $I_{D_{MAX}}$	0.6	A
Power Dissipation, P_{DISS}^2	7.5	W
RF Input Power, CW, T = 25 °C	+30	dBm
Storage Temperature	-65 to +150	°C

Notes:

1. Operation of this device outside the parameter ranges given above may cause permanent damage.
2. Pulsed 100uS PW, 20% DC

Recommended Operating Conditions¹

Parameter	Min	Typ	Max	Units
Operating Temp. Range	-40	+25	+85	°C
Drain Voltage Range, V_D	+12	+32	+40	V
Drain Bias Current, I_{DQ}		25		mA
Drain Current, I_D^4	-	0.25	-	A
Gate Voltage, V_G^3	-	-2.8	-	V
Power Dissipation (P_D) ^{2,4}	-	-	9.1	W
Power Dissipation (P_D), CW ²	-	-	6.5	W

Notes:

1. Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.
2. Package base at 85 °C
3. To be adjusted to desired I_{DQ}
4. Pulsed, 100uS PW, 20% DC

Measured Load Pull Performance – Power Tuned^{1, 2}

Parameter	Typical Values				Units
	4	4.4	5	5.5	
Frequency, F	4	4.4	5	5.5	GHz
Drain Voltage, V_D	32	32	32	32	V
Drain Bias Current, I_{DQ}	25	25	25	25	mA
Output Power at 3dB compression, P_{3dB}	38.4	38.3	38.3	38.2	dBm
Power Added Efficiency at 3dB compression, PAE_{3dB}	50.1	50.4	49.5	53.0	%
Gain at 3dB compression, G_{3dB}	9.6	9.7	9.7	10.3	dB

Notes:

1. Pulsed, 100 uS Pulse Width, 20% Duty Cycle
2. Load-pull characteristic Impedance, $Z_o = 50 \Omega$.

Measured Load Pull Performance – Efficiency Tuned^{1, 2}

Parameter	Typical Values				Units
	2.7	2.9	3.1	3.3	
Frequency, F	2.7	2.9	3.1	3.3	GHz
Drain Voltage, V_D	32	32	32	32	V
Drain Bias Current, I_{DQ}	25	25	25	25	mA
Output Power at 3dB compression, P_{3dB}	37.6	36.8	37.1	36.8	dBm
Power Added Efficiency at 3dB compression, PAE_{3dB}	60.1	61.5	59.6	59	%
Gain at 3dB compression, G_{3dB}	10.3	10.3	10.1	10.7	dB

Notes:

1. Pulsed, 100 uS Pulse Width, 20% Duty Cycle
2. Load-pull characteristic Impedance, $Z_o = 50 \Omega$.

RF Characterization 5.3 – 5.9 GHz EVB – 5.4 GHz Performance¹

Parameter	Min	Typ	Max	Units
Linear Gain, G_{LIN}	–	11.7	–	dB
Output Power at 3dB compression point, P3dB	–	5.7	–	W
Drain Efficiency at 3dB compression point, DEFF3dB	–	53.1	–	%
Gain at 3dB compression point, G3dB	–	8.7	–	dB

Notes:

- $V_D = +32\text{ V}$, $I_{DQ} = 25\text{ mA}$, Temp = +25 °C, Pulse Width = 100 uS, Duty Cycle = 20%

RF Characterization 4 – 6.0 GHz EVB – 4.7 GHz Performance¹

Parameter	Min	Typ	Max	Units
Linear Gain, G_{LIN}	–	11.8	–	dB
Output Power at 3dB compression point, P3dB	–	5.6	–	W
Drain Efficiency at 3dB compression point, DEFF3dB	–	51.7	–	%
Gain at 3dB compression point, G3dB	–	8.8	–	dB

Notes:

- $V_D = +32\text{ V}$, $I_{DQ} = 25\text{ mA}$, Temp = +25 °C, Pulse Width = 100 uS, Duty Cycle = 20%

RF Characterization – Mismatch Ruggedness at 5.3 and 5.9 GHz

Symbol	Parameter	dB Compression	Typical
VSWR	Impedance Mismatch Ruggedness	3	10:1

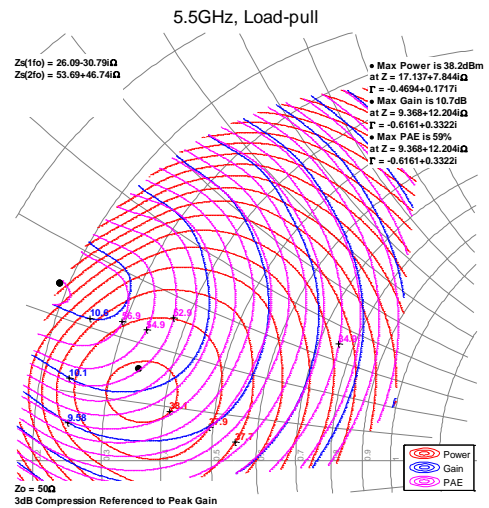
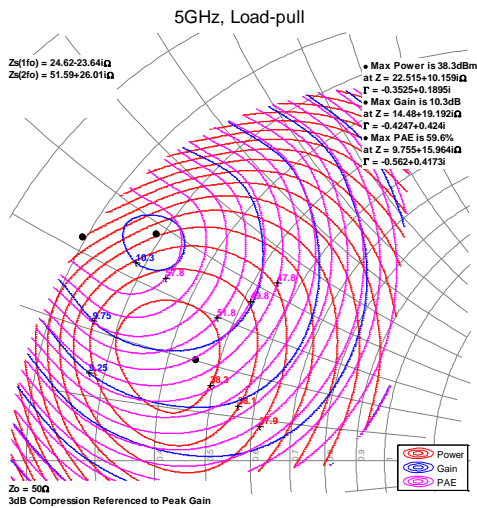
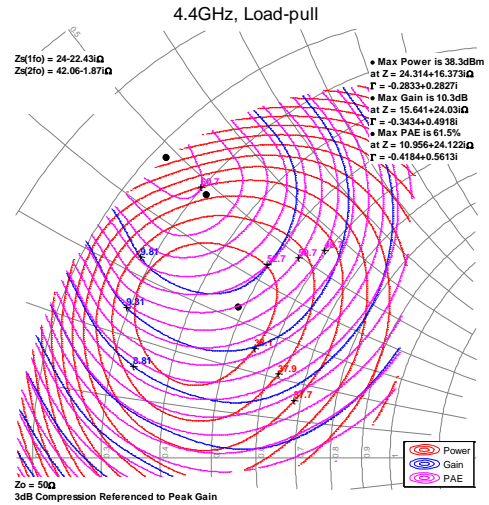
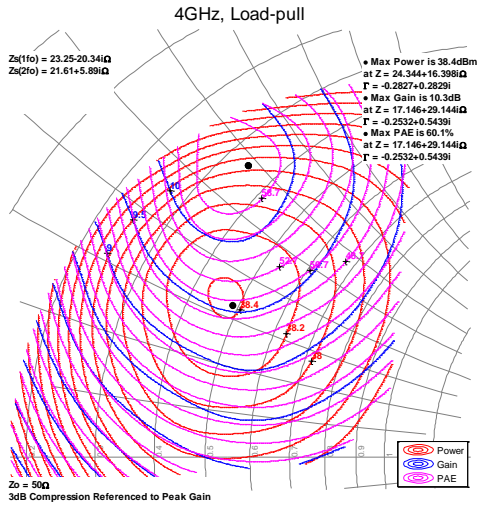
Test conditions unless otherwise noted: $T_A = 25\text{ °C}$, $V_D = 32\text{ V}$, $I_{DQ} = 25\text{ mA}$

Input drive power is determined at pulsed 3dB compression under matched condition at EVB output connector.

Measured Load-Pull Smith Charts^{1, 2}

Notes:

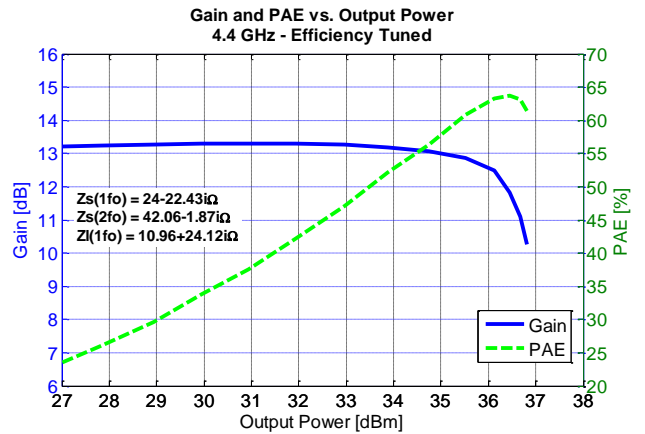
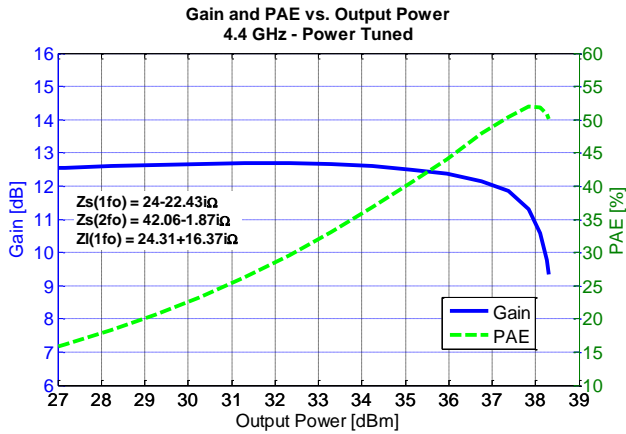
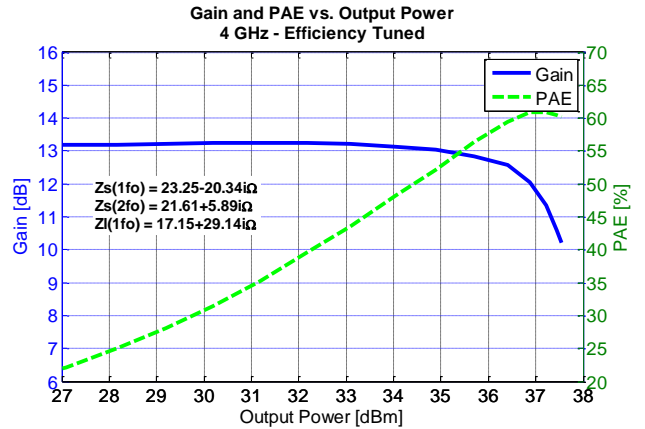
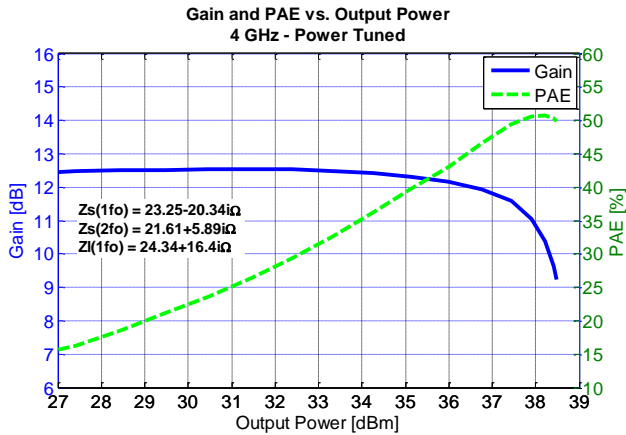
1. Test Conditions: $V_D = 32\text{ V}$, $I_{DQ} = 25\text{ mA}$, $100\text{ }\mu\text{s}$ Pulse Width, 20% Duty Cycle



Typical Measured Performance – Load-Pull Drive-up^{1, 2}

Notes:

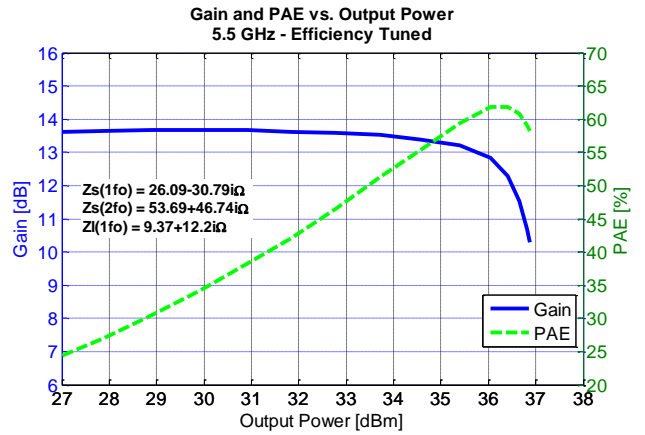
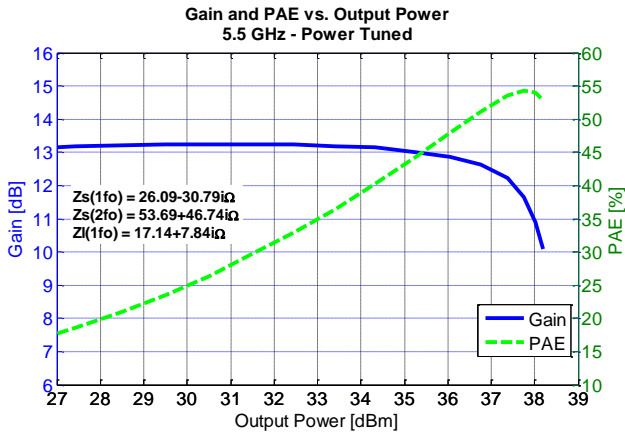
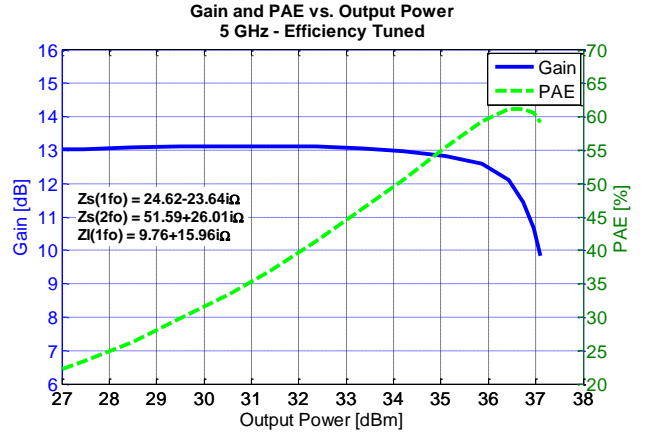
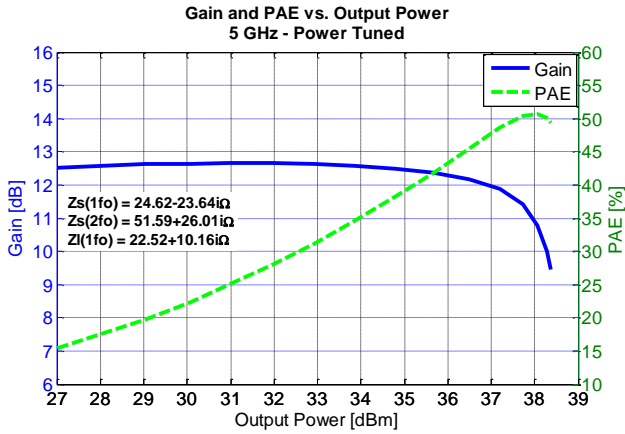
1. Pulsed signal with 100uS pulse width and 20% duty cycle



Typical Measured Performance – Load-Pull Drive-up^{1, 2}

Notes:

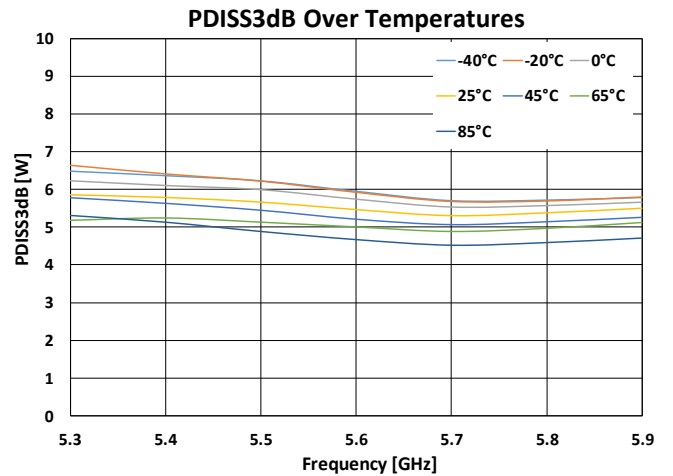
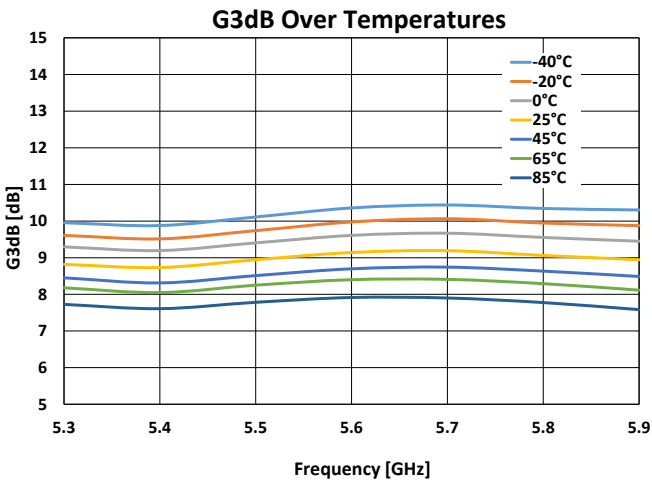
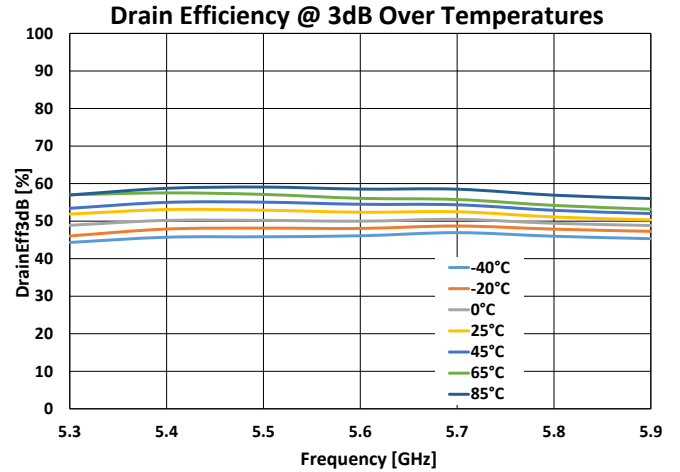
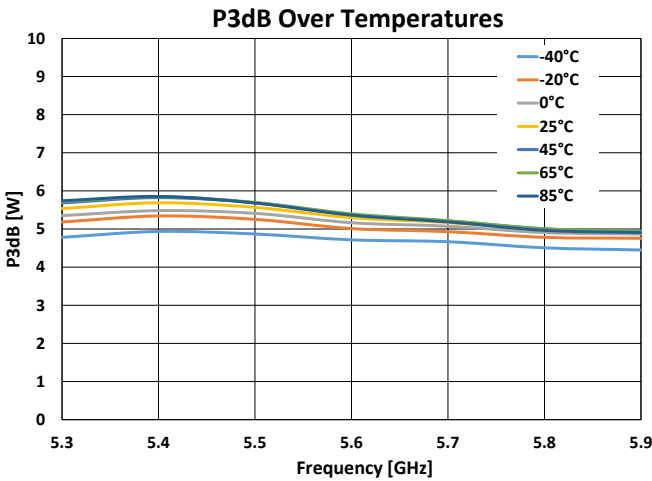
1. Pulsed signal with 100uS pulse width and 20% duty cycle



Power Driveup Performance Over Temperatures Of 5.3 – 5.9 GHz EVB^{1,2}

Notes:

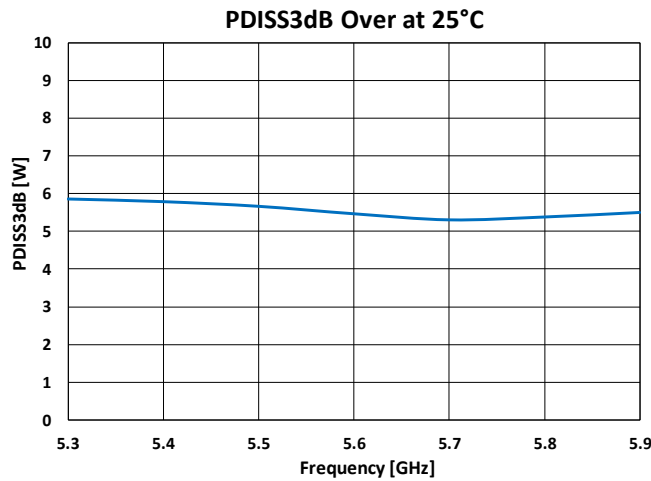
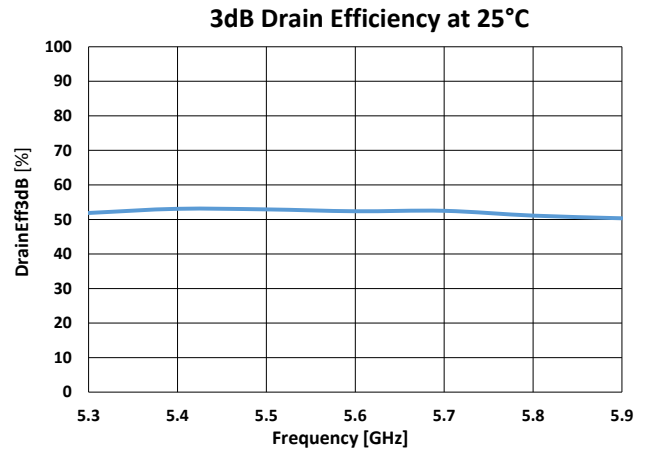
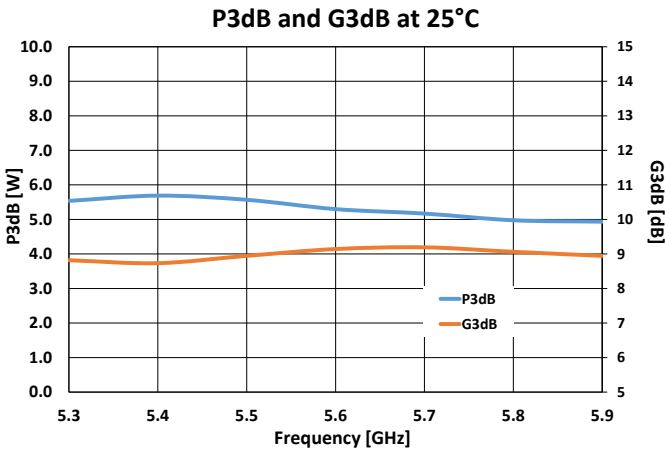
1. Test Conditions: $V_D = 32\text{ V}$, $I_{DQ} = 25\text{ mA}$, 20 μs Pulse Width, 20% Duty Cycle
2. The dissipation power limit is conservative because it is specified at DUT only without accounting for the loss of the output matching network.



Power Driveup Performance At 25°C Of 5.3 – 5.9 GHz EVB^{1, 2}

Notes:

1. Test Conditions: $V_D = 32\text{ V}$, $I_{DQ} = 25\text{ mA}$, 20 μs Pulse Width, 20% Duty Cycle
2. The dissipation power limit is conservative because it is specified at DUT only without accounting for the loss of the output matching network..

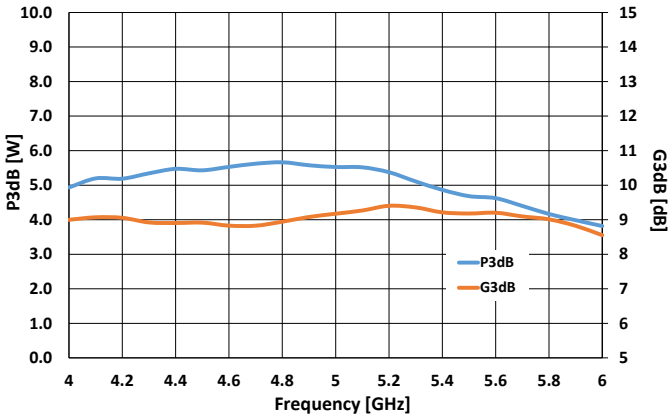


Power Driveup Performance At 25°C Of 4 – 6 GHz EVB^{1, 2}

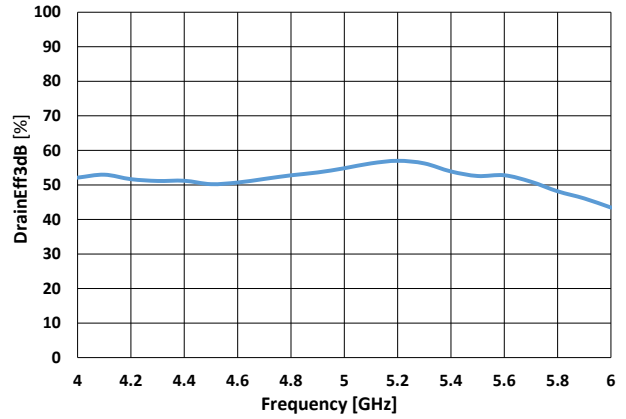
Notes:

1. Test Conditions: $V_D = 32\text{ V}$, $I_{DQ} = 25\text{ mA}$, 100 μs Pulse Width, 20% Duty Cycle
2. The dissipation power limit is conservative because it is specified at DUT only without accounting for the loss of the output matching network..

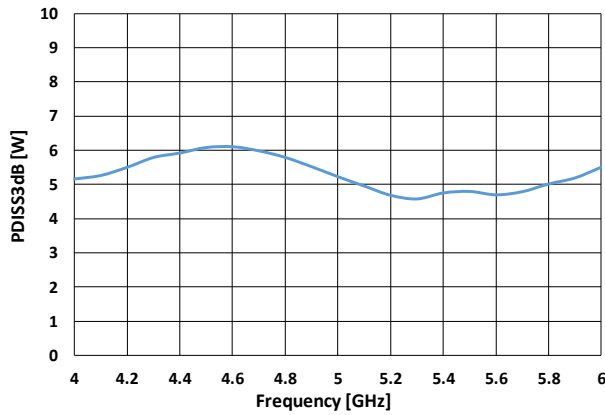
P3dB and G3dB at 25°C



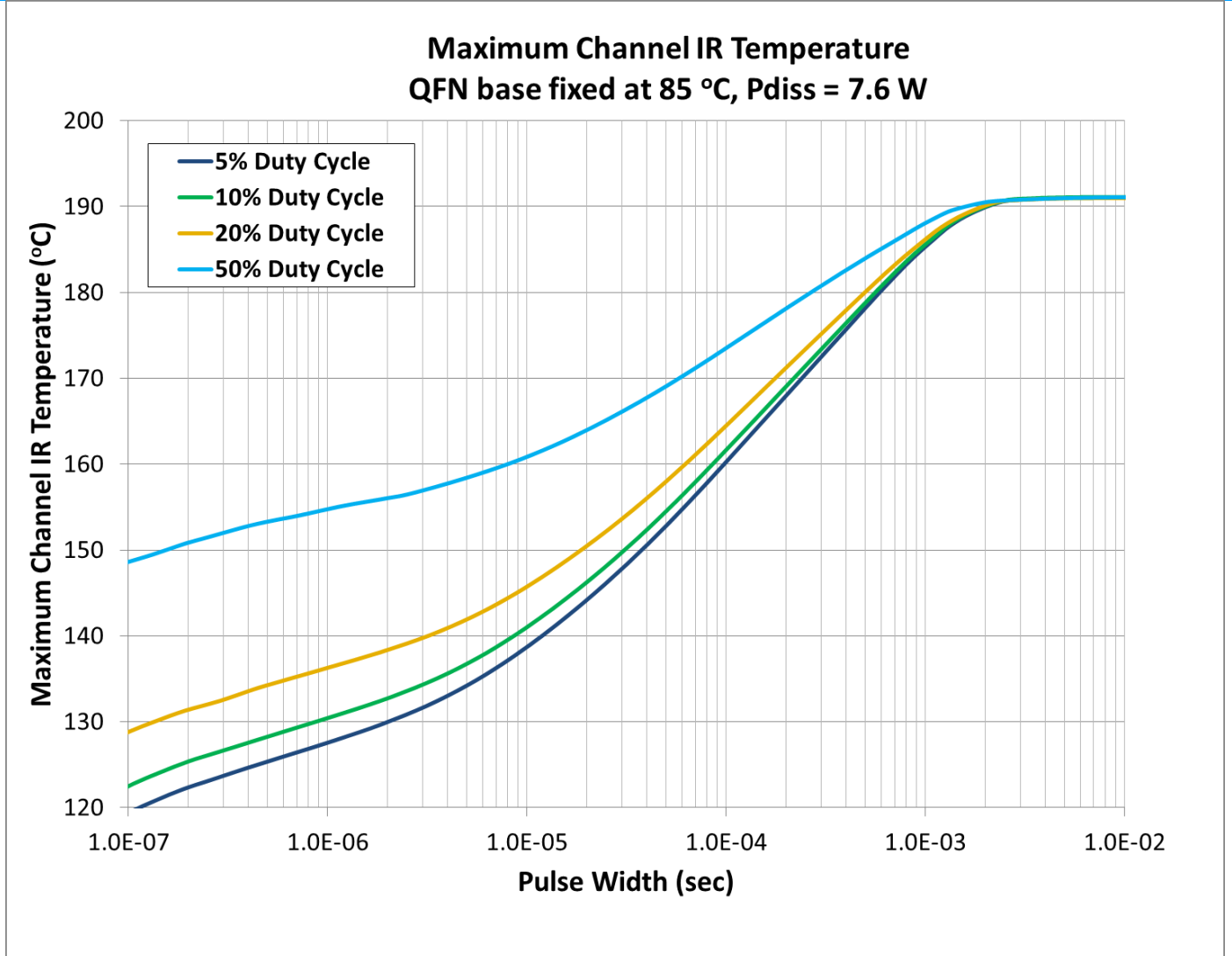
3dB Drain Efficiency at 25°C



PDISS3dB at 25°C



Thermal and Reliability Information – Pulsed¹

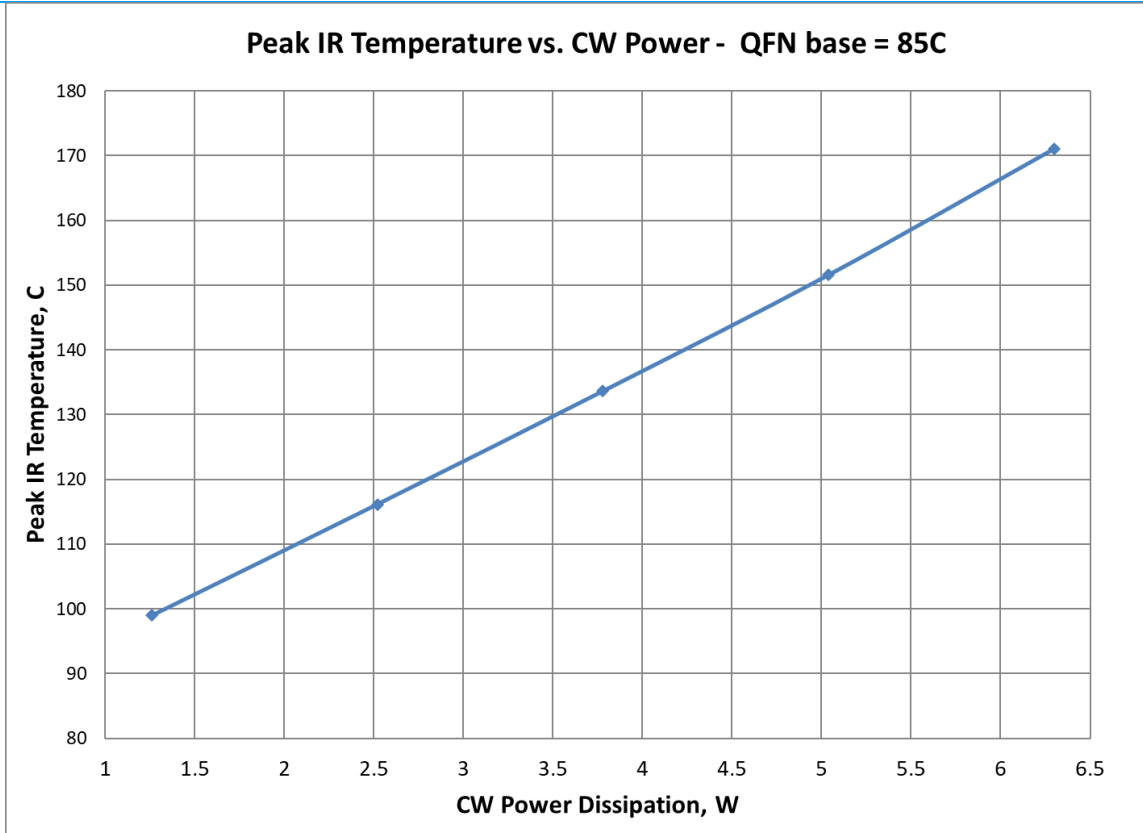


Parameter	Conditions	Values	Units
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$T_{CASE} = +85^{\circ}C$, $T_{CH} = 160^{\circ}C$, $P_{DISS} = 7.6 W$, 100 μ S PW, 5% DC	9.9	$^{\circ}C/W$
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$T_{CASE} = +85^{\circ}C$, $T_{CH} = 162^{\circ}C$, $P_{DISS} = 7.6 W$, 100 μ S PW, 10% DC	10.1	$^{\circ}C/W$
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$T_{CASE} = +85^{\circ}C$, $T_{CH} = 165^{\circ}C$, $P_{DISS} = 7.6 W$, 100 μ S PW, 20% DC	10.4	$^{\circ}C/W$
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$T_{CASE} = +85^{\circ}C$, $T_{CH} = 173^{\circ}C$, $P_{DISS} = 7.6 W$, 100 μ S PW, 50% DC	11.6	$^{\circ}C/W$

Notes:

1. Thermal resistance is measured to package backside.
2. Refer to the following document: [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

Thermal and Reliability Information – CW¹



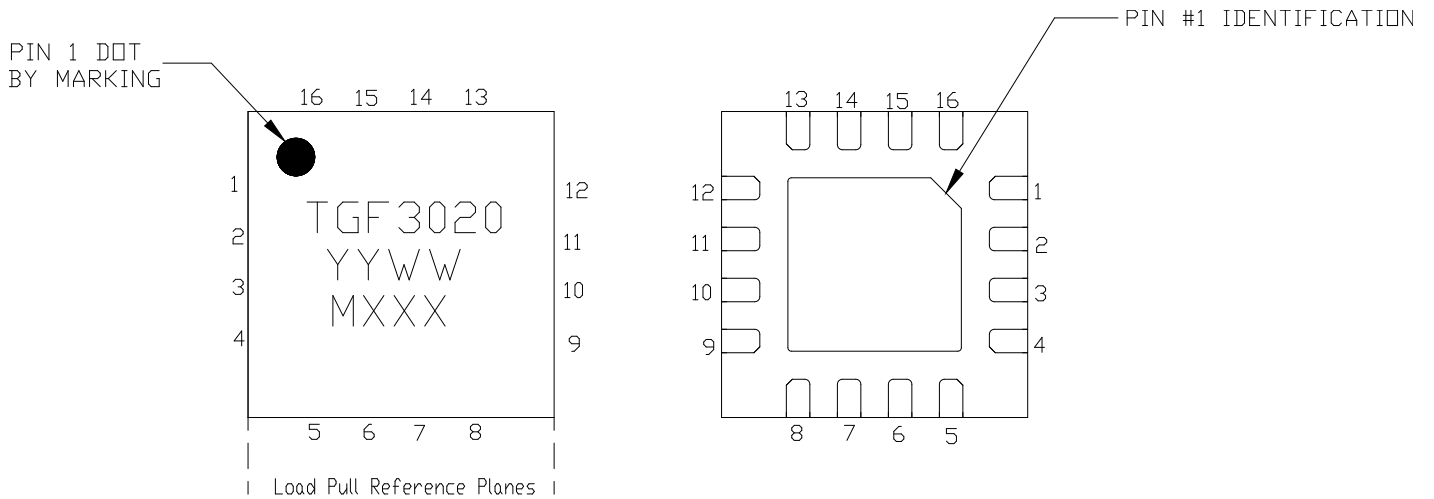
Parameter	Conditions	Values	Units
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$T_{CASE} = +85^{\circ}C$, $T_{CH} = 116^{\circ}C$, $P_{DISS} = 2.52 W$	12.4	$^{\circ}C/W$
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$T_{CASE} = +85^{\circ}C$, $T_{CH} = 133^{\circ}C$, $P_{DISS} = 3.78 W$	12.9	$^{\circ}C/W$
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$T_{CASE} = +85^{\circ}C$, $T_{CH} = 152^{\circ}C$, $P_{DISS} = 5.04 W$	13.2	$^{\circ}C/W$
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$T_{CASE} = +85^{\circ}C$, $T_{CH} = 171^{\circ}C$, $P_{DISS} = 6.30 W$	13.7	$^{\circ}C/W$

Notes:

1. Thermal resistance is measured to package backside.
2. Refer to the following document: [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

Pin Configuration and Description¹

Note 1: The TGF3020-SM will be marked with the “TGF3020” designator and a lot code marked below the part designator. The “YY” represents the last two digits of the calendar year the part was manufactured, the “WW” is the work week of the assembly lot start, the MXXX” is the production lot number.



Pin	Symbol	Description
2, 3	RF IN / V_G	Gate
10, 11	RF OUT / V_D	Drain
1, 4, 5, 6, 7, 8, 9, 12, 13, 14, 15, 16	NC	No Connection ¹
	Source	Source / Ground / Backside of part

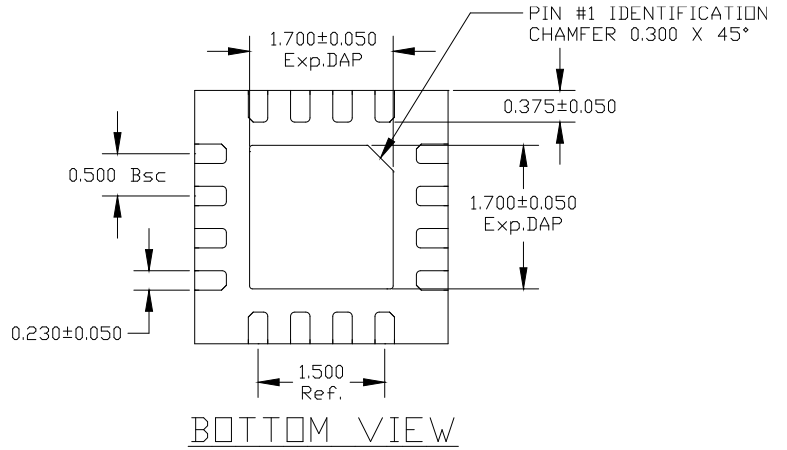
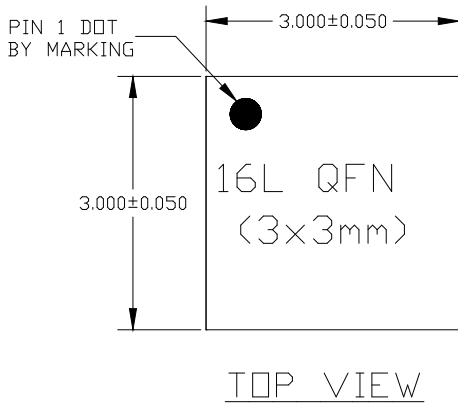
Note 1: Grounding pin 6 will cause performance degradation.

Mechanical Drawing¹

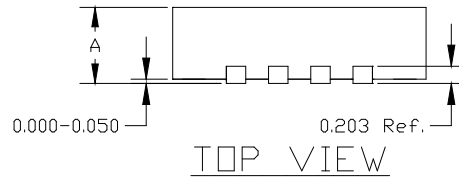
Note 1:

Unless otherwise noted, all dimension tolerances are +/-0.127 mm.

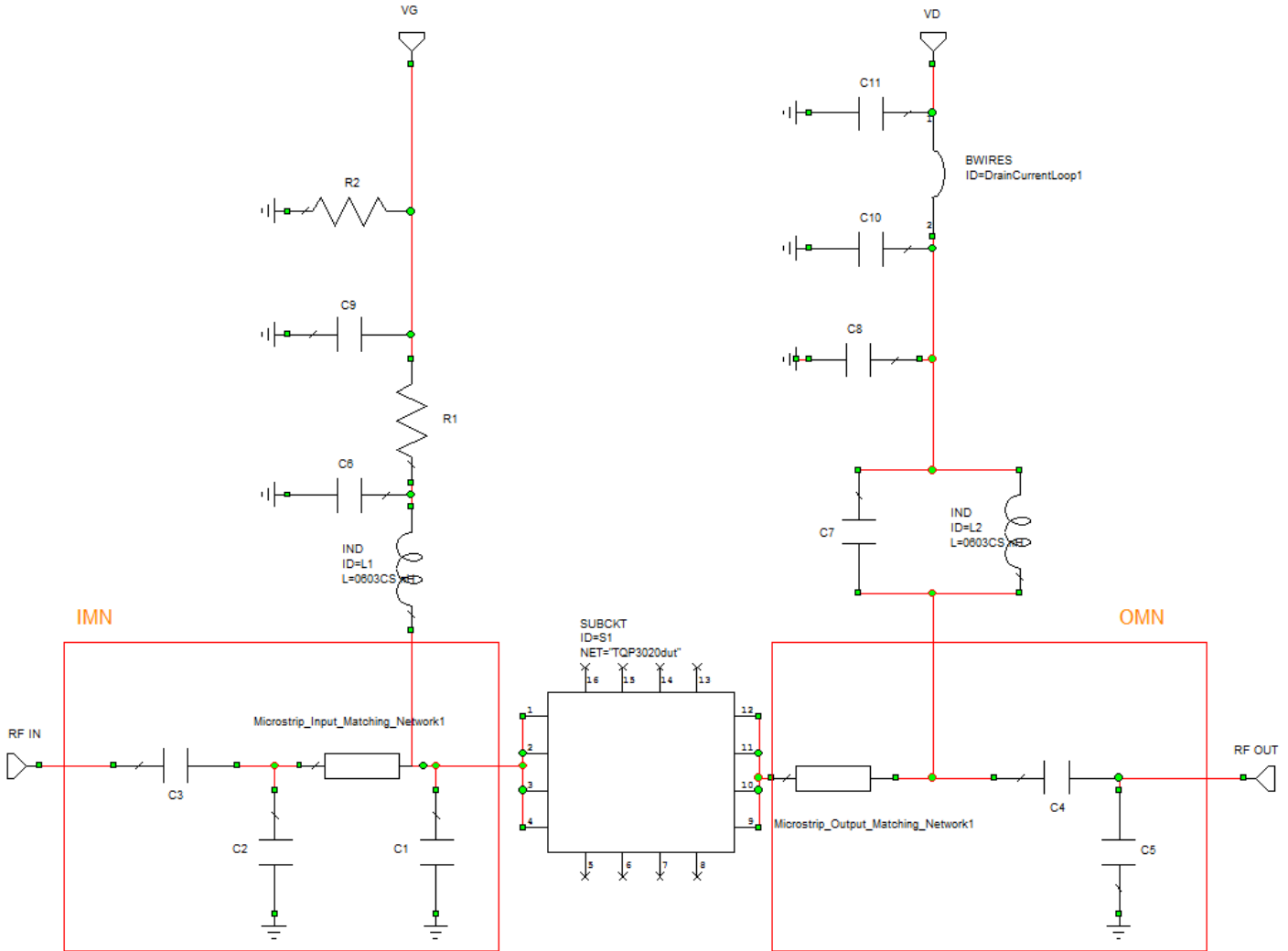
This package is lead-free/RoHS-compliant. The plating material on the leads is NiAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and tin-lead (maximum 245°C reflow temperature) soldering processes.



A	SLP	
	MAX.	0.900
NOM.	0.850	
MIN.	0.800	



5.3 – 5.9 GHz Application Circuit - Schematic



Bias-up Procedure

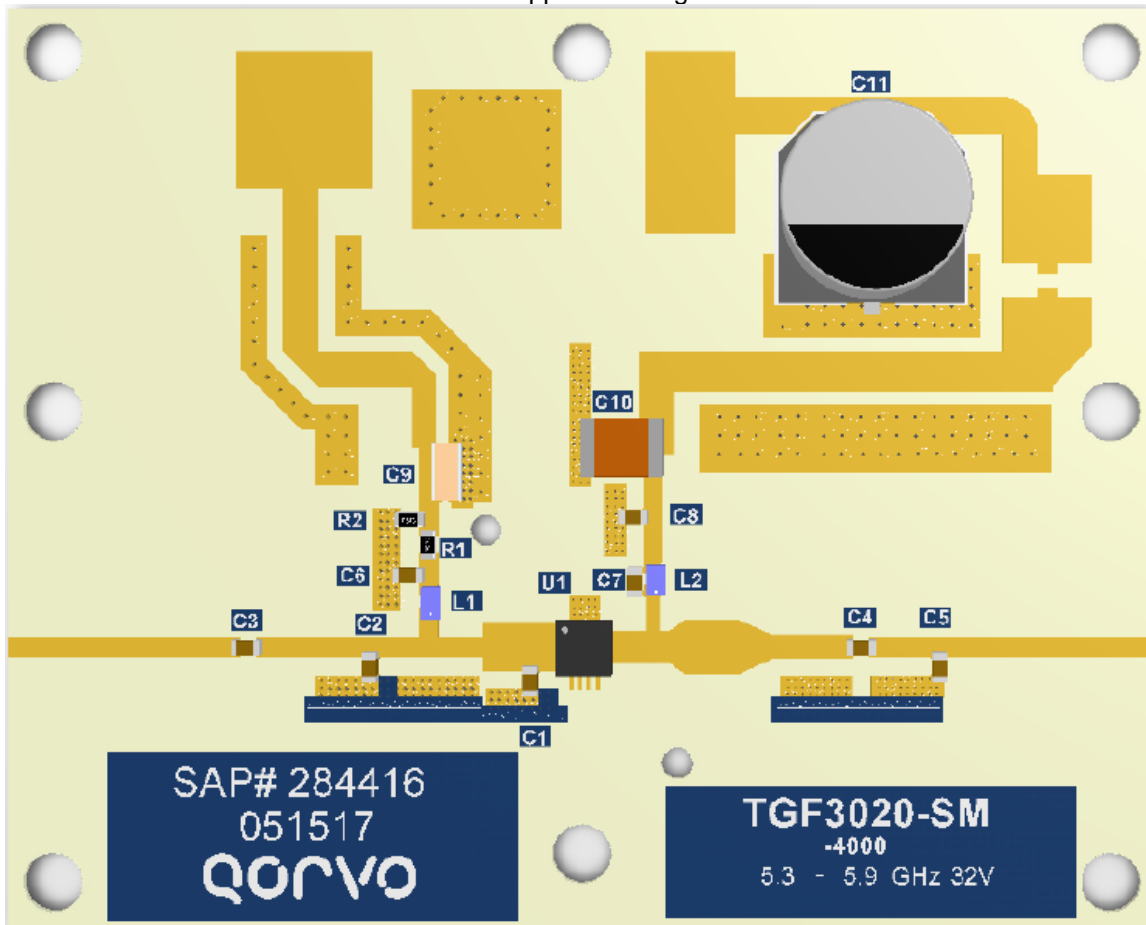
1. Set V_G to -3.5 V.
2. Set I_D current limit to 30 mA.
3. Apply 32 V V_D .
4. Slowly adjust V_G until I_D is set to 25 mA.
5. Set I_D current limit to 0.3 A (Pulsed operation.)
6. Apply RF.

Bias-down Procedure

1. Turn off RF signal.
2. Turn off V_D
3. Wait 2 seconds to allow drain capacitor to discharge.
4. Turn off V_G

3.1 – 3.5 GHz Application Circuit - Layout

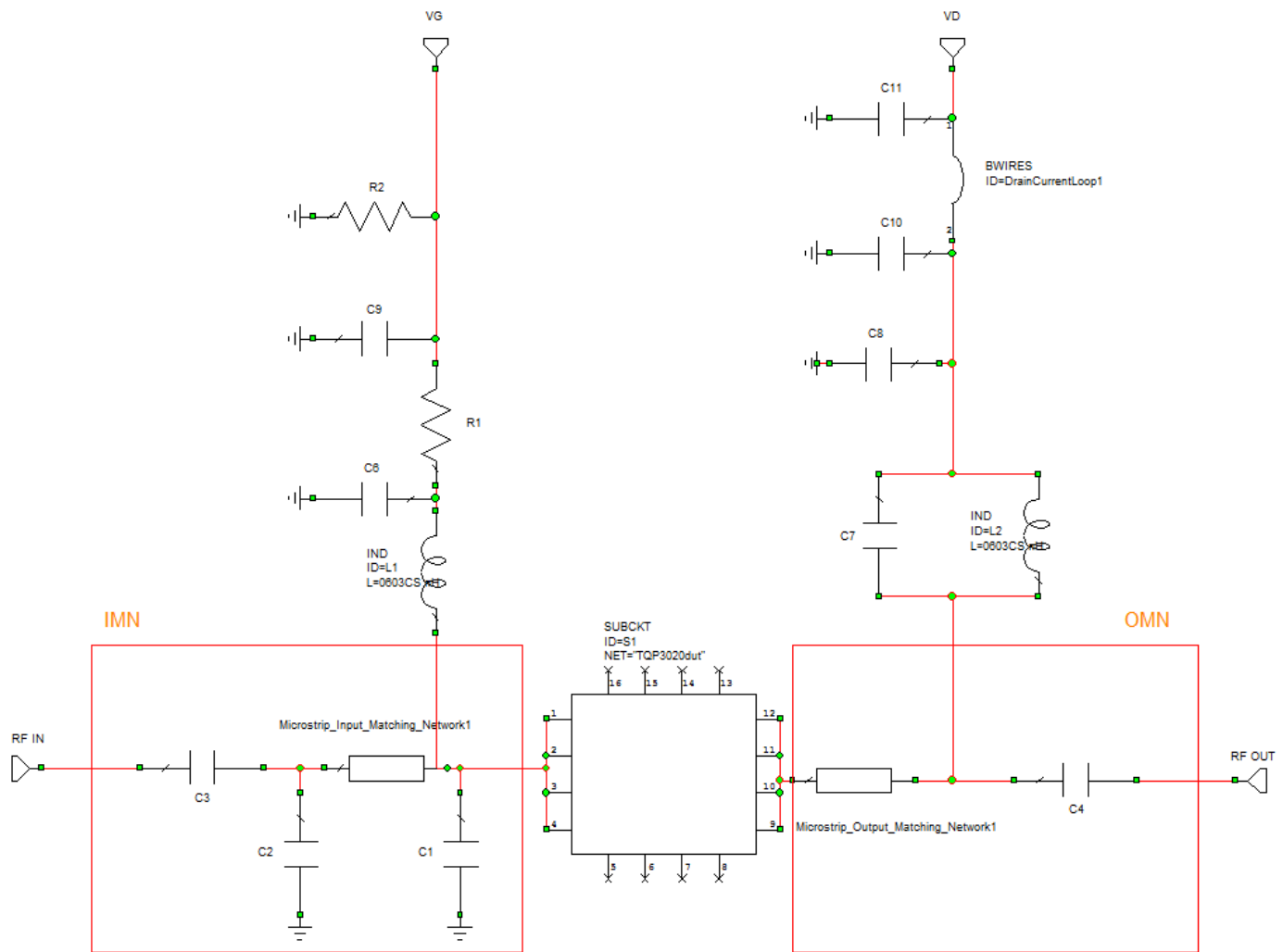
Board material is RO4350B 0.020" thickness with 1oz copper cladding. Overall EVB size is 2" x 2.5".



3.1 – 3.5 GHz Application Circuit - Bill of Materials

Reference Design	Value	Qty	Manufacturer	Part Number
R1	10 Ω	1		Generic 0603
R2	1 kΩ	1		Generic 0603
C1, C5	0.2 pF	2	PPI	0603N0R2AW251X
C2	0.3 pF	1	PPI	0603N0R3AW251X
C3, C4	5.1 pF	2	PPI	0603N5R1AW251X
C6, C7, C8	3.3 pF	3	PPI	0603N3R3AW251X
C11	220 uF	1	United Chemicon	EMVY500ADA221MJA0G
C9	10 uF	1	TDK	C1632X5R0J106M130AC
C10	1 uF	1	AVX	18121C105KAT2A
L1	3.9nH	1	CoilCraft	0603CS-3N9X_E
L2	2.2nH	1	CoilCraft	0603CS-2N2X_E

4 – 6 GHz Application Circuit - Schematic



Bias-up Procedure

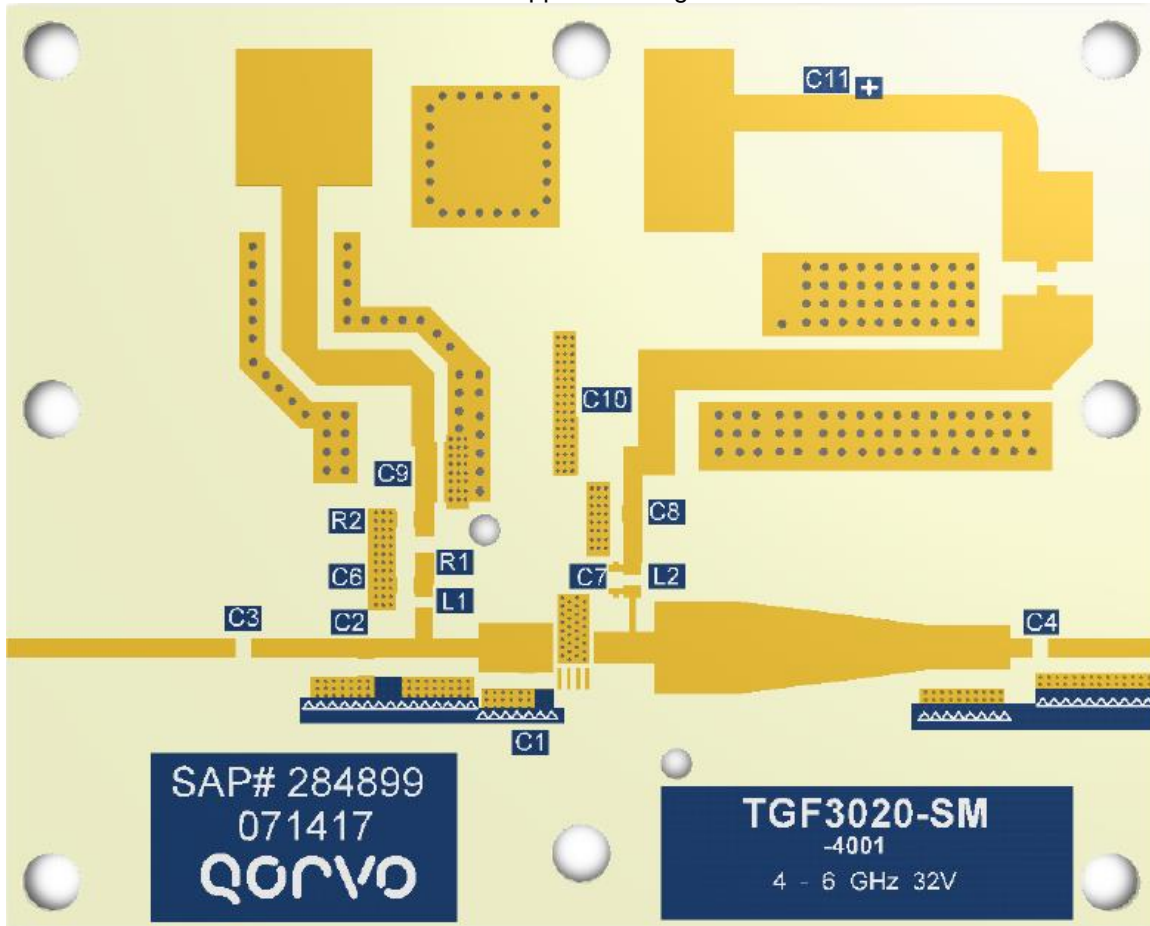
2. Set V_G to -4 V.
4. Set I_D current limit to 30 mA.
5. Apply 32 V V_D .
6. Slowly adjust V_G until I_D is set to 25 mA.
8. Set I_D current limit to 0.3 A (Pulsed operation.)
9. Apply RF.

Bias-down Procedure

3. Turn off RF signal.
4. Turn off V_D
5. Wait 2 seconds to allow drain capacitor to discharge.
7. Turn off V_G

4 – 6 GHz Application Circuit - Layout

Board material is RO4350B 0.020" thickness with 1oz copper cladding. Overall EVB size is 2" x 2.5".



4 – 6 GHz Application Circuit - Bill of Materials

Reference Design	Value	Qty	Manufacturer	Part Number
R1	10 Ω	1		Generic 0603
R2	1 k Ω	1		Generic 0603
C1	0.2 pF	1	PPI	0603N0R2AW251X
C2	0.3 pF	1	PPI	0603N0R3AW251X
C3	5.1 pF	1	PPI	0603N5R1AW251X
C4	10 pF	1	PPI	0603N100AW251X
C6, C7, C8	3.3 pF	3	PPI	0603N3R3AW251X
C11	220 μ F	1	United Chemicon	EMVY500ADA221MJA0G
C9	10 μ F	1	TDK	C1632X5R0J106M130AC
C10	1 μ F	1	AVX	18121C105KAT2A
L1	3.9nH	1	CoilCraft	0603CS-3N9X_E
L2	1.8nH	1	CoilCraft	0603CS-1N8X_E

Recommended Solder Temperature Profile

