TGF3021-SM

30 W, 32 V, 0.03 to 4 GHz, GaN RF Transistor

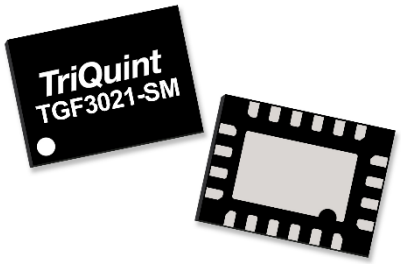
Product Overview

The TGF3021-SM is a 30 W (P_{1dB}) discrete GaN on SiC HEMT which operates from 0.03 to 4.0 GHz. The device is constructed with proven TQGaN25 processes, which features advanced field plate techniques to optimize power and efficiency at high drain bias operating conditions. This optimization can potentially lower system costs in terms of fewer amplifier line-ups and lower thermal management costs.

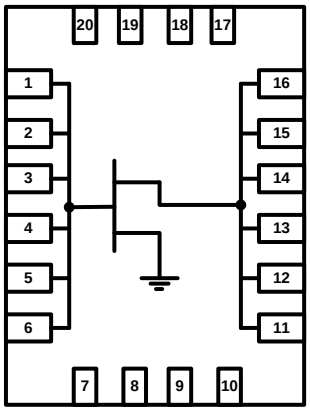
The device is housed in an industry-standard 3 x 4 mm surface mount QFN package.

Lead-free and ROHS compliant

Evaluation boards are available upon request.



Functional Block Diagram



Key Features

- Frequency: 0.03 to 4.0 GHz
- Output Power (P_{1dB}): 36.0 W at 2 GHz
- Linear Gain: 19.3 dB at 2 GHz
- Typical PAE_{1dB}: 72.7% at 2 GHz
- Operating Voltage: 32 V
- Low thermal resistance package
- CW and Pulse capable
- 3 x 4 mm package

Pad Configuration

Pad No.	Symbol
11 - 16	V_D / RF OUT
1 - 6	V_G / RF IN
7 – 10, 20 - 17	NC
Back side	Source

Applications

- Military radar
- Civilian radar
- Land mobile and military radio communications
- Test instrumentation
- Wideband and narrowband amplifiers
- Jammers

Ordering Information

Part Number	Description
TGF3021-SM	QFN Packaged Part
TGF3021-SM-EVB1	0.05 – 0.55 GHz EVB

Absolute Maximum Ratings

Parameter	Rating
Drain to Gate Voltage (V_{DG})	100 V
Gate Voltage Range (V_G)	−7 to 2 V
Drain Current (I_D)	5.8 A
Gate Current (I_G)	−7.5 to 16.8 mA
CW RF Input Power (P_{IN})	See page 8.
Storage Temperature	−40 to 150°C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Value	Units
Drain Voltage Range (V_D)	32 (Typ.)	V
Drain Quiescent Current (I_{DQ})	65	mA
Peak Drain Current (I_D)	1800 (Typ.)	mA
Gate Voltage (V_G)	−2.7 (Typ.)	V

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Thermal and Reliability Information - CW (1)

Test conditions unless otherwise noted: T_A = 25 °C, V_D = 32 V, I_{DQ} = 65 mA

Symbol	Parameter	Freq	Min	Typical	Max	Units
G_{LIN}	Linear Gain, Power Tuned	2.0 GHz		19.1		dB
		2.5 GHz		17.4		
		3.0 GHz		16.3		
		3.5 GHz		15.3		
P_{1dB}	Output Power at 1 dB Gain Compression, Power Tuned	2.0 GHz		43.8		dBm
		2.5 GHz		43.7		
		3.0 GHz		43.6		
		3.5 GHz		43.4		
PAE_{1dB}	Power-Added Efficiency at 1 dB Gain Compression, Efficiency Tuned	2.0 GHz		70.6		%
		2.5 GHz		63		
		3.0 GHz		62.3		
		3.5 GHz		62.5		
G_{1dB}	Gain at 1 dB Compression, Power Tuned	2.0 GHz		18.1		dB
		2.5 GHz		16.4		
		3.0 GHz		15.3		
		3.5 GHz		14.3		

RF Characterization – 0.05 – 0.55 GHz EVB Performance at 0.25 GHz

Test conditions unless otherwise noted: T_A = 25 °C, V_D = 32 V, I_{DQ} = 65 mA, Signal: CW

Symbol	Parameter	Min	Typical	Max	Units
G_{LIN}	Linear Gain		21.8		dB
P_{1dB}	Output Power at 1 dB Gain Compression		25.7		W
PAE_{1dB}	Power-Added Efficiency at 1 dB Gain Compression		52.4		%
G_{1dB}	Gain at 1 dB Compression		20.8		dB
Gate Leakage	V_D = +10 V, V_G = −3.7 V	-8.3		-0.1	mA

RF Characterization – Mismatch Ruggedness at 512 MHz

Test conditions unless otherwise noted: T_A = 25 °C, V_D = 32 V, I_{DQ} = 65 mA
Driving input power is determined at pulsed compression under matched condition at EVB output connector.

Symbol	Parameter	dB Compression	Typical
VSWR	Impedance Mismatch Ruggedness	1	10:1

Thermal and Reliability Information - CW (1)

Parameter	Test Conditions	Value	Units
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 11.3 W, Tbaseplate = 85°C	3.2	ºC/W
Channel Temperature, T_{CH}		121	°C
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 15.1 W, Tbaseplate = 85°C	3.3	°C/W
Channel Temperature, T_{CH}		126	°C
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 18.9 W, Tbaseplate = 85°C	3.3	ºC/W
Channel Temperature, T_{CH}		148	°C
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 22.7 W, Tbaseplate = 85°C	3.4	ºC/W
Channel Temperature, T_{CH}		162	°C
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 30.2 W, Tbaseplate = 85°C	3.6	ºC/W
Channel Temperature, T_{CH}		194	°C

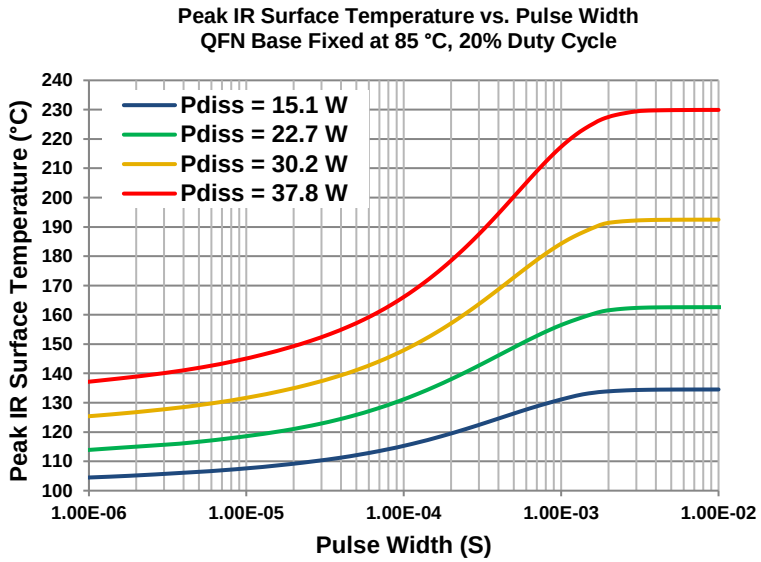
Notes:
1. Thermal resistance measured to bottom of package.
2. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

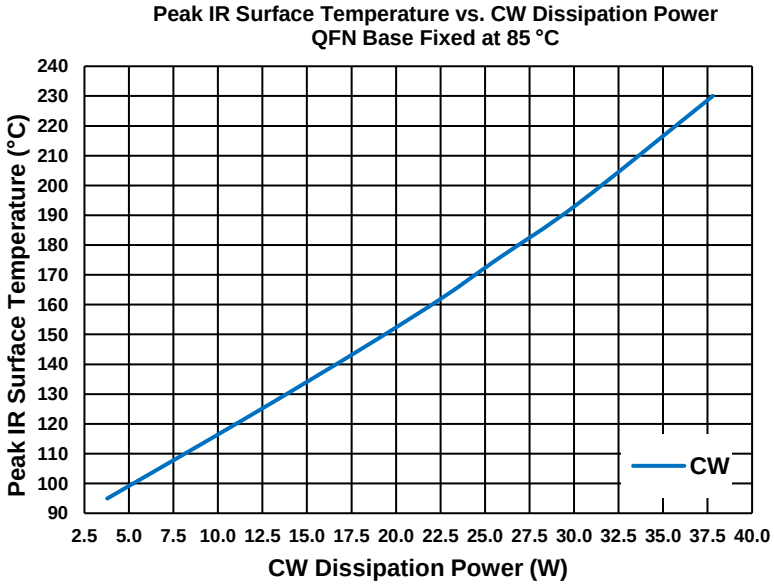
Thermal and Reliability Information - Pulsed (1)

Parameter	Test Conditions	Value	Units
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 15.1 W, Tbaseplate = 85°C Pulse Width = 100 uS Duty Cycle = 5%	2.0	ºC/W
Channel Temperature, T_{CH}		115	°C
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 22.7 W, Tbaseplate = 85°C Pulse Width = 100 uS Duty Cycle = 10%	2.0	°C/W
Channel Temperature, T_{CH}		131	°C
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 30.2 W, Tbaseplate = 85°C Pulse Width = 100 uS Duty Cycle = 20%	2.1	ºC/W
Channel Temperature, T_{CH}		148	°C
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 37.8 W, Tbaseplate = 85°C Pulse Width = 100 uS Duty Cycle = 20%	2.1	ºC/W
Channel Temperature, T_{CH}		166	°C

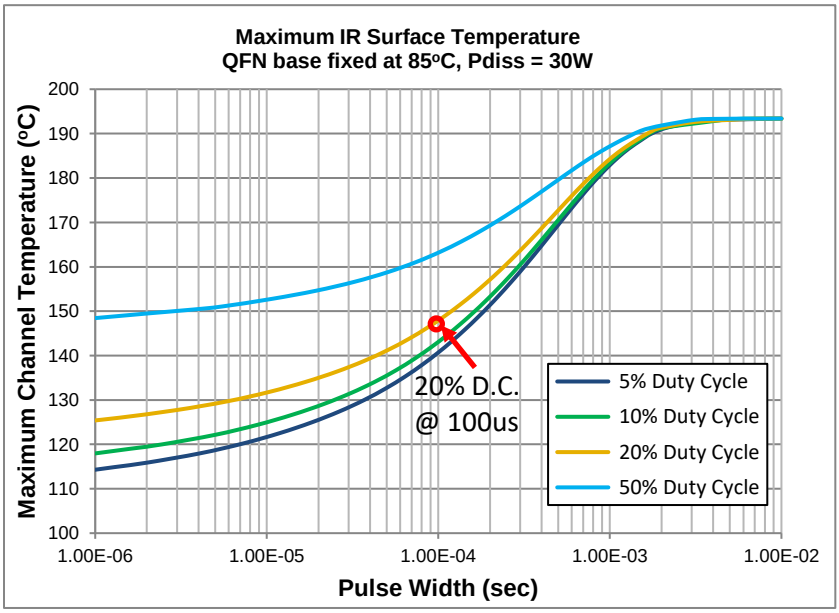
Notes:
1. Thermal resistance measured to bottom of package.
2. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Maximum Channel Temperature

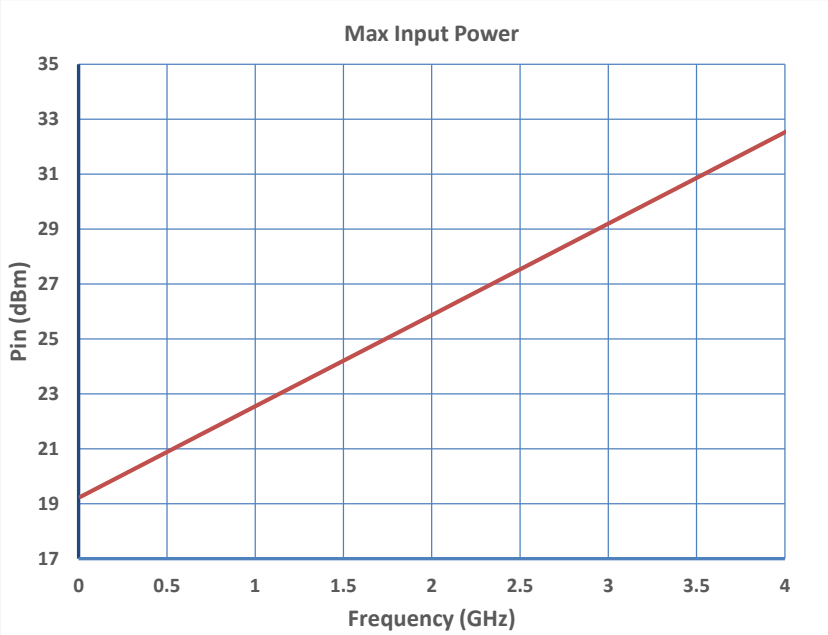




Maximum Channel Temperature



Maximum Input Power (1)

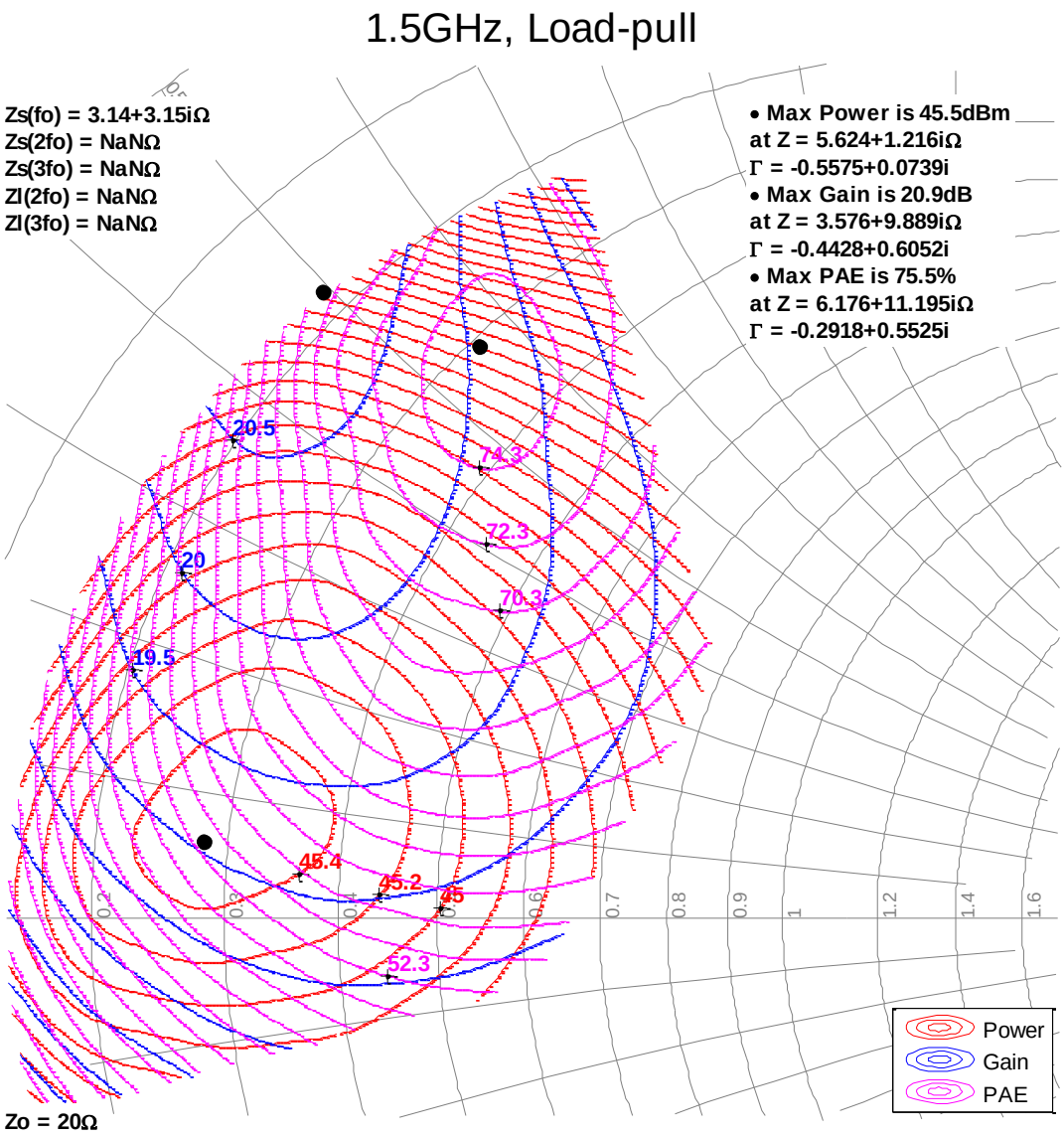


(1) Values are estimated at 25 °C and CW condition.

Model Load Pull Contours – Pulsed (1,2,3)

RF performance that the device typically exhibits when placed in the specified impedance environment. The impedances are not the impedances of the device, they are the impedances presented to the device via an RF circuit or load-pull system. The impedances listed follow an optimized trajectory to maintain high power and high efficiency.

Notes:
1. 32 V, 65 mA, Pulsed signal with 100 uS pulse width and 20% duty cycle. 3 dB compression referenced to peak gain.
2. See page 30 for load pull and source pull reference planes.
3. NaN means the impedances are undefined in load-pull system.



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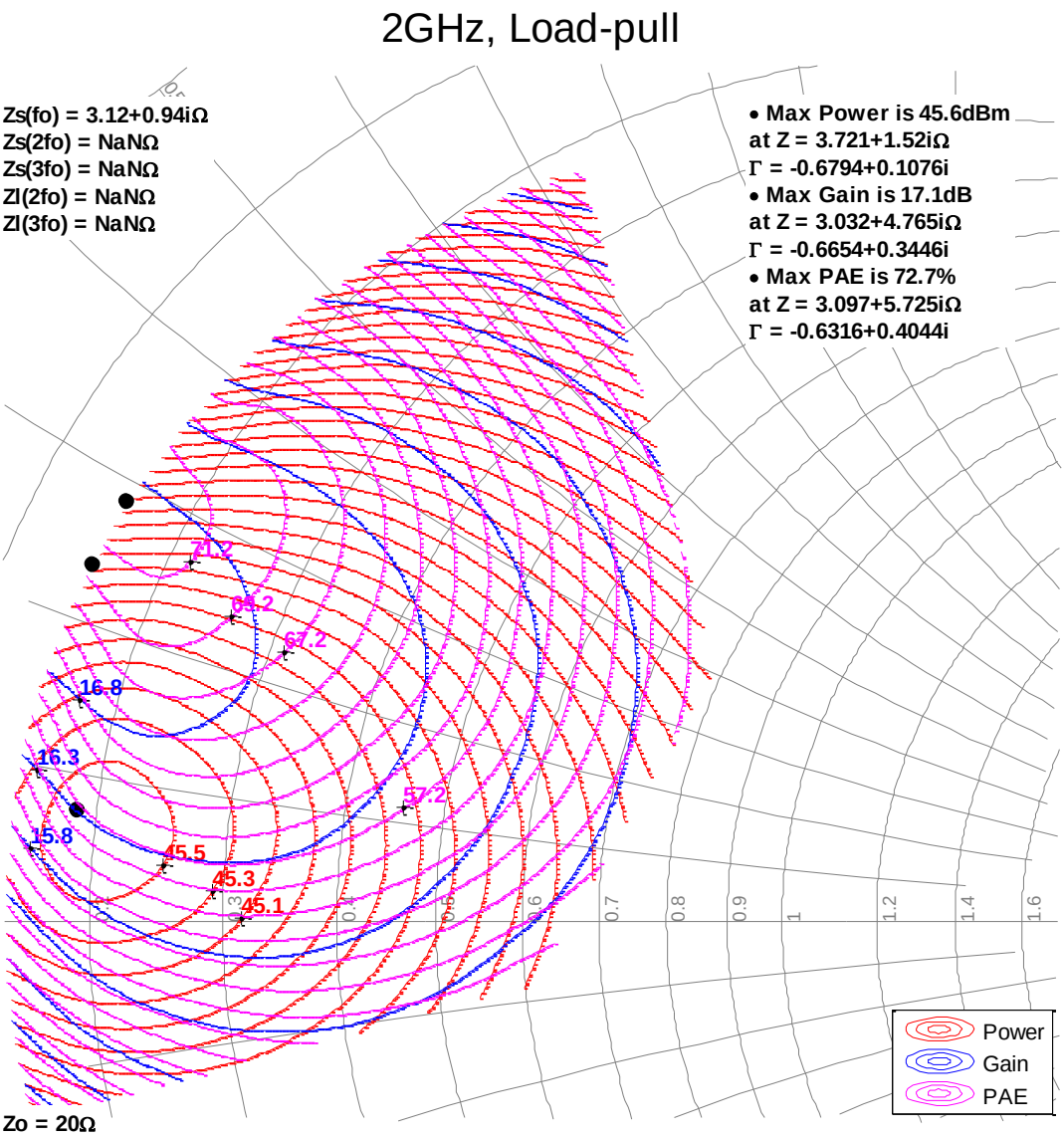

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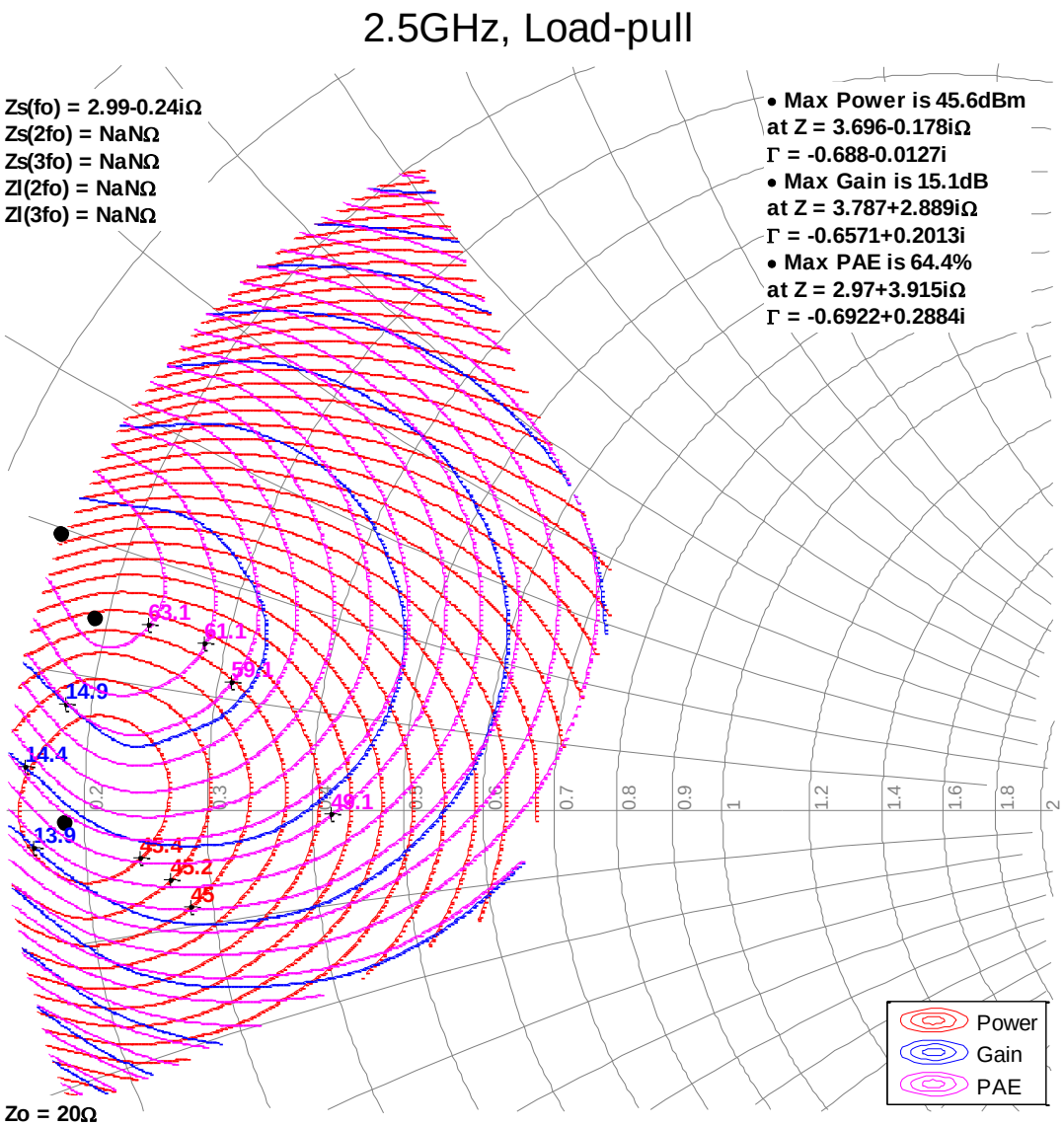

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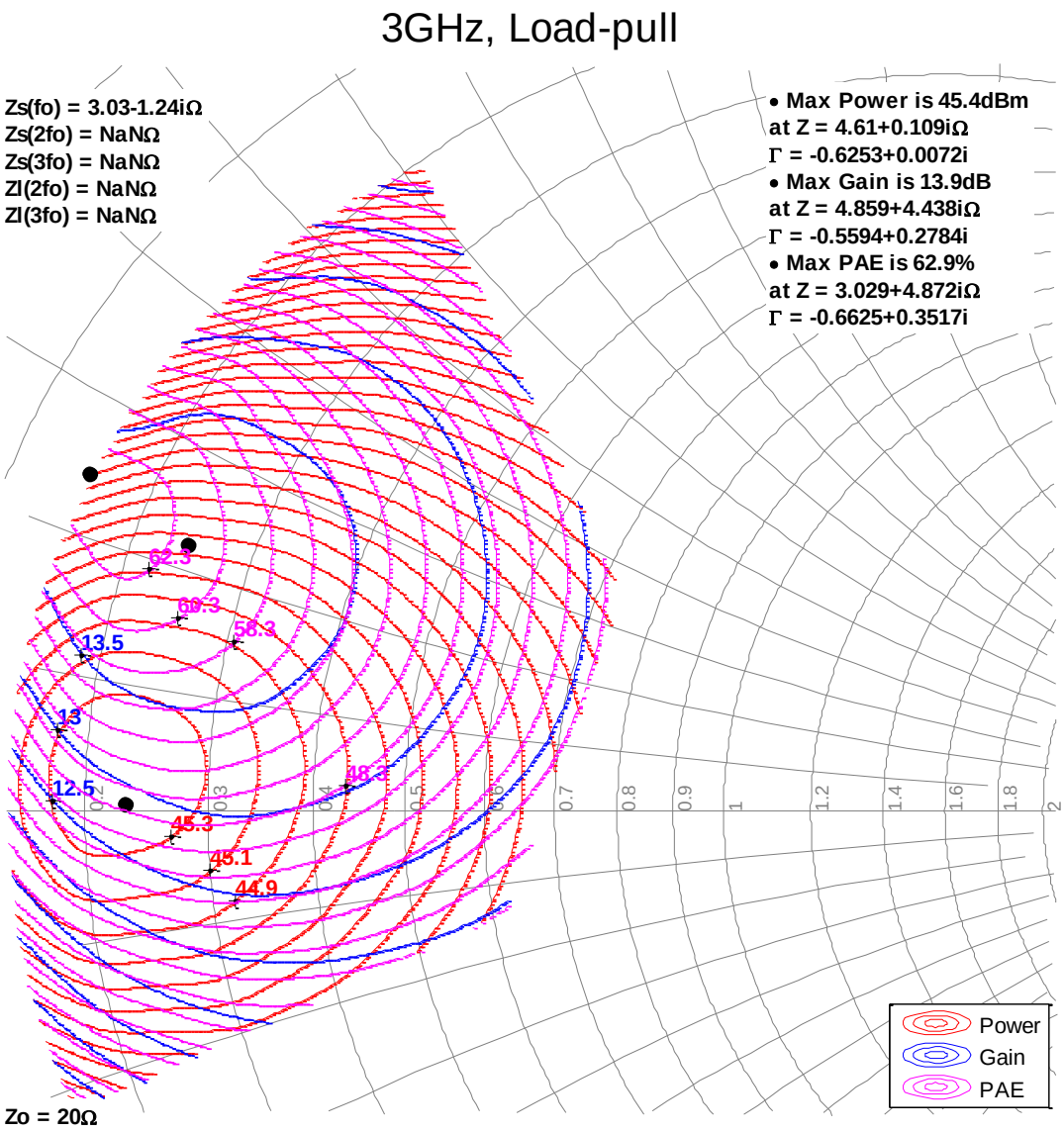

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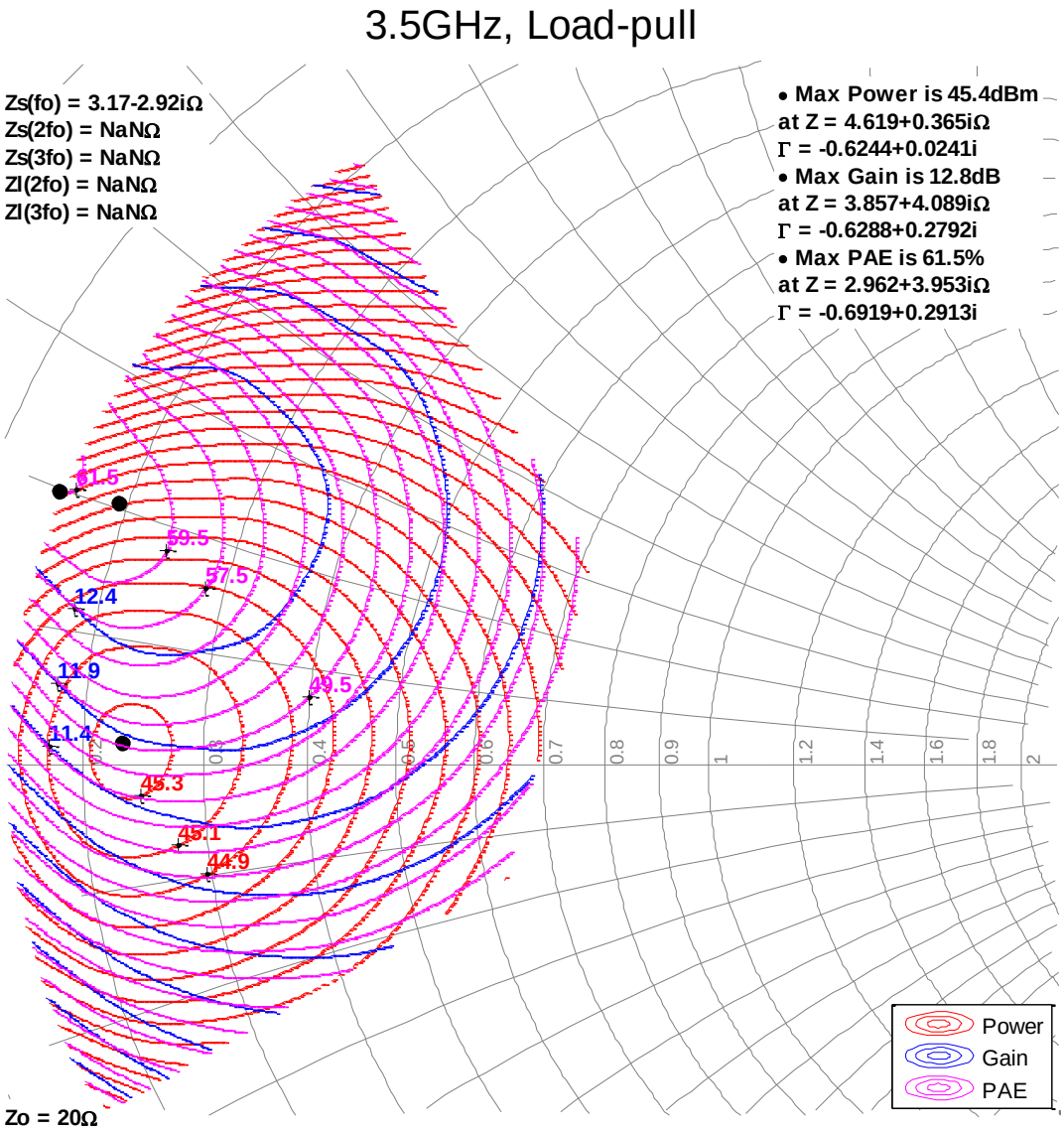

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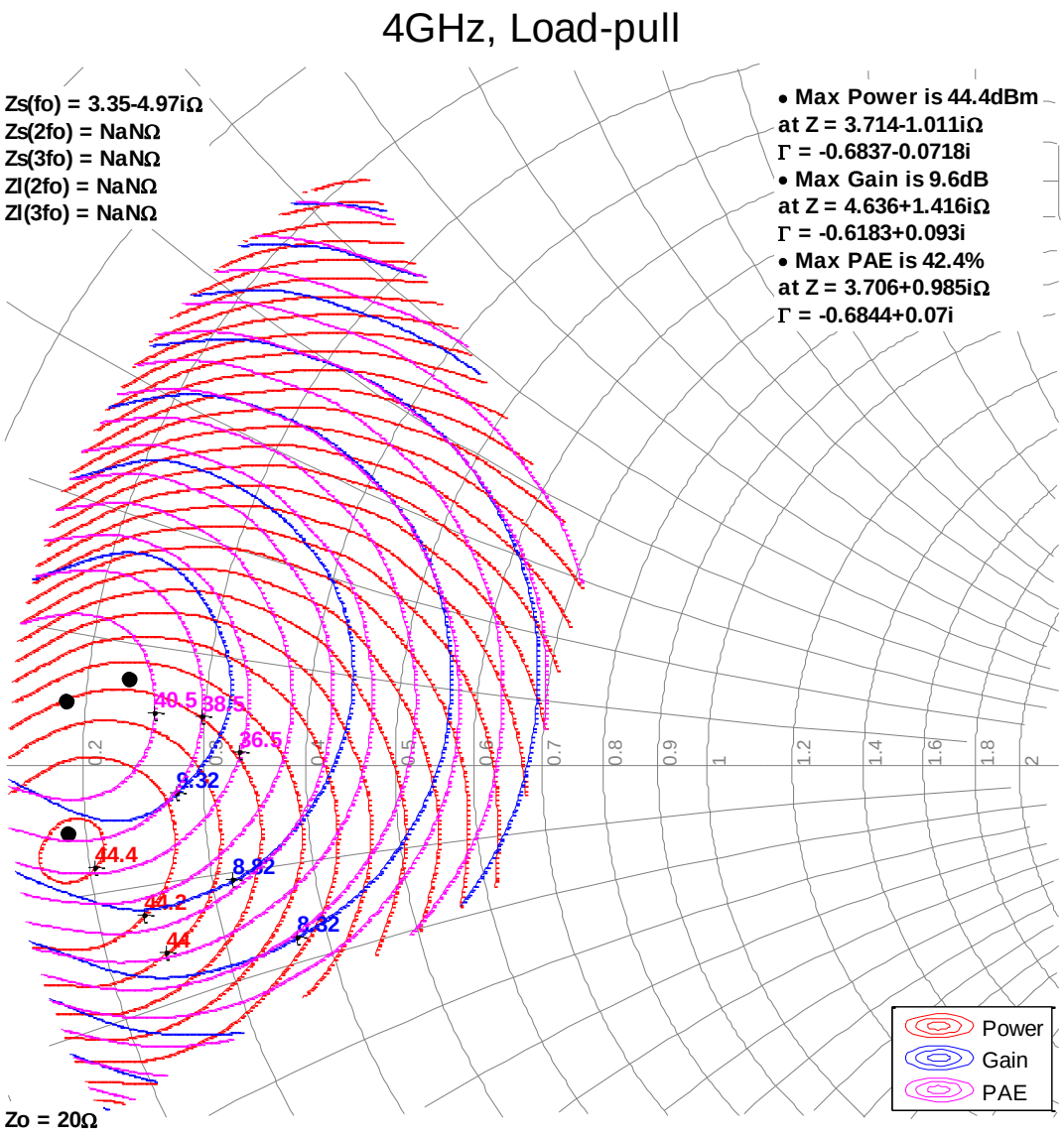

Model Load Pull Contours – CW (4, 5, 6)

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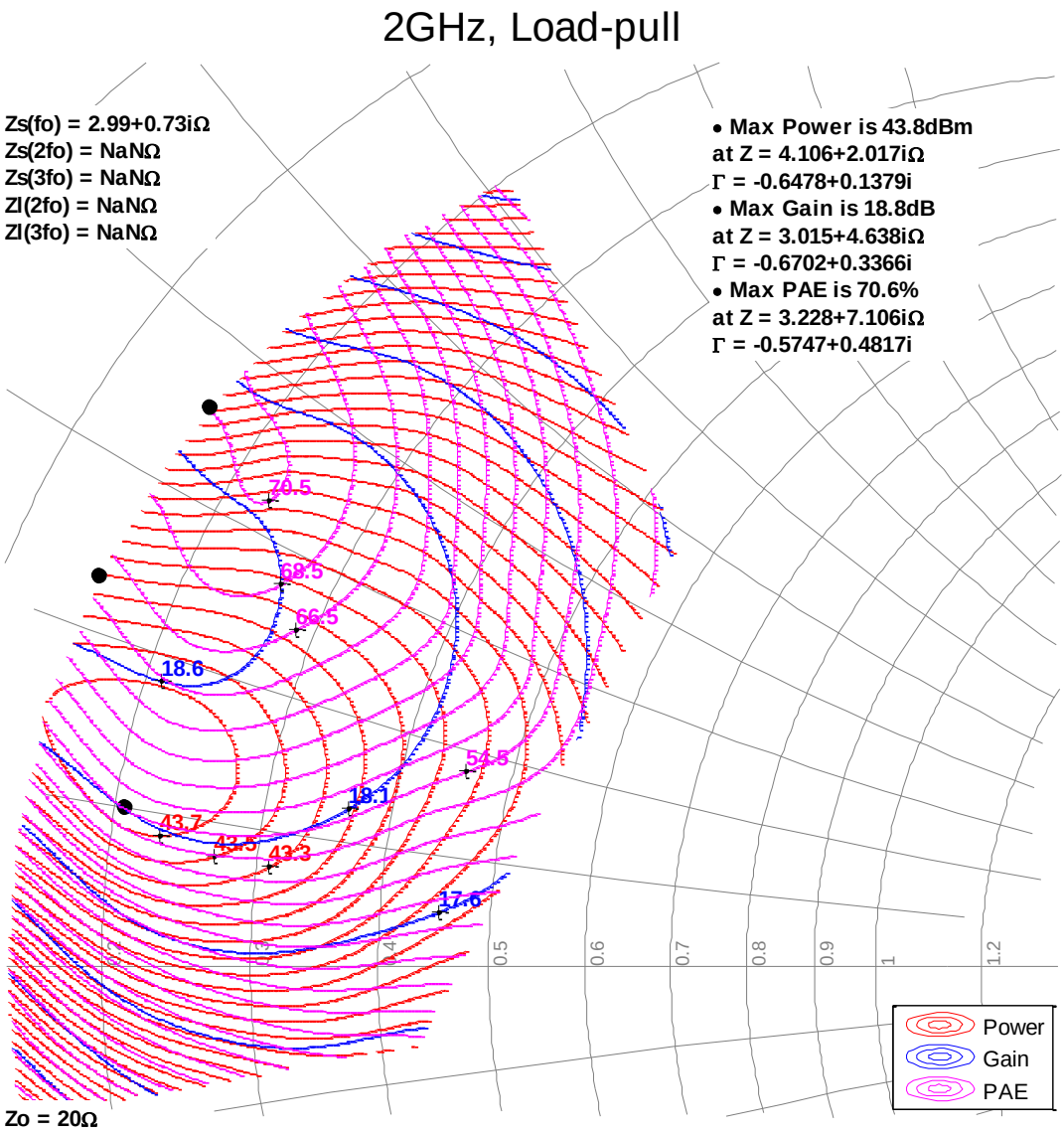
Notes:
4. 32 V, 65 mA, CW, 1 dB compression referenced to peak gain.
5. See page 28 for load pull and source pull reference planes.
6. NaN means the impedances are undefined in load-pull system.



Model Load Pull Contours – CW (4, 5, 6)

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Notes:
4. 32 V, 65 mA, CW, 1 dB compression referenced to peak gain.
5. See page 28 for load pull and source pull reference planes.
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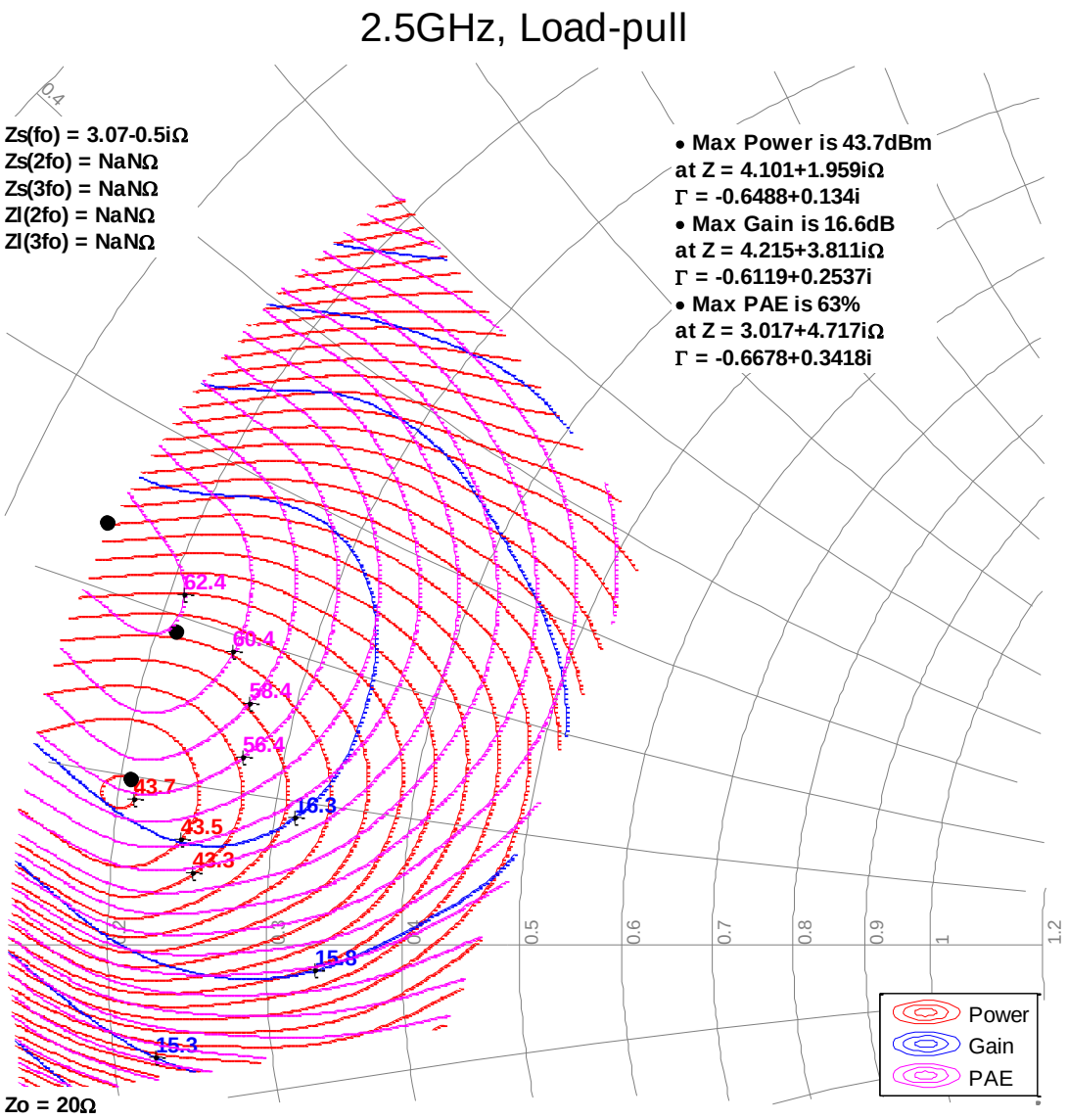

Model Load Pull Contours – CW (4, 5, 6)

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4. 32 V, 65 mA, CW, 1 dB compression referenced to peak gain.
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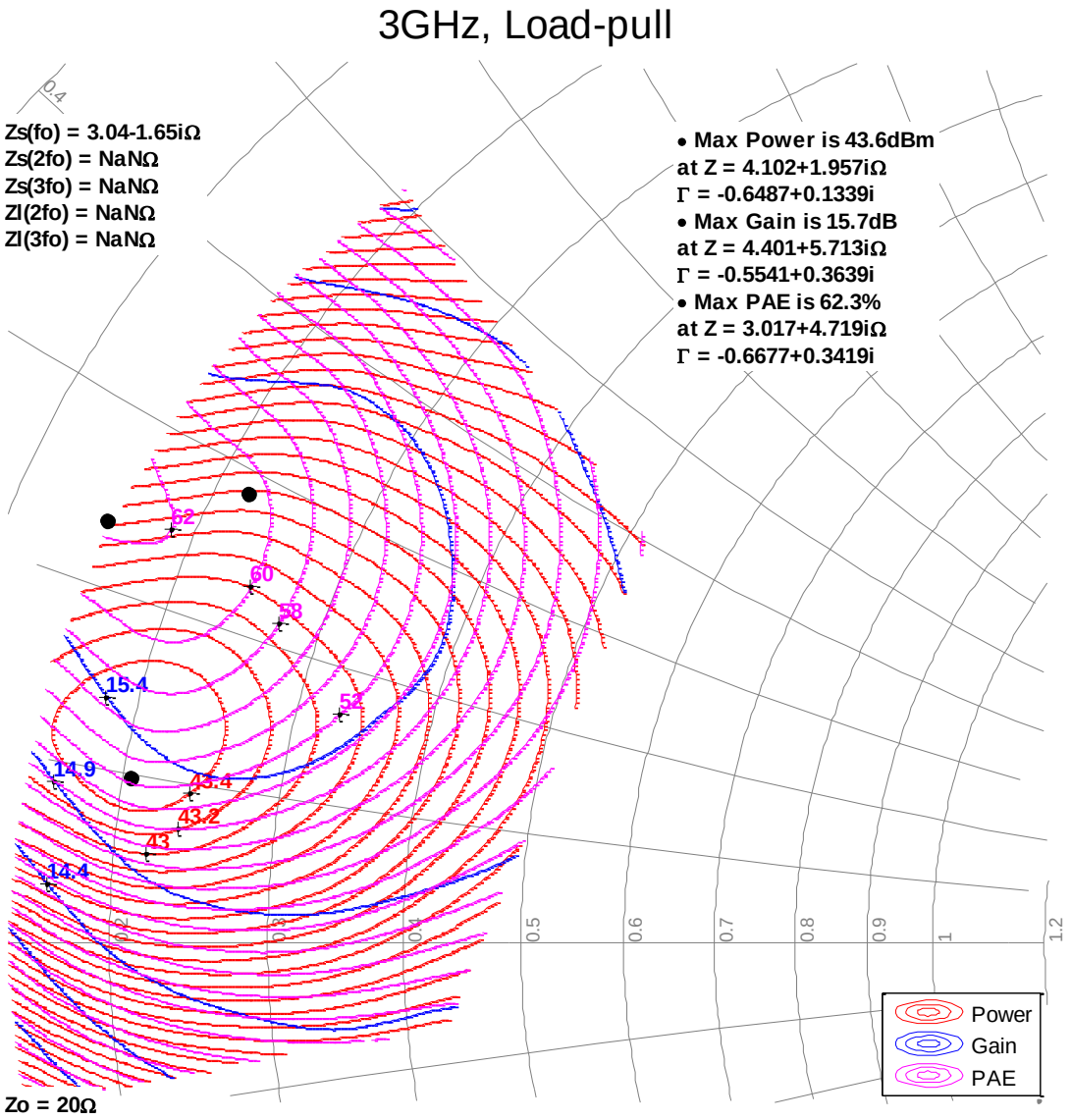
6. NaN means the impedances are undefined in load-pull system.



Model Load Pull Contours – CW (4, 5, 6)

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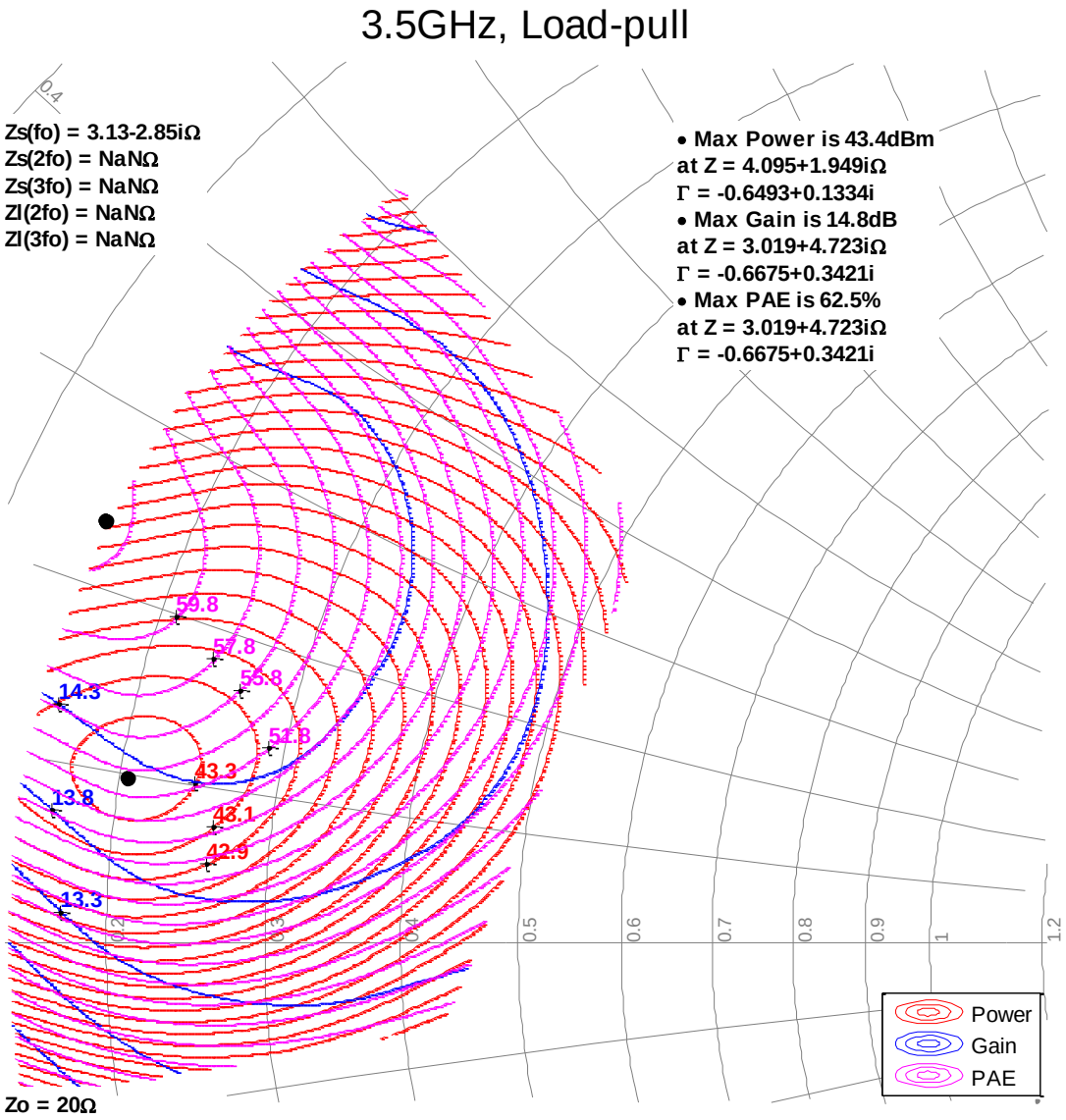
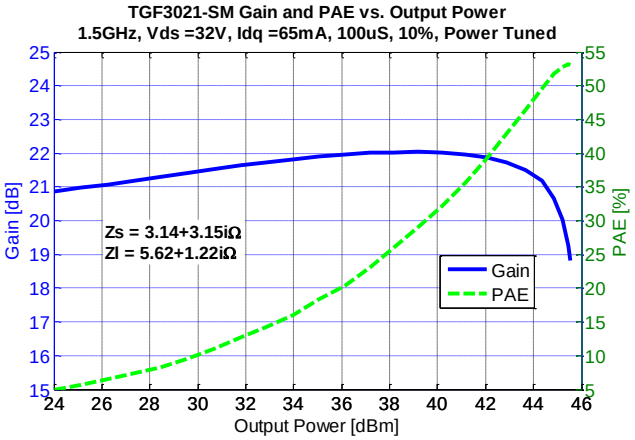
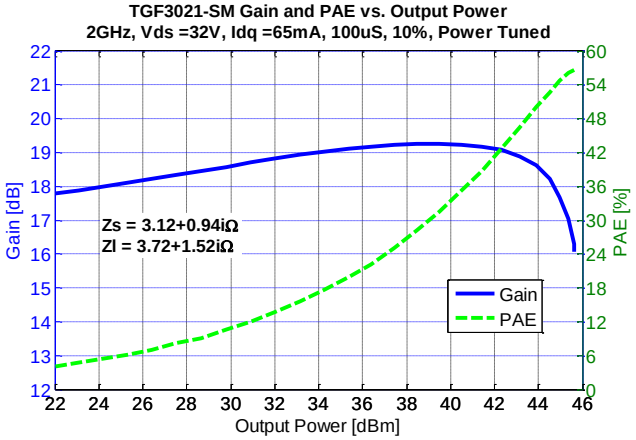
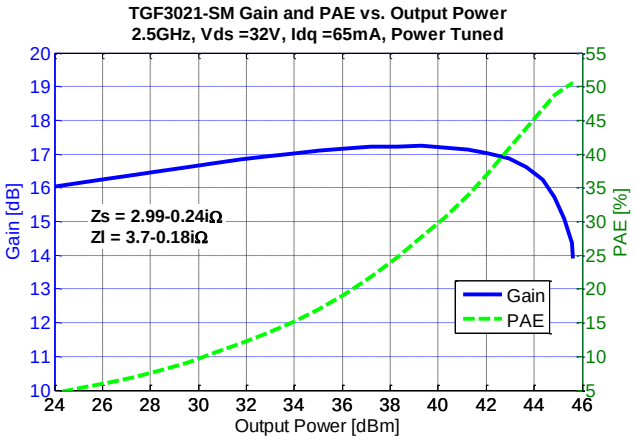


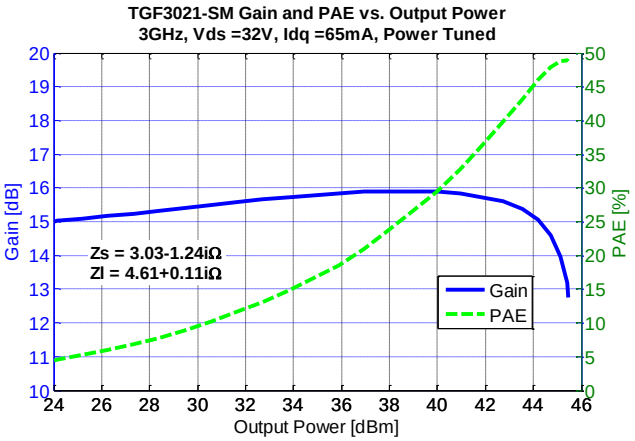
Typical Pulsed Performance – Power Tuned (1,2)

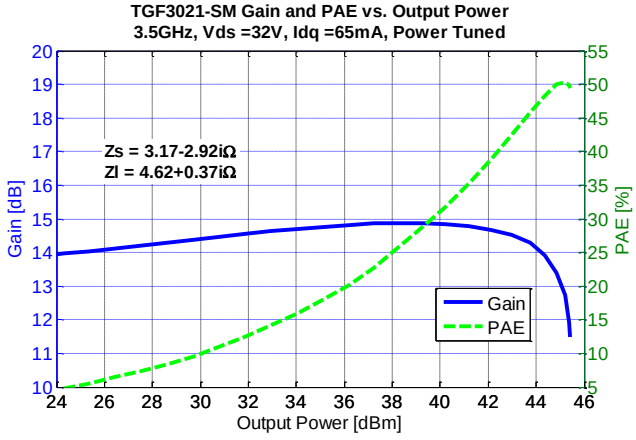
Notes:
1. Pulsed signal with 100 uS pulse width and 20% duty cycle
2. See page 28 for load pull and source pull reference planes where the performance was measured.

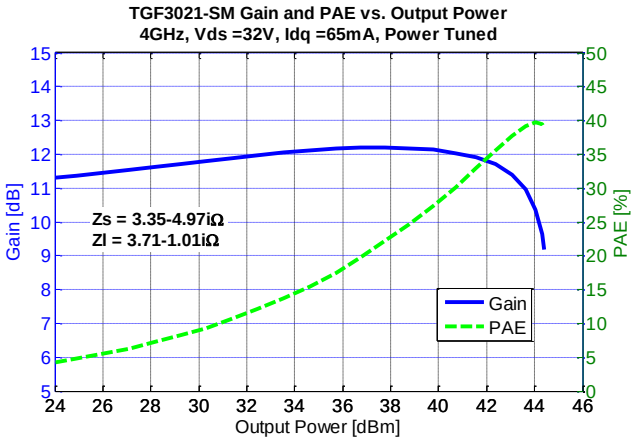






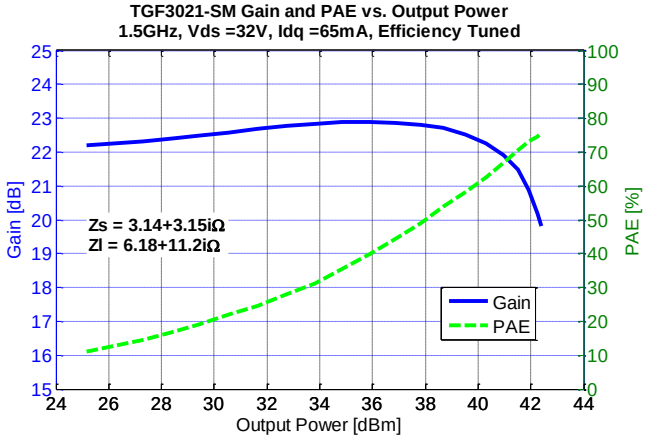


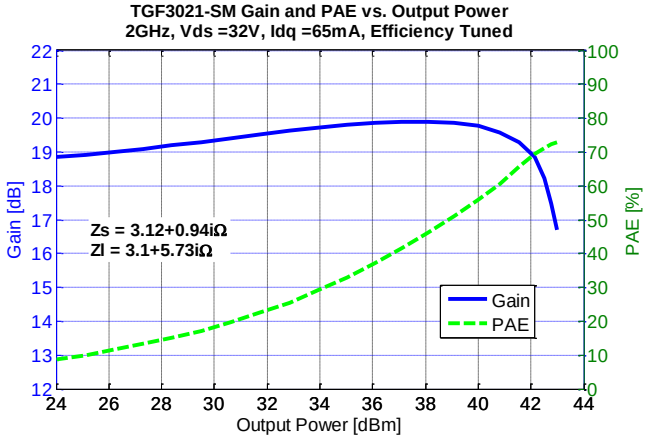


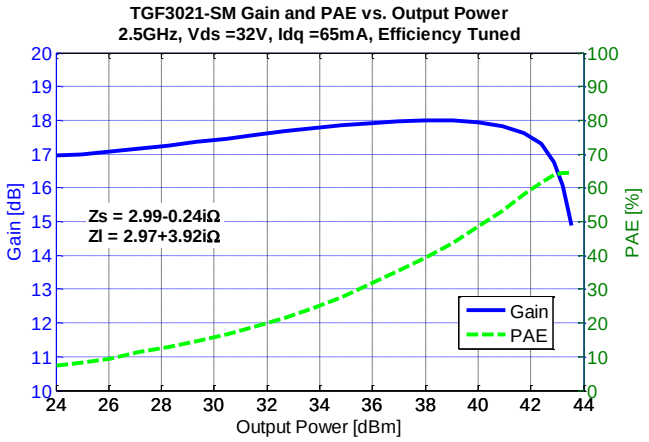


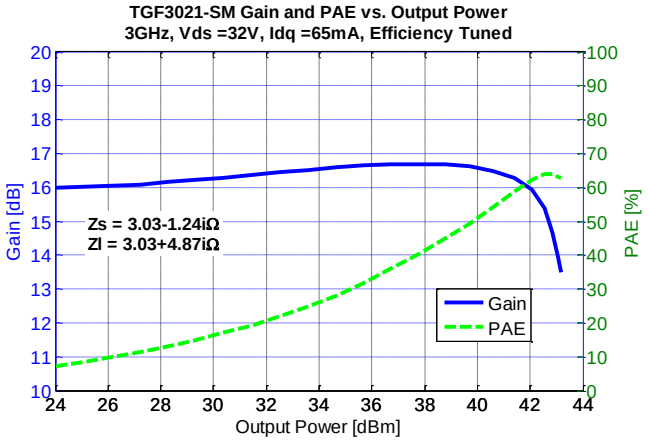
Typical Pulsed Performance – Efficiency Tuned (1,2)

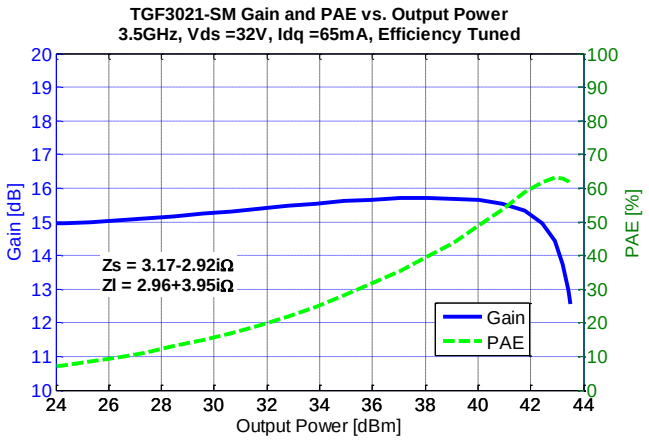
Notes:
1. Pulsed signal with 100 uS pulse width and 20% duty cycle
2. See page 28 for load pull and source pull reference planes where the performance was measured.

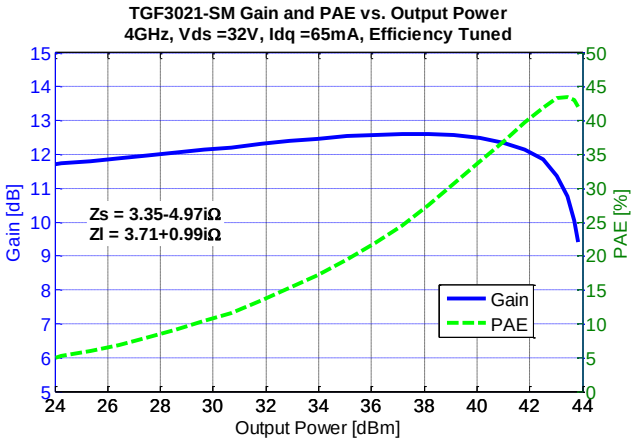






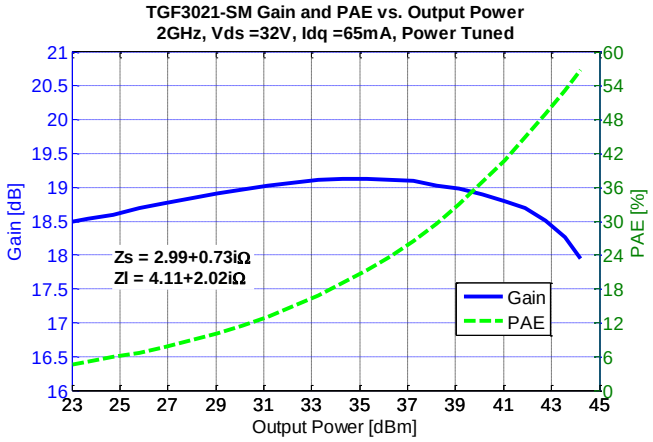


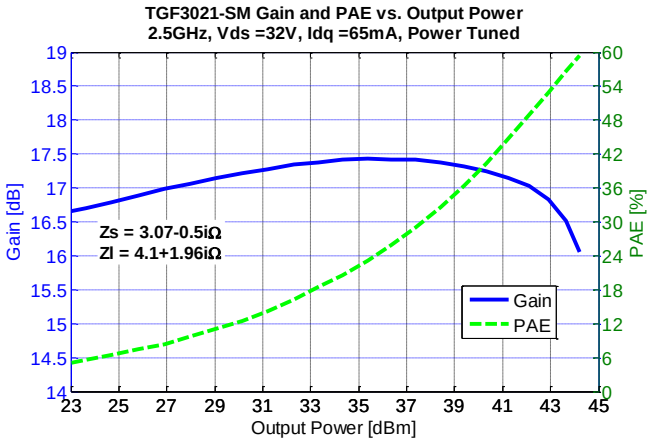


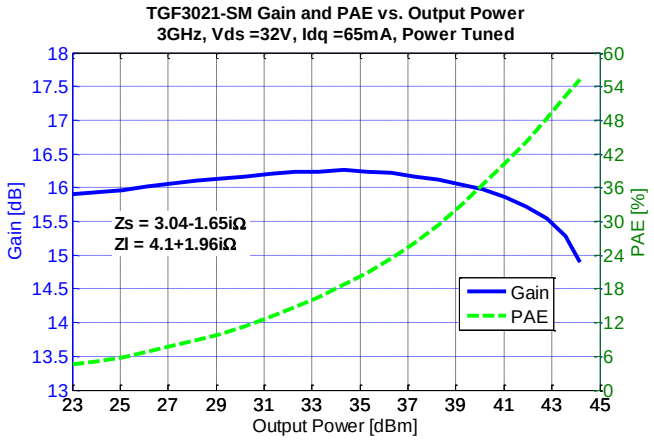


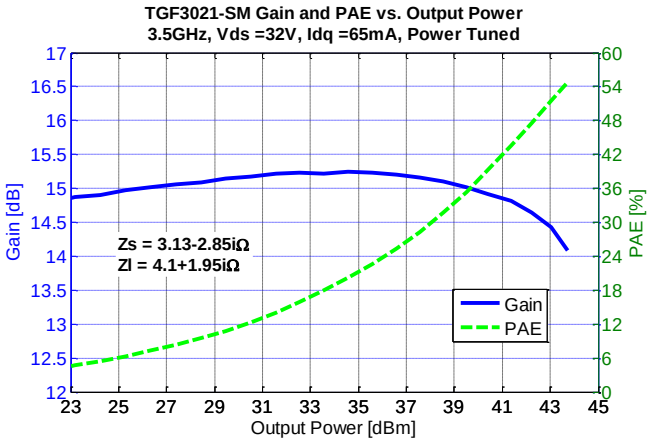
Typical CW Performance – Power Tuned (3, 4)

Notes:
3. CW signal
4. See page 28 for load pull and source pull reference planes where the performance was measured.



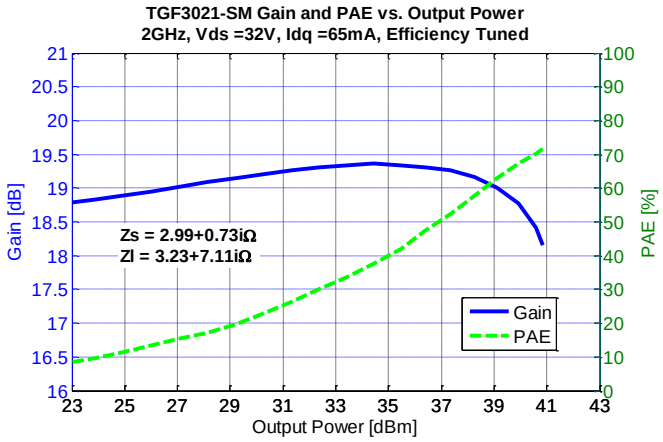


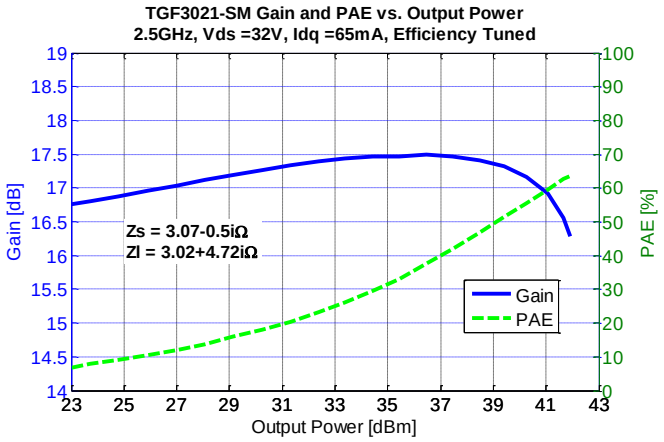


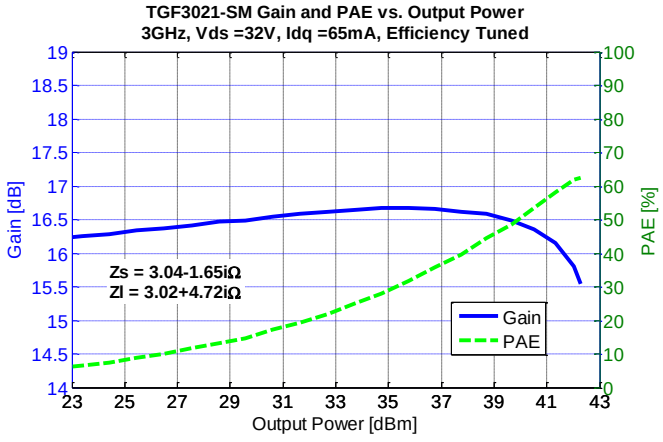


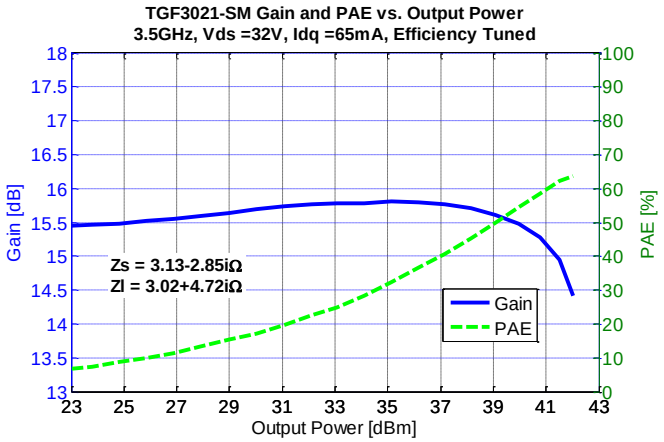
Typical CW Performance – Efficiency Tuned (3, 4)

Notes:
3. CW signal
4. See page 28 for load pull and source pull reference planes where the performance was measured.



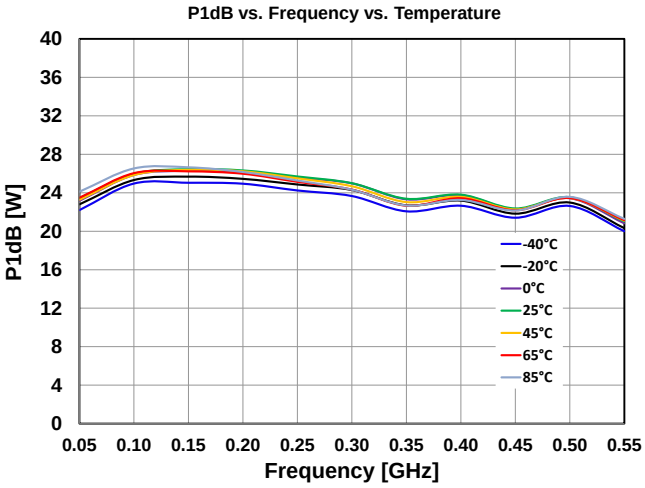


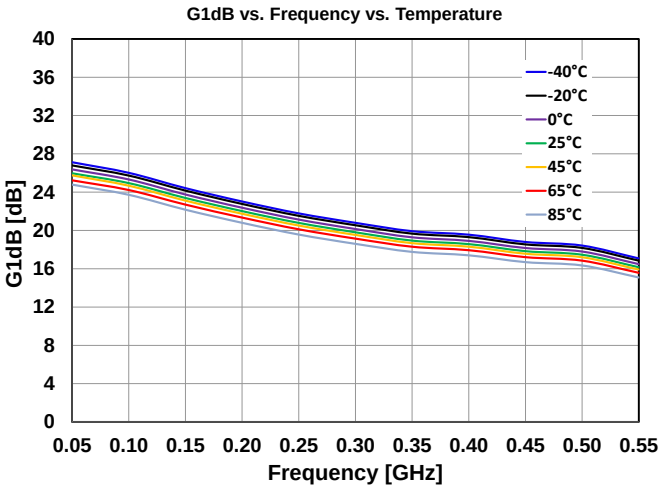


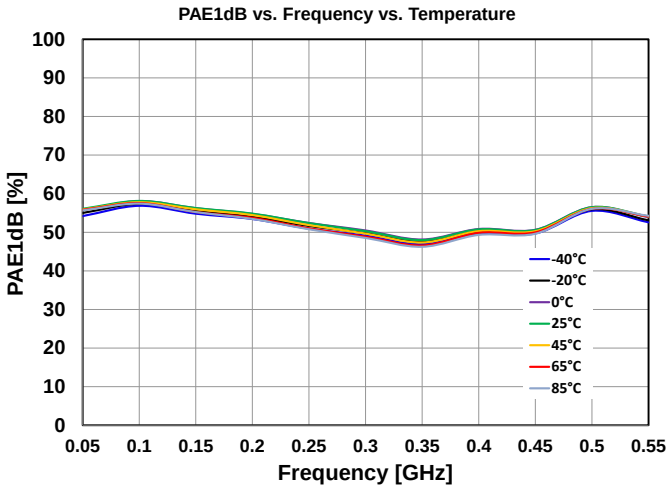


0.05 – 0.55 GHz Evaluation Board Performance Over Temperature (1, 2)

Performance measured on Qorvo's 0.05 GHz to 0.55 GHz Evaluation Board





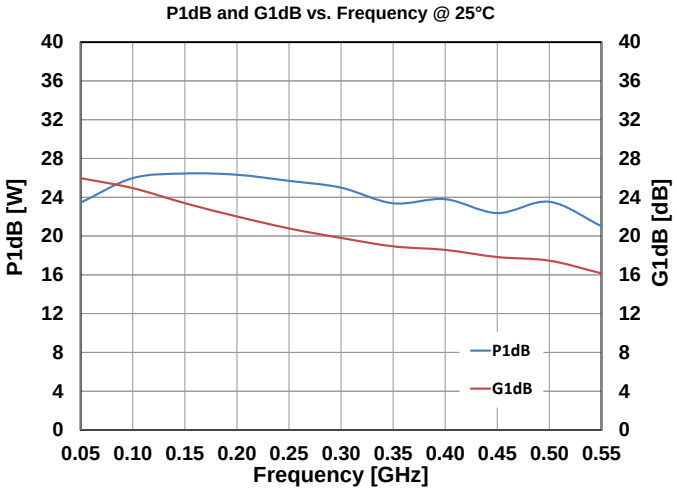


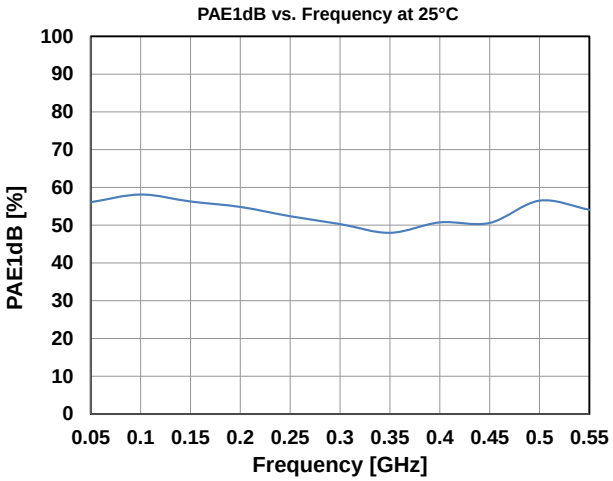
Notes:

1. Test Conditions: V_{DS} = 32 V, I_{DQ} = 65 mA
2. Test Signal: CW

0.05 – 0.55 GHz Evaluation Board Performance At 25°C (1, 2)

Performance measured on Qorvo's 0.05 GHz to 0.55 GHz Evaluation Board



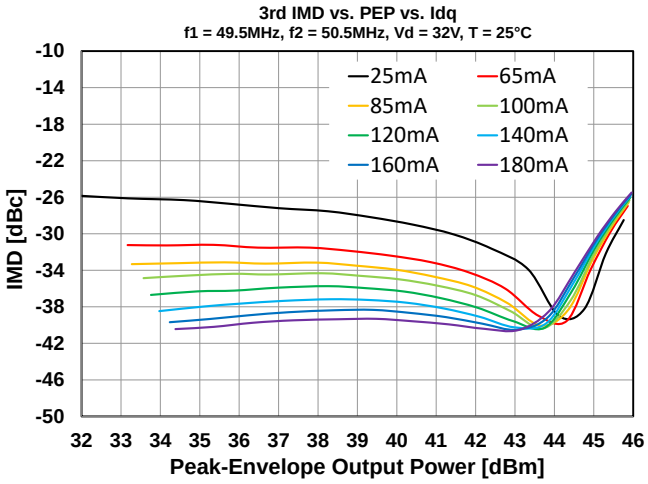


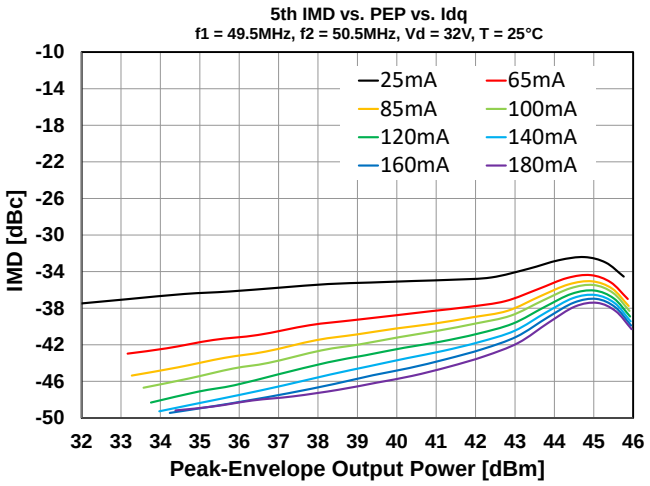
Notes:

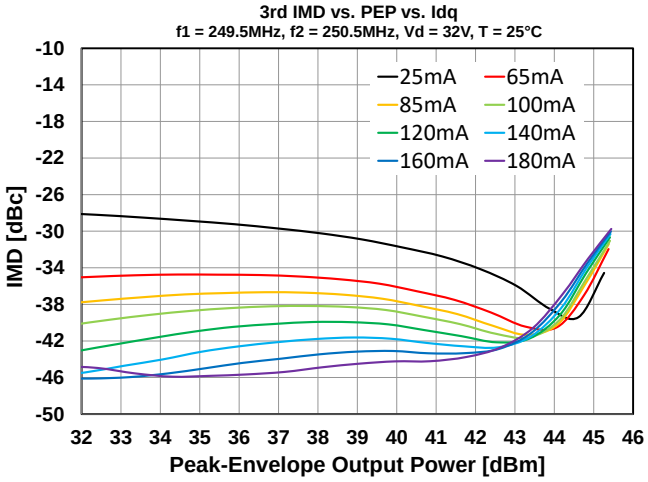
1. Test Conditions: V_{DS} = 32 V, I_{DQ} = 65 mA
2. Test signal: CW

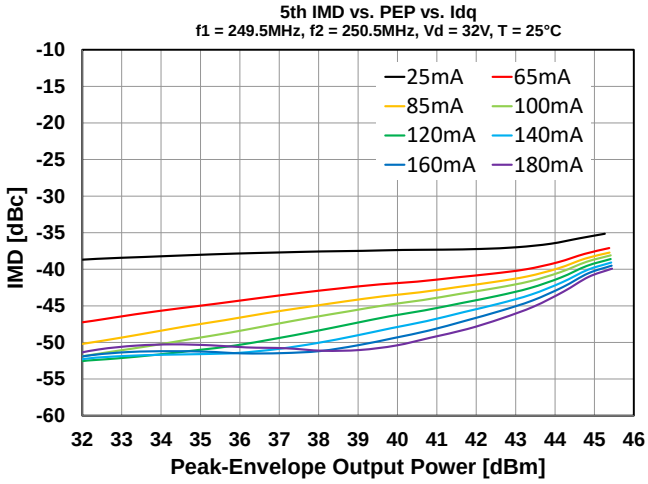
0.05 – 0.55 GHz Evaluation Board Performance - Two-Tone Measurements (1)

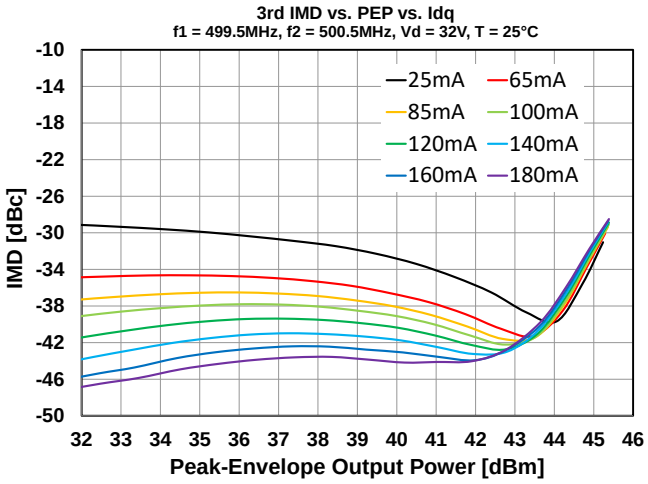
(1) The Intermode Modulation Distortion products (IMD) are referenced to peak-envelope output power, which is 6 dB above single-tone output power.

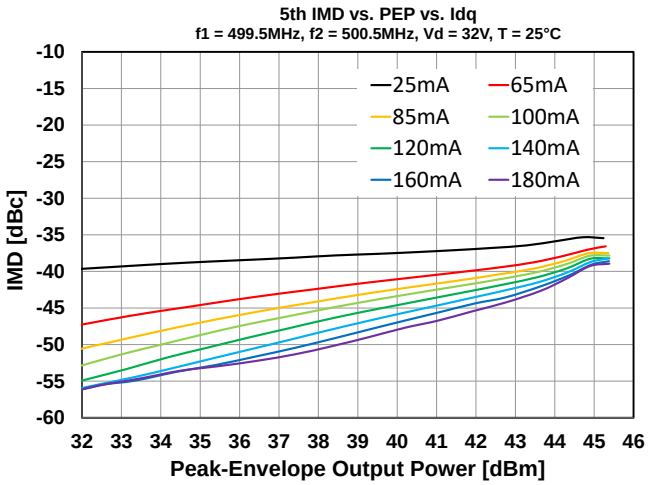




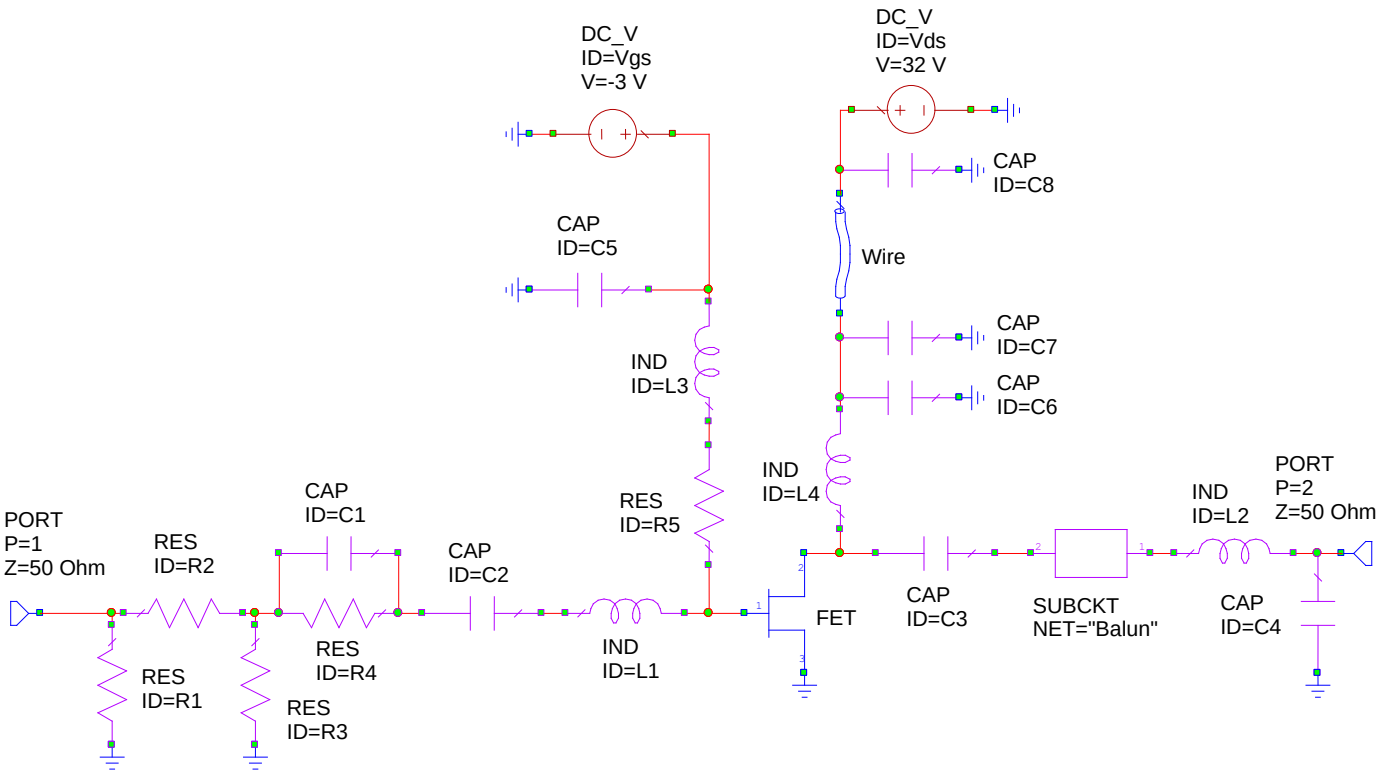








0.05 – 0.55 GHz Application Circuit



Bias-up Procedure

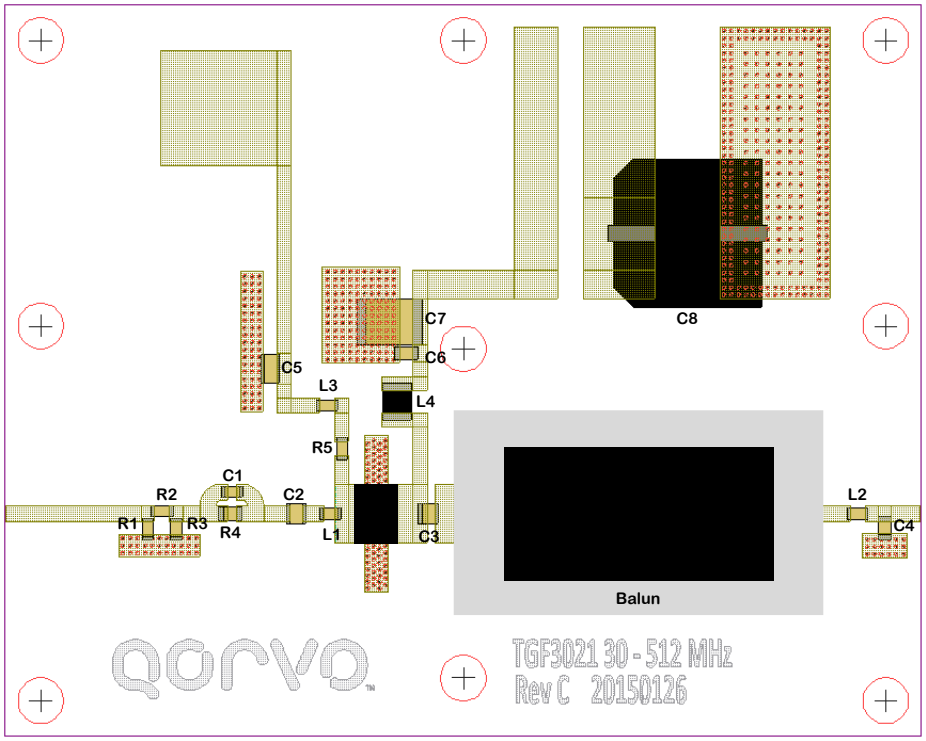
1. V_G set to -5 V.
2. V_D set to 32 V.
3. Adjust V_G more positive until quiescent I_D is 65 mA.
4. Apply RF signal.

Bias-down Procedure

1. Turn off RF signal.
2. Turn off V_D and wait 1 second to allow drain capacitor dissipation.
3. Turn off V_G.

0.05 – 0.55 GHz Evaluation Board Layout

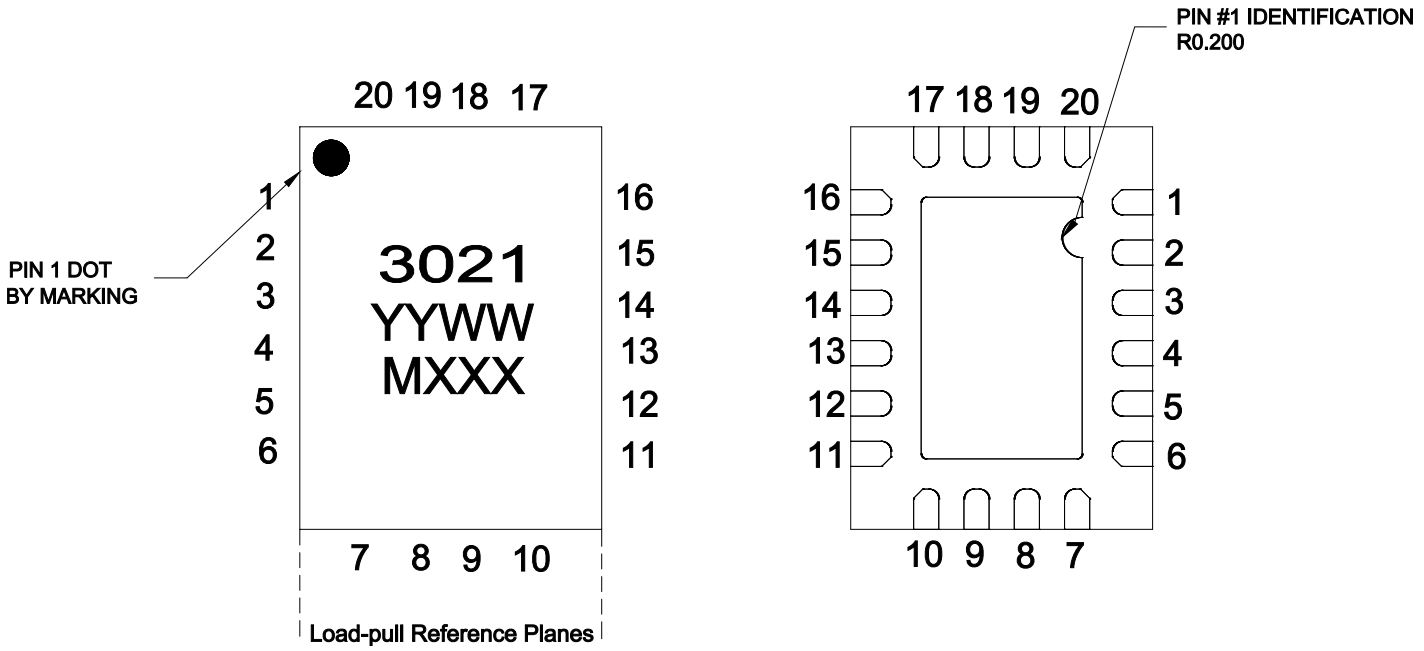
Top RF layer is 0.020" thick Rogers RO4350B, ε_r = 3.48. The pad pattern shown has been developed and tested for optimized assembly at Qorvo Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances.



0.05 – 0.55 GHz EVB Bill of Materials

Reference Design	Value	Qty	Manufacturer	Part Number
R1, R3	432 Ω	2	Any	Generic 0603
R2	11.3 Ω	1	Any	Generic 0603
R4	23.7 Ω	1	Any	Generic 0603
R5	10 Ω	1	Any	Generic 0603
C1	15 pF	1	ATC	600S150AT250XT
C2, C3	820 pF	2	ATC	700A821JW050XT
C4	2.7 pF	1	ATC	600S2R7AT250XT
C5	10 uF	1	Murata	GRM188R60J6ME47D
C6	82 pF	1	ATC	600S820FT250XT
C7	10 uF	1	TDK	C5750X7R1H106K320KB
C8	220 uF	1	Nichicon	UWT1H221ML1GS
L1	15 nH	1	Coilcraft	0603HC-15NX
L2	10 nH	1	Coilcraft	0603HC-10NX
L3	1200 nH	1	Coilcraft	0603LS-122X
L4	1100 nH	1	Coilcraft	108AF-112X
Balun	NA	1	Anaren	XMT0310B5012

Pin Layout



Pin Description

Pin	Symbol	Description
11 - 16	V_D / RF OUT	Drain voltage / RF Output to be matched to 50 ohms; see EVB Layout on page 27 as an example.
1 - 6	V_G / RF IN	Gate voltage / RF Input to be matched to 50 ohms; see EVB Layout on page 27 as an example.
7 – 10, 17 - 20	NC	Not connected
Back side	Source	Source connected to ground

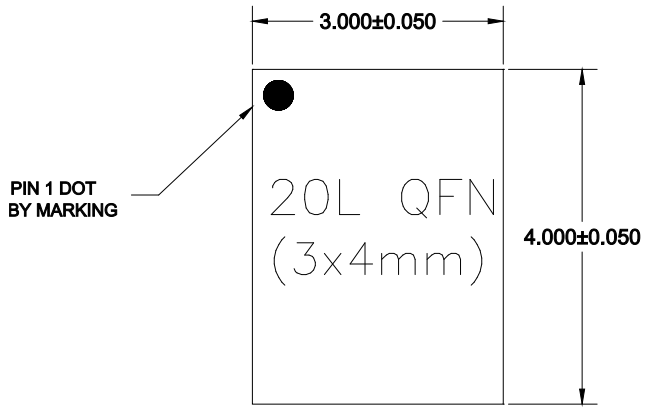
Notes:

Thermal resistance measured to back side of package

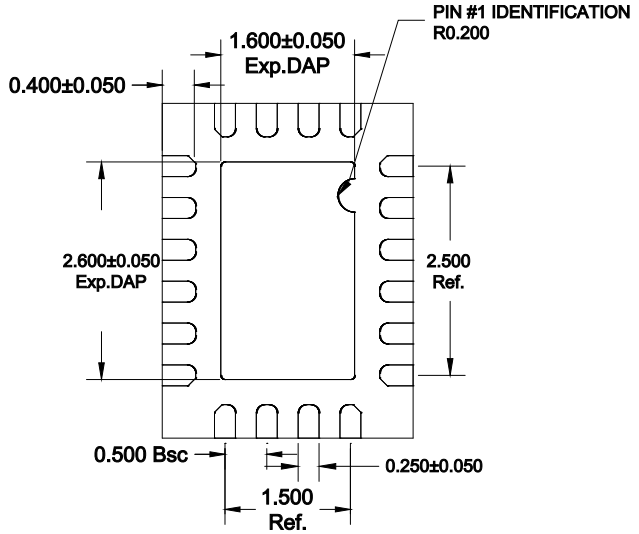
The TGF3021-SM will be marked with the “3021” designator and a lot code marked below the part designator The “YY” represents the last two digits of the calendar year the part was manufactured, the “WW” is the work week of the assembly lot start, and the “MXXX” is the production lot number.

Mechanical Information

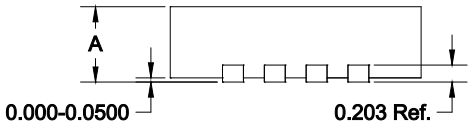
All dimensions are in millimeters.



TOP VIEW



BOTTOM VIEW



SIDE VIEW

		QFN
A	MAX.	0.900
	NOM.	0.850
	MIN.	0.800

Note:

Unless otherwise noted, all dimension tolerances are +/-0.127 mm.

This package is lead-free/RoHS-compliant. The plating material on the leads is NiPdAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and tin-lead (maximum 245°C reflow temperature) soldering processes.

Recommended Soldering Temperature Profile