TGL2201–SM

Wideband Dual Stage VPIN Limiter

Product Overview

Qorvo's TGL2201-SM is a packaged dual stage Limiter fabricated on Qorvo's proven GaAs VPIN process. Operating over 2 to 12 GHz, the TGL2201-SM provided the limiting action at high input signal levels and low loss at small signal.

The TGL2201-SM is suitable for a variety of wideband systems such as LNA/receiver protection in radars, phased arrays and jammers.

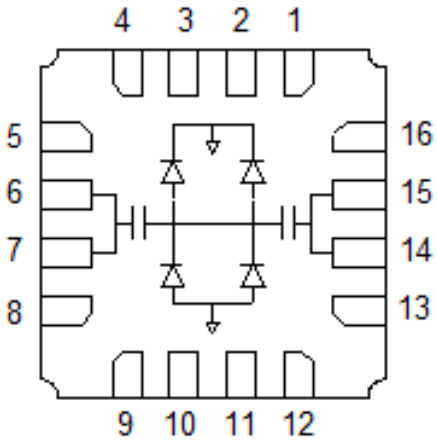
Lead-free and RoHS compliant.

QFN 3 x 3 mm 16 L Package

Key Features

- 2 to 12 GHz Passive, High Isolation Limiter
- Insertion Loss: < 1.0 dB, X-band
- Return Loss: > 10 dB
- Input Power CW Survivability up to 5 W
- Flat Leakage: < 18 dBm
- Recovery Time: < 115 ns
- Integrated DC Block on both input and output
- Package Dimensions: 3.00 x 3.00 x 1.35 mm

Functional Block Diagram



Applications

- LNA Receive Chain Protection
- Military Radar

Ordering Information

Part	Description
TGL2201–SM	Wideband VPIN Limiter
TGL2201-SM T/R	Wideband VPIN Limiter T/R
TGL2201-SM EVAL	EVAL BOARD

Standard Order Quantity = 100 pieces in a waffle pack
Standard T/R size = 500 pieces on a 7" reel.

Absolute Maximum Ratings

Parameter	Rating
RF Input Power, CW, 50 Ω, 25 °C	37 dBm
Mounting Temperature (30 s max)	260 °C
Storage Temperature	-55 to 150 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Passive – No Bias				
Temperature Range	-40	+25	+85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

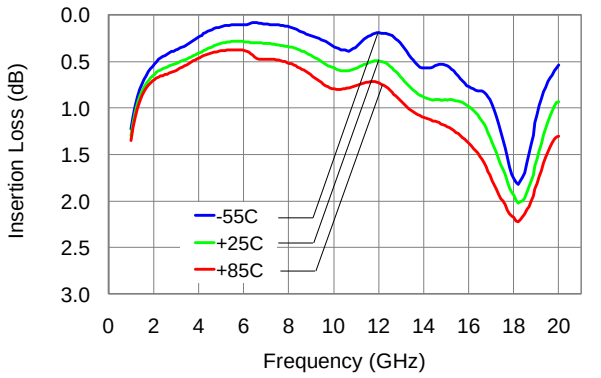
Test conditions unless otherwise noted: 25 °C

Parameter	Min	Typical	Max	Units
Operational Frequency Range	2		12	GHz
Insertion Loss		0.5	1.0	dB
Input Return Loss	10	12		dB
Output Return Loss	10	12		dB
Flat Leakage Power @ P_{IN} > 27 dBm		18		dBm
Recovery Time		< 115		ns

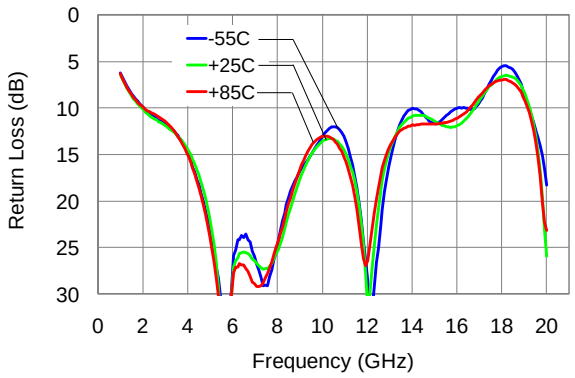
Performance Plots

Test conditions unless otherwise noted: Temp.=+25 °C

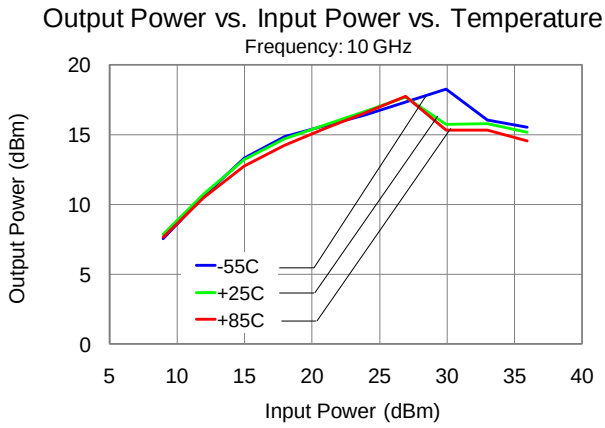
Insertion Loss vs. Frequency vs. Temperature



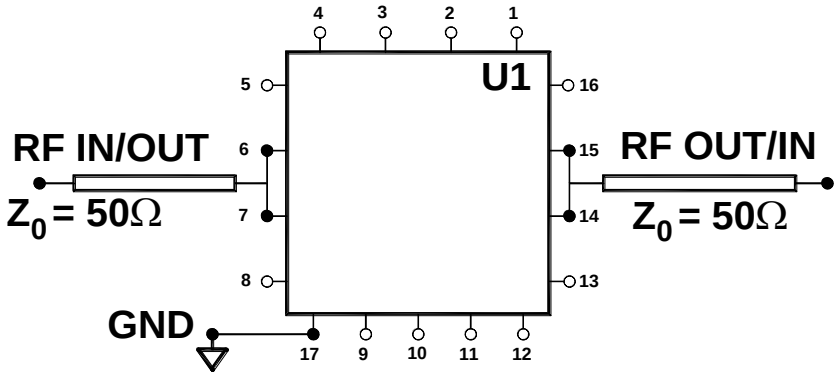
Return Loss vs. Frequency vs. Temperature



Output Power vs. Input Power vs. Temperature

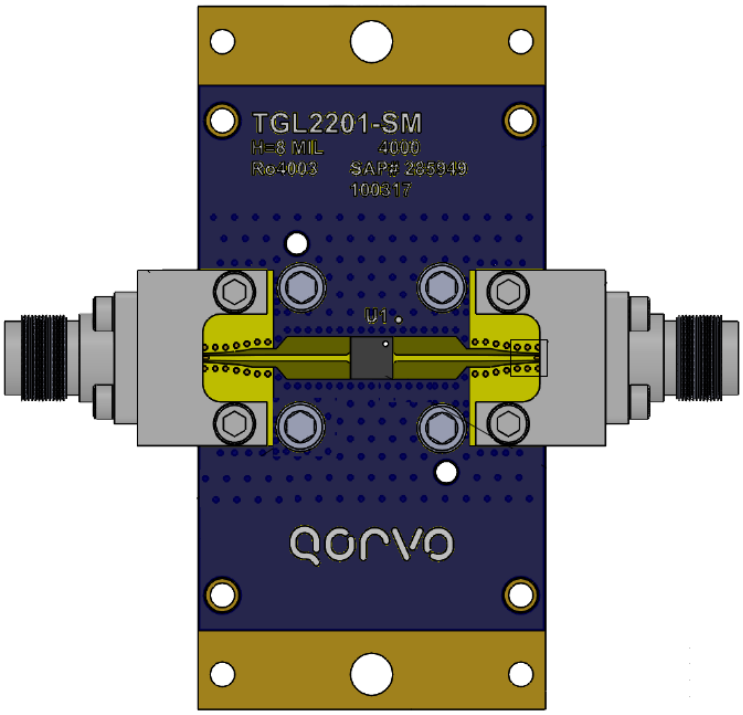


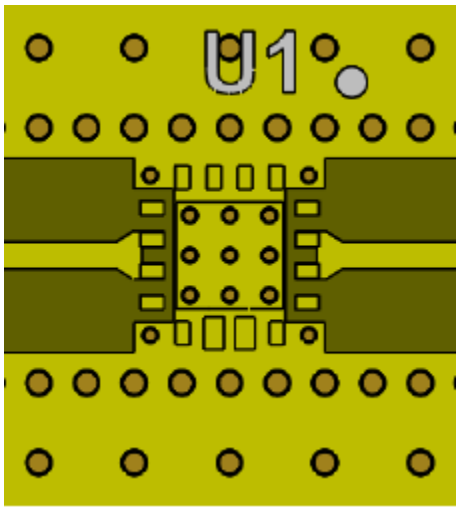
Application Circuit



Notes: A heat sink is recommended for high power operation (RF input > 1 W).

Evaluation Board (EVB) Layout & Mounting Detail





Mounting Detail

Notes:

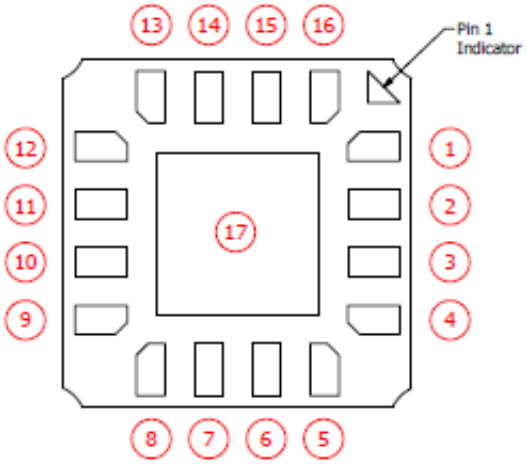
1. Top RF layer is 0.008” thick Rogers RO4003, ϵ_r = 3.55. Metal layers are 1-oz copper. Microstrip 50 Ω line width is .0174”. The microstrip line tapers to a 0.014” width at the connector interface. This PCB is designed for the Southwest Microwave end launch connector 1092-01A-5.

2. The pad pattern shown has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

3. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135”) diameter drill and have a final plated thru diameter of 0.25 mm (.010”).

4. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

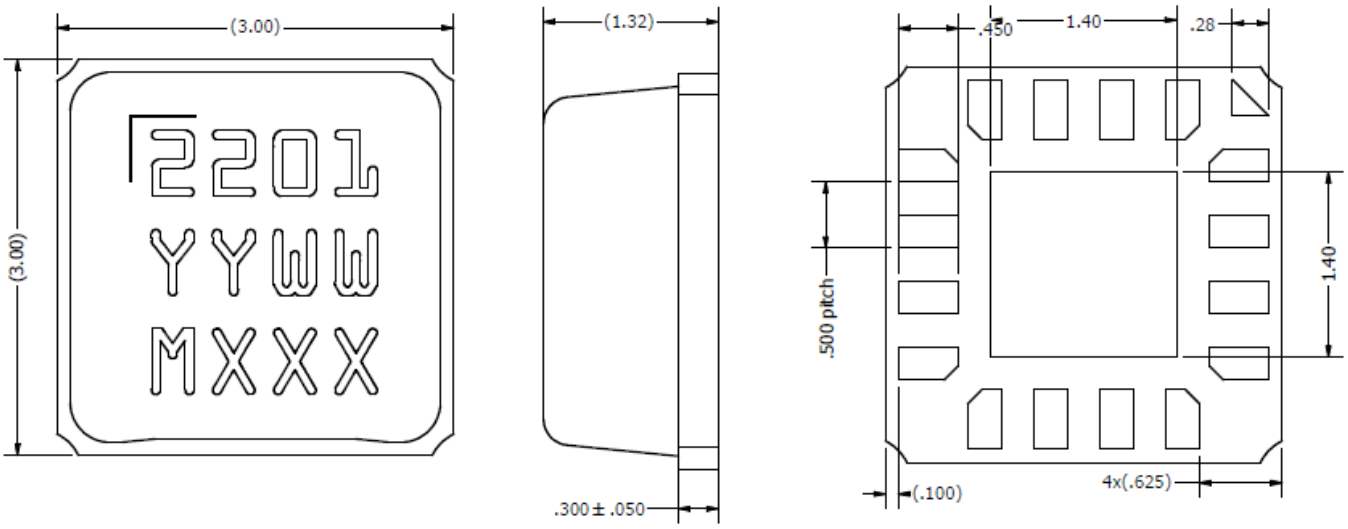
Pin Configuration and Description



Pin Description

Pin No.	Symbol	Description
1, 4, 9, 12	GND	Ground; Pins 1,4,9, and12 connected to 17 (backside paddle) inside package.
2, 3, 5, 8, 10, 11, 13, 16	N/C	No internal connection; may be grounded or left open on PCB
6, 7	RF IN/OUT	Input or output, matched to 50 ohms
14, 15	RF OUT/IN	Output or input, matched to 50 ohms
17	GND	On PCB, multiple vias should be employed under 17 to minimize inductance and thermal resistance; see page 8 for suggested mounting configuration.

Package Marking and Dimensions



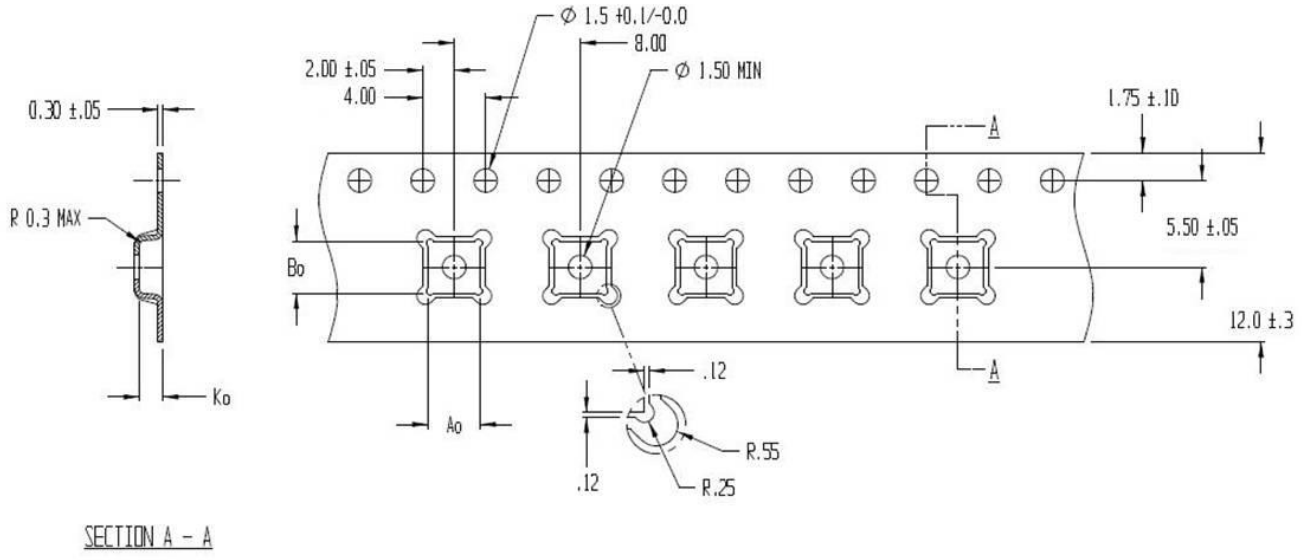
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS.
TOLERANCE IS +/- 0.075

NOTES:

1. PACKAGE BASE: ALUMINUM NITRIDE (AIN)
2. PACKAGE LID: LCD (Liquid Crystal Polymer)
3. PAD FINISH ON PACKAGE BASE:
   - Electroless Gold (Au): 0.5 – 1.5 µm
     OVER
   - Electroless Nickel (Ni): 2.0 µm minimum
4. PART MARKING:
   2201: PART NUMBER
   YY: PART ASSY YEAR
   WW: PART ASSY WEEK
   MXXX: BATCH ID

Tape and Reel Information

Standard T/R size = 500 pieces on a 7” reel.



Part	Feature	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.130	3.30
	Width	B0	0.130	3.30
	Depth	K0	0.059	1.50

Solderability

1. Compatible with the latest version of J-STD-020, Lead-free solder, 260° C.
2. The use of no-clean solder to avoid washing after soldering is recommended.
3. The package base is Aluminum Nitride (AIN) and the plating material on the leads is gold over nickel (Au-Ni).

Recommended Soldering Profile