TGL2208–SM

2 - 20 GHz Dual Stage VPIN Limiter

Product Overview

Qorvo's TGL2208-SM is a packaged dual stage Limiter fabricated on Qorvo's proven GaAs VPIN process. Operating over 2 to 20 GHz, the TGL2208-SM has < 1dB of insertion loss under small signal operation and flat leakage of < 18 dBm under large signal input.

The TGL2208-SM is suitable for a variety of systems that require input protection for sensitive receive channel components.

The TGL2208-SM is available in a low-cost, surface mount 14 lead 3 x 3 AIN QFN package comprised of a ceramic base with a plastic epoxy-sealed lid. TGL2208-SM is ideally suited to support both commercial and defense related applications.

Lead-free and RoHS compliant.

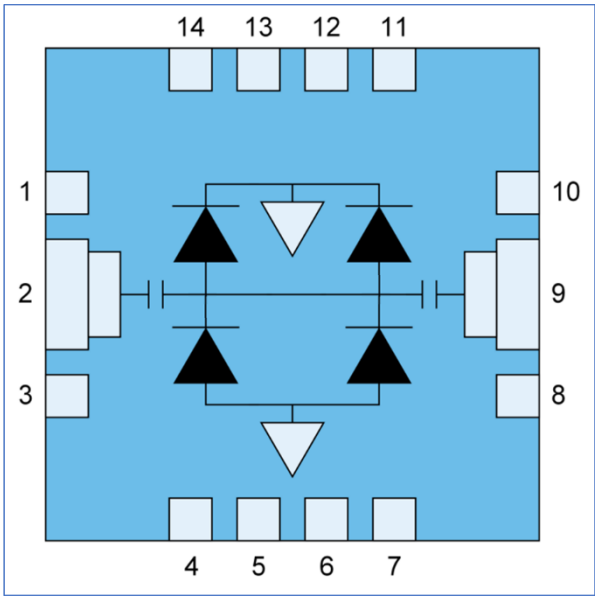
QFN 3 x 3 mm 14 L Package

Key Features

- Frequency Range: 2 to 20 GHz
- Insertion Loss: < 1.0 dB
- Return Loss: > 12 dB
- Input Power CW Survivability up to 5 W
- Flat Leakage: < 18 dBm
- Recovery Time: < 115 ns
- Integrated DC Block on both input and output
- Package Dimensions: 3.00 x 3.00 x 1.35 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Top View

Applications

- Receive Chain Protection
- Commercial and Military Radar

Ordering Information

Part	Description
TGL2208–SM	2–20 GHz VPIN Limiter
1100870	TGL2208-SM, EVAL BOARD

Absolute Maximum Ratings

Parameter	Rating
RF Input Power, CW, 50 Ω, 25 °C	37 dBm
Mounting Temperature (30 s max)	260 °C
Storage Temperature	-55 to 150 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Passive – No Bias				
Temperature Range	-40	+25	+85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

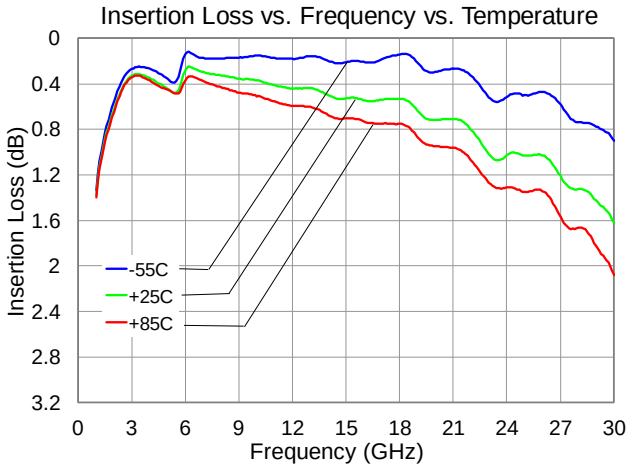
Electrical Specifications

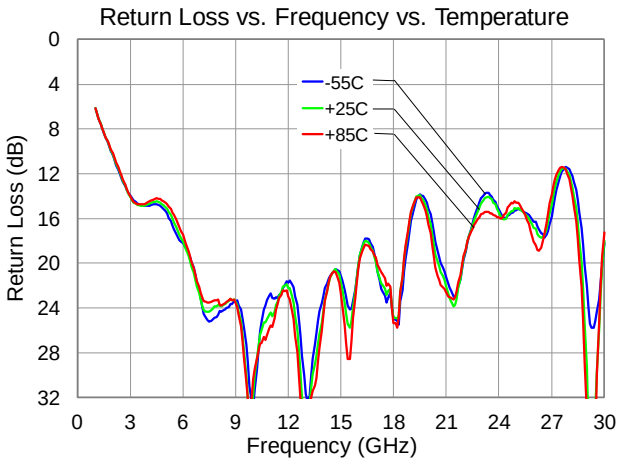
Test conditions unless otherwise noted: 25 °C

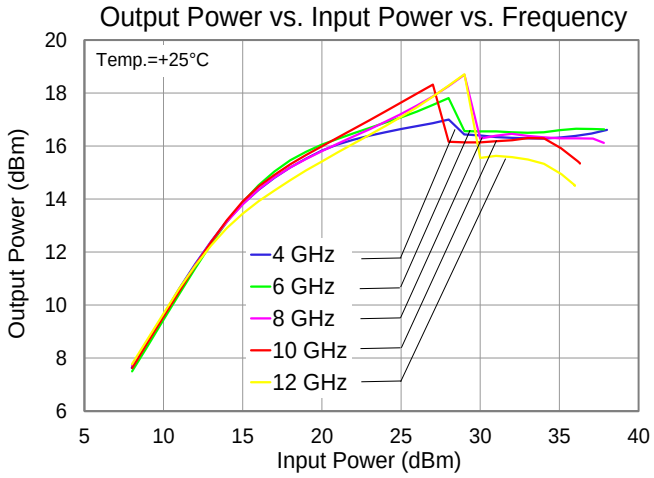
Parameter	Min	Typical	Max	Units
Operational Frequency Range	2		20	GHz
Insertion Loss		0.5		dB
Input Return Loss		15		dB
Output Return Loss		15		dB
Flat Leakage Power @ P_{IN} > 27 dBm		18		dBm
Recovery Time		< 115		ns
Insertion Loss Temperature Coefficient		0.003		dB/ °C

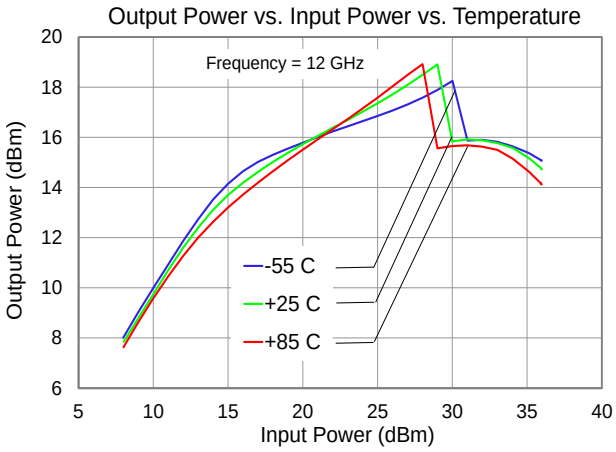
Performance Plots

Test conditions unless otherwise noted: Temp.=+25 °C

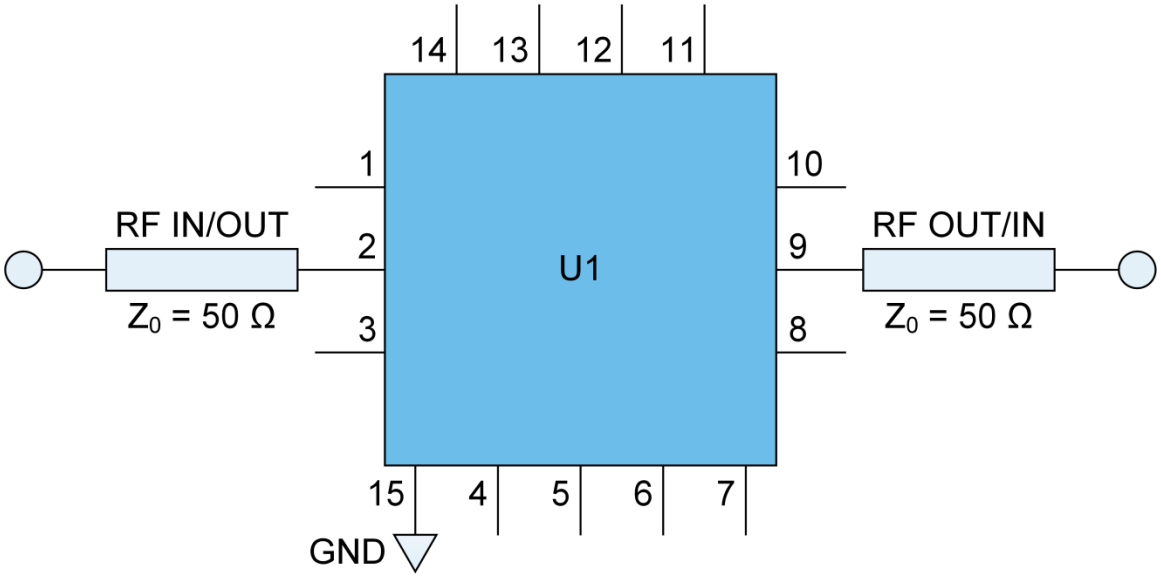






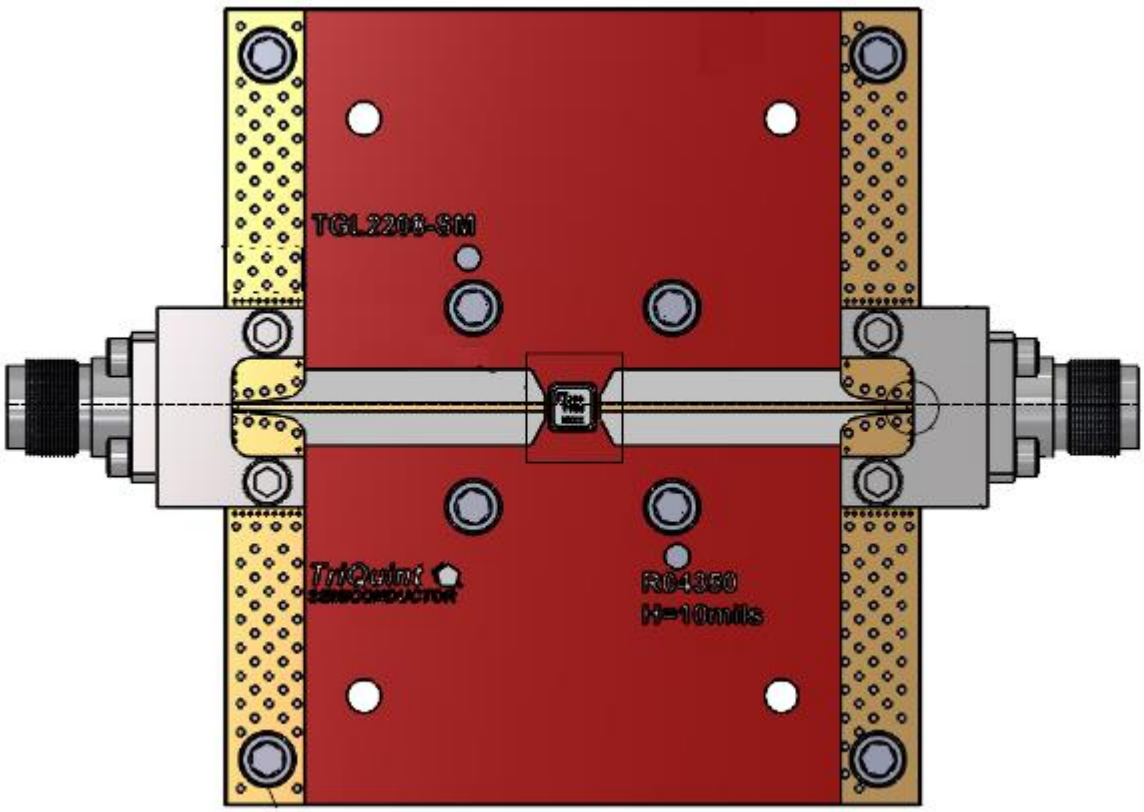


Application Circuit



Notes: A heat sink is recommended for high power operation (RF input > 1 W).

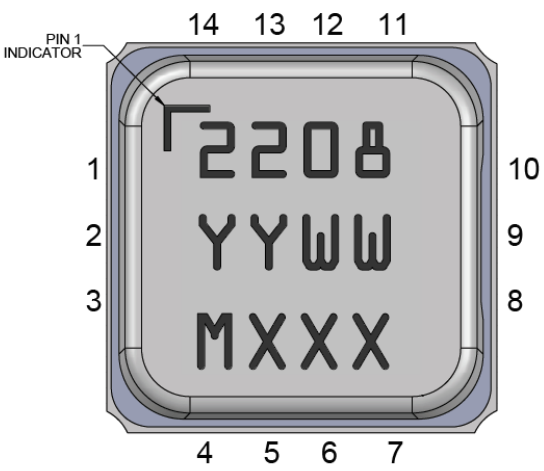
Application Information and Evaluation Board (EVB) Layout

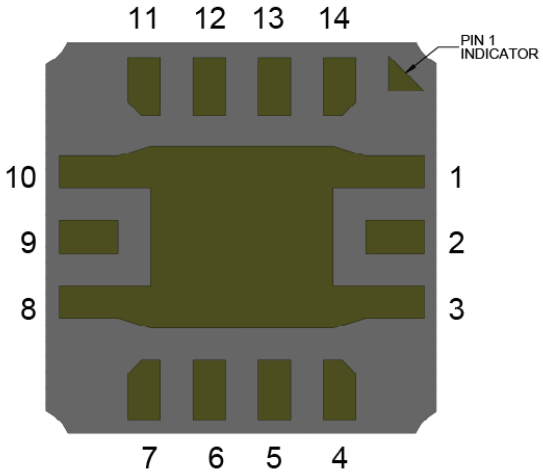


RF layer is 0.010” thick Rogers RO4350. Metal layers are 0.5-oz copper. Microstrip 50 Ω line width is 0.021”. The microstrip line taper at the connector interface is optimized for the Southwest Microwave end-launch connector 1092-01A-5.

The pad pattern shown has been developed and tested for optimized assembly at Qorvo Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

Pad Configuration and Description

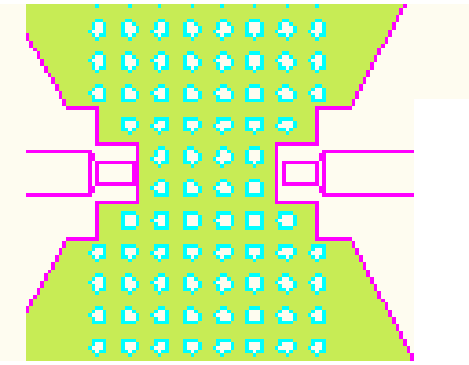




Pad No.	Label	Description
1, 3, 8, 10	GND	Pins 1,3,8 and 10 are connected to 15 (backside paddle) inside package.
2	RF Input	RF Input, matched to 50 Ohms.
4 – 7, 11 - 14	N/C	No internal connection; must be grounded or left open on PCB.
9	RF Output	RF Output, matched to 50 Ohms.
15	GND	On PCB, multiple vias should be employed under Pin 15 to minimize inductance and thermal resistance; see page 7 for suggested mounting configuration.

NOTE: The RF Input and RF Output ports are interchangeable.

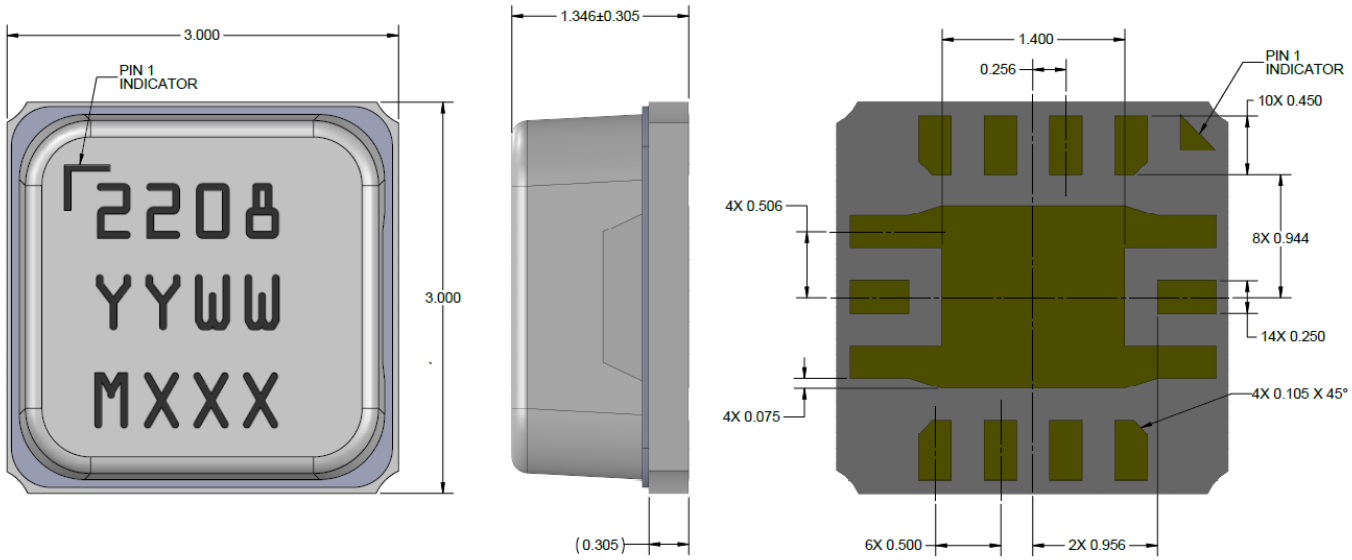
Evaluation Board PCB Mounting Detail



The pad pattern shown above has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

Ground / thermal vias are critical for the proper performance of this device. Vias should use a 0.008 in. diameter drill, and they are solid filled with non-conductive material and over plated shut.

Package Marking and Dimensions



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS (MM)
TOLERANCE IS +/- 0.127

NOTES:

1. PACKAGE BASE: CERAMIC
2. PACKAGE LID: PLASTIC
3. ALL METALIZED FEATURES ARE GOLD PLATED
4. THE PART IS EPOXY SEALED
5. PART MARKING:
   2208: PART NUMBER
   YY: PART ASSY YEAR
   WW: PART ASSY WEEK
   MXXX: BATCH ID

Assembly Notes

- Compatible with lead-free soldering process with 260°C peak reflow temperature.
- This package is non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing after soldering is recommended
- Solder rework not recommended.
- Contact plating: Ni-Au

Recommended Soldering Profile