TGL2210-SM

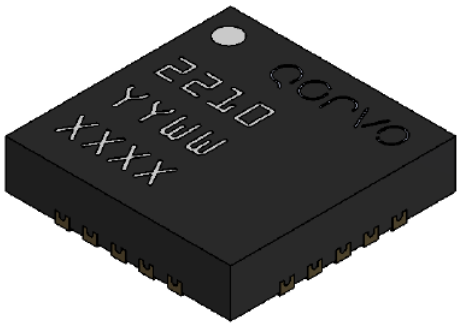
0.05 – 6 GHz 100 Watt VPIN Limiter

Product Overview

The Qorvo TGL2210-SM is a high-power receive protection circuit (limiter) operating from 0.05-6GHz. Capable of withstanding up to 100 W incident power levels, the TGL2210-SM allows < 17 dBm flat leakage to pass through and contributes < 0.7 dB in insertion loss.

Using Qorvo's passive GaAs VPIN technology, the TGL2210-SM does not require bias and is offered in a small 4 x 4 (mm) plastic overmold package. This simplifies system integration while maximizing performance and protection.

The TGL2210-SM is ideal for commercial and military radar applications, communications systems and electronic warfare where protecting sensitive receive components from damage is critical.

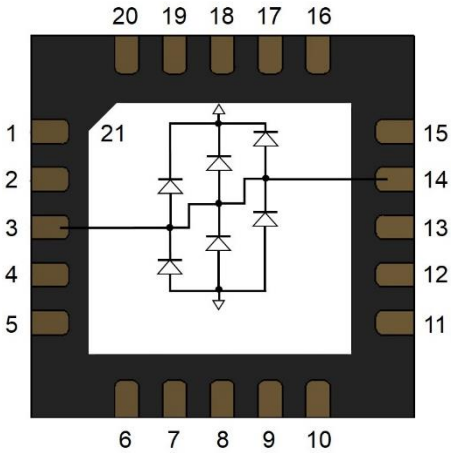


QFN 4x4 mm 20L

Key Features

- Frequency Range: 0.05 to 6.0 GHz
- Insertion Loss: < 0.7 dB
- Peak Power Handling: 100 W (pulsed)
- Flat Leakage: < 17 dBm
- Passive (no DC bias required)
- Recovery time < 40 ns
- QFN Package Dimensions: 4.0 x 4.0 x 0.85 mm

Functional Block Diagram



Top View

Applications

- Receive Chain Protection
- Commercial and Military Radar
- Communications
- Electronic Warfare

Ordering Information

Part	Description
TGL2210-SM	0.05–6.0 GHz 100W VPIN Limiter
TGL2210-SMEVB-01	Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Incident Power, Pulsed (PW = 10µs, DC = 10%), 50 Ω, 85 °C	110 W
Incident Power, CW, 50 Ω, 25 °C	85 W
Incident Power, CW, 50 Ω, 85 °C	70 W
Mounting Temperature (30 s max)	260 °C
Storage Temperature	-55 to 150 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units
Operating Temperature Range	-40	+25	+85	°C
Passive – No Bias				

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		0.05		6.0	GHz
Insertion Loss, Un-Tuned	Freq = 3.5 GHz		0.6	0.85	dB
Insertion Loss, Tuned	Freq = 3.5 GHz (1)		0.4		dB
Input Return Loss, Un-Tuned		9.5	11.0		dB
Output Return Loss, Un-Tuned		9.0	11.5		dB
Flat Leakage Power	@ P_{IN} > 30 dBm		< 17		dBm
Pulse Recovery Time			< 40		ns
Spike Leakage			< 0.5		dB
Insertion Loss Temperature Coefficient			0.001		dB/ °C

Notes: Test conditions unless otherwise noted: Temp = +25 °C, 50 Ω system.
1. Tuned EVB to improve 2-5 GHz

Thermal and Reliability Information

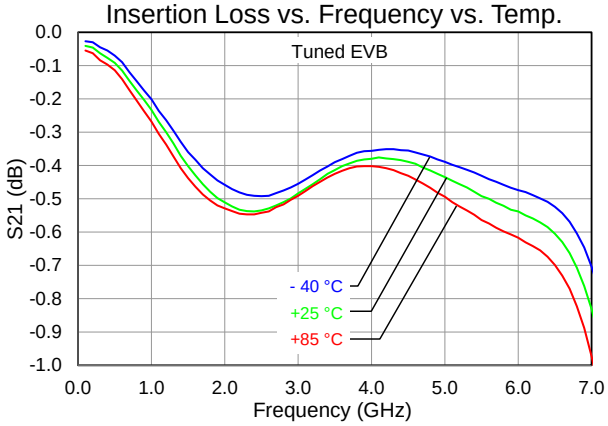
Parameter	Test Conditions	Value	Units
Incident Power (168 hours RF Operational Life Test (1))	4.5 GHz, CW, 50 Ω, 25 °C	31	W
	4.5 GHz, Pulsed, PW=10 µs, DC=10%, 50 Ω, 25 °C	100	W

Notes:
1. Test was terminated at 168 hours. Insertion Loss remained ≤ 1 dB for device under test.

Performance Plots – Small Signal

Test conditions unless otherwise noted: Temp.=+25 °C

Insertion Loss vs. Frequency vs. Temp.



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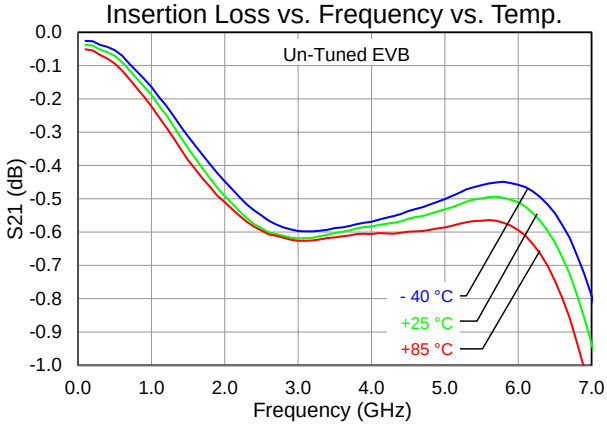
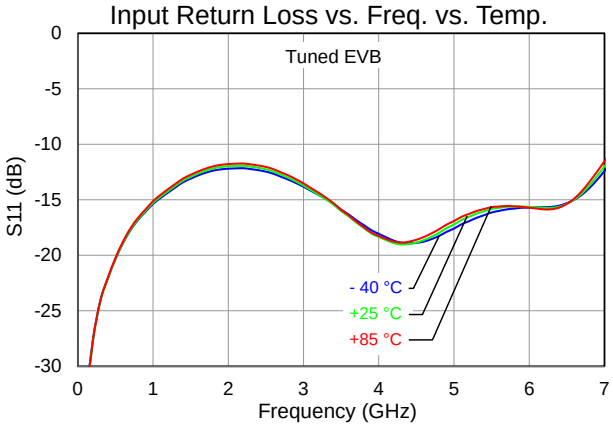


Input Return Loss vs. Freq. vs. Temp.



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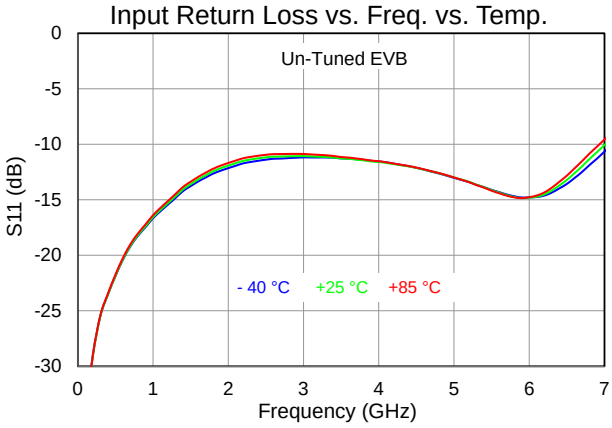
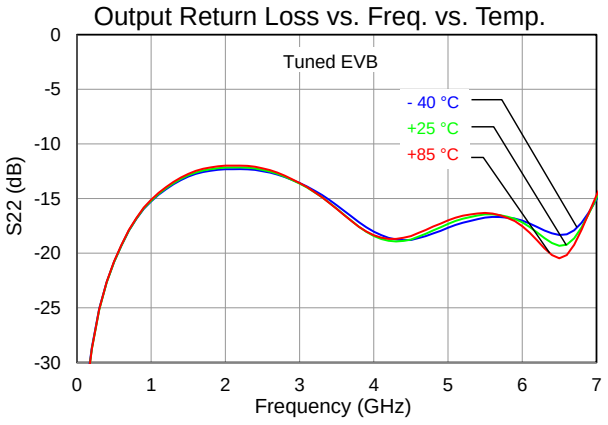


Output Return Loss vs. Freq. vs. Temp.



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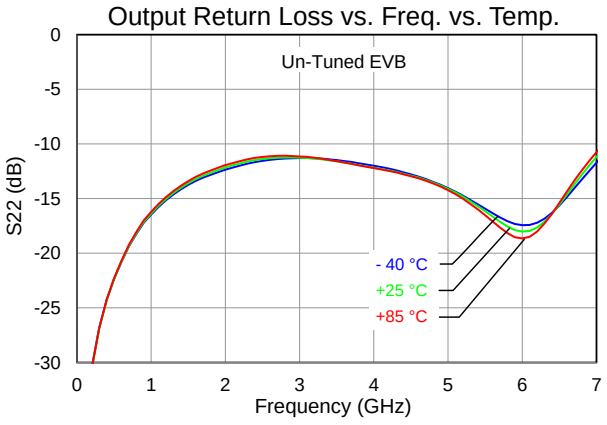

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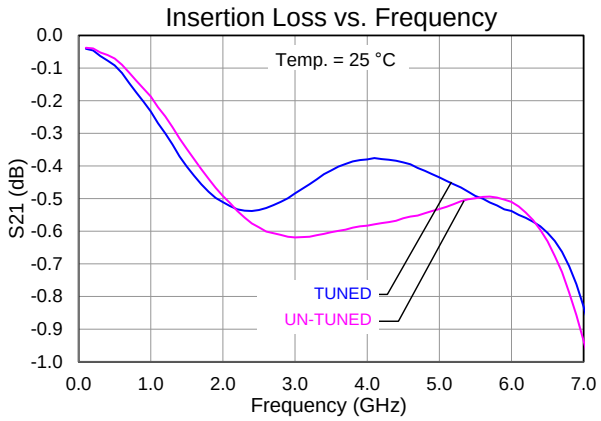
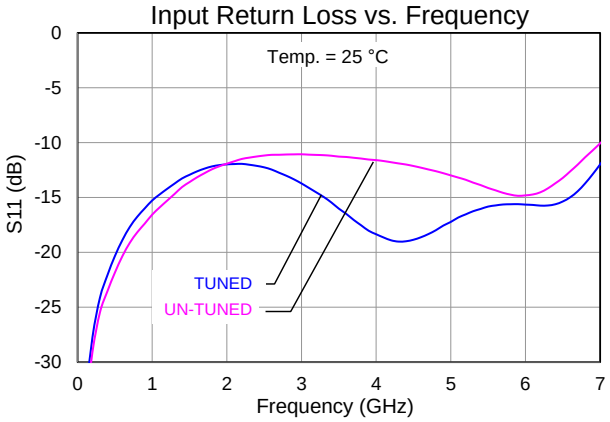
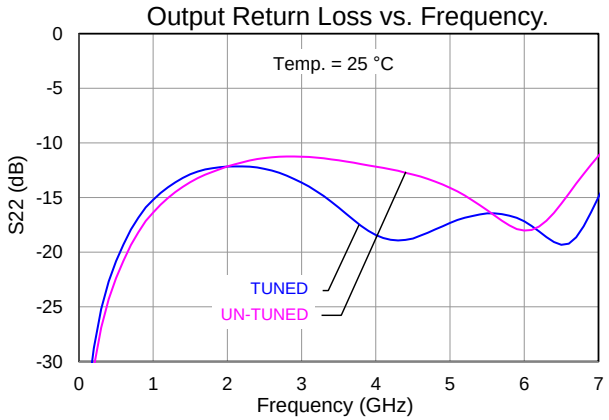


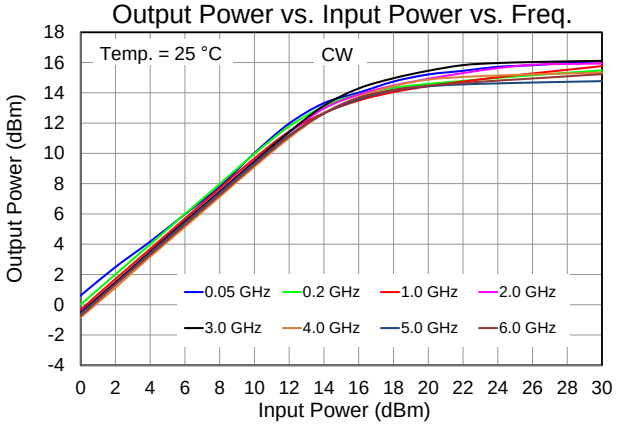




Performance Plots – Large Signal

Test conditions unless otherwise noted: Temp.=+25 °C

Output Power vs. Input Power vs. Freq.



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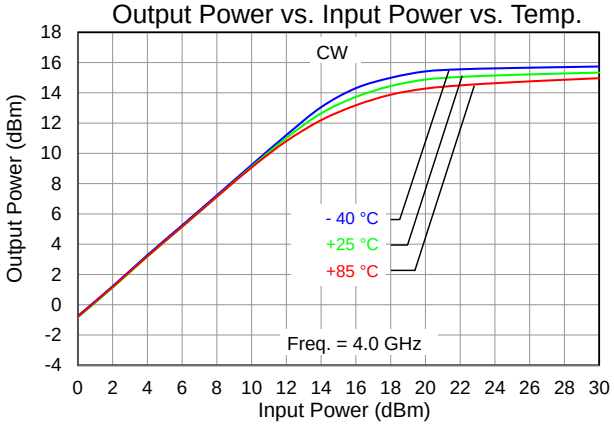

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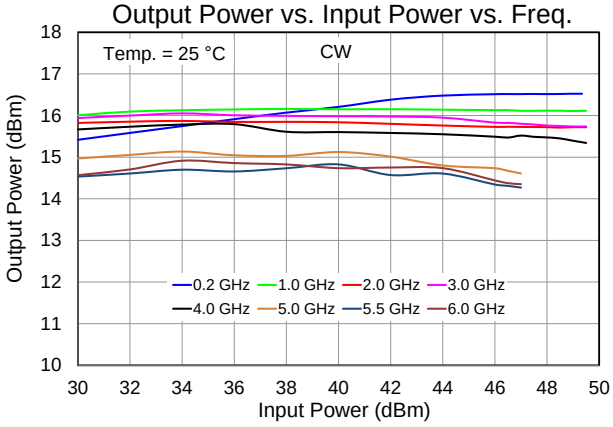
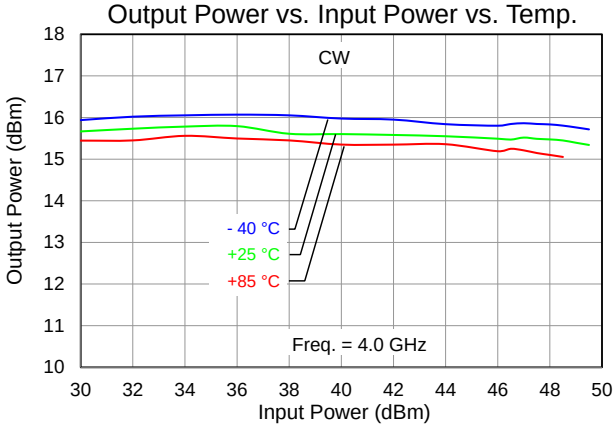
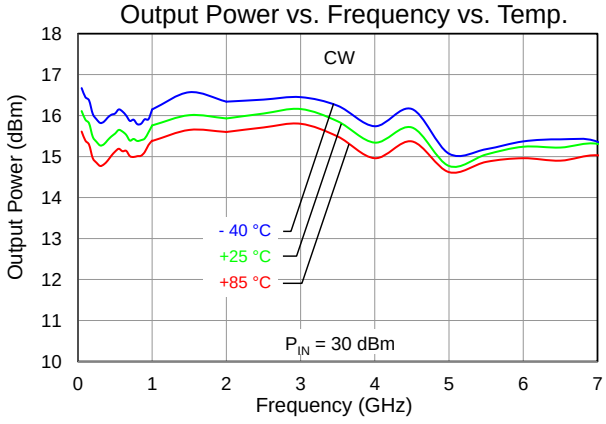


Output Power vs. Input Power vs. Temp.



Output Power vs. Frequency vs. Temp.



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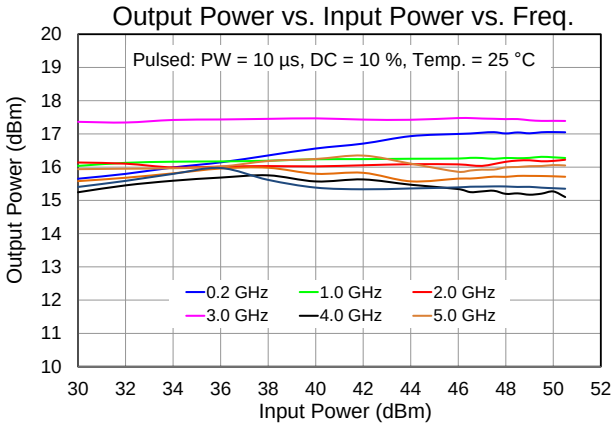
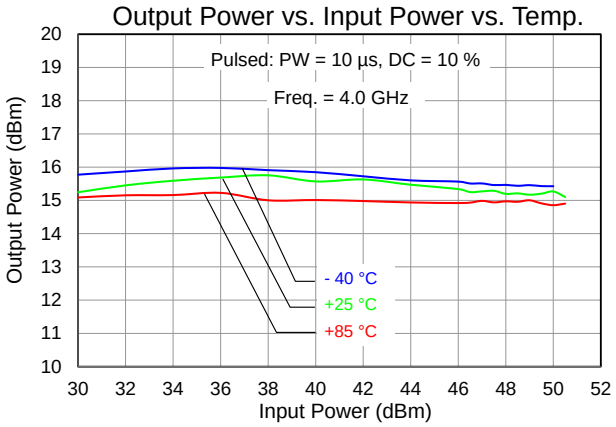
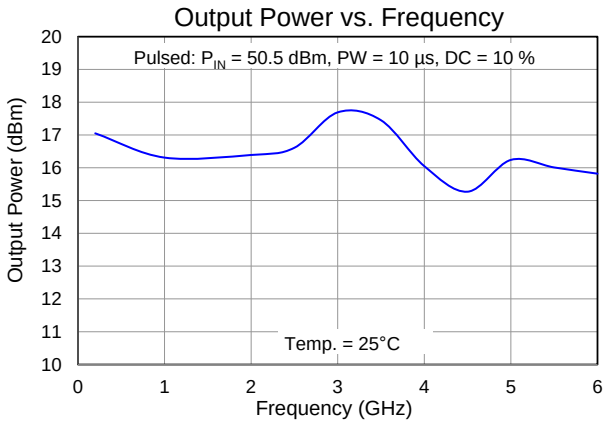
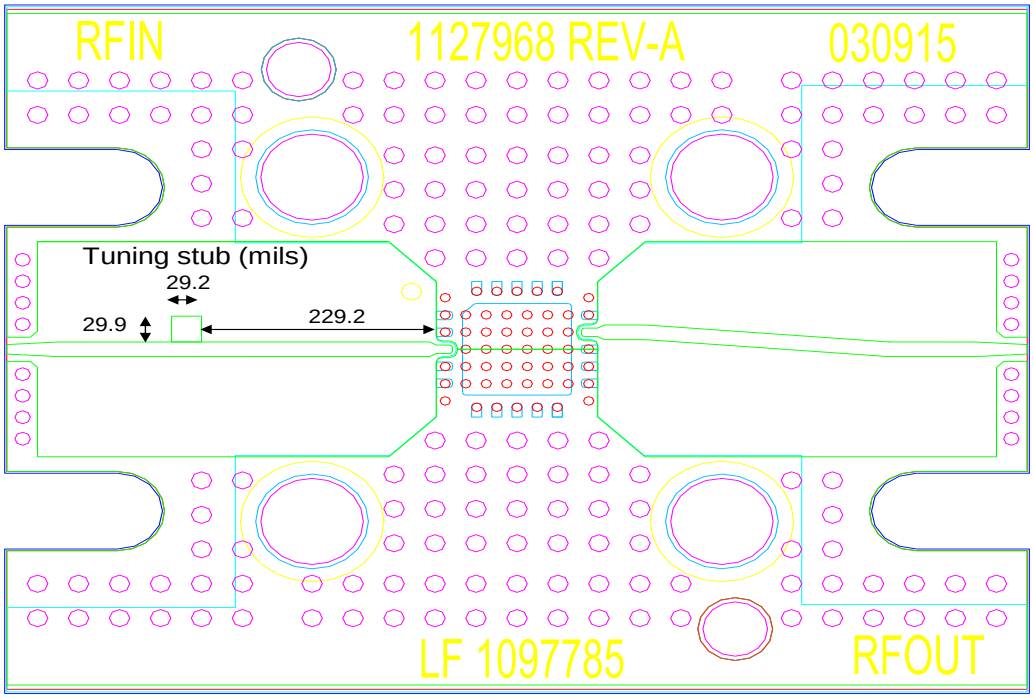


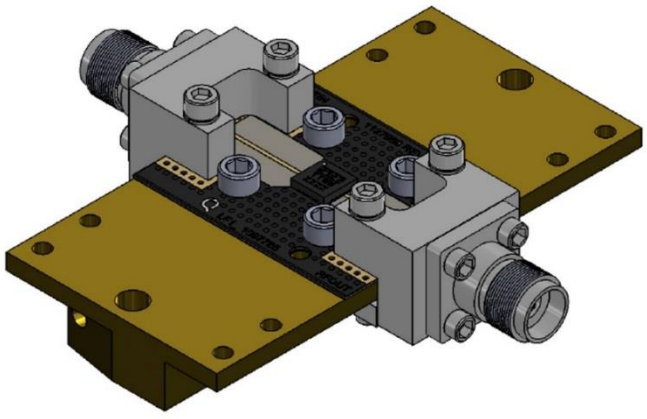


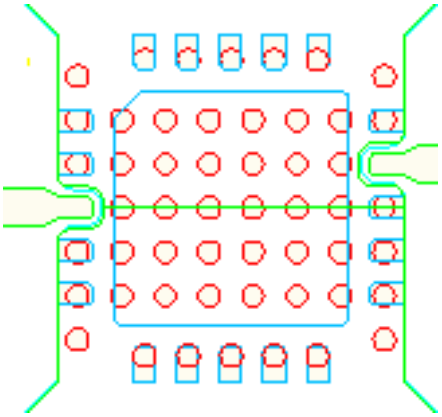


Evaluation Board PCB Information and Mounting Detail

TUNED PCB LAYOUT







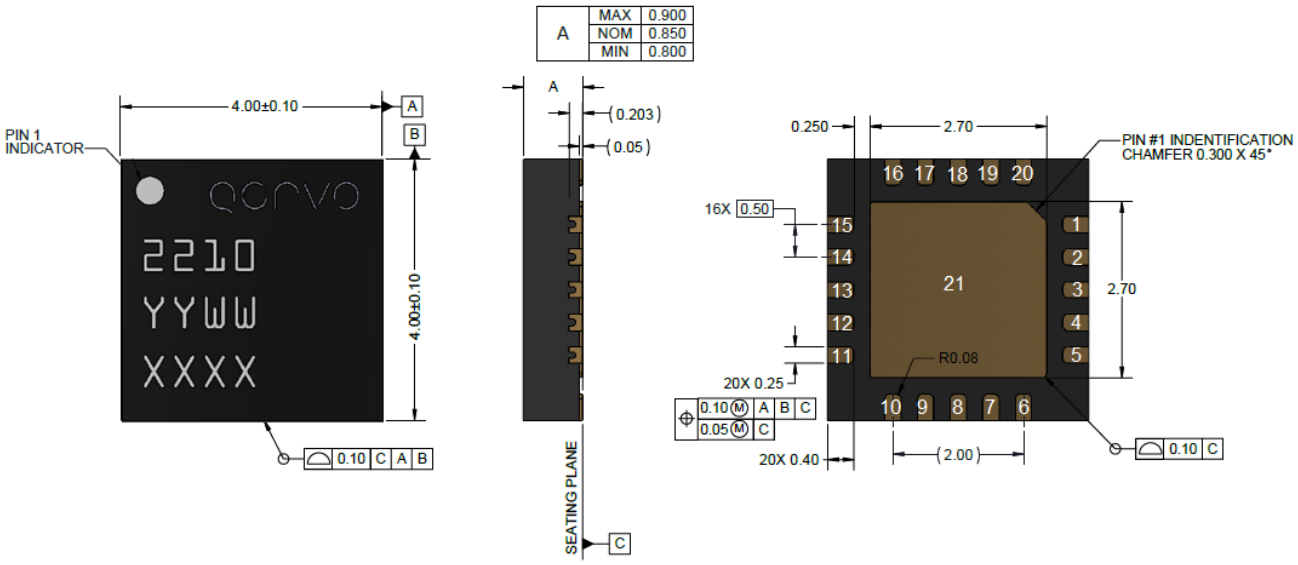
MOUNTING PATTERN

RF layer is 0.008” thick Rogers RO4003C. Metal layers are 0.5-oz copper. Microstrip 50 Ω line width is 0.050”. The microstrip line taper at the connector interface is optimized for the Southwest Microwave end-launch connector 1092-02A-5.

The pad pattern shown has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

- Ground / thermal vias under the DUT are critical for the proper performance of this device.
- The PCB shown herein utilizes copper filled vias (10 mils diameter) under the DUT to maximize heat transfer away from the DUT under large signal conditions.
- Thermal dissipation is low for normal non-limiting operation.

Package Marking, Dimensions and Pad Description



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
   Tolerances: XX = ± .05
   XXX = ± .025
2. Package Leads Are Gold Plated (NiPdAu)
3. Part Is Mold Encapsulated
4. Part Marking:
   2210: Part Number
   YY: Part assembly Year
   WW: Part Assembly Week
   XXXX: Batch ID

Package Pad	Symbol	Description
1, 2, 4 – 13, 15 – 20	NC	No Connection; recommend GND at the EVB level
3	RF Input	Input; matched to 50 Ohms; not DC blocked
14	RF Output	Output; matched to 50 Ohms; not DC blocked
21 (Slug)	GND	On PCB; multiple vias should be employed under the center pad (21) to minimize inductance and thermal resistance; see page 7 for suggested mounting configuration

Note: The RF Input and Output ports are not interchangeable.

Solderability

Compatible with both lead-free (260°C max. reflows temp.) and tin/lead (245°C max. reflows temp.) soldering processes.
Plating is Ni-Pd-Au, Au thickness of 0.00254-0.01016 µm.

Recommended Soldering Profile