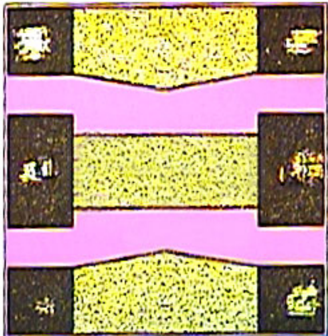
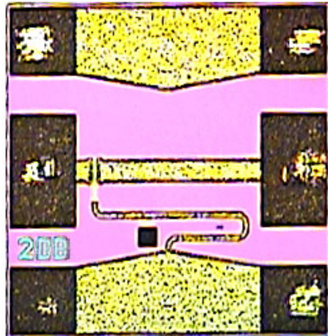
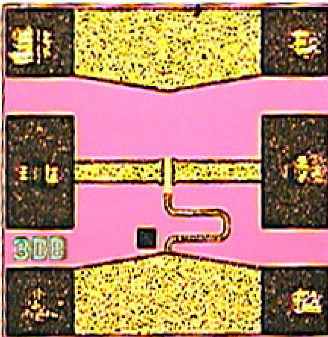
Wideband Fixed Attenuators

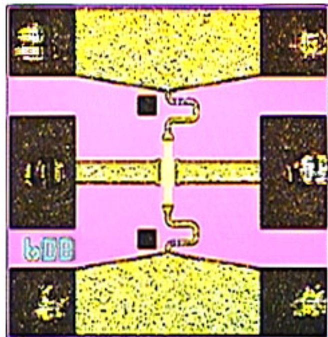




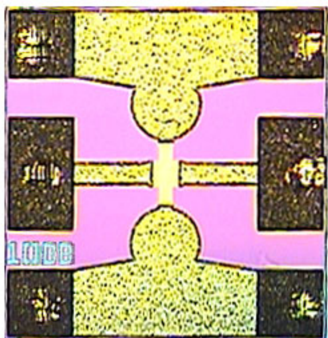
2 dB Attenuator



3 dB Attenuator



6 dB Attenuator



10 dB Attenuator

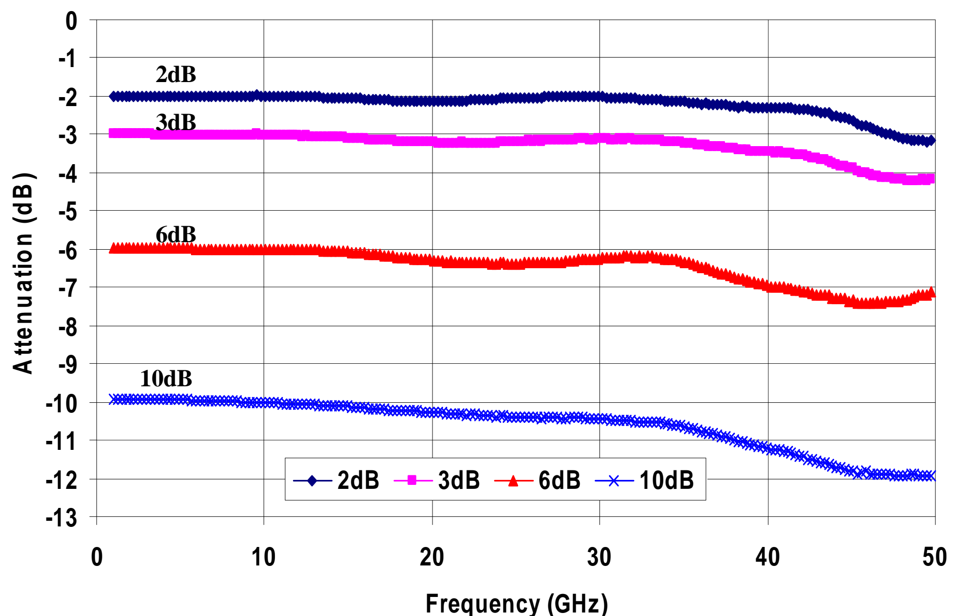
Key Features and Performance

- Fixed 0, 2, 3, 6 and 10dB Attenators
- Broadband Response DC to > 40 GHz
- Excellent Return Loss > 15 dB
- Power Handling = 20 dBm
- On-Chip Grounding Vias
- 3MI Passive Part
- Low Price
- Small size: 0.5 x 0.5 x 0.1 mm
  (0.02 X 0.02 X 0.004 in)

Primary Applications

- Point to Point Radio
- Fiber Optic
- Wideband Military & Space
- Test Equipment

Typical Electrical Characteristics
Attenuators Probed in Fixtures



Datasheet subject to change without notice.

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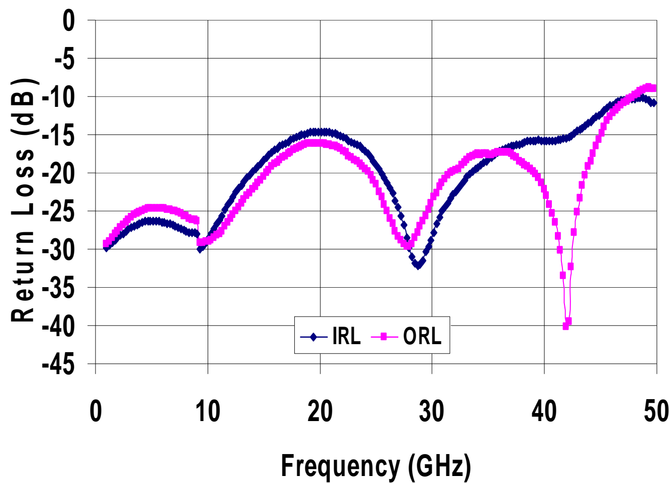
TABLE I
ELECTRICAL CHARACTERISTICS
(Ta = 25 ^{0}C Nominal)

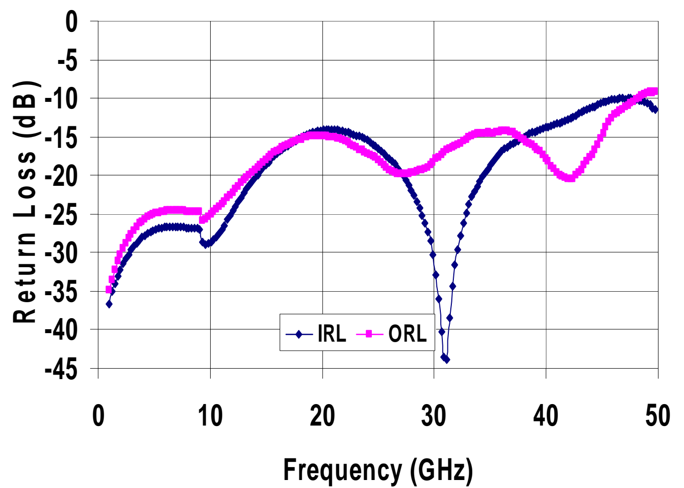
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	0dB Attenuation (-00)	DC – 30 GHz 1/	0	0.1	0.2	dB
	2dB Attenuation (-02)	DC – 30 GHz 1/	1.75	2	2.25	dB
	3dB Attenuation (-03)	DC – 30 GHz 1/	2.65	3	3.35	dB
	6dB Attenuation (-06)	DC – 30 GHz 1/	5.3	6	6.3	dB
	10dB Attenuation (-10)	DC – 30 GHz 1/	9.4	10	10.4	dB
IRL	Input Return Loss	DC – 40 GHz		15		dB
ORL	Output Return Loss	DC – 40 GHz		15		dB
	Maximum Power	2 - 18 GHz			20	dBm

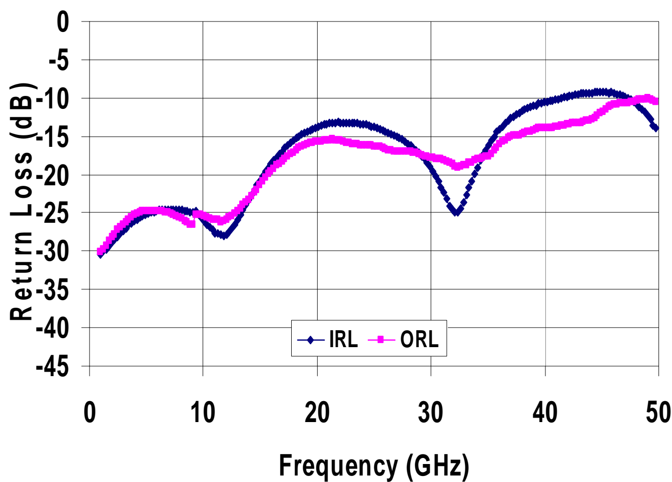
1/ Measured on wafer with RF probes. Bond wires are not included in this measurement. Wafer is sample tested at ~10%. TGL4201-00 is not RF tested.

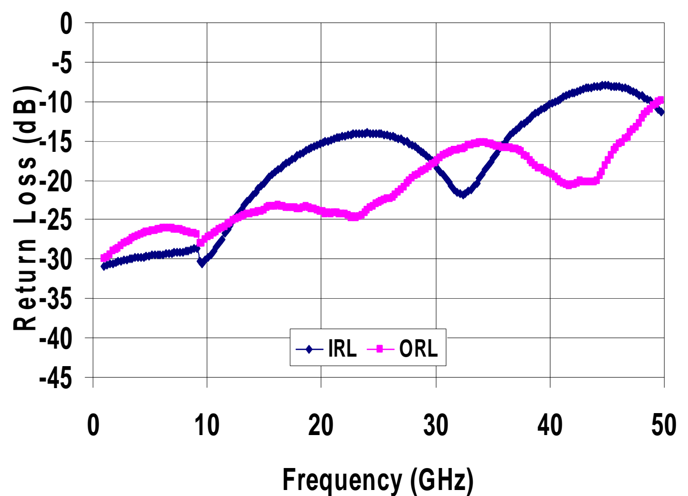
Typical Measurement Attenuators

Attenuators Probed in Fixtures









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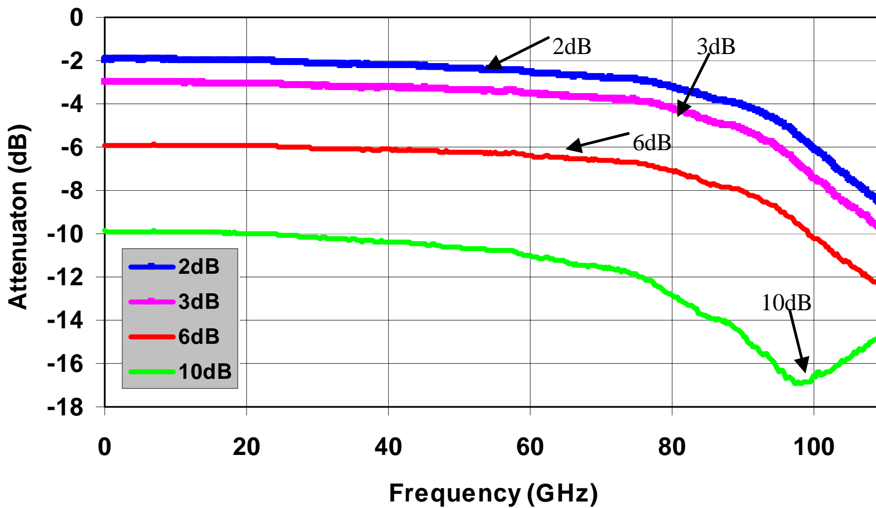
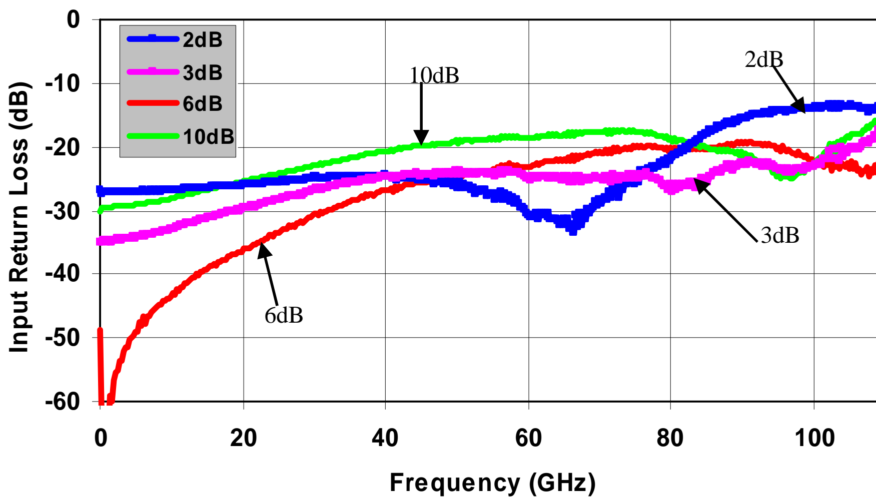
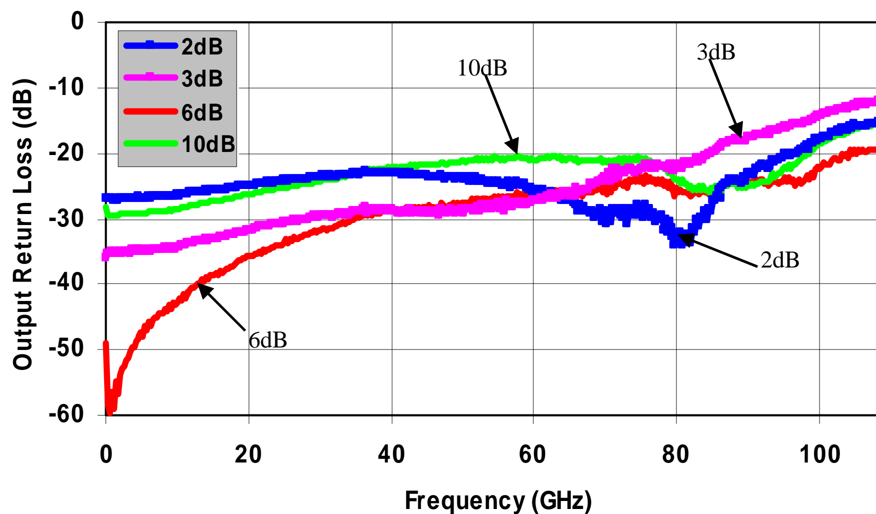
Typical Measurement Attenuators

No Bond Wires, Probed from 45 MHz to 110GHz







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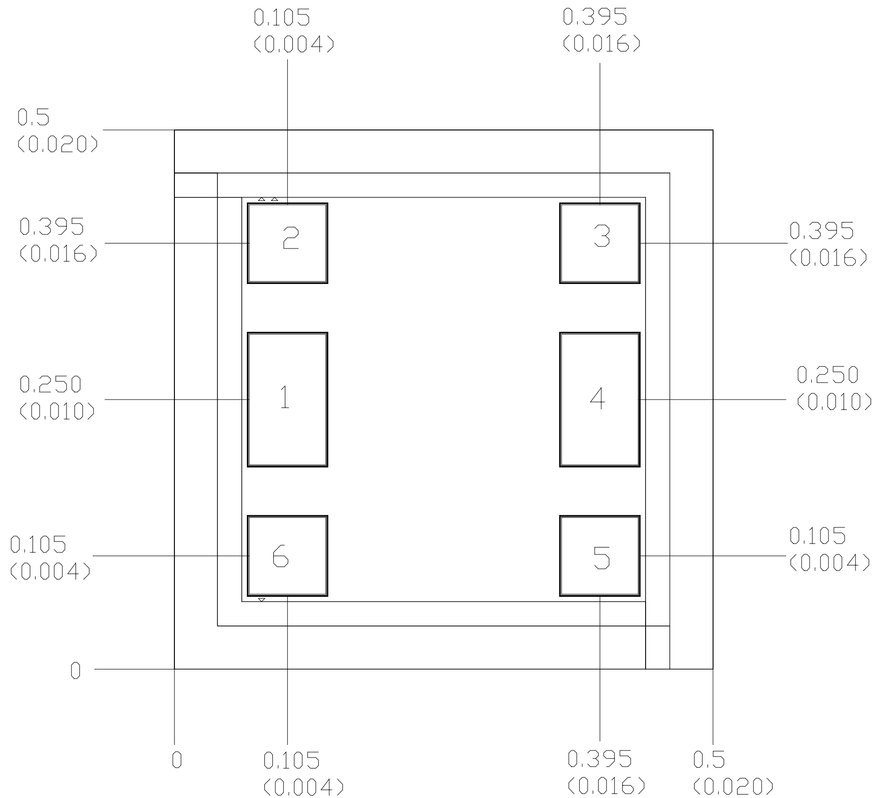
Mechanical Drawing



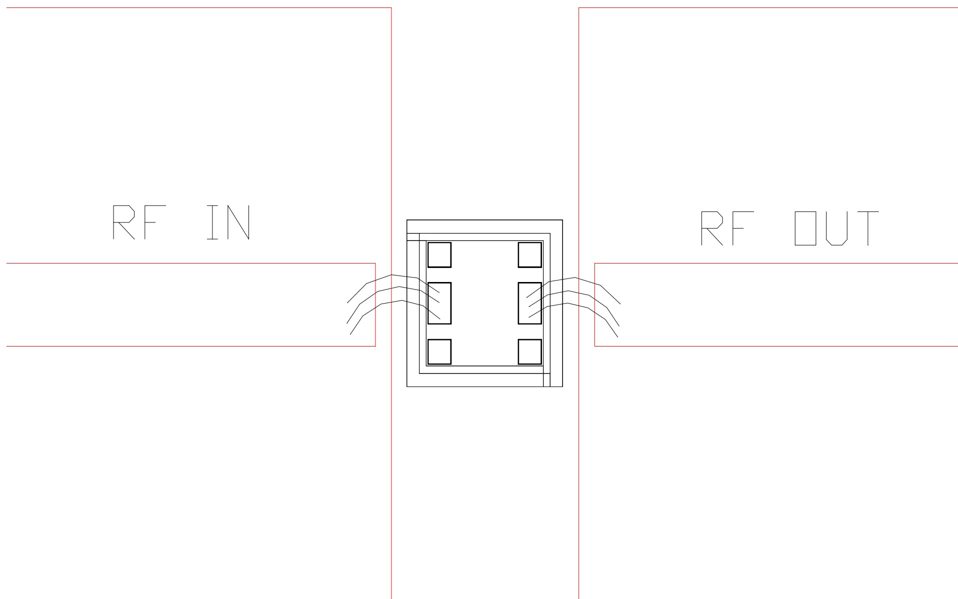
Units: millimeters (inches)
Thickness: 0.100 (0.004)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.051 (0.002)

Bond Pad	Function	Size (mm)	Size (in)
Bond Pad #1:	(RF In)	0.075 x 0.125	(0.003 x 0.005)
Bond Pad #2:	(N/C)*	0.075 x 0.075	(0.003 x 0.003)
Bond Pad #3:	(N/C)*	0.075 x 0.075	(0.003 x 0.003)
Bond Pad #4:	(RF Out)	0.075 x 0.125	(0.003 x 0.005)
Bond Pad #5:	(N/C)*	0.075 x 0.075	(0.003 x 0.003)
Bond Pad #6:	(N/C)*	0.075 x 0.075	(0.003 x 0.003)

* Note: GND is back side of MMIC

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Chip Assembly Diagram



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