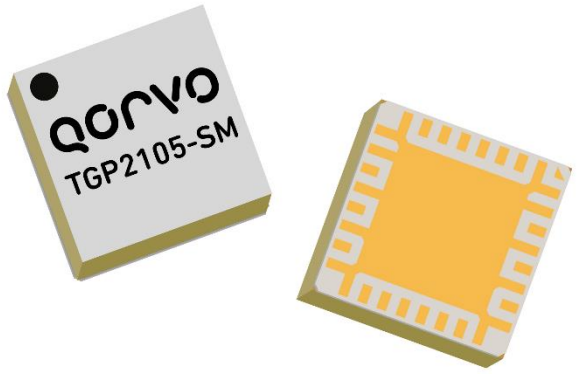
TGP2105-SM

6 - 18 GHz 6-Bit Digital Phase Shifter (+Vc)

Product Description

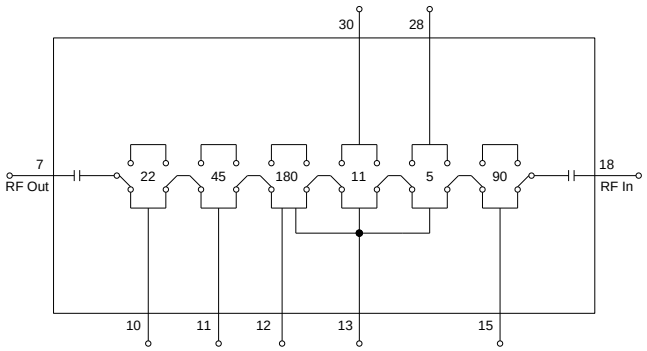
The Qorvo TGP2105-SM is a packaged 6-bit digital phase shifter fabricated on Qorvo's high performance 0.15 um GaAs pHEMT process. It operates over 6 to 18 GHz while providing 360° of phase coverage with a LSB of 5.625°. It also achieves a low RMS phase error of 4° with 8 dB of insertion loss over all states.

The TGP2105-SM uses positive switch logic, eliminating the need for a negative voltage rail. That, along with low insertion and a high degree of resolution makes the TGP2105-SM ideally suited for a variety of wideband phased array applications, including commercial and military radars, satellite-based communication systems and electronic warfare.



Air Cavity Ceramic QFN 5x5 mm 32L

Functional Block Diagram



Product Features

- Frequency Range: 6 to 18 GHz
- 6-Bit Digital Phase Shifter
- 360° Coverage, LSB = 5.625°
- RMS Phase Error: 4°
- RMS Amplitude Error: 0.45 dB
- Insertion Loss: <10 dB
- Return Loss: >12 dB
- Input P1dB: >25 dBm
- Input IP3: >41 dBm
- Control Voltage: 0/+5V
- QFN Package Dimensions: 5.0 x 5.0 x 1.45 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Applications

- Phased Array Antenna Systems
- Satellite Communication Systems
- Electronic Warfare

Ordering Information

Part No.	Description
TGP2105-SM	6-18 GHz 6-Bit Digital Phase Shifter
TGP2105-SMEVB01	TGP2105-SM Evaluation Board

Absolute Maximum Ratings

Parameter	Value
Control and Reference Voltage	6 V
Control Current	-15 to +5 mA
Power Dissipation	0.9 W
Input Power, CW, 50 Ω, 85°C	30 dBm
Channel Temperature	200 °C
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	-55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Extended application of Absolute Maximum Rating conditions may reduce device reliability.

Recommended Operating Conditions

Parameter	Value
Control Voltage (5^0, 11^0, 22^0, 45^0, 90^0, 180^0, REF)	0/+5 V
Operating Temperature Range	-40 ºC to +85 ºC

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed overall operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25 ºC. Control Voltage (REF, 5º, 11º, 22º, 45º, 90º, 180º) = 0/+5 V; See Bias Truth Table.

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		6		18	GHz
Insertion Loss			6 - 10		dB
Input Return Loss			>12		dB
Output Return Loss			>12		dB
RMS Phase Error			4		deg
RMS Amplitude Error			0.45		dB
Input P1dB			> 25		dBm
Input IP3	Tone Spacing = 10 MHz, Pin/Tone = 15 dBm		> 41		dBm
Insertion Loss Temperature Coefficient			0.008		dB/°C

Bias Truth Table

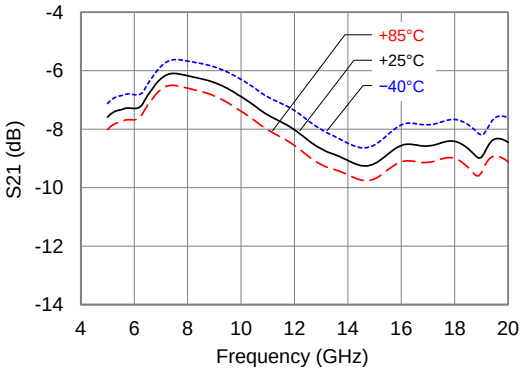
Logic “0” = 0 V, Logic “1” = +5 V
Voltage for Logic “1” of V_{CTRL} (5º, 11º, 22º, 45º, 90º, 180º) must be the same with V_{REF}

Phase Shifter	5^0	11^0	22^0	45^0	90^0	180^0	REF
0° (Reference)	0	0	0	0	0	0	1
5°	1	0	0	0	0	0	1
11°	0	1	0	0	0	0	1
22°	0	0	1	0	0	0	1
45°	0	0	0	1	0	0	1
90°	0	0	0	0	1	0	1
180°	0	0	0	0	0	1	1
355°	1	1	1	1	1	1	1

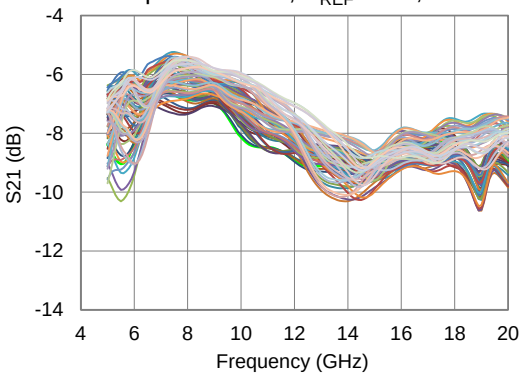
Performance Plots – Small Signal

Test conditions unless otherwise noted: 25 °C. Data de-embedded to device reference planes

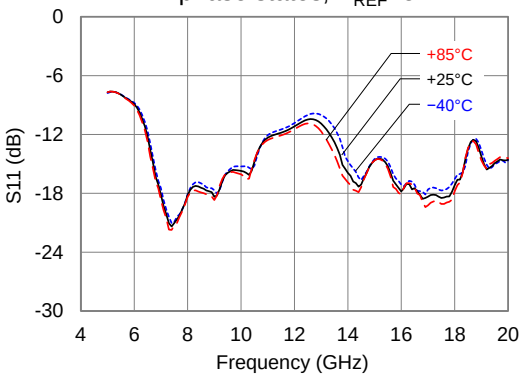
Average Insertion Loss vs. Temperature
All phase states; V_{REF} = 5 V



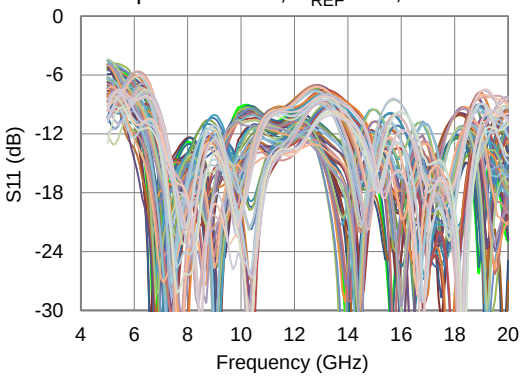
Insertion Loss vs. Frequency
All phase states; V_{REF} = 5 V, 25 °C



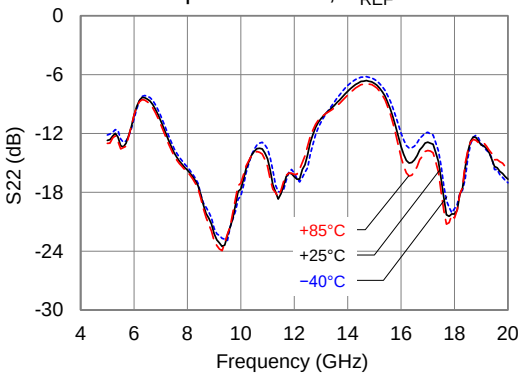
Average IRL vs. Temperature
All phase states; V_{REF}=5 V



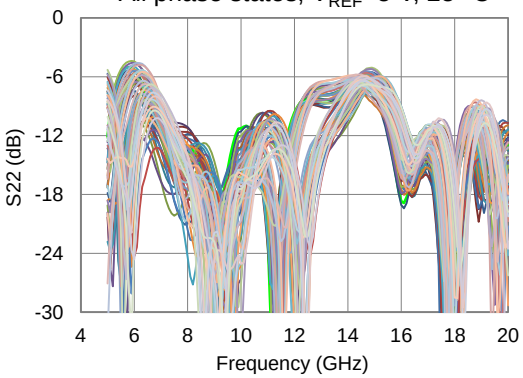
Input Return Loss vs. Frequency
All phase states; V_{REF}=5 V, 25 °C



Average ORL vs. Temperature
All phase states; V_{REF}=5 V



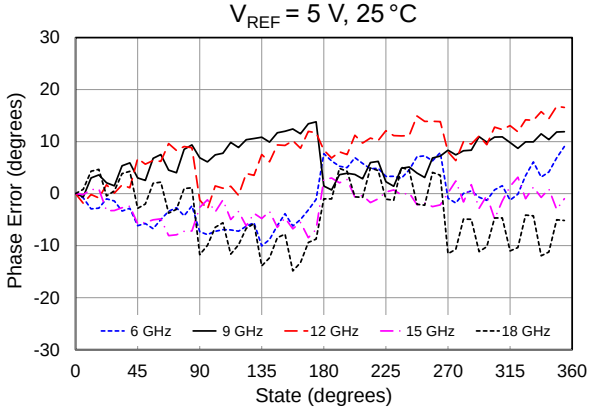
Output Return Loss vs. Frequency
All phase states; V_{REF}=5 V, 25 °C



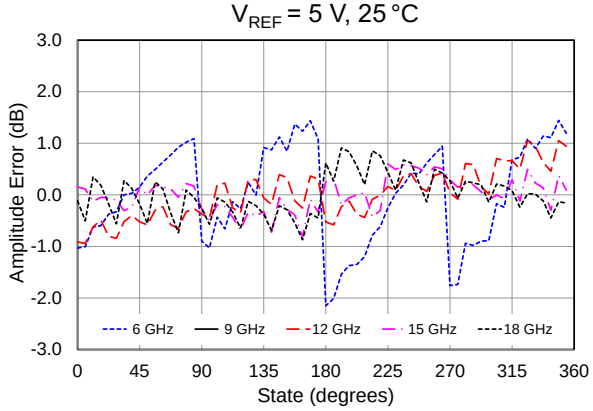
Performance Plots – Small Signal

Test conditions unless otherwise noted: 25 °C. Data de-embedded to device reference planes

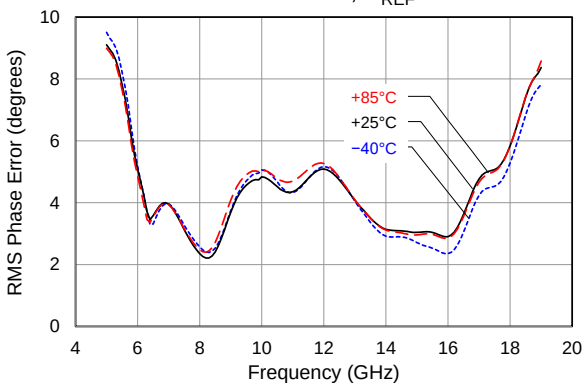
Phase Error vs. State
V_{REF} = 5 V, 25 °C



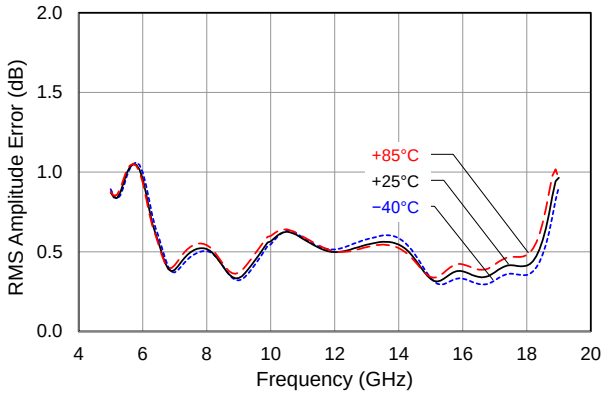
Amplitude Error vs. State
V_{REF} = 5 V, 25 °C



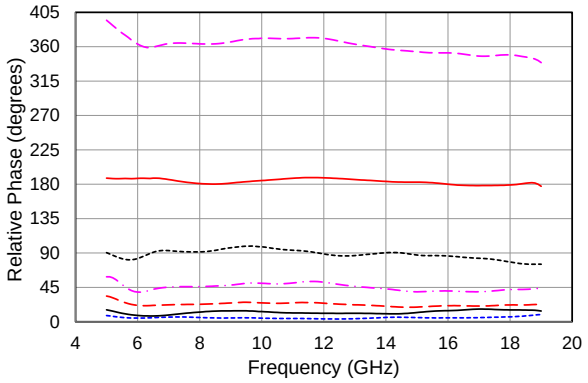
RMS Phase Error vs. Frequency
All Phase States, V_{REF} = 5 V



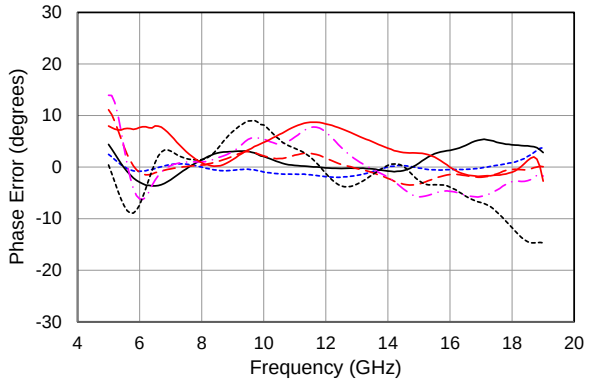
RMS Amplitude Error vs. Frequency
All Phase States, V_{REF} = 5 V



Relative Phase Shift vs. Frequency
Major States, V_{REF} = 5 V, 25 °C



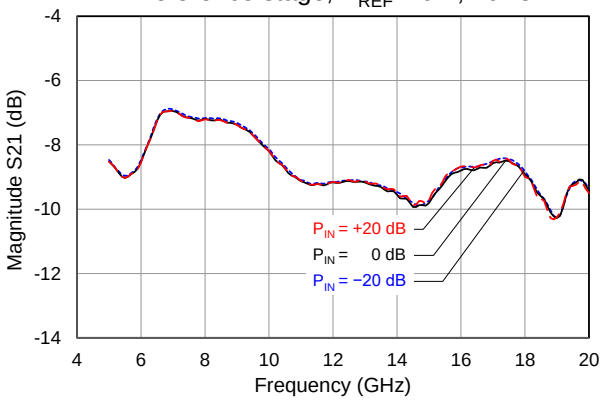
Phase Error vs. Frequency
Major States, V_{REF} = 5 V, 25 °C



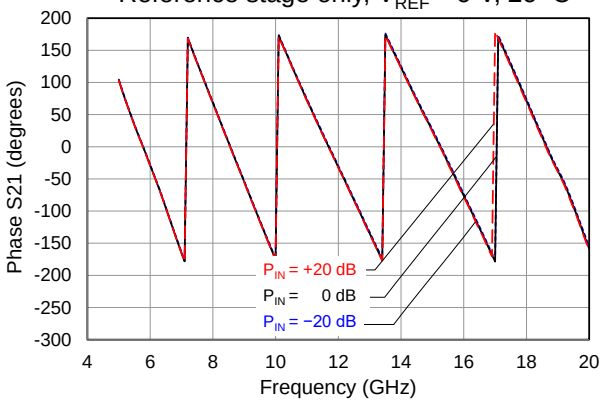
Performance Plots – Small Signal

Test conditions unless otherwise noted: 25 °C. Data de-embedded to device reference planes

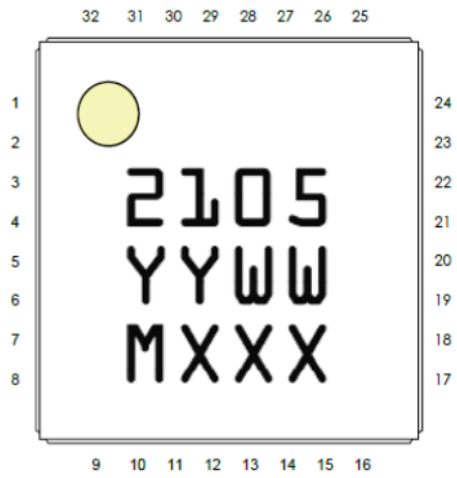
Insertion Loss vs. Freq. vs. P_{IN} (AM/AM)
Reference stage, V_{REF} = 5 V, 25 °C

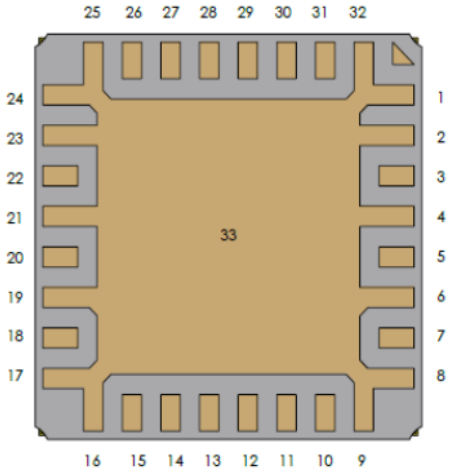


Insertion Loss vs. Freq. vs. P_{IN} (AM/PM)
Reference stage only, V_{REF} = 5 V, 25 °C



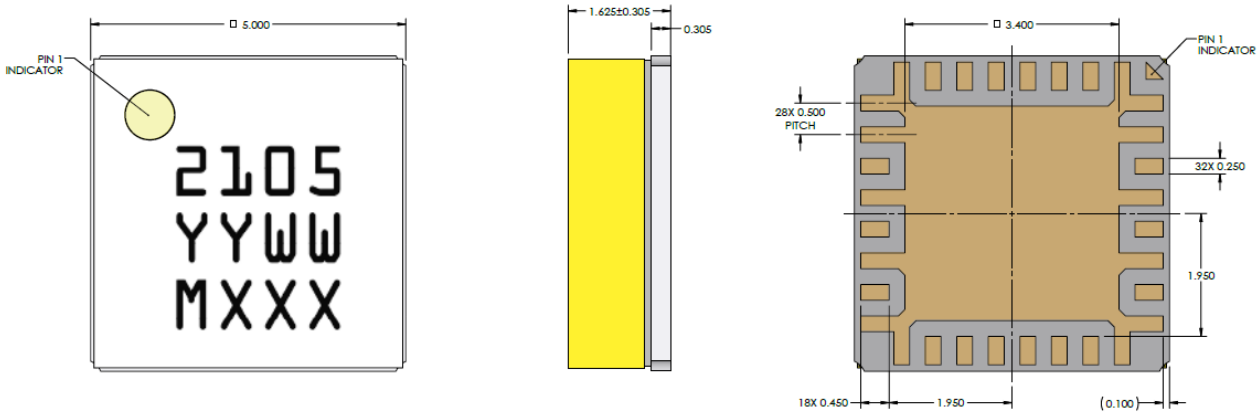
Package Pin Descriptions





Package Pad	Symbol	Description
1 - 6, 8 - 9, 14, 16,17, 19 - 27, 29, 31 - 32	GND	Internal grounding; must be grounded on PCB
7	RF Out	Output; matched to 50 Ohms; DC blocked
10	22°	22° Bit; De-Qing network is not required
11	45°	45° Bit; De-Qing network is not required
12	180°	180° Bit; De-Qing network is not required
13	REF	Reference; De-Qing network is not required
15	90°	90° Bit; De-Qing network is not required
18	RF In	Input; matched to 50 Ohms; DC blocked
28	5°	5° Bit; De-Qing network is not required
30	11°	11° Bit; De-Qing network is not required
33	GND	On PCB; multiple vias should be employed under the center pad (33) to minimize inductance and thermal resistance; see page 8 for suggested vias layout

Package Mechanical Drawing and Dimensions

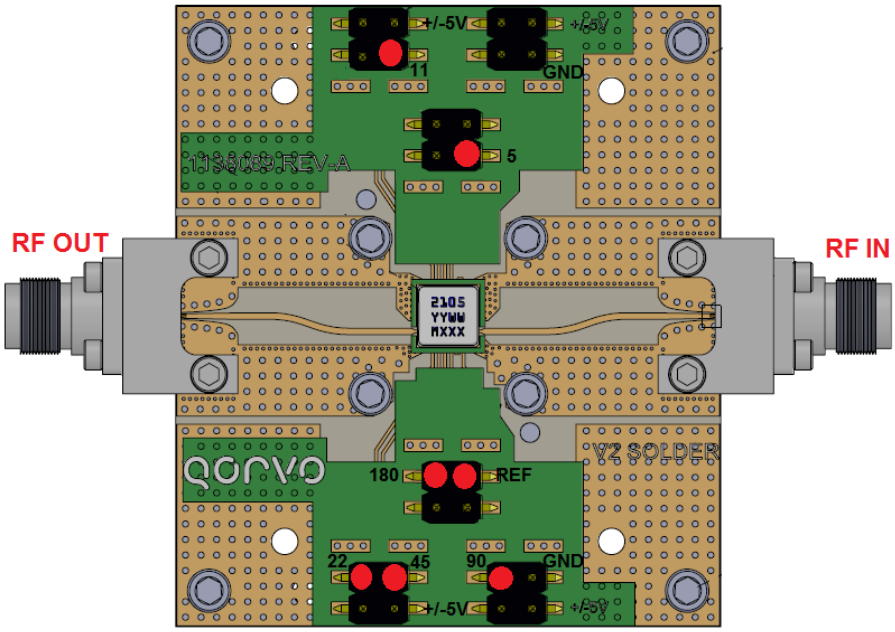


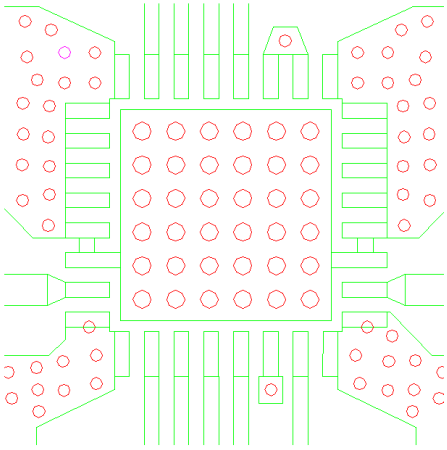
TOP VIEW SIDE VIEW BOTTOM VIEW

Package lead finish:
Ni / Au plating with minimum gold thickness of 0.5 µm
Materials:
Base: Ceramic, Lid: Laminate, Part is epoxy sealed
Part Marking:
2105 = Part Number, YY = Part Assembly Year, WW = Part Assembly Week, MXXX = Batch ID

Unless otherwise specified dimensions are in mm.
Tolerances: XXX = ± 0.127

Evaluation Board (EVB) Layout Assembly





Via Pattern

RF layer is 0.010” thick Rogers RO4350. Metal layers are 1-oz copper. The microstrip line taper at the connector interface is optimized for the Southwest Microwave end-launch connector 1092-01A-5.

Ground / thermal vias under the DUT are critical for the proper performance of this device. The PCB shown herein utilizes copper filled vias under the DUT.

The pad pattern shown has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company careful process development is recommended.

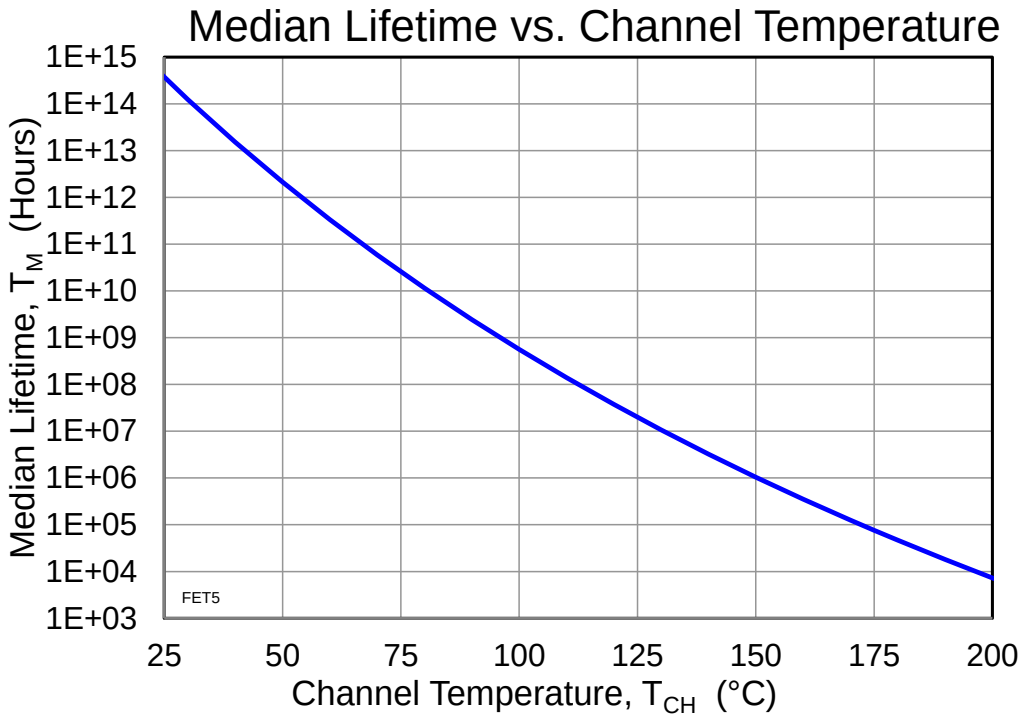
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	P_{DISS} = 0.09 W, T_{BASE} = 85°C	22	ºC/W
Channel Temperature (T_{CH}) (2)		87	°C
Median Lifetime (T_M)		3.8E+9	Hrs

Notes:
1. Thermal resistance measured to back of package.
2. Under normal (lifetime) operating conditions, self-heating is not a significant contributor to channel temperature.

Median Lifetime

Test Conditions: 6.0 V; Failure Criterion = 10% reduction in I_{DQ_MAX}



Assembly Notes

Compatible with both lead-free (260°C peak reflow temp.) and tin/lead (245°C peak reflow temp.) soldering processes.

This package is air-cavity and non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing after soldering is highly recommended.

Solder rework not recommended.

Contact plating: Ni-Au.

Recommended Soldering Temperature Profile