TGP2109-SM

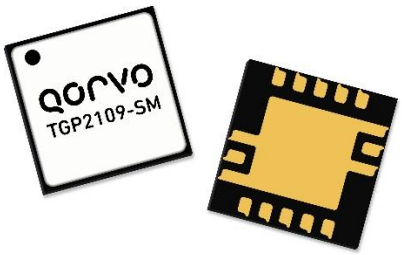
8 - 12 GHz 6-Bit Digital Phase Shifter

Product Description

Qorvo's TGP2109-SM is a packaged 6-bit digital phase shifter fabricated on Qorvo's high performance 0.15µm GaAs pHEMT process. It operates over 8 to 12 GHz and provides 360° of phase coverage with a LSB of 5.625°. It also achieves a low RMS phase error of 4° with 6 dB of insertion loss.

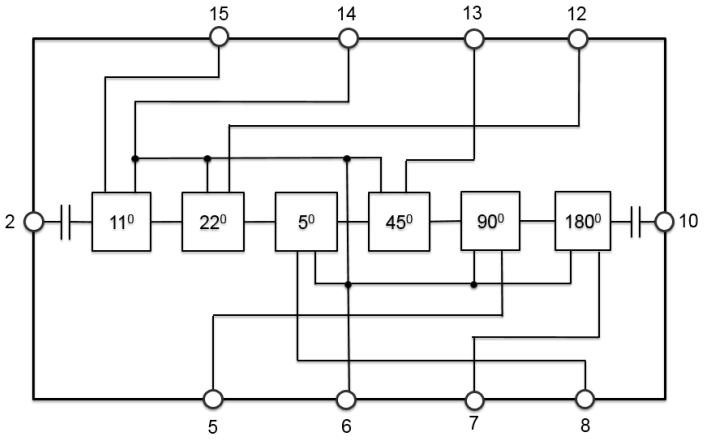
The TGP2109-SM was developed for simple system integration. It uses positive only switch logic eliminating the need for a negative voltage rail. In addition, both ports are matched to 50 ohms with DC blocking capacitors. Ease of use along with low insertion loss and a high degree of resolution makes the TGP2109-SM ideally suited for a variety of x-band phased array applications including commercial and military radars and phase array communication systems.

The device is lead-free and RoHS compliant.



QFN 4x4 mm 16L

Functional Block Diagram



Product Features

- Frequency Range: 8 to 12 GHz
- 6-Bit Digital Phase Shifter
- Bi-Directional
- 360° Coverage, LSB = 5.625°
- RMS Phase Error: 4°
- RMS Amplitude Error: 0.5 dB
- Insertion Loss: 6 dB
- Return Loss: 10 dB IRL; 15 dB ORL
- Input P1dB: 29 dBm
- Input IP3: >40 dBm
- IM3: <-50 dBc
- Control Voltage: VL: 0V to +0.2V, VH: +3V to +5V
- QFN Package Dimensions: 4.0 x 4.0 x 1.64 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Applications

- X-Band Radar
- Satellite Communication Systems

Ordering Information

Part No.	Description
TGP2109-SM	8-12 GHz 6-Bit Digital Phase Shifter
TGP2109-SM EVB	TGP2109-SM Evaluation Board

Absolute Maximum Ratings

Parameter	Value
Control and Reference Voltage	6 V
Control Current	0.5 mA
Power Dissipation	1.5 W
Input Power, CW, 50 Ω, 85°C	33 dBm
Channel Temperature	200 °C
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	-55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Extended application of Absolute Maximum Rating conditions may reduce device reliability.

Recommended Operating Conditions

Parameter	Value
Control Voltage VH	+3 V to + 5 V
Control Voltage VL	0 V to + 0.2 V
Control Current (Total)	< 100 µA
Temperature Range	-40 to +85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed overall operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25°C. Control Voltage: VL = 0 V, VH = +5 V, see Bias Truth Table.

Parameter	Min	Typical	Max	Units
Operational Frequency Range	8		12	GHz
Insertion Loss		6		dB
Input Return Loss		10		dB
Output Return Loss		15		dB
RMS Phase Error		4		deg
RMS Amplitude Error		0.5		dB
Input P1dB		29		dBm
Input IP3 (Tone Spacing = 10 MHz, Pin/Tone = 16 dBm)		> 40		dBm
IM3 (Tone Spacing = 10 MHz, Pin/Tone = 16 dBm)		< -50		dBc
Insertion Loss Temperature Coefficient		0.004		dB/°C

Bias Truth Table

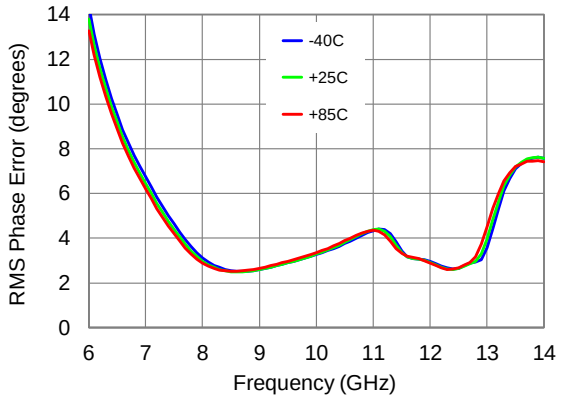
Logic “0” = VL, value from 0 to +0.2 V; Logic “1” = VH = VREF, value from +3 V to +5 V

Phase Shifter	B1	B2	B3	B4	B5	B6	VREF
0° (Reference)	0	0	1	1	1	1	1
5°	1	0	1	1	1	1	1
11°	0	1	1	1	1	1	1
22°	0	0	0	1	1	1	1
45°	0	0	1	0	1	1	1
90°	0	0	1	1	0	1	1
180°	0	0	1	1	1	0	1
355°	1	1	0	0	0	0	1

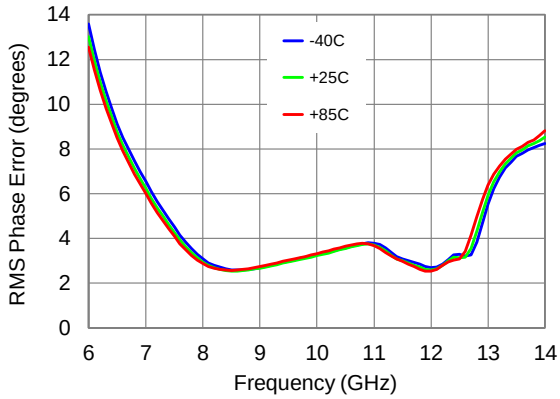
Performance Plots – Small Signal

Test conditions unless otherwise noted: 25 °C. Data de-embedded to device reference planes

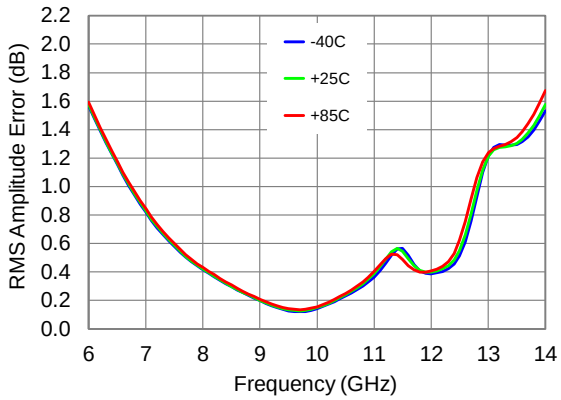
RMS Phase Error vs. Freq. vs. Temp
VL = 0 V, VH = 5 V, All Phase States



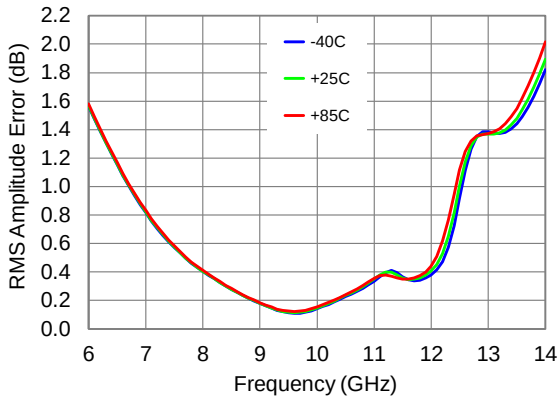
RMS Phase Error vs. Freq. vs. Temp
VL = 0 V, VH = 3 V, All Phase States



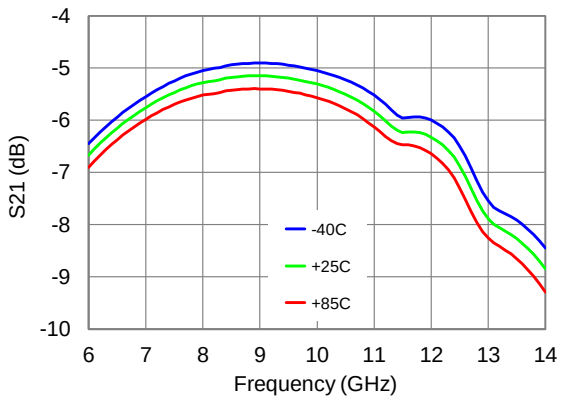
RMS Amplitude Error vs. Freq vs. Temp.
VL = 0 V, VH = 5 V, All Phase States



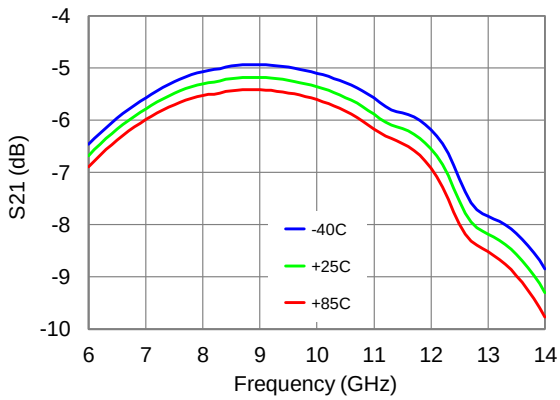
RMS Amplitude Error vs. Freq vs. Temp.
VL = 0 V, VH = 3 V, All Phase States



Avg. Insertion Loss vs. Freq. vs. Temp.
VL = 0 V, VH = 5 V, All Phase States



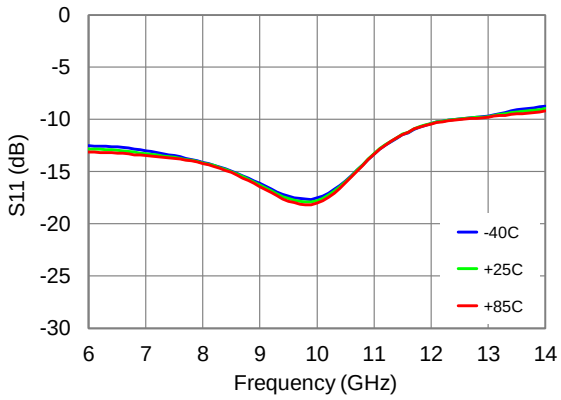
Avg. Insertion Loss vs. Freq. vs. Temp.
VL = 0 V, VH = 3 V, All Phase States



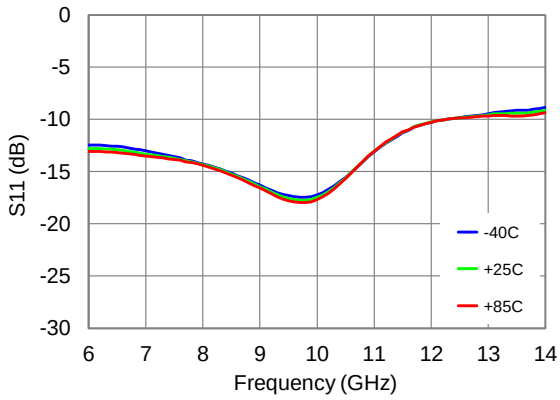
Performance Plots – Small Signal

Test conditions unless otherwise noted: 25 °C. Data de-embedded to device reference planes

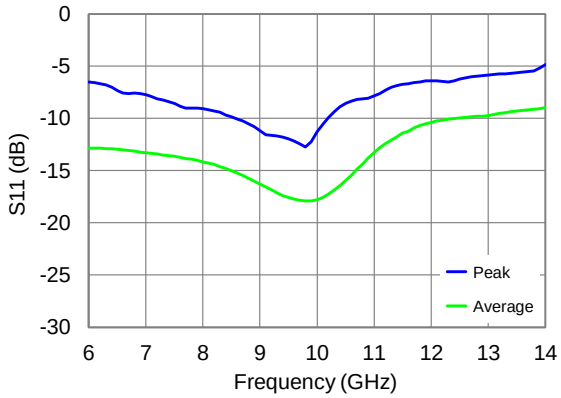
Avg. IRL vs. Freq. vs.Temp.
VL = 0 V, VH = 5 V, All Phase States



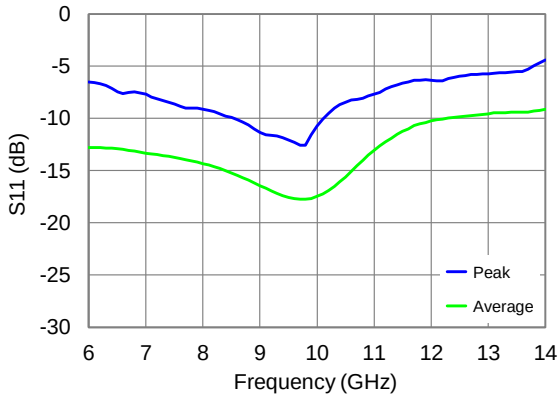
Avg. IRL vs. Freq. vs.Temp.
VL = 0 V, VH = 3 V, All Phase States



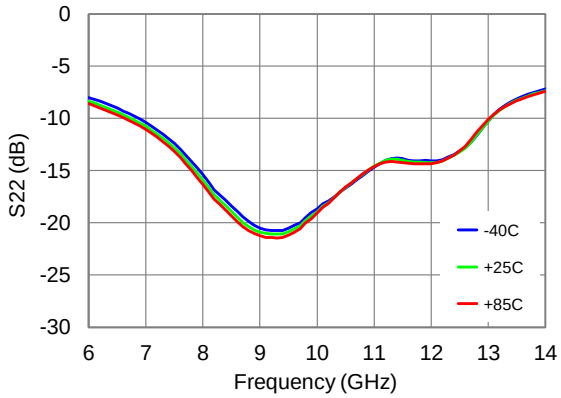
IRL vs. Freq.
VL = 0 V, VH = 5 V, All Phase States



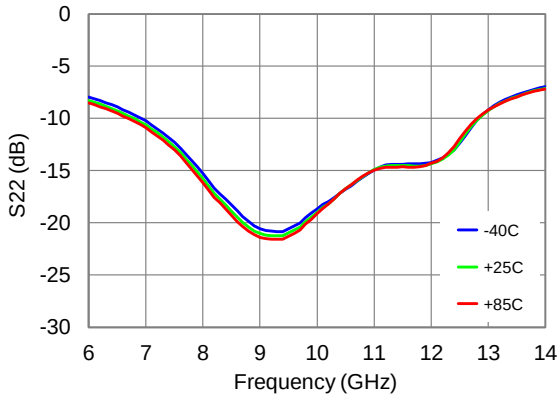
IRL vs. Freq.
VL = 0 V, VH = 3 V, All Phase States



Avg. ORL vs. Freq. vs. Temp
VL = 0 V, VH = 5 V, All Phase States

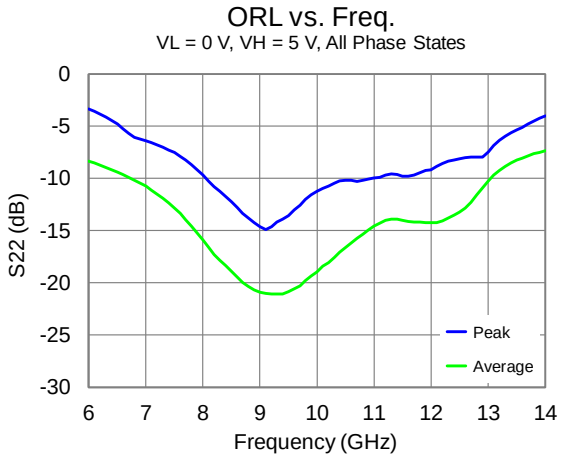


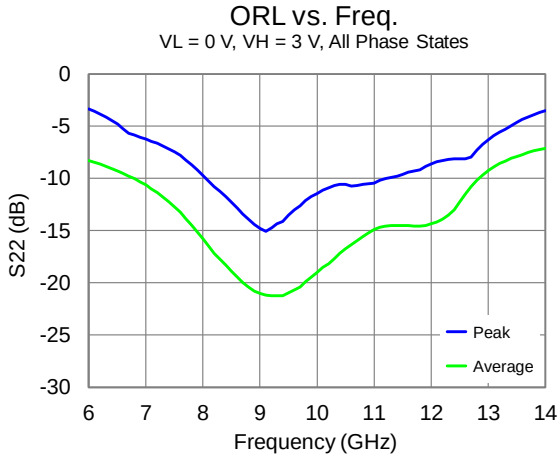
Avg. ORL vs. Freq. vs. Temp
VL = 0 V, VH = 3 V, All Phase States



Performance Plots – Small Signal

Test conditions unless otherwise noted: 25 °C. Data de-embedded to device reference planes

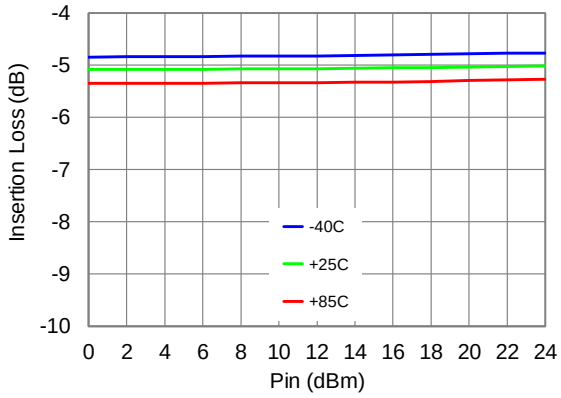




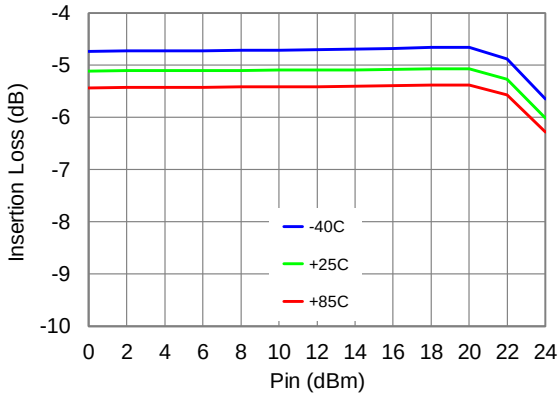
Performance Plots – Large Signal

Test conditions unless otherwise noted: Freq = 10 GHz, 25 °C. Data de-embedded to device reference planes

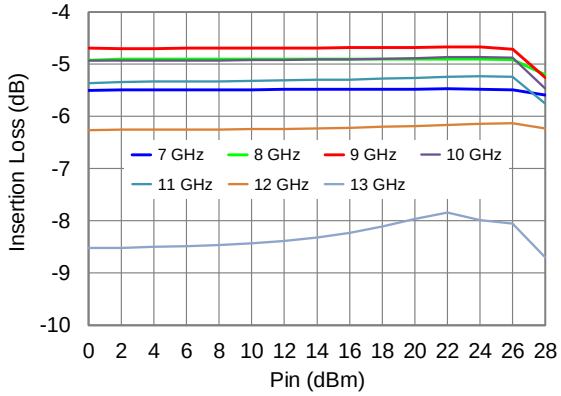
Insertion Loss vs. Pin vs. Temperature
VL = 0 V, VH = 5 V, Phase State = 0 deg



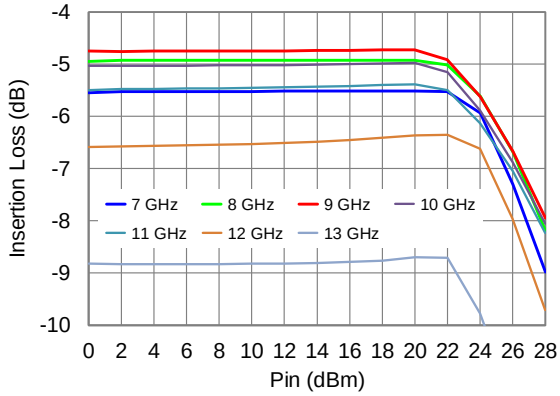
Insertion Loss vs. Pin vs. Temperature
VL = 0 V, VH = 3 V, Phase State = 0 deg



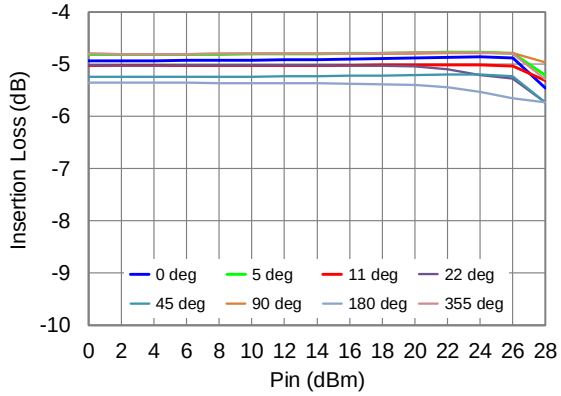
Insertion Loss vs. Pin vs. Frequency
VL = 0 V, VH = 5 V, Phase State = 0 deg



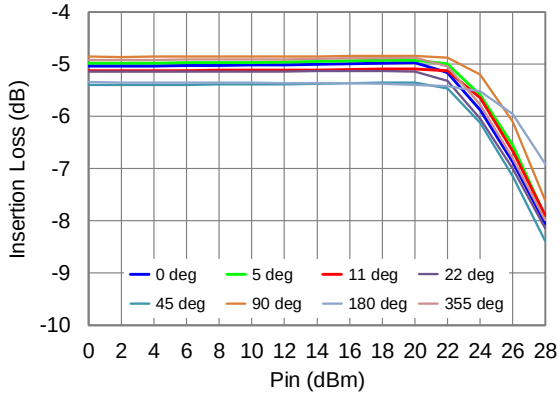
Insertion Loss vs. Pin vs. Frequency
VL = 0 V, VH = 3 V, Phase State = 0 deg



Insertion Loss vs. Pin
VL = 0 V, VH = 5 V, Major Phase States



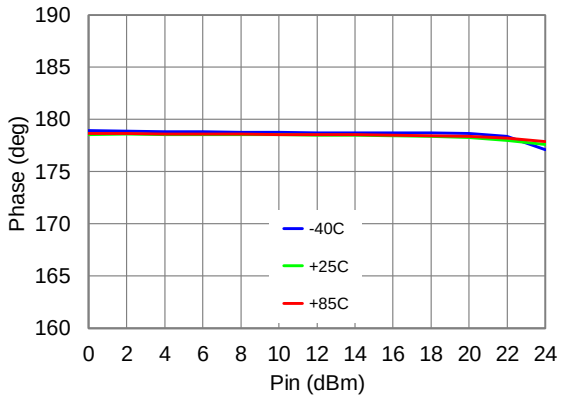
Insertion Loss vs. Pin
VL = 0 V, VH = 3 V, Major Phase States



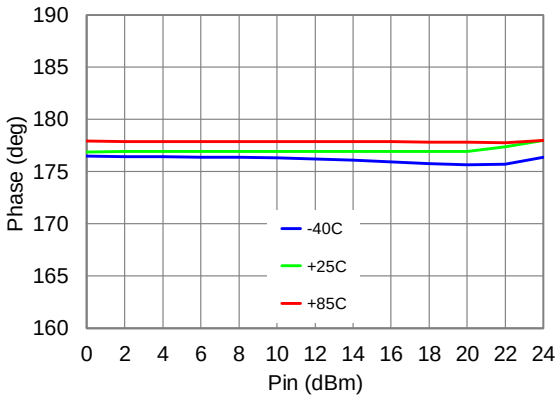
Performance Plots – Large Signal

Test conditions unless otherwise noted: Freq = 10 GHz, 25 °C. Data de-embedded to device reference planes

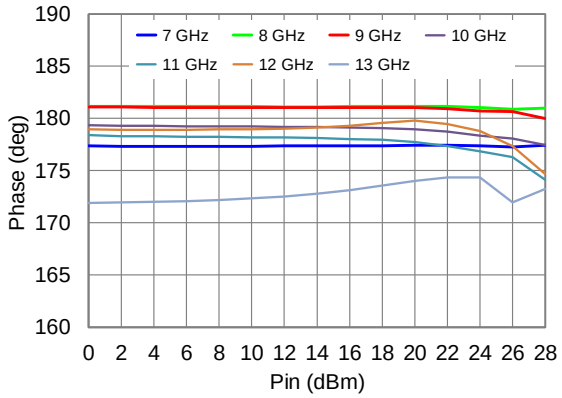
Phase vs. Pin vs. Temperature
VL = 0 V, VH = 5 V, Phase State = 180 deg



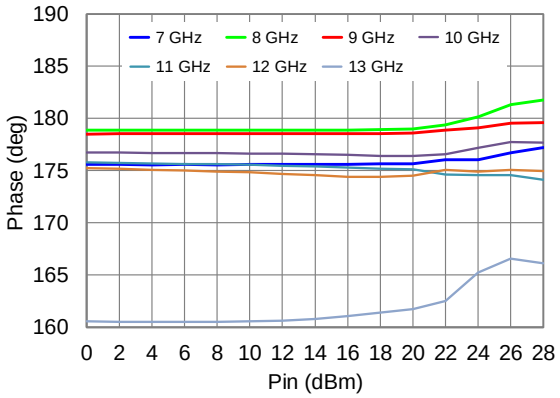
Phase vs. Pin vs. Temperature
VL = 0 V, VH = 3 V, Phase State = 180 deg



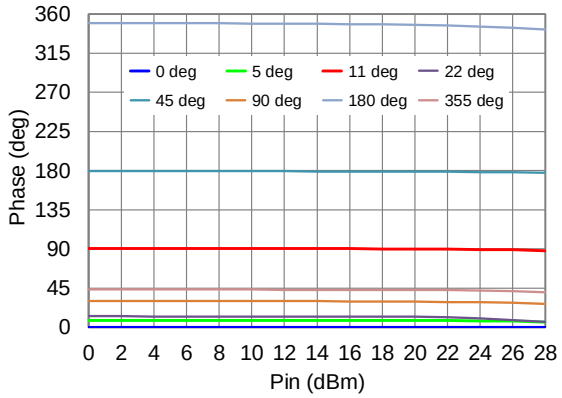
Phase vs. Pin vs. Frequency
VL = 0 V, VH = 5 V, Phase State = 180 deg



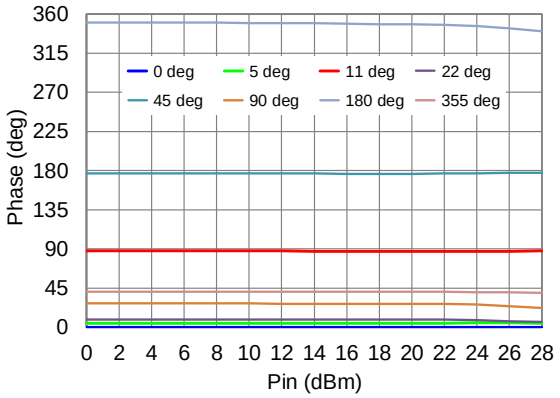
Phase vs. Pin vs. Frequency
VL = 0 V, VH = 3 V, Phase State = 180 deg



Phase vs. Pin
VL = 0 V, VH = 5 V, Major Phase States



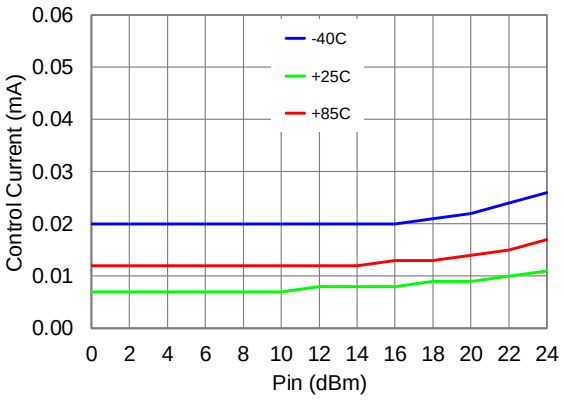
Phase vs. Pin
VL = 0 V, VH = 3 V, Major Phase States



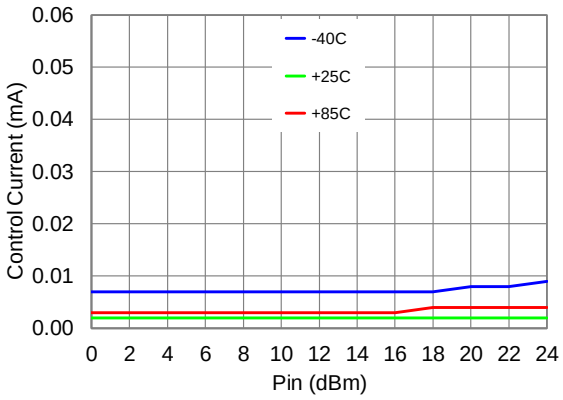
Performance Plots – Large Signal

Test conditions unless otherwise noted: Total current of VH, Freq = 10 GHz, 25 °C

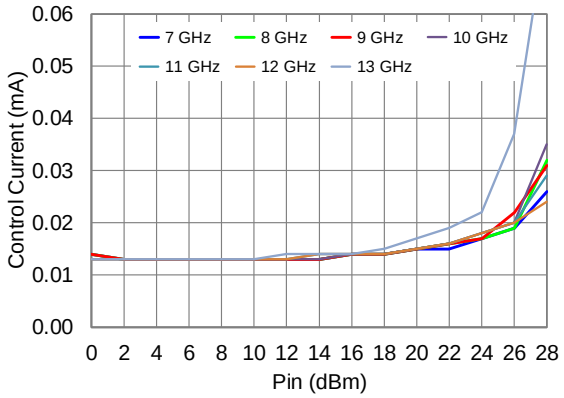
Control Current vs. Pin vs. Temperature
VL = 0 V, VH = 5 V, Phase State = 0 deg



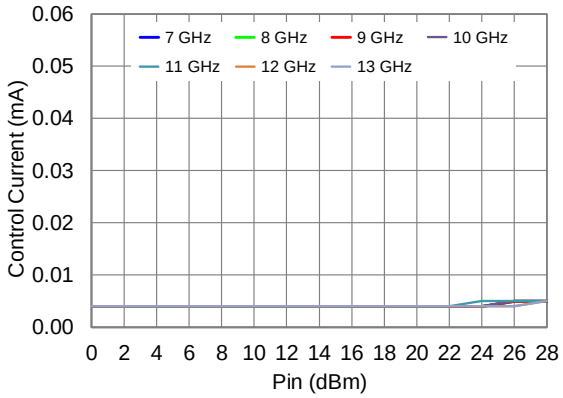
Control Current vs. Pin vs. Temperature
VL = 0 V, VH = 3 V, Phase State = 0 deg



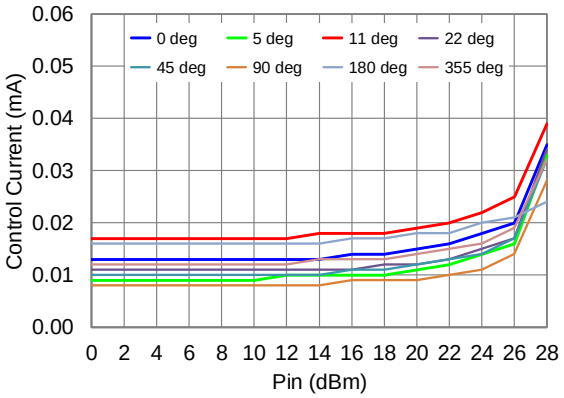
Control Current vs. Pin vs. Frequency
VL = 0 V, VH = 5 V, Phase State = 0 deg



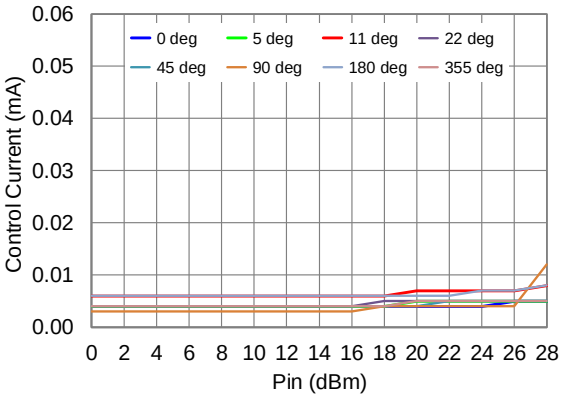
Control Current vs. Pin vs. Frequency
VL = 0 V, VH = 3 V, Phase State = 0 deg



Control Current vs. Pin vs. Phase States
VL = 0 V, VH = 5 V



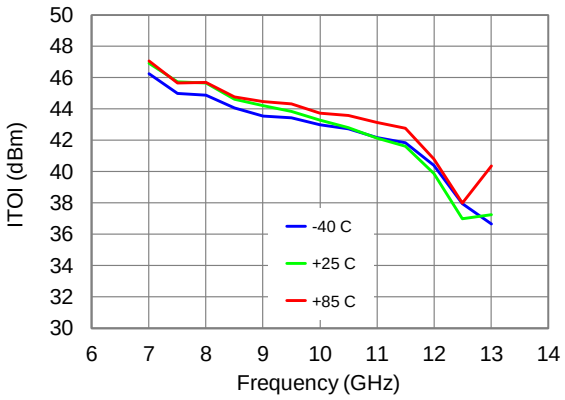
Control Current vs. Pin vs Phase States
VL = 0 V, VH = 3 V



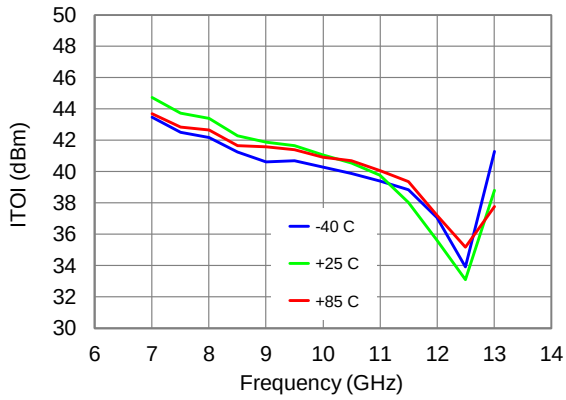
Performance Plots – Linearity

Test conditions unless otherwise noted: Tone Spacing = 10 MHz, 25 °C. Data de-embedded to device reference planes

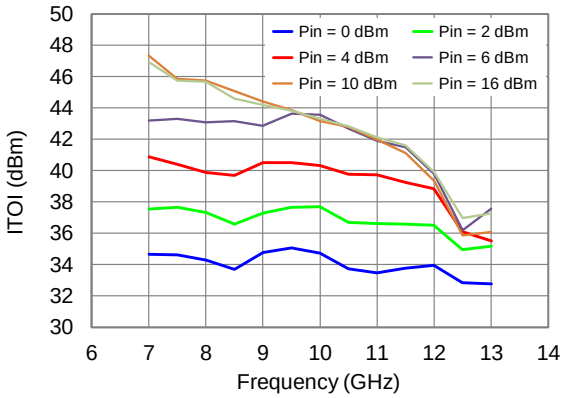
ITOI vs. Freq. vs. Temperature
VL = 0 V, VH = 5 V, Pin/Tone = 16 dBm, Phase State = 0 deg



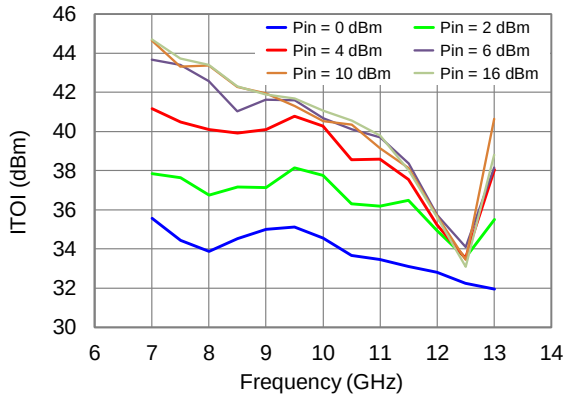
ITOI vs. Freq. vs. Temperature
VL = 0 V, VH = 3 V, Pin/Tone = 16 dBm, Phase State = 0 deg



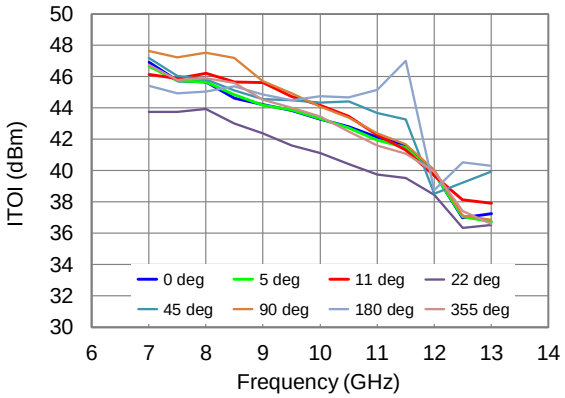
ITOI vs. Freq. vs. Pin/Tone
VL = 0 V, VH = 5 V, Phase State = 0 deg



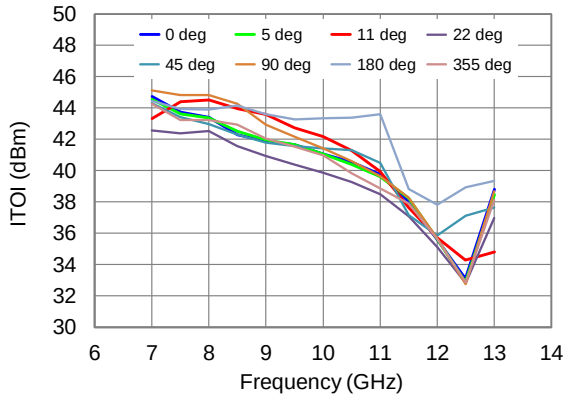
ITOI vs. Freq. vs. Pin/Tone
VL = 0 V, VH = 3 V, Phase State = 0 deg



ITOI vs. Freq. vs. Major Phase States
VL = 0 V, VH = 5 V, Pin/Tone = 16 dBm



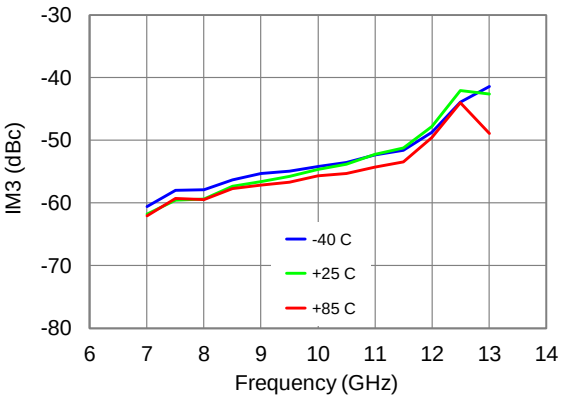
ITOI vs. Freq. vs. Major Phase States
VL = 0 V, VH = 3 V, Pin/Tone = 16 dBm



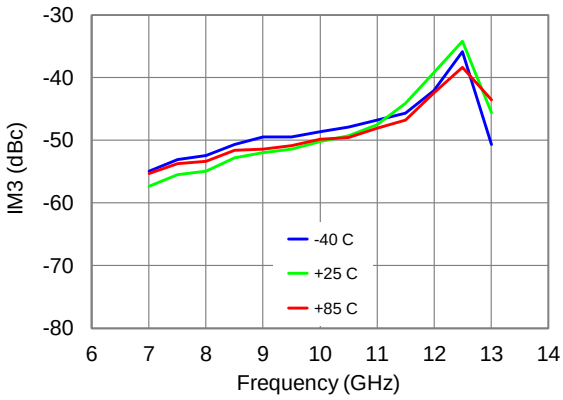
Performance Plots – Linearity

Test conditions unless otherwise noted: Tone Spacing = 10 MHz, 25 °C. Data de-embedded to device reference planes

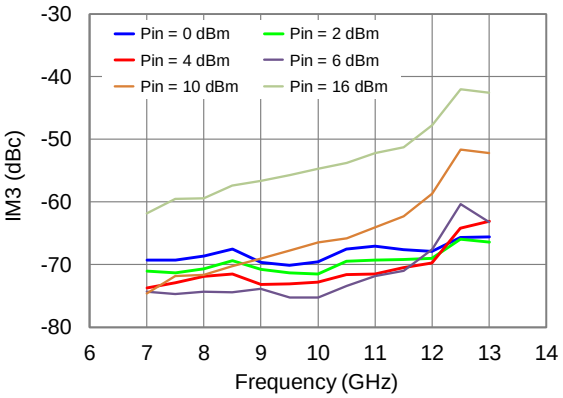
IM3 vs. Freq. vs. Temperature
VL = 0 V, VH = 5 V, Pin/Tone = 16 dBm, Phase State = 0 deg



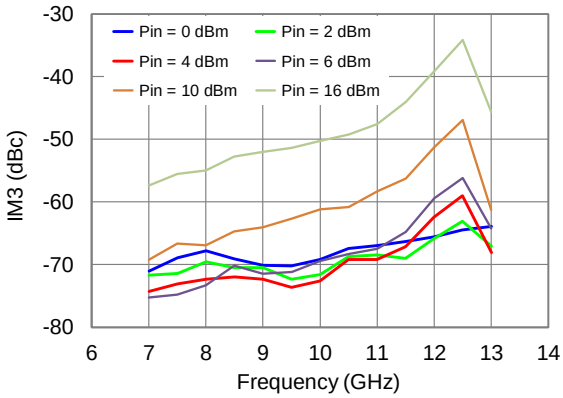
IM3 vs. Freq. vs. Temperature
VL = 0 V, VH = 3 V, Pin/Tone = 16 dBm, Phase State = 0 deg



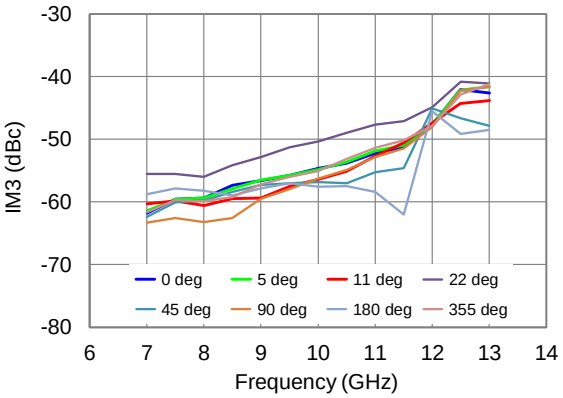
IM3 vs. Freq. vs. Pin/Tone
VL = 0 V, VH = 5 V, Phase State = 0 deg



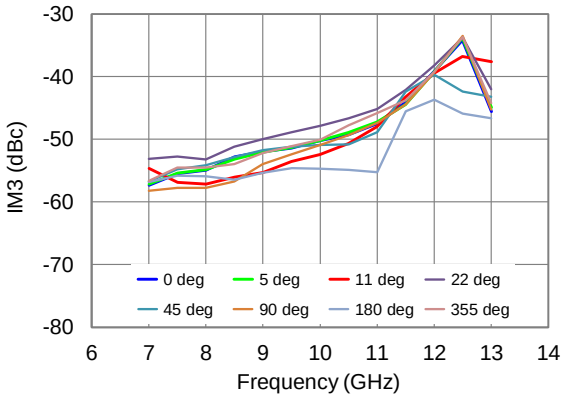
IM3 vs. Freq. vs. Pin/Tone
VL = 0 V, VH = 3 V, Phase State = 0 deg



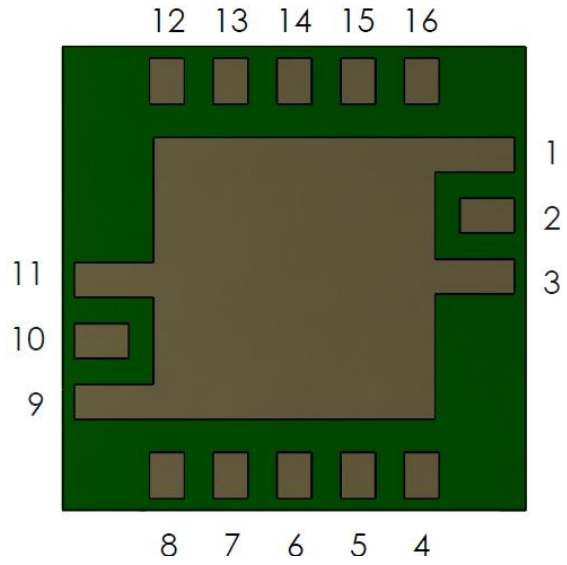
IM3 vs. Freq. vs. Major Phase States
VL = 0 V, VH = 5 V, Pin/Tone = 16 dBm



IM3 vs. Freq. vs. Major Phase States
VL = 0 V, VH = 3 V, Pin/Tone = 16 dBm

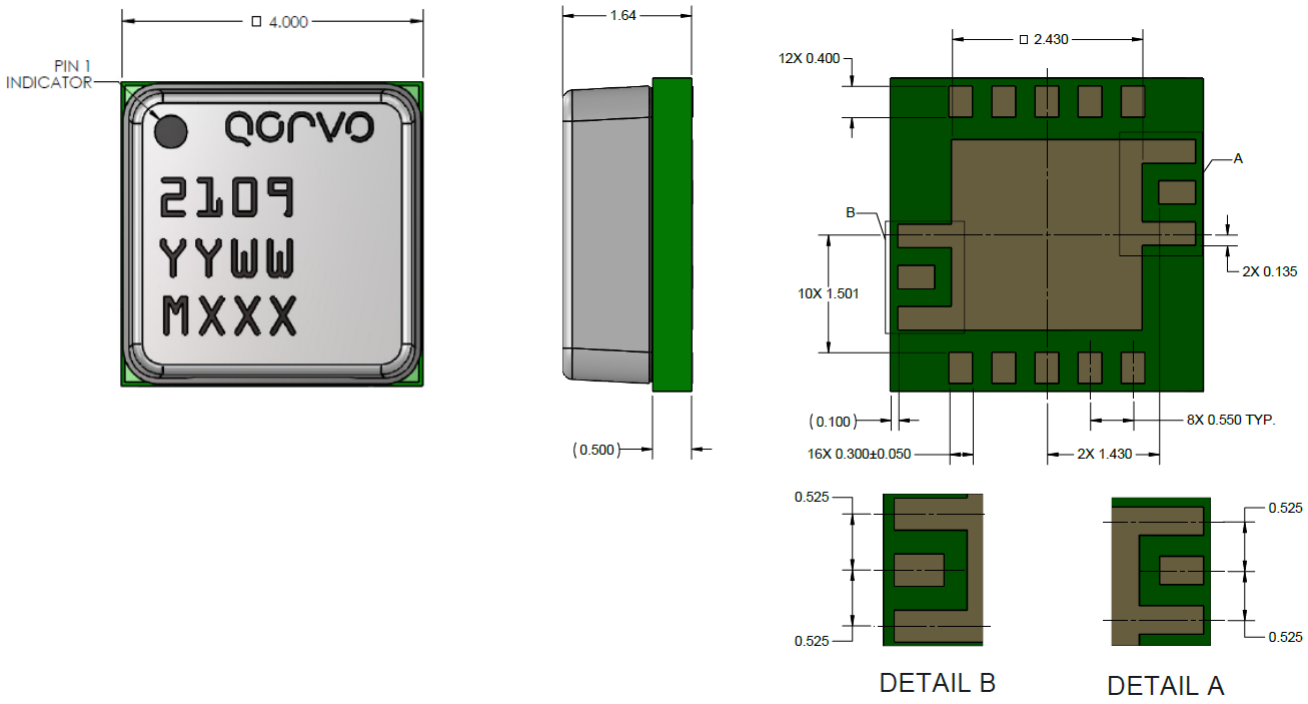


Package Pin Descriptions



Package Pad	Symbol	Description
1, 3, 9, 11	GND	Internal grounding; must be grounded on PCB
2	RF Input	Input; matched to 50 Ohms; DC blocked; interchangeable to RF Output
4, 16	N/C	No Connection; recommend GND at the EVB level
5	B5	90° Bit
6, 14	REF	Reference; VREF can be biased to either side of the package
7	B6	180° Bit
8	B1	5° Bit
10	RF Output	Output; matched to 50 Ohms; DC blocked; interchangeable to RF Input
12	B3	22° Bit
13	B4	45° Bit
15	B2	11° Bit
17 (Slug)	GND	On PCB; multiple vias should be employed under the center pad (17) to minimize inductance and thermal resistance; see page 13 for suggested vias layout

Package Mechanical Drawing and Dimensions



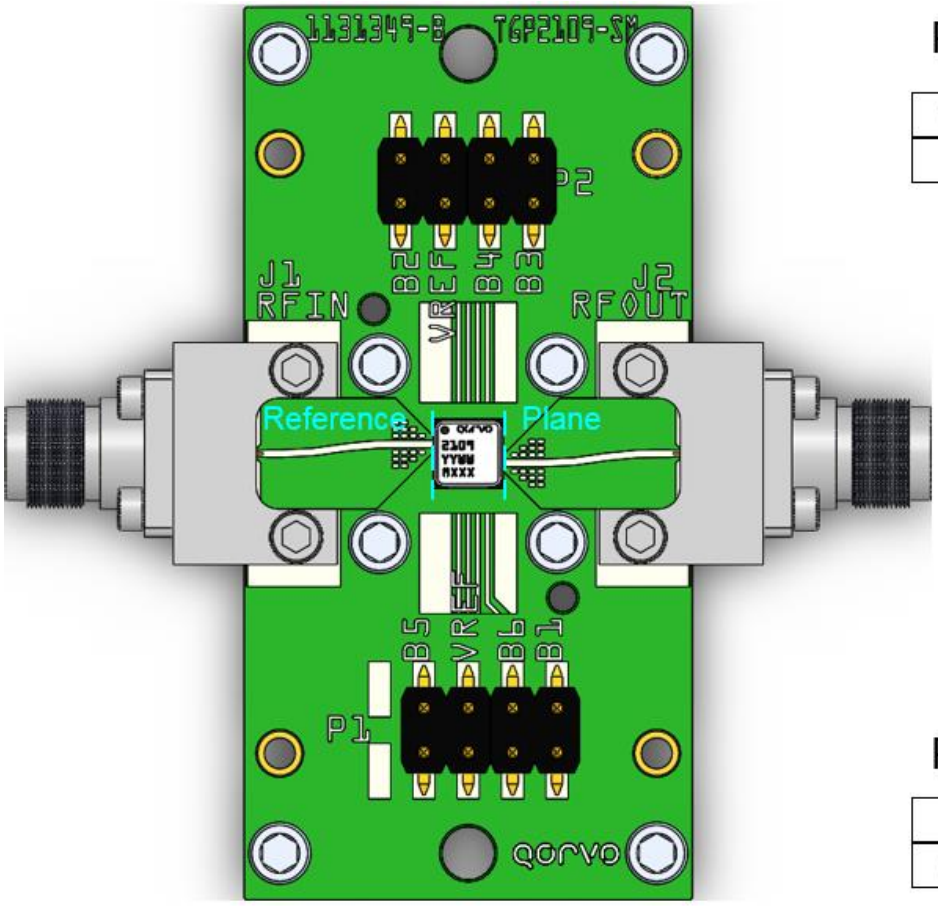
Units: mm
Tolerances: unless specified
.xx = ± 0.25
.xxx = ± 0.100
Angles = 0.5º

Materials:
Lid: Plastic
Base: Laminate
Plating: All metalized features are NiAu plated

The part is epoxy sealed

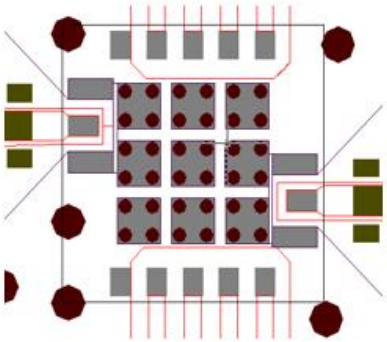
Marking:
2109: Part number
YY: Part Assembly year
WW: Part Assembly week
MXXX: Batch ID

Applications and EVB Information



P2 Connectors (Top)

GND	GND	GND	GND
B2	VREF	B4	B3



P1 Connectors (Bottom)

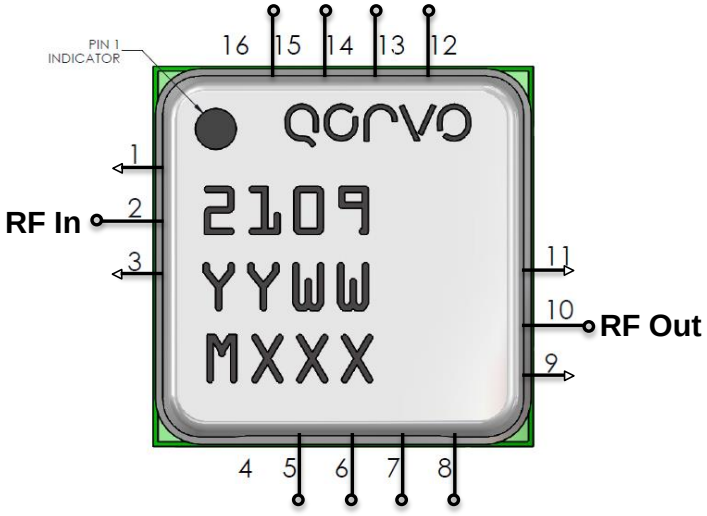
B5	VREF	B6	B1
GND	GND	GND	GND

RF layer is 0.008” thick Rogers RO4003C. Metal layers are 0.5-oz copper. The microstrip line taper at the connector interface is optimized for the Southwest Microwave end-launch connector 1092-02A-5.

Ground / thermal vias under the DUT are critical for the proper performance of this device. The PCB shown herein utilizes copper filled vias (8 mils diameter) under the DUT.

The pad pattern shown has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

De-Quing network is not required; VREF can be biased to either side of the package (pin #6 or #14).

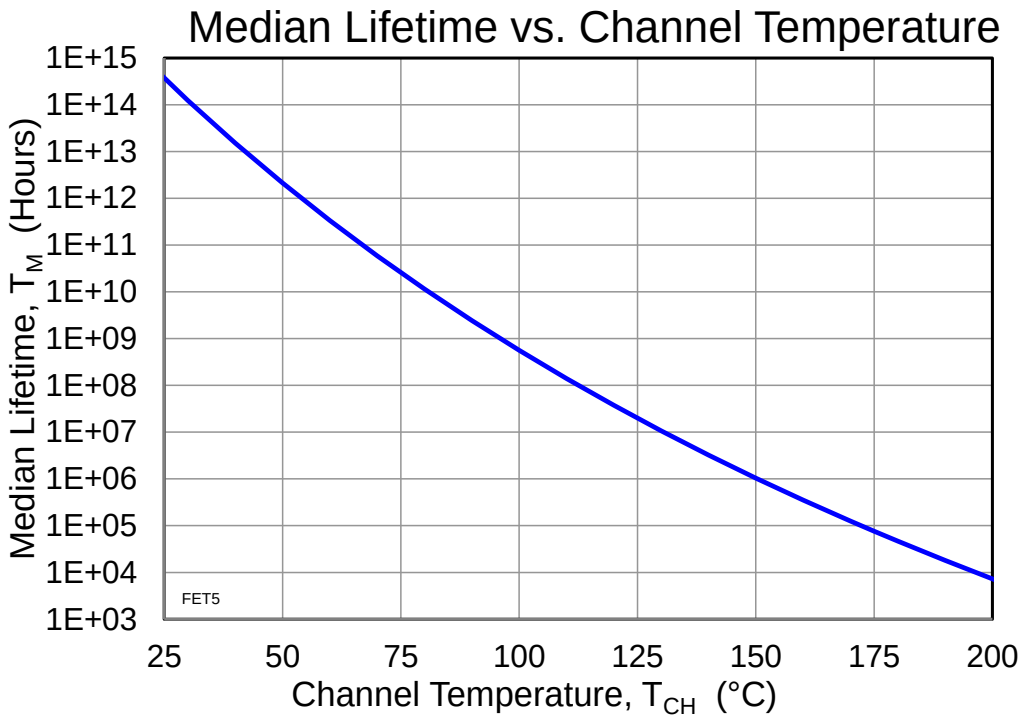


Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Channel Temperature (T_{CH})	T_{BASE} = 85°C	85	°C
Median Lifetime (T_M)		5.2E+9	Hrs

Notes:
1. Under normal (lifetime) operating conditions, self-heating is not a significant contributor to channel temperature.

Median Lifetime



Solderability

1. Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C.
2. The use of no-clean solder to avoid washing after soldering is recommended.
3. Package lead plating is NiAu.

Recommended Soldering Temperature Profile