ASYMMETRICAL-BIDIRECTIONAL THYRISTOR SPD

TISP4A270H3BJ LCAS R_{LINE} Protector

Optimized LCAS R_{LINE} Protector

TISP4A270H3BJ $V_{(BO)}$ Derived from:
-Break Switch, SW1 & SW2, Ratings
-Ring Return Switch, SW3, Rating
-Ringing Access Switch, SW4, Rating
-Switch Isolation Ratings
-Battery Voltage Range of -40 V to -60 V
-Power Fault Conditions
-Lightning Impulse Conditions
-LCAS Characteristic Temperature Range

TISP4A270H3BJ Designed for:
-Battery-Backed Ringing Circuits
Voltage Swing . . . . . .+148 V to -206 V
Allows . . . . . .103 V rms Ringing with -60 V Battery
Temperature Range . .-40 °C to +85 °C

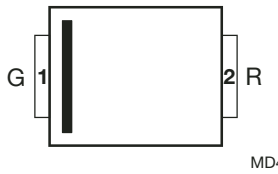
Device	V_{DRM} V	$V_{(BO)}$ V
'4A270	+160	+217
	-222	-270

Rated for International Surge Wave Shapes

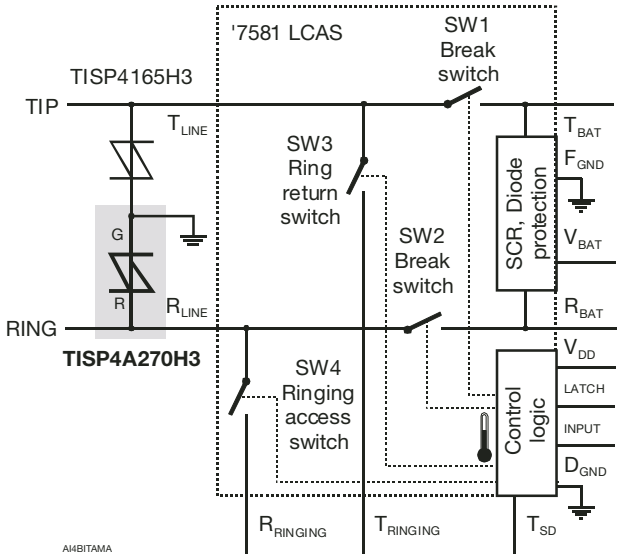
Wave Shape	Standard	I_{PPSM} A
2/10	GR-1089-CORE	500
10/700	ITU-T K.20/45/21	150
10/1000	GR-1089-CORE	100

.....UL Recognized Component

SMB Package (Top View)



Device Symbol and Circuit Application



Description

The TISP4A270H3BJ is an asymmetrical-bidirectional thyristor surge protective device (SPD). It is designed to limit the peak voltages on the R_{LINE} (Ring Line) terminal of '7581/2/3 LCAS (Line Card Access Switch) devices. The TISP4A270H3BJ must have the bar-indexed terminal 1 (G) connected to the protective ground and terminal 2 (R) connected to the R_{LINE} terminal.

The TISP4A270H3BJ voltages are chosen to give R_{LINE} terminal protection for all LCAS switch conditions. The most potentially stressful condition is low level power cross when the switches are closed. Under this condition, the TISP4A270H3BJ limits the voltage and corresponding LCAS dissipation until the LCAS thermal trip operates and opens the switches.

Under open-circuit ringing conditions, the R_{LINE} terminal will have high peak voltages. For battery backed ringing, the R_{LINE} terminal will have a larger peak negative voltage than positive, i.e. the peak voltages are asymmetric. The TISP4A270H3BJ has a similar voltage asymmetry which will allow the maximum possible ringing voltage, while still giving protection. With a connected telephone line, the LCAS T_{LINE} (Tip Line) terminal voltage levels will be less than 50 % of the open-circuit R_{LINE} terminal values. So the T_{LINE} terminal can be protected by a symmetrical-bidirectional overvoltage protector of the TISP4xxxH3BJ series.

How To Order

Device	Package	Carrier	Order As
TISP4A270H3BJ	BJ (SMB/DO-214AA with J-Bend)	R (Embossed Tape Reeled)	TISP4A270H3BJR-S

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex
APRIL 2002 - REVISED JANUARY 2007
Specifications are subject to change without notice.
Customers should verify actual device performance in their specific applications.

Description (Continued)

These devices allow signal voltages up to the maximum off-state voltage value, V_{DRM}, see Figure 1. Voltages above V_{DRM} are clipped and will not exceed the breakover voltage, $V_{(BO)}$, level. If sufficient current flows due to the overvoltage, the device switches into a low-voltage on-state condition, which diverts the current from the overvoltage though the device. When the diverted current falls below the holding current, I_H, level the devices switches off and restores normal system operation.

The TISP4A270H3BJ is guaranteed to voltage limit and withstand the listed international lightning surges in both polarities. This high current protection device is in a plastic SMB package (JEDEC DO-214AA) and supplied in embossed tape reel pack.

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating		Symbol	Value	Unit
Repetitive peak off-state voltage, (see Note 1)	T_A = 25 °C T_A = -40 °C	V_{DRM}	+160/-222 148/-206	V
Non-repetitive peak on-state pulse current (see Notes 2 and 3)				
2/10 (GR-1089-CORE, 2/10 voltage wave shape)		I_{PPSM}	500	A
5/310 (ITU-T K.44, 10/700 µs voltage wave shape used in K.20/45/21)			150	
10/1000 (GR-1089-CORE, 10/1000 voltage wave shape)			100	
Non-repetitive peak on-state current (see Notes 2, 3 and 4)				
20 ms (50 Hz) full sine wave		I_{TSM}	55	A
16.7 ms (60 Hz) full sine wave			60	
1000 s 50 Hz/60 Hz a.c.			2.2	
Initial rate of rise of on-state current, Exponential current ramp, Maximum ramp value < 200 A		di_T/dt	400	A/µs
Junction temperature		T_J	-40 to +150	°C
Storage temperature range		T_{stg}	-65 to +150	°C

NOTES: 1. See Figure 7 for voltage values at intermediate temperatures.
2. Initially, the TISP4A270H3BJ must be in thermal equilibrium with T_J = 25 °C.
3. The surge may be repeated after the TISP4A270H3BJ returns to its initial conditions.
4. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. See Figure 6 for the current ratings at other durations. Derate current values at -0.61 %/°C for ambient temperatures above 25 °C.

Overload Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Maximum overload on-state current without open circuit, 50 Hz/60 Hz a.c. (see Note 5)			
0.03 s	$I_{T(OV)M}$	60	A rms
0.07 s		40	
1.6 s		8	
5.0 s		7	
1000 s		2.2	

NOTE 5: Peak overload on-state current during a.c. power cross tests of GR-1089-CORE and UL 1950/60950. These electrical stress levels may damage the TISP4A270H3BJ silicon chip. After test, the pass criterion is either that the device is functional or, if it is faulty, that it has a short circuit fault mode. In the short circuit fault mode, the following equipment is protected as the device is a permanent short across the line. The equipment would be unprotected if an open circuit fault mode developed.

Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	V_D = +100 V and -200 V	T_A = 25 °C			±5	μA
			T_A = 85 °C			±10	
$V_{(BO)}$	Breakover voltage	dv/dt = ±250 V/ms, R_{SOURCE} = 300 Ω				+217 -270	V
$V_{(BO)}$	Ramp breakover voltage	dv/dt ≤ ±1 kV/μs, Linear voltage ramp, Maximum ramp value = ±500 V dv/dt = ±20 A/μs, Linear current ramp, Maximum ramp value = ±10 A				+231 -288	V
$I_{(BO)}$	Breakover current	dv/dt = ±250 V/ms, R_{SOURCE} = 300 Ω		±0.15		±0.6	A
I_H	Holding current	I_T = ±5 A, di/dt = +/-30 mA/ms		±0.15		±0.6	A
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value < 0.85V_{DRM}		±5			kV/μs
I_D	Off-state current	V_D = ±50 V	T_A = 85 °C			±10	μA
C_{off}	Off-state capacitance	f = 1 MHz, V_d = 1 V rms	V_D = 100 V		21	23	pF
			V_D = 50 V		27	29	
			V_D = 10 V		41	46	
			V_D = 5 V		48	53	
			V_D = 2 V		56	62	
			V_D = 1 V		61	67	
			V_D = 0		68	74	
			V_D = -1 V		62	68	
			V_D = -2 V		56	62	
			V_D = -5 V		48	52	
			V_D = -10 V		40	45	
			V_D = -50 V		25	28	
			V_D = -100 V		20	22	

Thermal Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\Theta JA}$	Junction to free air thermal resistance	EIA/JESD51-3 PCB, I_T = $I_{TSM(1000)}$, T_A = 25 °C, (see Note 6)			113	°C/W
		265 mm x 210 mm populated line card, 4-layer PCB, I_T = $I_{TSM(1000)}$, T_A = 25 °C		50		

NOTE 6: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

Parameter Measurement Information

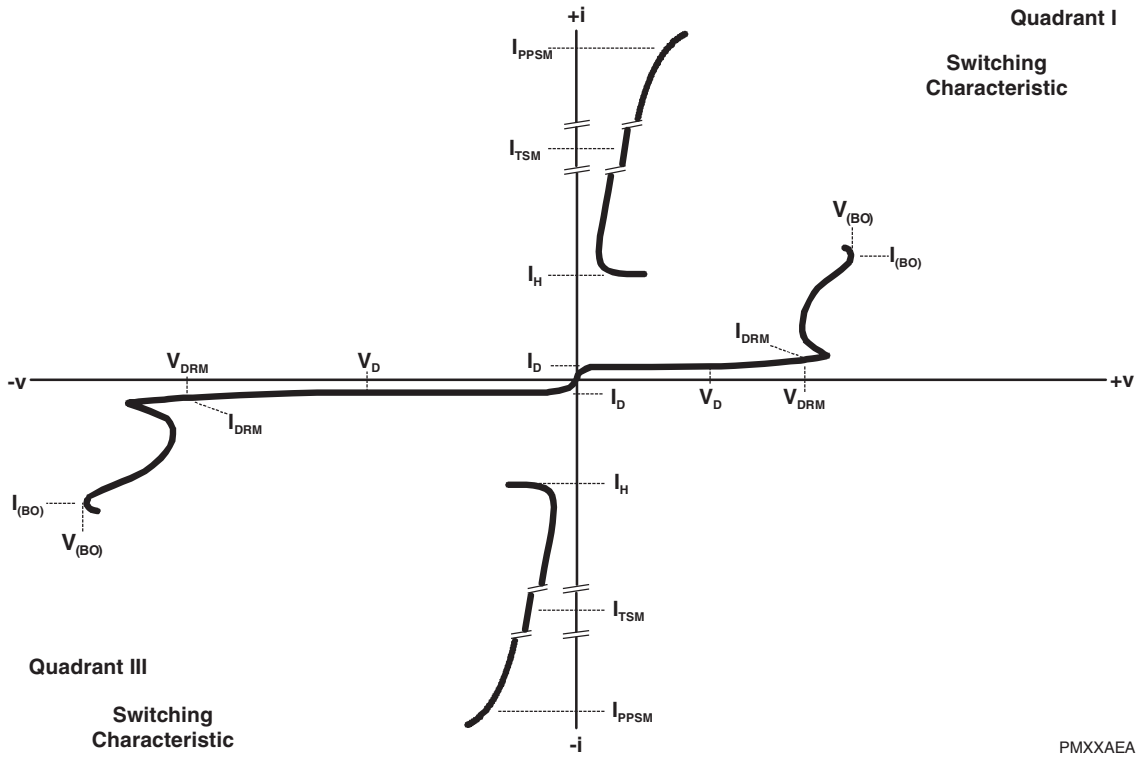


Figure 1. Voltage-Current Characteristic for R and G Terminal Pair
All Measurements are Referenced to the G Terminal

Typical Characteristics

OFF-STATE CURRENT vs JUNCTION TEMPERATURE

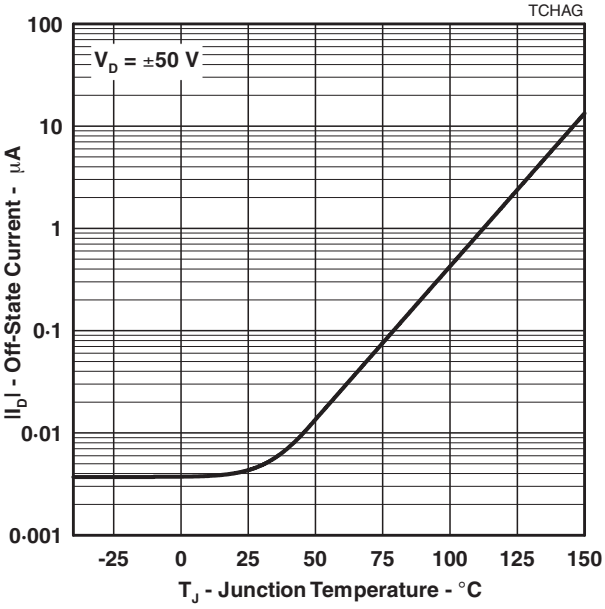


Figure 2.

NORMALIZED BREAKOVER VOLTAGE vs JUNCTION TEMPERATURE

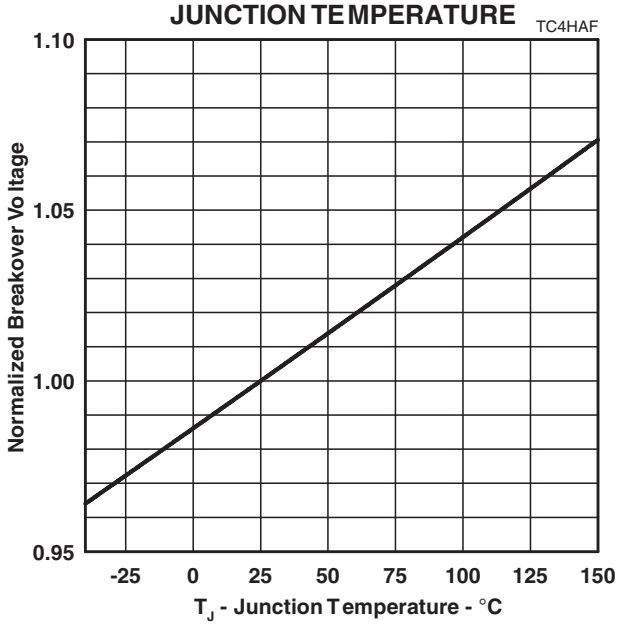


Figure 3.

ON-STATE CURRENT vs ON-STATE VOLTAGE

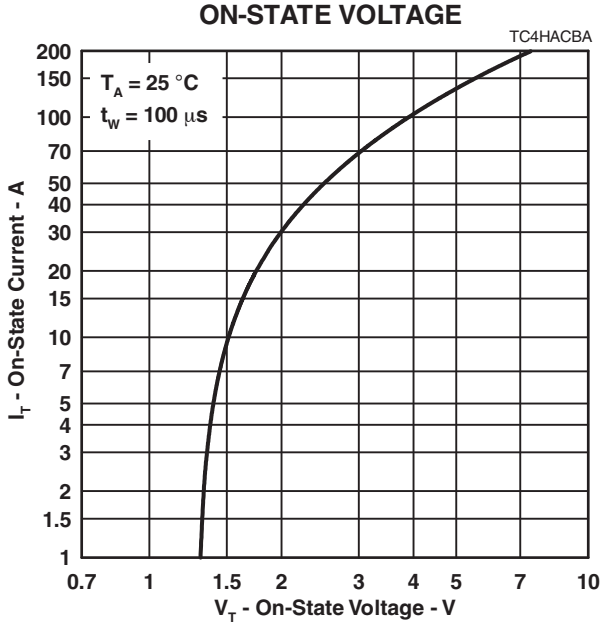


Figure 4.

NORMALIZED HOLDING CURRENT vs JUNCTION TEMPERATURE

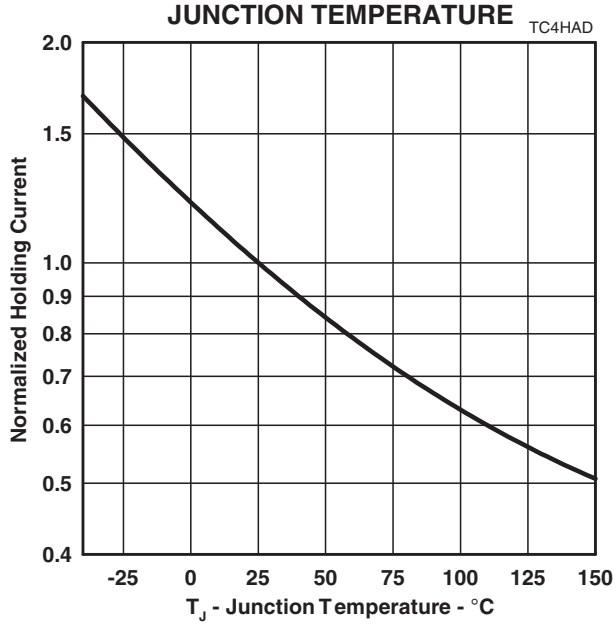


Figure 5.

Rating and Thermal Information

NON-REPETITIVE PEAK ON-STATE CURRENT vs CURRENT DURATION

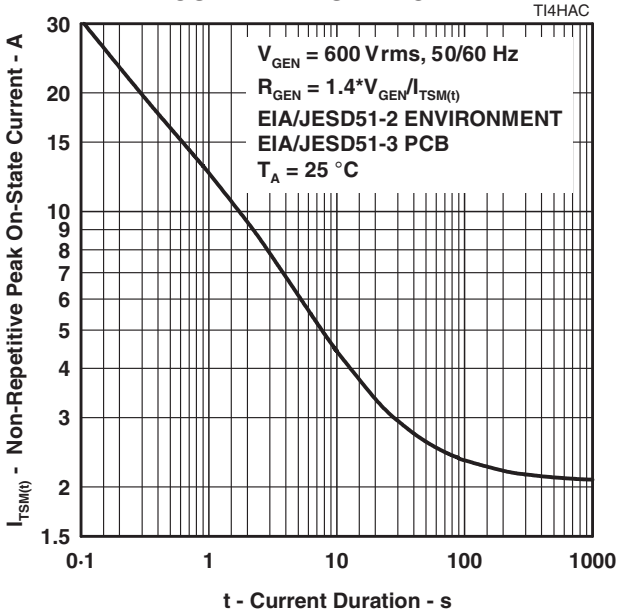


Figure 6.

V_{DRM} DERATING FACTOR vs MINIMUM AMBIENT TEMPERATURE

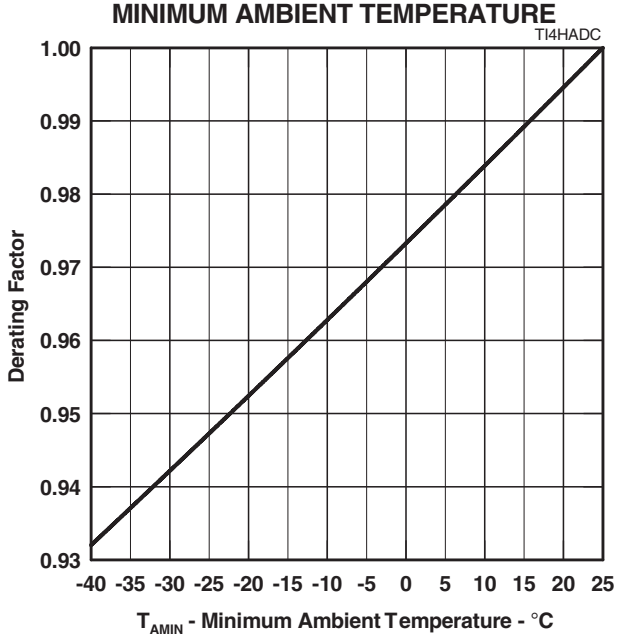


Figure 7.

APPLICATIONS INFORMATION

Calculation of the TISP4A270H3BJ Voltage Values

Figure 8 and the following text summarizes the derivation process for the TISP4A270H3BJ voltages. Details of the full process and other design aspects are covered by the document entitled *TISP4A270H3BJ - Optimized '758x LCAS Overvoltage Protection*.

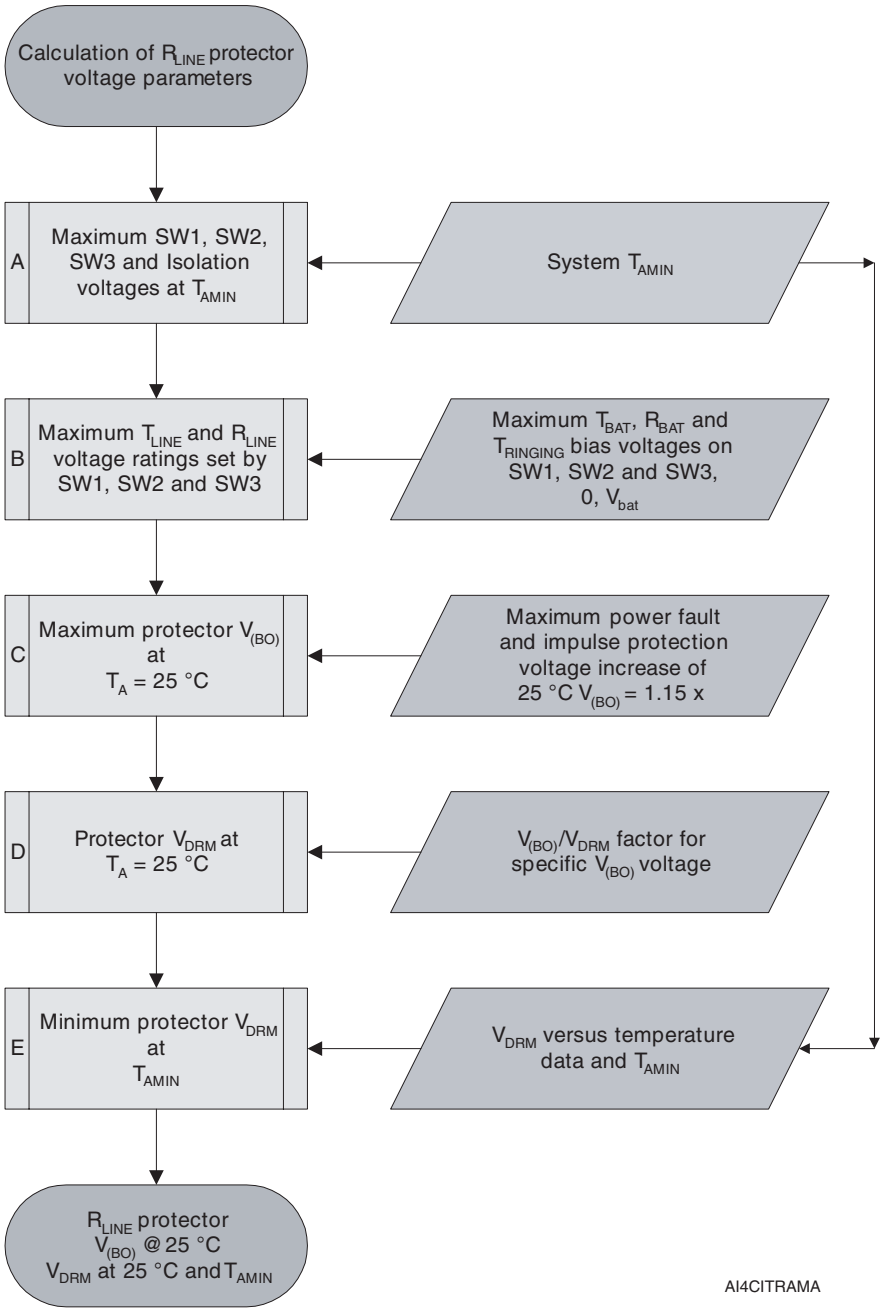


Figure 8. Derivation of TISP4A270H3BJ $V_{(BO)}$ and V_{DRM}

Calculation of the TISP4A270H3BJ Voltage Values (Continued)

Box A: The voltage rating of the break and ring return switches and their isolation decreases with temperature. At the minimum LCAS operating temperature of -40 °C, the switch rating is ±310 V.

Box B: A switch pole voltage rating to ground is reduced by any opposing bias voltage applied to the other pole. For battery-backed ringing the d.c. bias on $T_{RINGING}$ is zero. Bias voltages are applied to the R_{BAT} and T_{BAT} poles by the SLIC. For SLIC output levels of zero and -60 V, the R_{LINE} and T_{LINE} voltage ratings to ground become +250 V and -310 V at -40 °C.

Box C: Allowing for the extreme condition of a power fault at -40 °C, the overvoltage protector $V_{(BO)}$ at its highest temperature must not exceed +250 V and -310 V. The IEEE Standard *C62.37.1-2000, IEEE Guide for the Application of Thyristor Surge Protective Devices, pp 25-27* recommends a factor of 1.15 for the ratio of the power fault $V_{(BO)}$ to the 25 °C $V_{(BO)}$. Applying this factor makes the 25 °C $V_{(BO)}$ voltage values +217 V and -270 V.

Box D: From the $V_{(BO)}$ values the values of protector 25 °C V_{DRM} were determined as +160 V and -222 V.

Box E: Derating the 25 °C V_{DRM} down to the LCAS minimum operating temperature gives -40 °C V_{DRM} values of +148 V and -206 V. A further rating check has to be done on the ringing access switch, SW4. The limit condition is in the negative ringing polarity. The applied ringing voltage to the $R_{RINGING}$ terminal must not exceed -205 V when the R_{LINE} terminal is at +250 V. For a battery voltage of -40 V and -60 V the a.c. ringing levels must not exceed 117 V rms and 102 V rms respectively. In IVD (Integrated Voice Data) applications the a.c. ringing level must be reduced by the level of digital signal applied to the line. For a 20 V peak ADSL signal level, the ringing voltages reduce to 103 V rms and 89 V rms respectively.

Figure 9 shows a typical application circuit. Fuses F1 and F2 need high breaking capacity to safely interrupt 40 A rms (UL 60950) and 60 A rms (Telcordia GR-1089-CORE) currents from a 600 V rms source. The Bourns® Telefuse™ type B1250T is a surface mount fuse which has UL recognition for these UL and Telcordia standards. The TISP4A270H3BJ is overload rated to carry currents up to 60 A rms for the time period that it takes the fuse to operate.

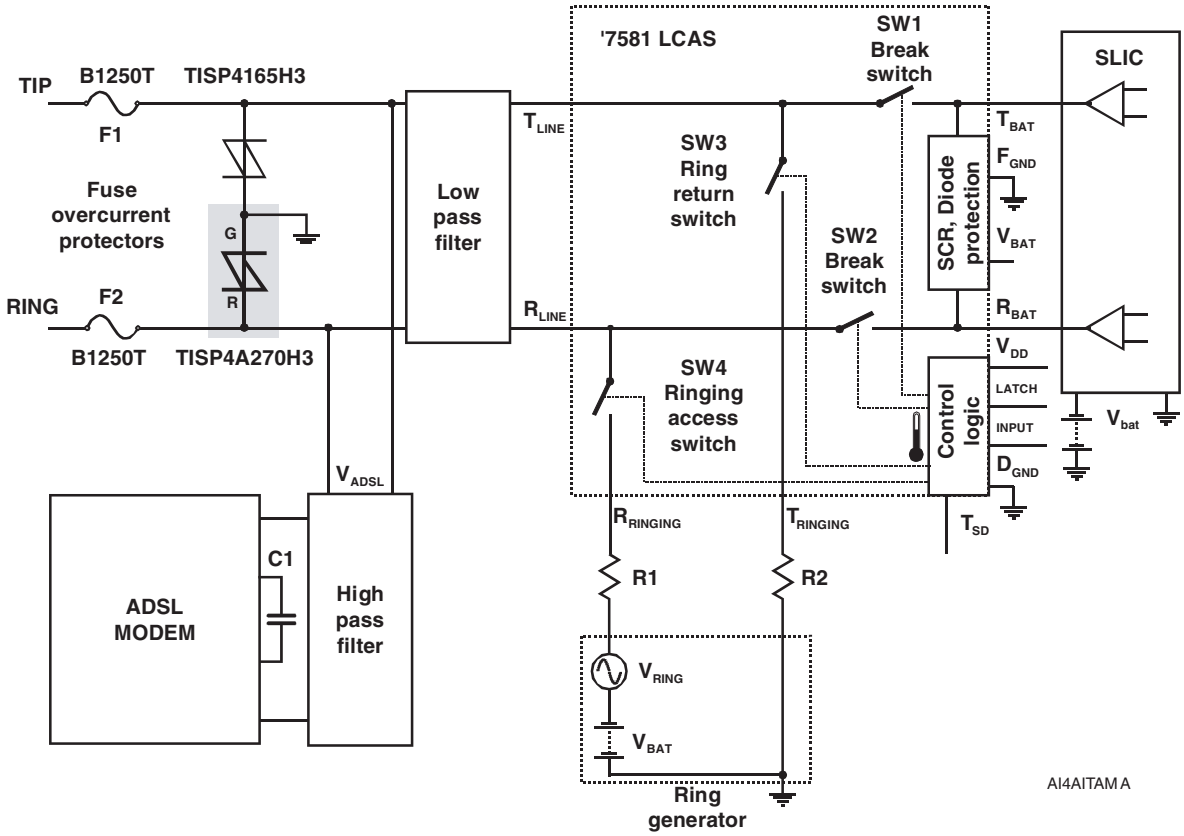


Figure 9. ADSL IVD using Common Protection