

# TJA1086G

## FlexRay active star coupler

Rev. 1 — 13 July 2017

Product data sheet

## 1. General description

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The TJA1086G is a FlexRay active star coupler that connects two branches of a FlexRay network. The TJA1086G is compliant with the FlexRay electrical physical layer specification V3.0.1/ISO17458-4 (see [Ref. 1](#) and [Ref. 2](#)).

Several TJA1085G and TJA1086G devices can be connected via their TRXD0/1 interfaces to increase the number of branches in the network. A dedicated Communication Controller (CC) interface allows for integration into an ECU. The TJA1086G supports low-power management by offering bus wake-up capability along with battery supply and voltage regulator control. The TJA1086G meets industry standards for EMC/ESD performance and provides enhanced bus error detection, low current consumption and unmatched asymmetric delay performance.

## 2. Features and benefits

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### 2.1 General

- Compliant with FlexRay Electrical Physical Layer specification V3.0.1/ISO17458-4
- Automotive product qualification in accordance with AEC-Q100
- Data transfer rates from 2.5 Mbit/s to 10 Mbit/s
- Supports 60 ns minimum bit time at 400 mV differential voltage
- Low-power management for battery-supplied ECUs
- Very low current consumption in AS\_Sleep mode
- Leadless HVQFN44 package with improved Automated Optical Inspection (AOI) capability

### 2.2 Functional

- Supports autonomous active star operation independent of the host ensuring the TJA1086G remains active even if the host fails or is switched off
- Branches can be independently configured
- Branch extension via TRXD0/1 inner star interface
- 16-bit bidirectional SPI interface up to 2 Mbit/s for host communication
- Full host control over branch status
- Enhanced wake-up capability:
  - ◆ Remote wake-up via wake-up pattern and dedicated FlexRay data frames
  - ◆ Local wake-up via pin LWU
  - ◆ Wake-up source recognition
  - ◆ configurable per branch
- Enhanced supply voltage monitoring on  $V_{IO}$ ,  $V_{CC}$ ,  $V_{BUF}$  and  $V_{BAT}$



- Auto I/O level adaptation to host controller supply voltage  $V_{IO}$
- Can be used in 14 V, 24 V and 48 V powered systems
- Enhanced bus error detection - detects short-circuit conditions on the bus
- Instant transmitter shut-down interface (BGE pin)
- Selective branch shut-down (partial networking)

### 2.3 Robustness

- Bus pins protected against  $\pm 8$  kV ESD pulses according to HBM and  $\pm 6$  kV ESD pulses according to IEC61000-4-2
- All pins protected against  $\pm 1000$  V ESD according to CDM
- All pins protected against  $\pm 200$  V ESD according to MM
- No reverse currents from the digital input pins to  $V_{IO}$  or  $V_{CC}$  when the TJA1086G is not powered up
- Bus pins short-circuit proof to battery voltage (14 V, 24 V or 48 V) and ground
- Overtemperature detection and protection
- Bus pins protected against transients in automotive environment (according to ISO 7637 class C)

### 2.4 Active star functional classes

- Active star - communication controller interface
- Active star - bus guardian interface
- Active star - voltage regulator control
- Active star - logic level adaptation
- Active star - host interface
- Active star - increased voltage amplitude transmitter

### 3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		4.75	-	5.25	V
V <sub>uvd(VCC)</sub>	undervoltage detection voltage on pin V <sub>CC</sub>	V <sub>CC1</sub> /V <sub>CC2</sub> connected on pcb	4.45	-	4.715	V
I <sub>CC</sub>	supply current	AS_Normal mode; V <sub>BGE</sub> = V <sub>IO</sub> ; V <sub>TXEN</sub> = 0 V; R <sub>bus</sub> = 45 Ω	-	95	120	mA
V <sub>BAT</sub>	battery supply voltage		4.75	-	60	V
V <sub>uvd(VBAT)</sub>	undervoltage detection voltage on pin V <sub>BAT</sub>		4.45	-	4.715	V
I <sub>BAT</sub>	battery supply current	AS_Sleep mode; wake-up enabled on all branches; T <sub>vj</sub> ≤ 85 °C	-	38	70	μA
		normal power modes	-	0.1	1	mA
V <sub>IO</sub>	supply voltage on pin V <sub>IO</sub>		2.8	-	5.25	V
V <sub>uvd(VIO)</sub>	undervoltage detection voltage on pin V <sub>IO</sub>		2.55	-	2.765	V
I <sub>IO</sub>	supply current on pin V <sub>IO</sub>	normal power modes	-	-	1	mA
V <sub>ESD</sub>	electrostatic discharge voltage	IEC 61000-4-2 on pins BP and BM to ground	-6	-	+6	kV

### 4. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
TJA1086GHN	HVQFN44	plastic thermal enhanced very thin quad flat package; no leads; 44 terminals; body 9 × 9 × 0.85 mm	SOT1113-1

5. Block diagram

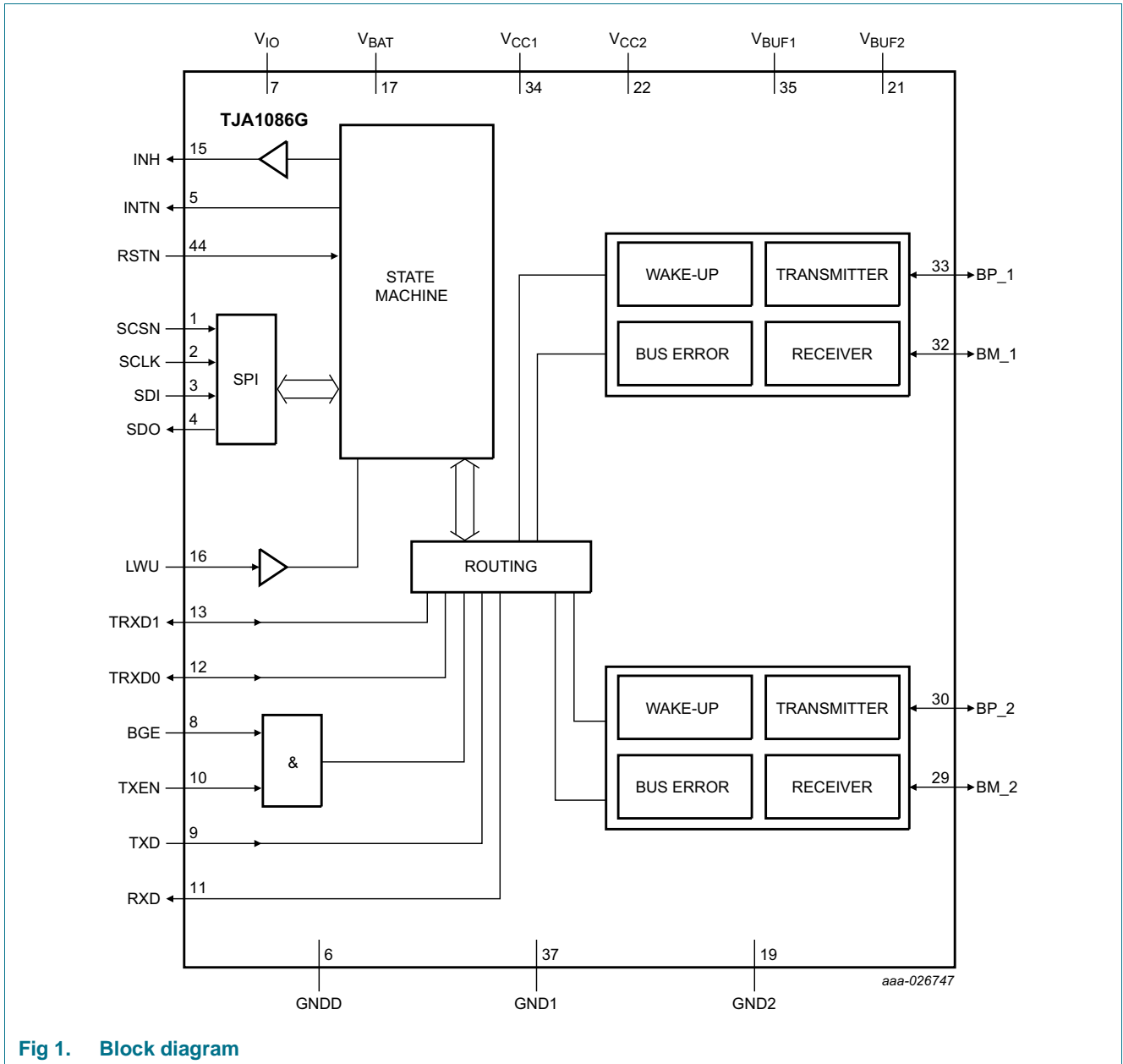
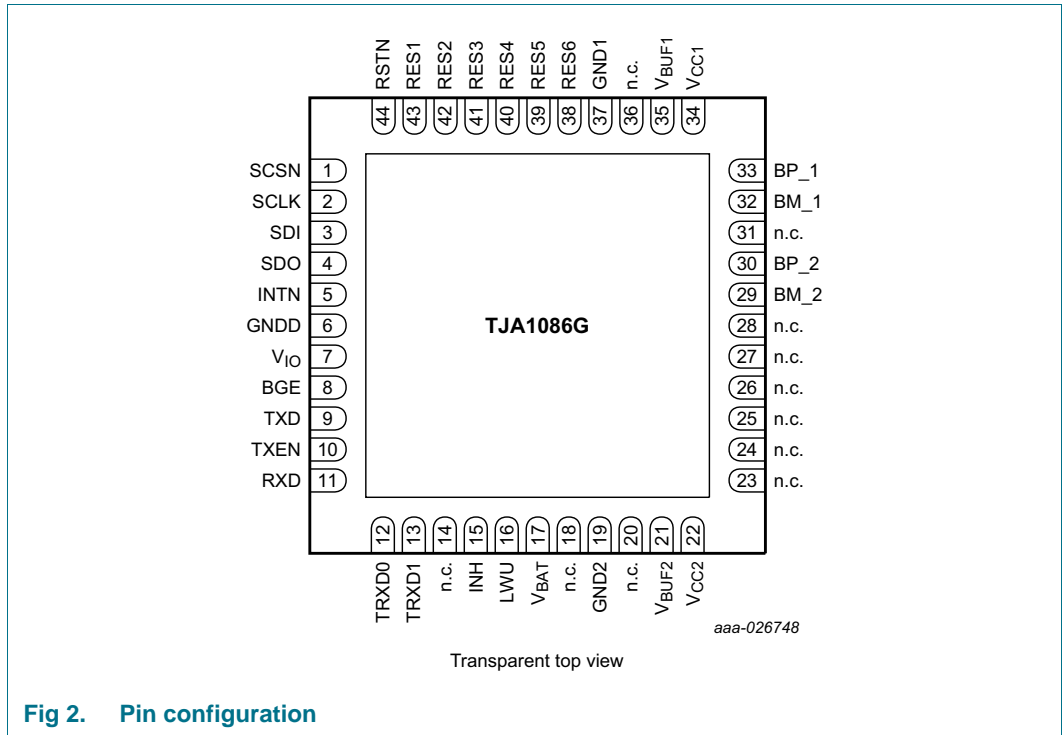


Fig 1. Block diagram

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type <sup>[1]</sup>	Description
SCSN	1	I	SPI chip select input; internal pull-up
SCLK	2	I	SPI clock signal; internal pull-down
SDI	3	I	SPI data input; internal pull-down
SDO	4	O	SPI data output; 3-state output
INTN	5	O	interrupt output; open-drain output, low-side driver
GNDD	6	G	ground for digital circuits <sup>[2]</sup>
V <sub>IO</sub>	7	P	supply voltage for V <sub>IO</sub> voltage level adaptation
BGE	8	I	bus guardian enable input; internal pull-down
TXD	9	I	transmit data input; internal pull-down
TXEN	10	I	transmitter enable input; internal pull-up
RXD	11	O	receive data output
TRXD0	12	IO	data bus line 0 for inner star connection
TRXD1	13	IO	data bus line 1 for inner star connection
n.c.	14	-	not connected; to be connected to GND in application
INH	15	O	inhibit output; for switching external voltage regulator

Table 3. Pin description ...continued

Symbol	Pin	Type <sup>[1]</sup>	Description
LWU	16	I	local wake-up input; internal pull-up or pull-down (depends on voltage at pin LWU)
V <sub>BAT</sub>	17	P	battery supply voltage
n.c.	18	-	not connected; to be connected to GND in application
GND2	19	G	ground connection 2 <sup>[2]</sup>
n.c.	20	-	not connected; to be connected to GND in application
V <sub>BUF2</sub>	21	P	buffer supply voltage 2 <sup>[3]</sup>
V <sub>CC2</sub>	22	P	supply voltage 2 <sup>[4]</sup>
n.c.	23	-	not connected; to be left open in the application
n.c.	24	-	not connected; to be left open in the application
n.c.	25	-	not connected; to be connected to GND in application
n.c.	26	-	not connected; to be left open in the application
n.c.	27	-	not connected; to be left open in the application
n.c.	28	-	not connected; to be connected to GND in application
BM_2	29	IO	bus line minus for branch 2 <sup>[5]</sup>
BP_2	30	IO	bus line plus for branch 2 <sup>[6]</sup>
n.c.	31	-	not connected; to be connected to GND in application
BM_1	32	IO	bus line minus for branch 1 <sup>[5]</sup>
BP_1	33	IO	bus line plus for branch 1 <sup>[6]</sup>
V <sub>CC1</sub>	34	P	supply voltage 1 <sup>[4]</sup>
V <sub>BUF1</sub>	35	P	buffer supply voltage 1 <sup>[3]</sup>
n.c.	36	-	not connected; to be connected to GND in application
GND1	37	G	ground connection 1 <sup>[2]</sup>
RES6	38	-	reserved; to be connected to GND in application
RES5	39	-	reserved; to be connected to GND in application
RES4	40	-	reserved; to be connected to GND in application
RES3	41	-	reserved; to be connected to GND in application
RES2	42	-	reserved; to be connected to GND in application
RES1	43	-	reserved; to be connected to GND in application
RSTN	44	I	reset input; internal pull-up

[1] IO: input/output; O: output; I: input; P: power supply; G: ground.

[2] GND1, GND2, GNDD and the exposed center pad of HVQFN44 package must be connected together on the PCB; references in the data sheet to GND can be assumed to encompass GND1, GND2, GNDD and the exposed center pad of HVQFN4 unless stated otherwise.

[3] V<sub>BUF1</sub> and V<sub>BUF2</sub> must be connected together on the PCB; note that references in the data sheet to V<sub>BUF</sub> can be assumed to encompass V<sub>BUF1</sub> and V<sub>BUF2</sub> unless stated otherwise.

[4] V<sub>CC1</sub> and V<sub>CC2</sub> must be connected together on the PCB; note that references in the data sheet to V<sub>CC</sub> can be assumed to encompass V<sub>CC1</sub> and V<sub>CC2</sub> unless stated otherwise.

[5] References in the data sheet to BM (e.g. pin BM or V<sub>BM</sub>) can be assumed to encompass BM\_1 and BM\_2 unless stated otherwise.

[6] References in the data sheet to BP (e.g. pin BP or V<sub>BP</sub>) can be assumed to encompass BP\_1 and BP\_2 unless stated otherwise.

## 7. Functional description

### 7.1 Supply voltage

The TJA1086G state machine is adequately supplied if at least one of  $V_{BAT}$ ,  $V_{CC}$  or  $V_{BUF}$  is available. The internal supply voltage to the state machine is denoted by  $V_{DIG}$ .  $V_{BUF}$  is an auxiliary supply and is only needed for forwarding the wake-up pattern when  $V_{CC}$  is not available.

### 7.2 Host Control (HC) and Autonomous Power (AP) modes - APM flag

The APM flag determines whether the TJA1086G is host-controlled or is operating in Autonomous Power mode. It is in AP mode by default.

The TJA1086G sets the APM flag:

- at power-on
- when a wake-up event is detected (on TRXD0/1, local or remote)
- when a  $V_{CC}$  undervoltage event is detected in AS\_Normal mode
- when a  $V_{IO}$  undervoltage event lasts longer than  $t_{to(und)}(V_{IO})$

The host can set or reset the APM flag at any time.

### 7.3 Signal router

The signal router transfers data received on an input channel to all channels configured as outputs. If data is being received on more than one input channel at the same time, the channel that was first to signal activity is selected and data on the other channel/s is ignored. Whether or not the data on an output channel is transmitted depends on whether the output channel is enabled or disabled.

The TJA1086G contains the following data input channels:

- Branches 1 and 2
- TRXD0/1 interface (inner star interface)
- TXD/TXEN interface

The TJA1086G contains the following data output channels:

- Branches 1 and 2
- TRXD0/1 interface
- RXD pin

#### 7.3.1 TRXD collision

When the TRXD0/1 interface is configured as an output channel, a TRXD collision is detected ( $COLL\_TRXD = 1$ ) if pins TRXD0 and TRXD1 are both LOW for longer than  $t_{det(col)}(TRXD)$ , generating a CLAMP\_ERROR interrupt.

When a TRXD collision is detected, the TJA1086G transmits a DATA\_0 to all other active output channels (irrespective of the actual data on the selected input channel), until the selected input channel detects idle state.

## 7.4 Wake-up

The TJA1086G supports the following wake-up mechanisms:

- Remote wake-up via the bus (wake-up pattern or dedicated wake-up frame)
- Local wake-up via pin LWU
- Activity on the inner star interface (pins TRXD0 and TRXD1)

Any wake-up event will generate a WU interrupt. A remote wake-up on a branch will generate an EVENT\_BRx interrupt to indicate the branch where the wake-up pattern or dedicated data frame was detected.

The host can identify the wake-up source by polling the General Status register (WU\_TRXD = 1 for a TRXD0/1 wake-up; WU\_LOCAL = 1 for a local wake-up) and the Branch Status register (WU\_BRx = 1 for a remote wake-up).

### 7.4.1 Remote wake-up

When the TJA1086G is in AS\_Standby or AS\_Sleep, both branches are monitored for wake-up events. When a valid wake-up pattern or data frame is detected on one of the branches, the relevant WU\_BRx status bit is set and the wake-up pattern/data frame is forwarded to the other branch (if enabled).

A remote wake-up event occurring during an AS\_Normal-to-AS\_Standby or AS\_Normal-to-AS\_Sleep transition will also be detected, setting the relevant WU\_BRx status bit and generating WU and EVENT\_BRx interrupts.

#### 7.4.1.1 Bus wake-up via wake-up pattern

A wake-up pattern consists of at least two consecutive wake-up symbols. A wake-up symbol consists of a DATA\_0 phase lasting longer than  $t_{\text{det(wake)DATA}_0}$ , followed by an idle phase lasting longer than  $t_{\text{det(wake)idle}}$ , provided both wake-up symbols occur within a time span of  $t_{\text{det(wake)tot}}$  (see [Figure 3](#)). The transceiver also wakes up if the idle phases are replaced by DATA\_1 phases.

A wake-up event is not detected if an invalid wake-up pattern is received. See [Ref. 1](#) for more details on invalid wake-up patterns.



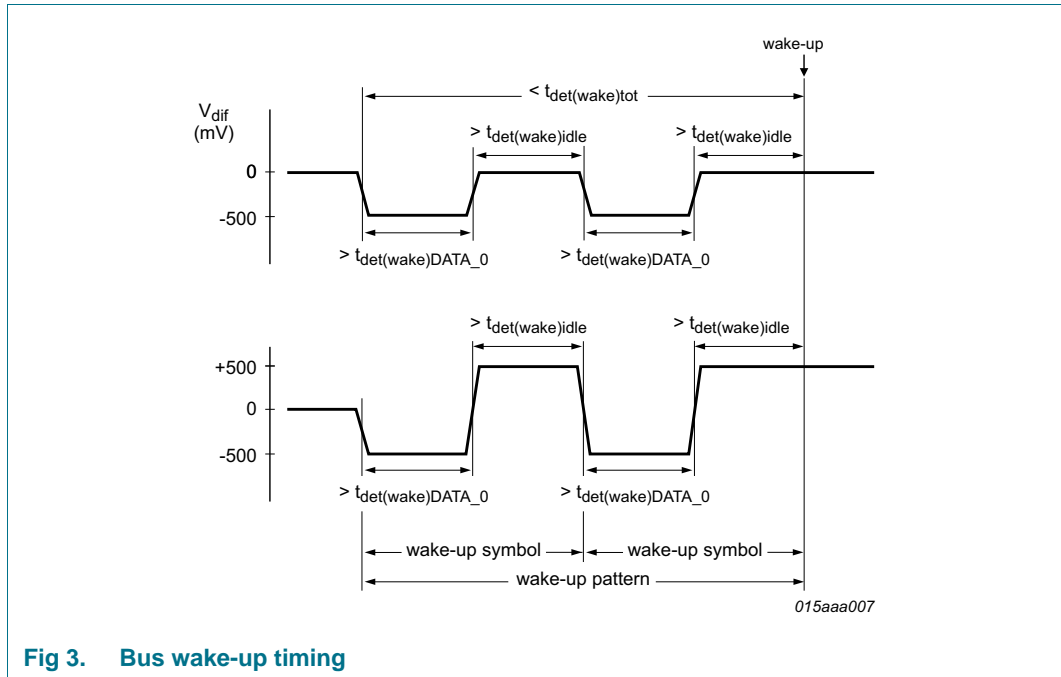


Fig 3. Bus wake-up timing

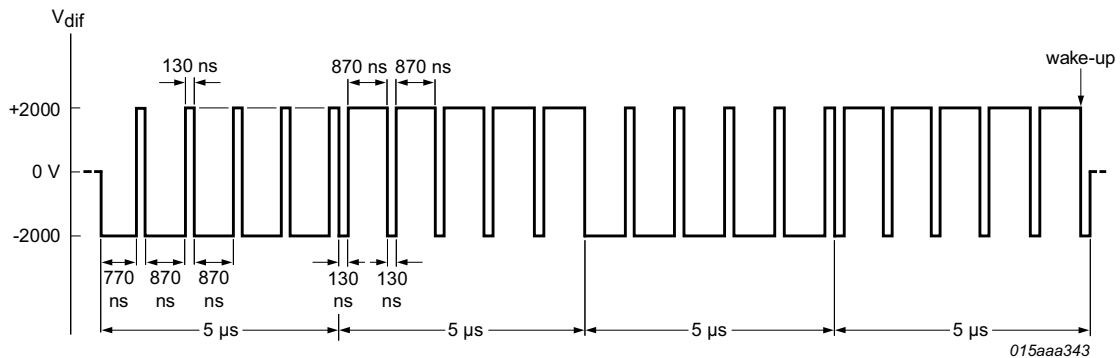
See [Ref. 1](#) for more details of the wake-up mechanism.

7.4.1.2 Bus wake-up via dedicated FlexRay data frame

The TJA1086G detects a wake-up event when a dedicated data frame emulating a valid wake-up pattern, as shown in [Figure 4](#), is received.

The Data\_0 and Data\_1 phases of the emulated wake-up symbol are interrupted by the Byte Start Sequence (BSS) preceding each byte in the data frame. With a data rate of 10 Mbit/s, the interruption has a maximum duration of 130 ns and does not prevent the transceiver from recognizing the wake-up pattern in the payload.

For longer interruptions at lower data rates (5 Mbit/s and 2.5 Mbit/s), the wake-up pattern should be used (see [Section 7.4.1.1](#)).



The duration of each interruption is 130 ns.  
 The transition time from DATA\_0 to DATA\_1 and vice versa is about 20 ns.  
 The TJA1086G wake-up flag is set on receipt of the following frame payload:  
 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,  
 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,  
 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,  
 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF

Fig 4. Minimum bus pattern for bus wake-up via dedicated FlexRay data frame

7.4.2 Local wake-up via pin LWU

Local wake-up is detected when the voltage on pin LWU is lower than  $V_{th(wake)(LWU)}$  for longer than  $t_{det(wake)(LWU)}$  (falling edge on pin LWU). When local wake-up is detected, the WU\_LOCAL status bit is set and a WU interrupt is generated. At the same time, the internal biasing of this pin is switched to pull-down.

If the voltage on pin LWU rises and remains above  $V_{th(wake)(LWU)}$  for longer than  $t_{det(wake)(LWU)}$  (rising edge on pin LWU), local wake-up is not detected and the biasing on pin LWU is switched to pull-up.

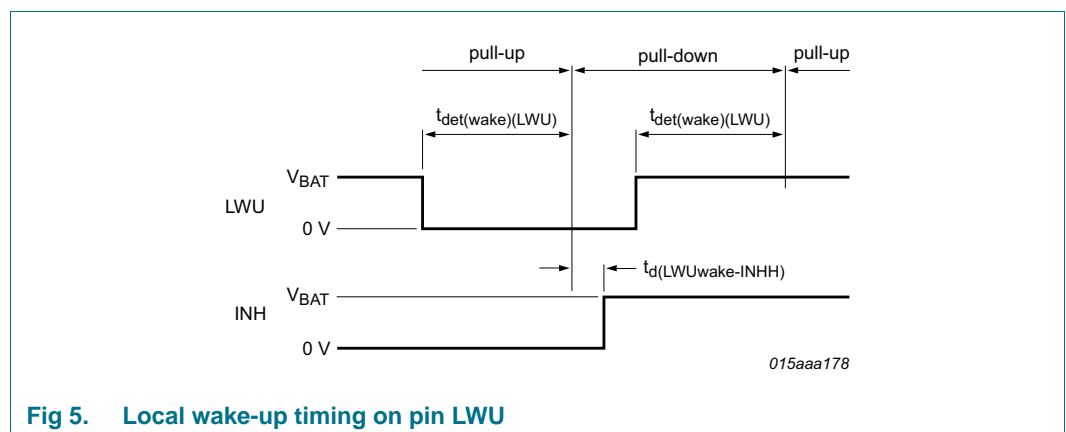


Fig 5. Local wake-up timing on pin LWU

7.4.3 Wake-up via the TRXD0/1 interface

If the voltage on pin TRXD0 or pin TRXD1 is LOW for longer than  $t_{det(wake)(TRXD)}$ , a WU interrupt is generated and the WU\_TRXD status bit is set.

## 7.5 Communication controller interface

### 7.5.1 Bus activity and idle detection

The following mechanisms for activity and idle detection are valid in normal power modes:

- If the absolute differential voltage on the bus lines is higher than  $|V_{i(dif)det(act)}|$  for  $t_{det(act)(bus)}$ , activity is detected on the bus lines
- If, after bus activity detection, the differential voltage on the bus lines is higher than  $V_{IH(dif)}$ , pin RXD will go HIGH
- If, after bus activity detection, the differential voltage on the bus lines is lower than  $V_{IL(dif)}$ , pin RXD will go LOW
- If the absolute differential voltage on the bus lines is lower than  $|V_{i(dif)det(act)}|$  for  $t_{det(idle)(bus)}$ , then idle is detected on the bus lines (pin RXD is switched HIGH or remains HIGH)

Additionally, activity and idle can be detected:

- if pin TXEN is LOW for longer than  $t_{det(act)(TXEN)}$ , activity is detected on pin TXEN
- if pin TXEN is HIGH for longer than  $t_{det(idle)(TXEN)}$ , idle is detected on pin TXEN
- if pin TRXD0 or TRXD1 is LOW for longer than  $t_{det(act)(TRXD)}$ , activity is detected on the TRXD0/1 interface
- if pins TRXD0 and TRXD1 are both HIGH for longer than  $t_{det(idle)(TRXD)}$ , idle is detected on the TRXD0/1 interface

**Table 4. Transmitter input signals: TXD, TXEN and BGE<sup>[1]</sup>**

TXD	TXEN	BGE	V <sub>IO</sub> UV detected	RXD	Bus	TRXD0	TRXD1	Operating mode
X	H	X	no	HIGH	idle	high ohmic <sup>[2]</sup>	high ohmic <sup>[2]</sup>	AS_Normal
X	X	L	no	HIGH	idle	high ohmic <sup>[2]</sup>	high ohmic <sup>[2]</sup>	AS_Normal
L	L	H	no	LOW	DATA_0	LOW	high ohmic <sup>[2]</sup>	AS_Normal
H	L	H	no	HIGH	DATA_1	high ohmic <sup>[2]</sup>	LOW	AS_Normal
X	X	X	no	HIGH	idle	high ohmic <sup>[2]</sup>	high ohmic <sup>[2]</sup>	AS_Standby, <sup>[3]</sup> AS_Sleep <sup>[3]</sup>
X	X	X	yes	LOW	idle	high ohmic <sup>[2]</sup>	high ohmic <sup>[2]</sup>	AS_Normal, AS_Standby, <sup>[3]</sup> AS_Sleep <sup>[3]</sup>
X	X	X	X	HIGH	float	high ohmic <sup>[2]</sup>	high ohmic <sup>[2]</sup>	AS_PowerOff, AS_Reset

[1] The transmitter is activated by a falling edge on pin TXD while TXEN is LOW and BGE is HIGH.

[2] Internal pull-up resistor (R<sub>pu</sub>) to V<sub>BUF</sub>.

[3] BP and BM biased to GND.

**Table 5. Bus as input**

Bus	V <sub>IO</sub> UV detected	RXD	TRXD0	TRXD1	Operating mode
DATA_0	no	LOW	LOW	high ohmic <sup>[1]</sup>	AS_Normal
DATA_1	no	HIGH	high ohmic <sup>[1]</sup>	LOW	AS_Normal
idle	no	HIGH	high ohmic <sup>[1]</sup>	high ohmic <sup>[1]</sup>	AS_Normal
X	no	HIGH	high ohmic <sup>[1]</sup>	high ohmic <sup>[1]</sup>	AS_Standby, AS_Sleep

**Table 5. Bus as input**

Bus	V <sub>IO</sub> UV detected	RXD	TRXD0	TRXD1	Operating mode
DATA_0	yes	LOW	LOW	high ohmic <sup>[1]</sup>	AS_Normal
DATA_1	yes	LOW	high ohmic <sup>[1]</sup>	LOW	AS_Normal
idle	yes	LOW	high ohmic <sup>[1]</sup>	high ohmic <sup>[1]</sup>	AS_Normal
X	yes	LOW	high ohmic <sup>[1]</sup>	high ohmic <sup>[1]</sup>	AS_Standby, AS_Sleep
X	X	HIGH	high ohmic <sup>[1]</sup>	high ohmic <sup>[1]</sup>	AS_PowerOff, AS_Reset

[1] Internal pull-up resistor (R<sub>pu</sub>) to V<sub>BUF</sub>.

**Table 6. TRXD0/1 interface configured as input**

TRXD0	TRXD1	V <sub>IO</sub> UV detected	RXD	Bus	Operating mode
X	falling edge	no	HIGH	DATA_1	AS_Normal <sup>[1]</sup>
HIGH	HIGH	no	HIGH	idle	AS_Normal
falling edge	X	X	LOW	DATA_0	AS_Normal <sup>[1]</sup>
X	falling edge	yes	LOW	DATA_1	AS_Normal <sup>[1]</sup>
HIGH	HIGH	yes	LOW	idle	AS_Normal
LOW	LOW	X	LOW	DATA_0	collision detected on TRXD0/1

[1] Activity detected on TRXD0/TRXD1.

## 7.6 Bus error detection

The TJA1086G provides bus error detection on each branch during data transmission. When a transmit error (TxE\_BRx = 1) is detected on a branch, an EVENT\_BRx interrupt is generated to notify the host.

The following conditions trigger bus error detection:

- Short circuit BP to BM
- Short-circuit BP to GND
- Short-circuit BM to GND
- Short-circuit BP to V<sub>CC</sub> or V<sub>BAT</sub>
- Short-circuit BM to V<sub>CC</sub> or V<sub>BAT</sub>

## 7.7 Interrupt generation

Interrupts are generated when specific events take place or associated status bits in the General or Branch X status registers are set. When an interrupt is generated, the relevant interrupt status bit is set in the Interrupt Status register (see [Table 10](#)) and pin INTN is forced LOW.

Some interrupt status bits (PWON, WU, SPI\_ERROR and HC\_ERROR) are reset immediately after the Interrupt Status register has been read successfully (i.e. a rising edge on SCSN with no SPI\_ERROR).

The UV\_ERROR, CLAMP\_ERROR, TEMP\_ERROR and EVENT\_BRx status bits are reset after the flag (or flags) that triggered the interrupt has been reset and a successful read operation had been performed (these two events can occur in any order). Resetting these bits triggers a further falling edge on INTN to indicate to the host that the issue that triggered the interrupt has been resolved (except in the case of EVENT\_BRx if a branch wake-up event triggered the interrupt). See [Section 7.10.2.3](#) for further details.

INTN signaling conforms to the FlexRay Electrical Physical Layer specification V3.0.1 (see [Ref. 1](#)).

## 7.8 Operating modes

The TJA1086G features five operating modes.

AS\_PowerOff, AS\_Sleep and AS\_Standby are low-power modes in which the transceiver is unable to transmit or receive data streams on the bus. In AS\_PowerOff mode, only power-on reset detection is active. The SPI, the low-power receiver and wake-up detection are active in AS\_Sleep mode. Undervoltage detection is enabled on  $V_{CC}$ ,  $V_{BAT}$  and  $V_{BUF}$  in AS\_Standby and AS\_Normal modes.  $V_{IO}$  undervoltage detection is always enabled, except when the TJA1086G is in AS\_PowerOff mode.

In AS\_Normal mode, the TJA1086G can transmit and receive data streams on the bus.

Pin INH is HIGH in AS\_Normal, AS\_Standby and AS\_Reset, and floating in AS\_PowerOff and AS\_Sleep.

The dStarGoToSleep timer is started when the TJA1086G switches to AS\_Standby or AS\_Normal, or when idle is detected on the bus. The timer is halted and reset when activity is detected on the bus.

### 7.8.1 Operating mode transitions

#### 7.8.1.1 AS\_PowerOff

The TJA1086G switches to AS\_PowerOff from any mode if the internal supply to the state machine,  $V_{DIG}$ , falls below the power-on detection threshold voltage ( $V_{th(det)POR}$ ). It remains in AS\_PowerOff until  $V_{DIG}$  rises above the power-on recovery threshold voltage ( $V_{th(rec)POR}$ ), when it switches to AS\_Standby. Pins INTN and SDO are switched to a high-impedance state in AS\_PowerOff mode.

#### 7.8.1.2 AS\_Reset

The TJA1086G switches to AS\_Reset from any mode if pin RSTN goes LOW with no undervoltage detected on  $V_{IO}$ . It remains in AS\_Reset until pin RSTN goes HIGH, when it switches to AS\_Standby.

#### 7.8.1.3 AS\_Standby

The TJA1086G switches to AS\_Standby:

- from AS\_PowerOff when  $V_{DIG}$  rises above the power-on recovery threshold voltage ( $V_{th(rec)POR}$ )
- from AS\_Reset when pin RSTN goes HIGH
- from AS\_Normal when a  $V_{CC}$  undervoltage event is detected ( $V_{CC} < V_{uvd}(V_{CC})$ ) for longer than  $t_{det(uv)}(V_{CC})$

- from AS\_Normal in response to a host 'AS\_Standby' command (HC mode)
- from AS\_Sleep in response to a host 'AS\_Standby' command (HC mode)
- from AS\_Sleep when a wake-up event is detected

The TJA1086G switches from AS\_Standby:

- to AS\_Normal when a wake-up event is detected, provided  $V_{BUF} > V_{uvr}(V_{BUF})$
- to AS\_Normal when a  $V_{CC}$  undervoltage recovery event is detected ( $V_{CC} > V_{uvr}(V_{CC})$ ) for longer than  $t_{rec(uv)}(V_{CC})$ , provided  $V_{BUF} > V_{uvr}(V_{BUF})$
- to AS\_Normal in response to a host 'AS\_Normal' command (HC mode)
- to AS\_Sleep if the dStarGoToSleep timer expires (AP mode)
- to AS\_Sleep if a  $V_{CC}$  undervoltage event lasts longer than  $t_{to(uvd)}(V_{CC})$  (HC mode)
- to AS\_Sleep in response to a host 'AS\_Sleep' command (HC mode)

#### 7.8.1.4 AS\_Sleep

A wake-up event will trigger a transition to AS\_Standby (followed by a transition to AS\_Normal if  $V_{BUF} > V_{uvr}(V_{BUF})$ ).

The TJA1086G switches to AS\_Sleep:

- from AS\_Standby in response to a host 'AS\_Sleep' command (HC mode)
- from AS\_Standby if the dStarGoToSleep timer expires (AP mode)
- from AS\_Standby if a  $V_{CC}$  undervoltage event lasts longer than  $t_{to(uvd)}(V_{CC})$  (HC mode)
- from AS\_Normal in response to a host 'AS\_Sleep' command (HC mode)
- from AS\_Normal if the dStarGoToSleep timer expires (AP mode)

The TJA1086G switches from AS\_Sleep:

- to AS\_Standby in response to a host 'AS\_Standby' command (HC mode)
- to AS\_Standby when a wake-up event is detected.
- to AS\_Normal in response to a host 'AS\_Normal' command (HC mode)

#### 7.8.1.5 AS\_Normal

The TJA1086G switches to AS\_Normal:

- from AS\_Standby if a  $V_{CC}$  undervoltage recovery event is detected ( $V_{CC} > V_{uvr}(V_{CC})$ ) for longer than  $t_{rec(uv)}(V_{CC})$ , provided  $V_{BUF} > V_{uvr}(V_{BUF})$
- from AS\_Standby if a wake-up event is detected, provided  $V_{BUF} > V_{uvr}(V_{BUF})$  for longer than  $t_{rec(uv)}(V_{BUF})$
- from AS\_Standby or AS\_Sleep in response to a host 'AS\_Normal' command

The TJA1086G switches from AS\_Normal:

- to AS\_Standby when a  $V_{CC}$  undervoltage event is detected ( $V_{CC} < V_{uvd}(V_{CC})$ ) for longer than  $t_{det(uv)}(V_{CC})$

- if the TJA1086G is in HC mode, it will switch from AS\_Standby to AS\_Sleep if the  $V_{CC}$  undervoltage persists for longer than  $t_{to(uvd)(VCC)}$
- if the TJA1086G is in AP mode, it will switch to AS\_Sleep when the dStarGoToSleep timer expires
- to AS\_Standby in response to a host 'AS\_Standby' command (HC mode)
- to AS\_Sleep in response to a host 'AS\_Sleep' command (HC mode)
- to AS\_Sleep if the dStarGoToSleep timer expires (AP mode)

7.8.1.6 Operating mode transition diagram

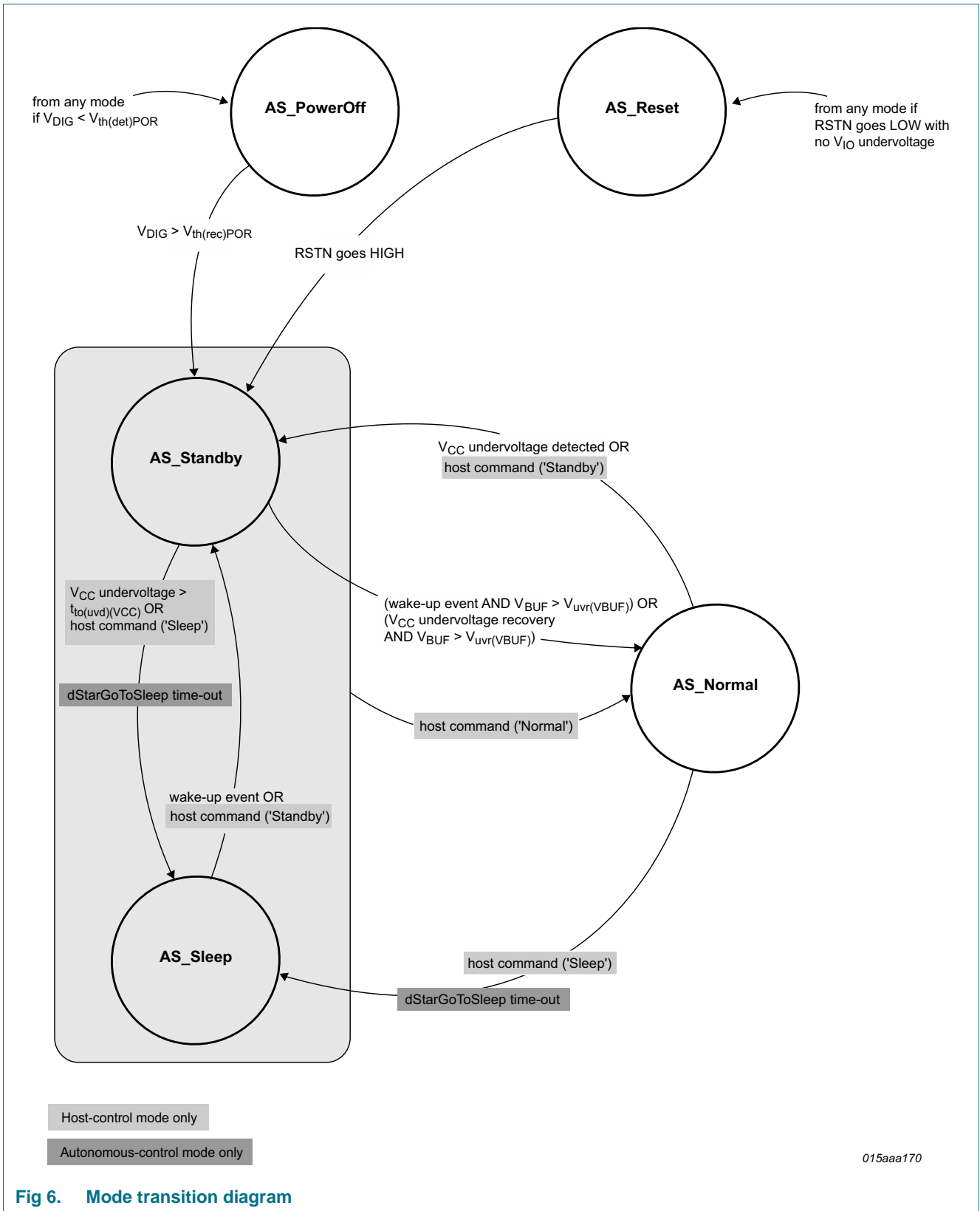


Fig 6. Mode transition diagram



## 7.9 Branch operating modes

Each of the two branches in the TJA1086G features six branch operating modes:

- **Branch\_Off**  
Both branches are in Branch\_Off mode when the TJA1086G is in AS\_PowerOff or AS\_Reset mode. The transmitter, normal receiver, low-power receiver and bus error detection are disabled. The bus pins are floating.
- **Branch\_LowPower**  
Both branches are in Branch\_LowPower mode when the TJA1086G is in AS\_Standby or AS\_Sleep mode. The transmitter, the normal receiver and bus error detection are disabled. The low-power receiver is active (i.e. remote wake-up is possible). The bus pins are biased to ground.
- **Branch\_Disabled**  
The TJA1086G switches to Branch\_Disabled if an overtemperature is detected. The 'Branch\_Disabled' and 'Branch\_Normal' commands allow the host to enable/disable a branch without affecting the other branch. The transmitter, normal receiver and bus error detection are disabled. Only the low-power receiver is active (remote wake-up is possible). The bus pins are biased to  $V_{o(idle)(BP)}$  and  $V_{o(idle)(BM)}$ .
- **Branch\_Normal**  
When a branch is in Branch\_Normal, the TJA1086G will be in AS\_Normal. The transmitter, normal receiver and bus error detection are active. The bus pins are biased to  $V_{o(idle)(BP)}$  and  $V_{o(idle)(BM)}$ .
- **Branch\_TxOnly1**  
In Branch\_TxOnly1 mode, the receiver is disabled, i.e. the received data is not forwarded to the signal router. The transmitter is active and bus error detection is active. The bus pins are biased to  $V_{o(idle)(BP)}$  and  $V_{o(idle)(BM)}$ .
- **Branch\_TxOnly2**  
This mode is host-controlled only and is operationally identical to Branch\_TxOnly1. It allows the host to switch off the receiver in response to error conditions.
- **Branch\_FailSilent**  
The transmitter, the low-power receiver and bus error detection are disabled. Only the receiver remains active to monitor the branch for idle or activity. Received data is not forwarded to the signal router. The bus pins are biased to  $V_{o(idle)(BP)}$  and  $V_{o(idle)(BM)}$ .

### 7.9.1 Branch operating mode transitions

Branch-related host commands can only be issued when the TJA1086G is in AS\_Normal mode.

#### 7.9.1.1 Branch\_Off

When the TJA1086G enters AS\_PowerOff or AS\_Reset, both branches switch to Branch-Off. When the TJA1086G subsequently switches to AS\_Standby, both branches switch to Branch\_LowPower.

#### 7.9.1.2 Branch\_LowPower

Both branches switch to Branch\_LowPower when the TJA1086G enters AS\_Standby or AS\_Sleep. Both branches will remain in this mode until the TJA1086G enters AS\_Normal. When this transition happens, any branch that was in Branch\_Disabled before switching to Branch\_LowPower will return to Branch\_Disabled. Otherwise, both branches switch to

Branch\_Normal.

#### 7.9.1.3 Branch\_Disabled

An overtemperature event (TEMP\_HIGH flag set) triggers a transition from Branch\_Normal to Branch\_Disabled in both branches.

If an overtemperature event triggered the transition from Branch\_Normal to Branch\_Disabled, both branches return to Branch\_Normal when the overtemperature problem has been resolved (TEMP\_WARN flag reset).

The 'Branch\_Disabled' and 'Branch\_Normal' commands can be used to enable/disable individual branches. A host command is also available to trigger a transition from Branch\_Disabled to Branch\_TxOnly1 ('Branch\_TxOnly').

If a branch switches from Branch\_Disabled to Branch\_LowPower because the TJA1086G has entered AS\_Standby or AS\_Sleep, it will return to Branch\_Disabled when the TJA1086G enters AS\_Normal.

#### 7.9.1.4 Branch\_FailSilent

A branch switches to Branch\_FailSilent:

- from Branch\_Normal if a branch is clamped (Clamp\_BRx flag set), provided clamp-detection is enabled (bit CLAMP\_DET set; see [Table 9](#))
- from Branch\_Normal if a transmit error (TxE\_BRx = 1) is detected, provided autonomous error confinement is enabled (bit AEC set; see [Table 9](#))
- from Branch\_TxOnly1 if a transmit error (TxE\_BRx = 1) is detected.

The branch remains in Branch\_FailSilent until idle is detected on both branches, when it switches to Branch\_TxOnly1 (a 'Branch\_TxOnly' command is needed in HC mode).

#### 7.9.1.5 Branch\_TxOnly1

A branch switches to Branch\_TxOnly1:

- from Branch\_Disabled in response to a 'Branch\_TxOnly' command (HC mode)
- from Branch\_FailSilent in response to a 'Branch\_TxOnly' command when both branches are idle (HC mode)
- from Branch\_FailSilent when both branches are idle (AP mode)

A branch switches from Branch\_TxOnly1:

- to Branch\_Normal when a transmission ends without error
- to Branch\_FailSilent if a transmit error is detected (TxE\_BRx = 1)

#### 7.9.1.6 Branch\_TxOnly2

This mode is purely host controlled. A branch switches to Branch\_TxOnly2 only in response to a 'Branch\_TxOnly' command issued in Branch\_Normal mode. The branch remains in Branch\_TxOnly2 mode until a 'Branch\_Normal' command is received.

#### 7.9.1.7 Branch\_Normal

A branch switches to Branch\_Normal:

- from Branch\_LowPower when the TJA1086G enters AS\_Normal mode (provided it was not in Branch\_Disabled before the transition to Branch\_LowPower mode)
- from Branch\_TxOnly2 in response to a host 'Branch\_Normal' command
- from Branch\_TxOnly1 when a transmission ends without error
- from Branch\_Disabled in response to a host 'Branch\_Normal' command
- from Branch\_Disabled when an overtemperature is resolved (TEMP\_WARN = 0), provided the overtemperature triggered the earlier transition to Branch\_Disabled.

A branch switches from Branch\_Normal:

- to Branch\_FailSilent if a branch is clamped, provided clamp-detection is enabled (CLAMP\_DET = 1)
- to Branch\_FailSilent if a transmit error is detected, provided bit AEC = 1
- to Branch\_TxOnly2 if a host 'Branch\_TxOnly' command is received
- to Branch\_Disabled if an overtemperature event is detected (TEMP\_HIGH = 1)

7.9.1.8 Branch operating mode transition diagram

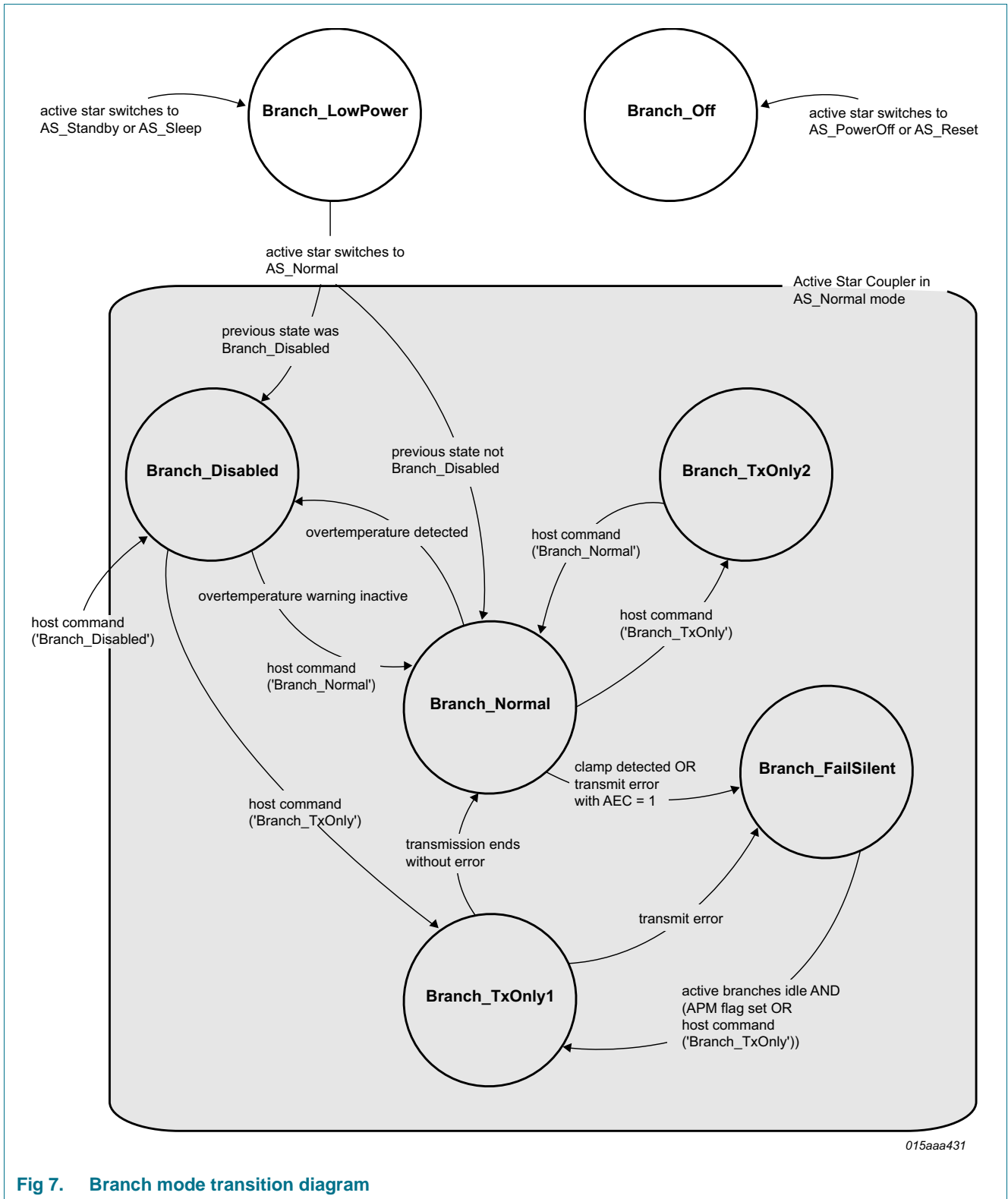


Fig 7. Branch mode transition diagram

### 7.10 SPI interface

The TJA1086G contains a bidirectional 16-bit Serial Peripheral Interface (SPI) for communicating with a host. The SPI allows the host to configure the TJA1086G and to access error and status information.

#### 7.10.1 Register access

The SPI supports full duplex data transfer, so status information is read out on pin SDO while control data is being shifted in on pin SDI. Bit sampling is performed on the falling edge of the clock signal on pin SCLK and data is shifted on the rising edge (MSB first; see [Figure 8](#)).

The clock signal must be LOW when SCSN goes LOW to initiate an SPI register access cycle.

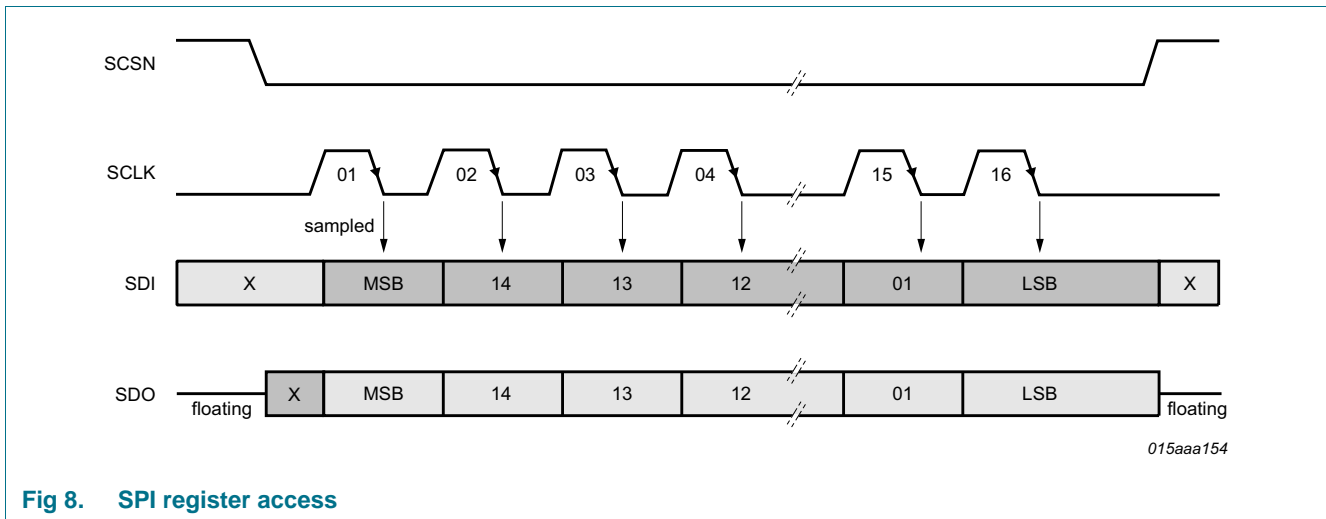


Fig 8. SPI register access

#### 7.10.2 SPI registers

The SPI register structure in the TJA1086G is illustrated in [Figure 9](#). The three MSBs (bits 15 to 13) contain the 3-bit register address. Bit 12 defines the selected register access as read/write or read only. If bit 12 is 1, the SPI data transfer will be read only and all data on the SDI pin will be ignored. If bit 12 is 0, data bits 11 to 0 will be written to the selected register.

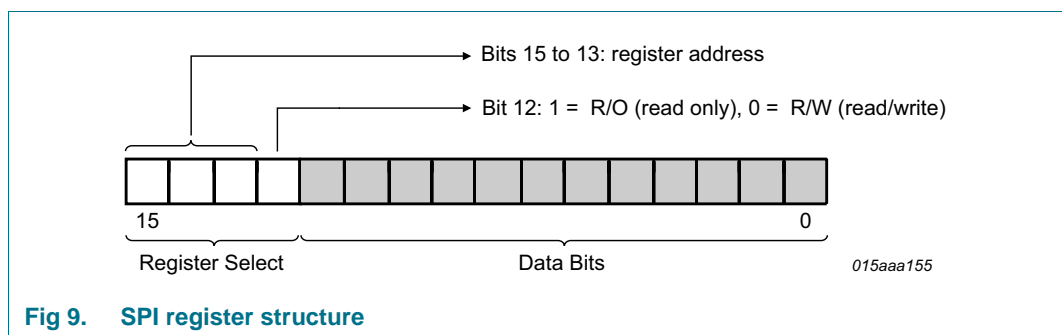


Fig 9. SPI register structure

The assignment of control and status register addresses is detailed in [Table 7](#). Data can only be written to the Control and Configuration registers (status registers are read-only by definition). Therefore the state of bit 12 is only evaluated when these registers are being accessed.

**Table 7. Register map**

Address bits 15, 14 and 13	Write access bit 12 <sup>[1]</sup>	Register
000	0 =R/W, 1 = R/O	Control register; see <a href="#">Table 8</a>
001	1 = R/O	Interrupt status register; see <a href="#">Table 10</a>
010	1 = R/O	General status register; see <a href="#">Table 11</a>
011	1 = R/O	Branch 1 status register; see <a href="#">Table 12</a>
100	1 = R/O	Branch 2 status register; see <a href="#">Table 12</a>
111	0 =R/W, 1 = R/O	Configuration register; see <a href="#">Table 9</a>

[1] Bit 12 is assumed to be 1 for status registers

The following subsections provide details of the bits in these registers and the control and status functionality assigned to each.

7.10.2.1 Control register

The read/write Control register allows the host controller to set the operating modes and to switch the TJA1086G between HC and AP modes.

Table 8. Control register bit description

Bit	Symbol	Access	Default	Description				
11:10	OPM	R/W	00	operating mode:				
				00: no change				
				01: AS_Standby				
				10: AS_Sleep				
9:8	CTRL_BR1	R/W	00	branch 1 control:				
				00: no change				
				01: Branch_Normal				
				10: Branch_TxOnly				
7:6	CTRL_BR2	R/W	00	branch 2 control:				
				00: no change				
				01: Branch_Normal				
				10: Branch_TxOnly				
5:2	reserved			after power-up, write 1111 once to bits [5:2] in AS_Standby before entering AS_Normal to minimize the power supply current				
				1	APM <sup>[1]</sup>	R/W	1	Autonomous Power mode
								0: disabled
								1: enabled
0	RESET_ERROR <sup>[2]</sup>	R/W	0	reset error flags and status bits				
				0: no change				
				1: reset flags/bits				

[1] The TJA1086G sets the APM flag at power-on, in response to a wake-up event (local, remote or TRXD), if a V<sub>CC</sub> undervoltage is detected in AS\_Normal or a V<sub>IO</sub> undervoltage is detected for longer than t<sub>to(und)(VIO)</sub>.

[2] Setting the RESET\_ERROR bit resets all error status bits in the General Status (bits 8 to 1) and Branch Status registers (bits 7 to 4).

### 7.10.2.2 Configuration register

The read/write Configuration register allows the host controller to configure a number of TJA1086G parameters and functions.

**Table 9. Configuration register bit description**

Bit	Symbol	Access	Default	Description
11	AEC	R/W	0	Autonomous error confinement:
				0: disabled
				1: enabled
10	BFT	R/W	1	Bus failure timer
				0: disabled
				1: enabled
9	WUD_BR1	R/W	1	wake-up detection on branch 1:
				0: disabled
				1: enabled
8	WUD_BR2	R/W	1	wake-up detection on branch 2:
				0: disabled
				1: enabled
7:6	reserved			after power-up, write 00 once to bits [7:6] to minimize the power supply current
5	CC_EN	R/W	0	CC interface enable (TXD and TXEN inputs; RXD output):
				0: disabled
				1: enabled
4	TRXD_EN	R/W	1	TRXD interface enable:
				0: disabled
				1: enabled
3	reserved			always 0
2	CLAMP_DET	R/W	1	clamping detection:
				0: disabled
				1: enabled
1	BIT_LATCHING	R/W	0	status bit latching:
				0: disabled
				1: enabled
0	PARITY	R	-	parity bit - odd parity (including parity bit)



**Autonomous Error Confinement (AEC):**

Setting the AEC bit enables the autonomous error confinement feature of the TJA1086G.

When AEC is enabled, a bus error (TxE\_BRx = 1) triggers a transition from Branch\_Normal to Branch\_FailSilent. AEC is disabled by default.

**Bus Failure Timer (BFT):**

Setting the BFT bit enables the bus failure timer.

When the BFT is enabled, pulses shorter than  $t_{to(BFT)}$  are ignored, resulting in more robust bus error detection. The BFT is enabled by default.

**Wake-up detection on branch x (WUD\_BRx):**

Setting the WUD\_BRx bit enables wake-up detection on the specified branch.

Each branch in a TJA1086G star network contains a low-power receiver for detecting remote wake-up events. These events can be enabled and disabled individually. This feature makes it possible to minimize quiescent current consumption, especially in AS\_Sleep mode. Wake-up detection is enabled by default on both branches.

**Communication Controller interface Enable (CC\_EN):**

Setting bit CC\_EN enables the communication controller interface.

A communication controller can be connected to the TJA1086G when CC\_EN = 1. If CC\_EN = 0, the RXD output driver is switched off to minimize current consumption in AS\_Normal mode. The CC interface is disabled by default.

**TRXD0/1 interface Enable (TRXD\_EN):**

Setting bit TRXD\_EN enables the TRXD0 and TRXD1 interfaces.

When the TRXD0/1 interfaces are enabled, several TJA1086G devices can be connected together to form a single active star. If only one TJA1086G is needed at any time, the TRXD0/1 interfaces can be disabled to minimize current consumption in AS\_Normal mode. The TRXD0 and TRXD1 interfaces are enabled by default.

**Clamp detection (CLAMP\_DET):**

Setting bit CLAMP\_DET enables clamp detection on TXEN, TRXD and on both branches.

When clamp detection is enabled, a CLAMP\_ERROR interrupt is generated if clamping is detected on TXEN (CLAMP\_TXEN = 1), TRXD (CLAMP\_TRXD = 1) or on a branch (CLAMP\_BRx). Clamp detection is enabled by default.

**Bit latching (BIT\_LATCHING):**

When bit latching is enabled (BIT\_LATCHING = 1), the status bits in the General and Branch X status registers reflect the latched state until the register is read. Once the register has been read, latching is released and the bits then reflect the current 'live' status. When bit latching is disabled, the status bits reflect the 'live' status at all times. Bit latching is disabled by default.

### 7.10.2.3 Interrupt Status register

The Interrupt Status register is read-only. When the TJA1086G sets a bit in this register, it triggers a falling edge on pin INTN. Bits PWON, WU, SPI\_ERROR and HC\_ERROR are reset after a successful read operation. The remaining bits are reset after the flag (or flags) that triggered the interrupt has been reset and a successful read operation has been performed (see [Section 7.7](#)).

**Table 10. Interrupt status register**

Bit	Symbol	Description
11	PWON	power-on detection:
		0: no power-on detected
		1: power-on detected
10	WU	wake-up event detection (any):
		0: no wake-up event detected
		1: wake-up event detected
9	EVENT_BR1	wake-up or bus error detection on branch 1:
		0: no wake-up or bus error detected
		1: wake-up or bus error detected
8	EVENT_BR2	wake-up or bus error detection on branch 2:
		0: no wake-up or bus error detected
		1: wake-up or bus error detected
7:6	reserved	
5	UV_ERROR	undervoltage detected on V <sub>BAT</sub> , V <sub>CC</sub> or V <sub>IO</sub> :
		0: no undervoltage detected
		1: undervoltage detected
4	CLAMP_ERROR	clamp error on TRXD, TXEN or branch or collision on TRXD:
		0: no clamping error detected
		1: clamping error detected
3	SPI_ERROR	SPI communication error:
		0: not detected
		1: detected
2	HC_ERROR	host command error:
		0: not detected
		1: detected
1	TEMP_ERROR	overtemperature error:
		0: not detected
		1: detected
0	PARITY	parity bit - odd parity (including parity bit)

**PWON:** A PWON interrupt is generated to signal a power-on event.

The PWON interrupt status bit is set when the TJA1086G leaves AS\_PowerOff or AS\_Reset. It is reset after a successful read operation on the Interrupt Status register.

**WU:** A WU interrupt indicates the occurrence of a wake-up event.

The WU interrupt status bit is set when a wake-up event is detected on a branch (WU\_BRx = 1), on TRXD0/1 (WU\_TRXD = 1), or on LWU (WU\_LOCAL = 1). It is reset after a successful read operation on the Interrupt Status register.

**EVENT\_BRx:** An EVENT\_BRx interrupt signals the occurrence of a significant event on the relevant branch.

The EVENT\_BRx interrupt status bit is set when any of the following events is detected on a branch:

- a wake-up event (WU\_BRx = 1)
- a bus error (TxE\_BRx = 1)
- clamping (CLAMP\_BRx = 1)

It is reset after the flag (or flags) that triggered the interrupt has been reset and the Interrupt Status register has been read successfully. Resetting EVENT\_BRx will trigger a falling edge on INTN to indicate to the host that the event that triggered the interrupt has been resolved (except when the interrupt was triggered by a branch wake-up event).

**UV\_ERROR:** A UV\_ERROR interrupt indicates that an undervoltage has occurred.

The UV\_ERROR interrupt status bit is set when a V<sub>BAT</sub> (UV\_VBAT = 1), V<sub>CC</sub> (UV\_VCC = 1) or V<sub>IO</sub> (UV\_VIO = 1) undervoltage is detected. It is reset after the flag (or flags) that triggered the interrupt has been reset and the Interrupt Status register has been read successfully. Resetting UV\_ERROR triggers a falling edge on INTN to indicate to the host that the undervoltage condition is no longer present.

**CLAMP\_ERROR:** A CLAMP\_ERROR interrupt indicates that an input channel has become clamped or a collision has occurred on the TRXD0/1 interface.

The CLAMP\_ERROR interrupt status bit is set when clamping is detected on TRXD (CLAMP\_TRXD = 1), on TXEN (CLAMP\_TXEN = 1) or on a branch (CLAMP\_BRx = 1) or if a collision is detected on TRXD0/TRXD1 (COLL\_TRXD = 1). It is reset after the flag (or flags) that triggered the interrupt has been reset and the Interrupt Status register has been read successfully. Resetting CLAMP\_ERROR triggers a falling edge on INTN to indicate to the host that the clamp or collision error has been corrected.

**SPI\_ERROR:** An SPI\_ERROR interrupt indicates that an error has occurred during SPI communications.

The SPI\_ERROR interrupt status bit is set if the number of SCLK cycles generated during a LOW phase on SCSN does not equal 16. It is reset after a successful read operation on the Interrupt Status register.

**HC\_ERROR:** A HC\_ERROR interrupt indicates that an invalid host command has been received.

The HC\_ERROR interrupt status bit is set when the host requests an illegal mode transition (as defined in the [Section 7.8.1](#) and [Section 7.9.1](#)). It is reset after a successful read operation on the Interrupt Status register.

**TEMP\_ERROR:** A TEMP\_ERROR interrupt signals the presence of an overtemperature condition.

The TEMP\_ERROR interrupt status bit is set when the temperature warning level (TEMP\_WARN = 1) or temperature high level (TEMP\_HIGH = 1) is exceeded. It is reset after the flag (or flags) that triggered the interrupt has been reset and the Interrupt Status register has been read successfully. Resetting TEMP\_ERROR triggers a falling edge on INTN to indicate to the host that the overtemperature condition is no longer present.

### 7.10.2.4 General Status register

The read-only General Status register contains status information not included in the Interrupt status register.

**Table 11. General status register**

Bit	Symbol	Description
11	WU_LOCAL	local wake-up on pin LWU:
		0: no wake-up detected
		1: wake-up detected
10	WU_TRXD	wake-up via TRXD0/TRXD1
		0: no wake-up detected
		1: wake-up detected
9	BGE_FB	BGE status feedback:
		0: if BGE is LOW
		1: if BGE is HIGH
8	UV_VBAT	V <sub>BAT</sub> undervoltage
		0: no undervoltage detected
		1: undervoltage detected
7	UV_VCC	V <sub>CC</sub> undervoltage
		0: no undervoltage detected
		1: undervoltage detected
6	UV_VIO	V <sub>IO</sub> undervoltage
		0: no undervoltage detected
		1: undervoltage detected
5	TEMP_WARN	temperature warning level
		0: not exceeded
		1: exceeded
4	TEMP_HIGH	temperature high level
		0: not exceeded
		1: exceeded
3	CLAMP_TRXD	clamping detection on TRXD:
		0: not detected
		1: detected
2	CLAMP_TXEN	clamping detection on TXEN:
		0: not detected
		1: detected
1	COLL_TRXD	collision detection on TRXD0 and TRXD1:
		0: not detected
		1: detected
0	PARITY	parity bit - odd parity (including parity bit)

**WU\_LOCAL:**

WU\_LOCAL is set when a local wake-up event is detected. A WU interrupt is generated.

WU\_LOCAL is reset after the General Status register has been read successfully or when the TJA1086G switches from AS\_Normal to AS\_Standby or AS\_Sleep. This ensures that a new wake-up event will be detected.

**WU\_TRXD:**

WU\_TRXD is set when a wake-up event is detected on the TRXD0/1 interface. A WU interrupt is generated.

WU\_TRXD is reset after the General Status register has been read successfully or when the TJA1086G switches from AS\_Normal to AS\_Standby or AS\_Sleep. This ensures that a new wake-up event will be detected.

**BGE\_FB:**

Bit BGE\_FB provides information about the voltage level on pin BGE.

BGE\_FB is set when the voltage on BGE is HIGH and reset when the voltage on BGE is LOW.

**UV\_VBAT:**

UV\_VBAT is set when a  $V_{BAT}$  undervoltage is detected, generating a UV\_ERROR interrupt.

If bit latching is enabled ( $BIT\_LATCHING = 1$ ), UV\_VBAT will remain set until the General Status register has been read, after which it will reflect the current 'live' situation (set if  $V_{BAT} < V_{uvd}(VBAT)$  for longer than  $t_{det(uv)}(VBAT)$  and reset if  $V_{BAT} > V_{uvr}(VBAT)$  for longer than  $t_{rec(uv)}(VBAT)$ ). If bit latching is not enabled, UV\_VBAT will reflect the 'live' situation at all times.

**UV\_VCC:**

UV\_VCC is set when a  $V_{CC}$  undervoltage is detected, generating a UV\_ERROR interrupt.

If bit latching is enabled ( $BIT\_LATCHING = 1$ ), UV\_VCC will remain set until the General Status register has been read, after which it will reflect the current 'live' situation (set if  $V_{CC} < V_{uvd}(VCC)$  for longer than  $t_{to(uvad)}(VCC)$  and reset if  $V_{CC} > V_{uvr}(VCC)$  for longer than  $t_{to(uvr)}(VCC)$ ). If bit latching is not enabled, UV\_VCC will reflect the 'live' situation at all times.

**UV\_VIO:**

UV\_VIO is set when a  $V_{IO}$  undervoltage is detected, generating a UV\_ERROR interrupt.

If bit latching is enabled ( $BIT\_LATCHING = 1$ ), UV\_VIO will remain set until the General Status register has been read, after which it will reflect the current 'live' situation (set if  $V_{IO} < V_{uvd}(VIO)$  for longer than  $t_{to(uvad)}(VIO)$  and reset if  $V_{IO} > V_{uvr}(VIO)$  for longer than  $t_{to(uvr)}(VIO)$ ). If bit latching is not enabled, UV\_VIO will reflect the 'live' situation at all times.

When a  $V_{IO}$  undervoltage is active, the digital inputs are disabled and the TJA1086G is unable to accept Host commands. If the  $V_{IO}$  undervoltage persists for longer than  $t_{to(uvad)}(VIO)$ , the APM flag is set and the TJA1086G switches from Host control to Autonomous control.

**TEMP\_WARN:**

TEMP\_WARN is set when the junction temperature rises above the temperature warning level, generating a TEMP\_ERROR interrupt.

If bit latching is enabled (BIT\_LATCHING = 1), TEMP\_WARN will remain set until the General Status register has been read, after which it will reflect the current 'live' situation (set when  $T_j > T_{j(\text{warn})}$  and reset when  $T_j < T_{j(\text{warn})}$  with no activity on the bus or on the CC and TRXD0/1 interfaces). If bit latching is not enabled, TEMP\_WARN will reflect the 'live' situation at all times.

**TEMP\_HIGH:**

TEMP\_HIGH is set when the junction temperature rises above the temperature high level. The output driver on the TRXD0/1 interface is disabled along with the branch transmitters (both branches switch to Branch\_Disabled). A TEMP\_ERROR interrupt is generated.

If bit latching is enabled (BIT\_LATCHING = 1), TEMP\_HIGH will remain set until the General Status register has been read, after which it will reflect the current 'live' situation (set when  $T_j > T_{j(\text{high})}$  and reset when  $T_j < T_{j(\text{high})}$  with no activity on the bus or on the CC and TRXD0/1 interfaces). If bit latching is not enabled, TEMP\_HIGH will reflect the 'live' situation at all times.

**CLAMP\_TRXD:**

CLAMP\_TRXD is set when the TRXD0/1 interface is configured as an input and TRXD0 or TRXD1 is clamped LOW for longer than  $t_{\text{detCL}}(\text{TRXD})$ . The output driver on the TRXD0/1 interface is disabled and data on the inputs is ignored. A CLAMP\_ERROR interrupt is generated.

If bit latching is enabled, CLAMP\_TRXD will remain set until the General Status register has been read, after which it will reflect the current 'live' situation (set when TRXD0 or TRXD1 clamped LOW and reset when TRXD0 and TRXD1 are HIGH). If bit latching is not enabled, CLAMP\_TRXD will reflect the 'live' situation at all times.

**CLAMP\_TXEN:**

CLAMP\_TXEN is set when the TXEN is clamped LOW for longer than  $t_{\text{detCL}}(\text{TXEN})$ . Data on TXD/TXEN is ignored and a CLAMP\_ERROR interrupt is generated.

If bit latching is enabled, CLAMP\_TXEN will remain set until the General Status register has been read, after which it will reflect the current 'live' situation (set when TXEN clamped LOW and reset when TXEN is HIGH). If bit latching is not enabled, CLAMP\_TXEN will reflect the 'live' situation at all times.

**COLL\_TRXD:**

COLL\_TRXD is set when a collision is detected on the TRXD0/1 interface (TRXD0 and TRXD1 LOW for longer than  $t_{\text{det(col)}}(\text{TRXD})$ ). A CLAMP\_ERROR interrupt is generated.

COLL\_TRXD is reset once the General Status register has been read.

### 7.10.2.5 Branch X status registers

There is a dedicated read-only status register for each branch, i.e. there are two Branch X status registers in total. Each register contains relevant status information of a branch.

**Table 12. Branch X status register**

Bit	Symbol	Description
11-9	STATE_BRx	state of active branch:
		000: Branch_Normal mode
		001: Branch_Disabled mode
		010: Branch_LowPower mode
		011: Branch_TxOnly_2 mode
		100: Branch_FailSilent mode
		101: Branch_TxOnly_1 mode
8	WU_BRx	wake-up status
		0: no wake-up detected
		1: wake-up detected
7	reserved	always 0
6	TxE_BRx	transmit error on branch
		0: not detected
		1: detected
5	reserved	always 0
4	CLAMP_BRx	clamp detection on branch
		0: not detected
		1: detected
3	reserved	always 0
2	reserved	always 1
1	reserved	always 0
0	PARITY	parity bit - odd parity (including parity bit)



**STATE\_BRx:**

Bits STATE\_BRx indicate the current branch operating mode.

**WU\_BRx:**

WU\_BRx is set when a remote wake-up event is detected on a branch. A WU interrupt is generated along with an EVENT\_BRx interrupt to indicate the branch where the wake-up pattern or dedicated data frame was detected.

WU\_BRx is reset after the Branch Status register has been read successfully or when the TJA1086G switches from AS\_Normal to AS\_Standby or AS\_Sleep. This ensures that a new wake-up event will be detected.

**TxE\_BRx:**

TxE\_BRx is set when a transmit error is detected on a branch, generating an EVENT\_BRx interrupt. A transmit error is detected when there is a mismatch between the transmitted and received signals.

If bit latching is enabled (BIT\_LATCHING = 1), TxE\_BRx will remain set until the register has been read, after which it is reset if no mismatch is found between transmitted and received signals or the branch leaves Branch\_Normal. If bit latching is not enabled, TxE\_BRx is reset if no mismatch is found in a data frame or the branch leaves Branch\_Normal.

**CLAMP\_BRx:**

CLAMP\_BRx is set when a branch is clamped for longer than  $t_{\text{detCL}(\text{bus})}$ , generating a CLAMP\_ERROR interrupt along with an EVENT\_BRx interrupt to indicate the branch.

If bit latching is enabled (BIT\_LATCHING = 1), CLAMP\_BRx will remain set until the register has been read, after which it is reset when idle is detected on the branch. If bit latching is not enabled, CLAMP\_BRx is reset when idle is detected on the branch.

## 8. Limiting values

**Table 13. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>BAT</sub>	battery supply voltage	[1]	-0.3	+48	V
		during load dump (400 ms max.)	-0.3	+60	V
I <sub>INH</sub>	current on pin INH	AS_Normal, AS_Standby or AS_Reset	-1	0	mA
V <sub>x</sub>	voltage on pin x[1]	on pins V <sub>CC</sub> , V <sub>BUF</sub> , V <sub>IO</sub> , TRXD0, TRXD1, BGE, TXD, TXEN, RSTN, INTN, SCSN, SCLK, SDI, SDO	-0.3	+5.5	V
		on pins INH, LWU	-0.3	V <sub>BAT</sub> + 0.3	V
		on pin RXD	-0.3	min(V <sub>IO</sub> + 0.3, 5.5)	V
		on any BM/BP pin with respect to other BP/BM pins and GND	-60	+60	V
I <sub>O(LWU)</sub>	output current on pin LWU		-15	-	mA
V <sub>trt</sub>	transient voltage	on pins LWU, V <sub>BAT</sub> , BP and BM [2]			
		pulse 1	-100	-	V
		pulse 2a	-	75	V
		pulse 3a	-150	-	V
		pulse 3b	-	100	V
T <sub>amb</sub>	ambient temperature		-40	+125	°C
T <sub>vj</sub>	virtual junction temperature	[3]	-40	+150	°C
T <sub>stg</sub>	storage temperature		-55	+150	°C
V <sub>ESD</sub>	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω) [4]			
		on pins BP and BM to GND	-6.0	+6.0	kV
		on pin LWU to GND [5]	-6.0	+6.0	kV
		on pin V <sub>BAT</sub> to GND [6]	-6.0	+6.0	kV
		Human Body Model (HBM); 100 pF, 1.5 kΩ [7]			
		on pins BP and BM to GND	-8.0	+8.0	kV
		on pins LWU and V <sub>BAT</sub> to GND [8]	-6.0	+6.0	kV
		on any other pin	-4.0	+4.0	kV
		Machine Model (MM); 200 pF, 0.75 μH, 10 Ω [9]			
		on any pin	-200	+200	V
Charged Device Model (CDM); field Induced charge; 4 pF [10]	on any pin		-1000	+1000	V

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

[2] According to IEC TS 62228 (2007), Section 4.2.4; parameters for standard pulses defined in ISO7637 part 2: 2004-06.

[3] In accordance with IEC 60747-1. An alternative definition of T<sub>vj</sub> is:  $T_{vj} = T_{amb} + P \times R_{th(j-a)}$ , where R<sub>th(j-a)</sub> is a fixed value used in the calculation of T<sub>vj</sub>. The rating for T<sub>vj</sub> limits the allowable combinations of power dissipation (P) and ambient temperature (T<sub>amb</sub>).

- [4] According to IEC TS 62228 (2007), Section 4.3; DIN EN 61000-4-2; verified by an external test house. The test result is equal to or better than  $\pm 6$  kV (unaided).
- [5] With 3.3 k $\Omega$  in series and 10 nF capacitor from LWU to GND.
- [6] With 100 nF from V<sub>BAT</sub> to GND.
- [7] According to AEC-Q100-002.
- [8] Guaranteed only when all n.c. pins are connected to GND.
- [9] According to AEC-Q100-003.
- [10] According to AEC-Q100-011 Rev-C1. The classification level is C6.

## 9. Thermal characteristics

**Table 14. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	dual-layer board <a href="#">[1]</a>	44	K/W
		four-layer board <a href="#">[2]</a>	22	K/W
R <sub>th(j-c)</sub>	thermal resistance from junction to case	in free air	3	K/W

- [1] According to JEDEC JESD51-2, JESD51-3 and JESD51-5 at natural convection on 1s board with thermal via array under the exposed pad connected to the second copper layer.
- [2] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35  $\mu\text{m}$ ) and thermal via array under the exposed pad connected to the first inner copper layer.

## 10. Static characteristics

**Table 15. Static characteristics**

All parameters are guaranteed for  $V_{BAT} = 4.45\text{ V to }60\text{ V}$ ;  $V_{CC} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{BUF} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{IO} = 2.55\text{ V to }5.25\text{ V}$ ;  $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$ ;  $C_{bus} = 100\text{ pF}$ ;  $R_{bus} = 40\text{ }\Omega\text{ to }55\text{ }\Omega$ ;  $C_{RXD} = 15\text{ pF}$  and  $C_{TRXD0} = C_{TRXD1} = 50\text{ pF}$  unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supply: pin <math>V_{BAT}</math></b>						
$V_{BAT}$	battery supply voltage	operating range	4.75	-	60	V
$I_{BAT}$	battery supply current	AS_Normal; no load on INH	-	0.1	1	mA
		AS_Standby; no load on INH; wake-up enabled on both branches; bits [7:6] in Configuration register (Table 9) set to 11	-	50	100	$\mu\text{A}$
		AS_Standby; no load on INH; wake-up enabled on both branches; bits [7:6] in Configuration register set to 00	-	38	80	$\mu\text{A}$
		AS_Sleep; wake-up enabled on both branches; bits [7:6] in Configuration register set to 11	-	50	100	$\mu\text{A}$
		AS_Sleep; wake-up enabled on both branches; bits [7:6] in Configuration register set to 00	-	38	80	$\mu\text{A}$
		AS_Sleep; wake-up enabled on both branches; bits [7:6] in Configuration register set to 11; $T_{vj} \leq 85\text{ }^{\circ}\text{C}$	-	50	90	$\mu\text{A}$
		AS_Sleep; wake-up enabled on both branches; bits [7:6] in Configuration register set to 00; $T_{vj} \leq 85\text{ }^{\circ}\text{C}$	-	38	70	$\mu\text{A}$
		AS_Sleep; wake-up disabled on both branches	-	25	55	$\mu\text{A}$
		AS_Sleep; wake-up disabled on both branches; $T_{vj} \leq 85\text{ }^{\circ}\text{C}$	-	25	45	$\mu\text{A}$
$V_{uvd}$	undervoltage detection voltage		4.45	-	4.715	V
$V_{uvr}$	undervoltage recovery voltage		4.475	-	4.74	V
$V_{uvhys}$	undervoltage hysteresis voltage		25	-	290	mV
<b>Power-on reset for <math>V_{DIG}</math></b>						
$V_{th(det)POR}$	power-on reset detection threshold voltage	of internal digital circuitry	3	-	3.4	V
$V_{th(rec)POR}$	power-on reset recovery threshold voltage	of internal digital circuitry	3.1	-	3.5	V
$V_{hys(POR)}$	power-on reset hysteresis voltage	of internal digital circuitry	100	-	500	mV

**Table 15. Static characteristics ...continued**

All parameters are guaranteed for  $V_{BAT} = 4.45\text{ V}$  to  $60\text{ V}$ ;  $V_{CC} = 4.45\text{ V}$  to  $5.25\text{ V}$ ;  $V_{BUF} = 4.45\text{ V}$  to  $5.25\text{ V}$ ;  $V_{IO} = 2.55\text{ V}$  to  $5.25\text{ V}$ ;  $T_{vj} = -40\text{ }^{\circ}\text{C}$  to  $+150\text{ }^{\circ}\text{C}$ ;  $C_{bus} = 100\text{ pF}$ ;  $R_{bus} = 40\text{ }\Omega$  to  $55\text{ }\Omega$ ;  $C_{RXD} = 15\text{ pF}$  and  $C_{TRXD0} = C_{TRXD1} = 50\text{ pF}$  unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$\Delta V_{(VCC-VDIG)}$	voltage difference between $V_{CC}$ and $V_{DIG}$	$V_{CC} = 4.45\text{ V}$ ; $V_{BAT} = V_{BUF} = 0\text{ V}$	-	-	1.0	V	
$\Delta V_{(VBAT-VDIG)}$	voltage difference between $V_{BAT}$ and $V_{DIG}$	$V_{BAT} = 4.45\text{ V}$ ; $V_{CC} = V_{BUF} = 0\text{ V}$	-	-	1.0	V	
$\Delta V_{(VBUF-VDIG)}$	voltage difference between $V_{BUF}$ and $V_{DIG}$	$V_{BUF} = 4.45\text{ V}$ ; $V_{CC} = V_{BAT} = 0\text{ V}$	-	-	1.0	V	
<b>Supply: pins <math>V_{CC1}</math> and <math>V_{CC2}</math> (connected on the PCB)</b>							
$V_{CC}$	supply voltage	operating range	4.75	-	5.25	V	
$I_{CC}$	supply current	AS_Normal; $V_{TXEN} = 0\text{ V}$ ; $V_{BGE} = V_{IO}$ ; $R_{bus} = 45\text{ }\Omega$ ; both branches in Branch_Normal; bits [5:2] in Control register (Table 8) set to 0000	[1]	-	95	120	mA
		AS_Normal; $V_{TXEN} = 0\text{ V}$ ; $V_{BGE} = V_{IO}$ ; $R_{bus} = 45\text{ }\Omega$ ; both branches in Branch_Normal; bits [5:2] in Control register set to 1111	[1]	-	95	120	mA
		AS_Normal; $V_{TXEN} = V_{IO}$ ; $V_{BGE} = 0\text{ V}$ ; $R_{bus} = 45\text{ }\Omega$ ; both branches in Branch_Normal and/or Branch_Disabled	[1]	-	-	80	mA
		AS_Standby	[1][2]	-	4	35	$\mu\text{A}$
		AS_Standby; $T_{vj} \leq 85\text{ }^{\circ}\text{C}$	[1][2]	-	4	15	$\mu\text{A}$
		AS_Sleep, AS_Reset	[1][2]	-	0	30	$\mu\text{A}$
		AS_Sleep, AS_Reset; $T_{vj} \leq 85\text{ }^{\circ}\text{C}$	[1][2]	-	0	10	$\mu\text{A}$
		$V_{uvd}$	undervoltage detection voltage		4.45	-	4.715
$V_{uvr}$	undervoltage recovery voltage		4.475	-	4.74	V	
$V_{uvhys}$	undervoltage hysteresis voltage		25	-	290	mV	
<b>Supply: pins <math>V_{BUF1}</math> and <math>V_{BUF2}</math> (connected on the PCB)</b>							
$V_{BUF}$	supply voltage on pin $V_{BUF}$	$5.5\text{ V} \leq V_{BAT} \leq 60\text{ V}$ ; $V_{CC} \leq V_{uvd}(V_{CC})$		4.5	-	5.25	V
		$4.5\text{ V} \leq V_{BAT} \leq 5.5\text{ V}$ ; $V_{CC} \leq V_{uvd}(V_{CC})$		3.5	-	5.25	V
$\Delta V_{(VCC-VBUF)}$	voltage difference between $V_{CC}$ and $V_{BUF}$	$V_{CC} \geq V_{uvr}(V_{CC})$	0	-	0.25	V	
$I_{ch}(VBAT-VBUF)$	charge current from $V_{BAT}$ to $V_{BUF}$	$5.5\text{ V} \leq V_{BAT} \leq 60\text{ V}$ ; $V_{CC} \leq V_{uvd}(V_{CC})$ ; $0\text{ V} \leq V_{BUF} \leq 4\text{ V}$	-200	-100	-30	$\mu\text{A}$	
$V_{uvd}$	undervoltage detection voltage		4.2	-	4.474	V	
$V_{uvr}$	undervoltage recovery voltage		4.225	-	4.499	V	

**Table 15. Static characteristics ...continued**

All parameters are guaranteed for  $V_{BAT} = 4.45\text{ V to }60\text{ V}$ ;  $V_{CC} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{BUF} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{IO} = 2.55\text{ V to }5.25\text{ V}$ ;  $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$ ;  $C_{bus} = 100\text{ pF}$ ;  $R_{bus} = 40\text{ }\Omega\text{ to }55\text{ }\Omega$ ;  $C_{RXD} = 15\text{ pF}$  and  $C_{TRXD0} = C_{TRXD1} = 50\text{ pF}$  unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{uvhys}$	undervoltage hysteresis voltage		25	-	299	mV
<b>Supply: pin <math>V_{IO}</math></b>						
$V_{IO}$	supply voltage on pin $V_{IO}$	operating range	2.8	-	5.25	V
$I_{IO}$	supply current on pin $V_{IO}$	AS_Normal; $V_{TXD} = V_{IO}$	-	-	1	mA
		AS_Standby; AS_Sleep; AS_PowerOff; $V_{SCSN} = V_{TXEN} = V_{RSTN} = V_{VIO}$	-	2	7	$\mu\text{A}$
$I_r$	reverse current	from digital input pin to $V_{IO}$ ; AS_PowerOff; $V_{TXEN} = V_{TXD} = V_{BGE} = V_{SCSN} =$ $V_{SCLK} = V_{SDI} = V_{RSTN} = 5.25\text{ V}$ ; $V_{CC} = V_{IO} = 0\text{ V}$	-5	-	+5	$\mu\text{A}$
$V_{uvd}$	undervoltage detection voltage		2.55	-	2.765	V
$V_{uvr}$	undervoltage recovery voltage		2.575	-	2.79	V
$V_{uvhys}$	undervoltage hysteresis voltage		25	-	240	mV
<b>Pin TXEN</b>						
$V_{IH}$	HIGH-level input voltage	AS_Normal	$0.7V_{IO}$	-	5.5	V
$V_{IL}$	LOW-level input voltage	AS_Normal	-0.3	-	$0.3V_{IO}$	V
$I_{IH}$	HIGH-level input current	$V_{TXEN} = V_{IO}$	-2	-	+2	$\mu\text{A}$
$I_{IL}$	LOW-level input current	$V_{TXEN} = 0.3V_{IO}$	-300	-	-50	$\mu\text{A}$
<b>Pin TXD</b>						
$V_{IH}$	HIGH-level input voltage	AS_Normal	$0.6V_{IO}$	-	5.5	V
$V_{IL}$	LOW-level input voltage	AS_Normal	-0.3	-	$0.4V_{IO}$	V
$R_{pd}$	pull-down resistance	to GND	50	150	400	$\text{k}\Omega$
$C_i$	input capacitance	with respect to all other pins at ground; $V_{TXD} = 100\text{ mV}$ ; $f = 5\text{ MHz}$	<sup>[3]</sup>	-	10	pF
<b>Pin BGE</b>						
$V_{IH}$	HIGH-level input voltage	AS_Normal	$0.7V_{IO}$	-	5.5	V
$V_{IL}$	LOW-level input voltage	AS_Normal	-0.3	-	$0.3V_{IO}$	V
$R_{pd}$	pull-down resistance	to GND	50	150	400	$\text{k}\Omega$
<b>Pin RXD</b>						
$I_{OH}$	HIGH-level output current	$V_{RXD} = V_{IO} - 0.4\text{ V}$	-15	-	-1	mA
$I_{OL}$	LOW-level output current	$V_{RXD} = 0.4\text{ V}$	1	-	15	mA
$V_{OH}$	HIGH-level output voltage	$I_{OH(RXD)} = -1\text{ mA}$	$V_{IO} - 0.4$	-	$V_{IO}$	V
$V_{OL}$	LOW-level output voltage	$I_{OL(RXD)} = 1\text{ mA}$	-	-	0.4	V

**Table 15. Static characteristics ...continued**

All parameters are guaranteed for  $V_{BAT} = 4.45\text{ V to }60\text{ V}$ ;  $V_{CC} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{BUF} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{IO} = 2.55\text{ V to }5.25\text{ V}$ ;  $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$ ;  $C_{bus} = 100\text{ pF}$ ;  $R_{bus} = 40\text{ }\Omega\text{ to }55\text{ }\Omega$ ;  $C_{RXD} = 15\text{ pF}$  and  $C_{TRXD0} = C_{TRXD1} = 50\text{ pF}$  unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V <sub>O</sub>	output voltage	when undervoltage on V <sub>IO</sub> ; V <sub>CC</sub> ≥ 4.75 V; R <sub>L</sub> = 100 kΩ to GND	-	-	500	mV	
		V <sub>CC</sub> = V <sub>BAT</sub> = V <sub>BUF</sub> = 0 V; R <sub>L</sub> = 100 kΩ to V <sub>IO</sub>	V <sub>IO</sub> - 500	-	V <sub>IO</sub>	mV	
<b>Pin RSTN</b>							
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>IO</sub>	-	5.5	V	
V <sub>IL</sub>	LOW-level input voltage		-0.3	-	0.3V <sub>IO</sub>	V	
I <sub>IH</sub>	HIGH-level input current	V <sub>RSTN</sub> = V <sub>IO</sub>	-1	-	+1	μA	
I <sub>IL</sub>	LOW-level input current	V <sub>RSTN</sub> = 0.3V <sub>IO</sub>	-300	-	-30	μA	
<b>Pins TRXD0 and TRXD1</b>							
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>BUF</sub>	-	5.5	V	
V <sub>IL</sub>	LOW-level input voltage		-0.3	-	0.3V <sub>BUF</sub>	V	
V <sub>OL</sub>	LOW-level output voltage	R <sub>pu</sub> = 200 Ω	-0.3	-	+0.8	V	
C <sub>i</sub>	input capacitance	with respect to all other pins at GND; V <sub>TXD</sub> = 100 mV; f = 5 MHz	[3]	-	15	pF	
R <sub>pu</sub>	pull-up resistance	to V <sub>BUF</sub>	2.5	5	10	kΩ	
<b>Pins BP and BM</b>							
V <sub>IH(dif)</sub>	differential HIGH-level input voltage	AS_Normal; -10 V ≤ V <sub>cm</sub> ≤ +15 V	[4]	150	-	300	mV
V <sub>IL(dif)</sub>	differential LOW-level input voltage	AS_Normal; -10 V ≤ V <sub>cm</sub> ≤ +15 V	[4]	-300	-	-150	mV
		AS_Standby; AS_Sleep; -10 V ≤ V <sub>cm</sub> ≤ +15 V	[4]	-400	-	-125	mV
ΔV <sub>i(dif)(H-L)</sub>	differential input voltage difference between HIGH-level and LOW-level	V <sub>cm</sub> = 2.5 V; AS_Normal	[4]	-30	-	+30	mV
V <sub>OH(dif)</sub>	differential HIGH-level output voltage	4.75 V ≤ V <sub>BUF</sub> ≤ 5.25 V		600	-	2000	mV
		4.45 V ≤ V <sub>BUF</sub> ≤ 5.25 V		530	-	2000	mV
V <sub>OL(dif)</sub>	differential LOW-level output voltage	4.75 V ≤ V <sub>BUF</sub> ≤ 5.25 V		-2000	-	-600	mV
		4.45 V ≤ V <sub>BUF</sub> ≤ 5.25 V		-2000	-	-530	mV
V <sub>O(idle)(BP)</sub>	idle output voltage on pin BP	Branch_Normal		0.4V <sub>BUF</sub>	-	0.6V <sub>BUF</sub>	V
		Branch_LowPower		-0.1	-	+0.1	V
V <sub>O(idle)(BM)</sub>	idle output voltage on pin BM	Branch_Normal		0.4V <sub>BUF</sub>	-	0.6V <sub>BUF</sub>	V
		Branch_LowPower		-0.1	-	+0.1	V
I <sub>O(idle)BP</sub>	idle output current on pin BP	-60 V ≤ V <sub>BP</sub> ≤ +60 V; no bus load		-7.5	-	+7.5	mA
I <sub>O(idle)BM</sub>	idle output current on pin BM	-60 V ≤ V <sub>BM</sub> ≤ +60 V; no bus load		-7.5	-	+7.5	mA
V <sub>O(idle)(dif)</sub>	differential idle output voltage			-25	0	+25	mV
V <sub>i(dif)det(act)</sub>	activity detection differential input voltage (absolute value)	AS_Normal; -10 V ≤ V <sub>cm</sub> ≤ +15 V	[4]	150	-	300	mV
V <sub>cm(bus)(DATA_0)</sub>	DATA_0 bus common-mode voltage	Branch_Transmit		0.4V <sub>BUF</sub>	-	0.65 × V <sub>BUF</sub>	V

**Table 15. Static characteristics ...continued**

All parameters are guaranteed for  $V_{BAT} = 4.45\text{ V to }60\text{ V}$ ;  $V_{CC} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{BUF} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{IO} = 2.55\text{ V to }5.25\text{ V}$ ;  $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$ ;  $C_{bus} = 100\text{ pF}$ ;  $R_{bus} = 40\text{ }\Omega\text{ to }55\text{ }\Omega$ ;  $C_{RXD} = 15\text{ pF}$  and  $C_{TRXD0} = C_{TRXD1} = 50\text{ pF}$  unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$V_{cm(bus)(DATA\_1)}$	DATA_1 bus common-mode voltage	Branch_Transmit	$0.4V_{BUF}$	-	$0.65 \times V_{BUF}$	V	
$R_i$	input resistance	$R_{bus} = \infty\ \Omega$	10	20	40	k $\Omega$	
$R_{i(dif)(BP-BM)}$	differential input resistance between pin BP and pin BM	$R_{bus} = \infty\ \Omega$	20	40	80	k $\Omega$	
$Z_{o(eq)TX}$	transmitter equivalent output impedance	$C_{bus} = 100\text{ pF}$ ; $R_{bus} = 40\ \Omega$ or $100\ \Omega$	[5]	35	100	$\Omega$	
$C_{i(BP)}$	input capacitance on pin BP	with respect to all other pins at GND; $V_{BP} = 100\text{ mV}$ ; $f = 5\text{ MHz}$	[3]	-	15	pF	
$C_{i(BM)}$	input capacitance on pin BM	with respect to all other pins at GND; $V_{BM} = 100\text{ mV}$ ; $f = 5\text{ MHz}$	[3]	-	15	pF	
$C_{i(dif)(BP-BM)}$	differential input capacitance between pin BP and pin BM	$V_{BP} = 100\text{ mV}$ ; $V_{BM} = 100\text{ mV}$ ; $f = 5\text{ MHz}$	[3]	-	5	pF	
$I_{L(BP)}$	input leakage current on pin BP	AS_PowerOff; $V_{BP} = V_{BM}$ ; $0\text{ V} \leq V_{BP} \leq 5\text{ V}$		-5	0	+5	$\mu\text{A}$
		loss of ground; $V_{BP} = V_{BM} = 0\text{ V}$ ; all other pins connected to 16 V via $0\ \Omega$	[3]	-1600	-	+1600	$\mu\text{A}$
$I_{L(BM)}$	input leakage current on pin BM	AS_PowerOff; $V_{BP} = V_{BM}$ ; $0\text{ V} \leq V_{BM} \leq 5\text{ V}$		-5	0	+5	$\mu\text{A}$
		loss of ground; $V_{BP} = V_{BM} = 0\text{ V}$ ; all other pins connected to 16 V via $0\ \Omega$	[3]	-1600	-	+1600	$\mu\text{A}$
$ I_{O(sc)} $	short-circuit output current (absolute value)	on pin BP; $-5\text{ V} \leq V_{BP} \leq +60\text{ V}$ ; $R_{sc} \leq 1\ \Omega$ ; $t_{sc} \geq 1500\ \mu\text{s}$	[6][8]	-	-	60	mA
		on pin BM; $-5\text{ V} \leq V_{BM} \leq +60\text{ V}$ ; $R_{sc} \leq 1\ \Omega$ ; $t_{sc} \geq 1500\ \mu\text{s}$	[6][8]	-	-	60	mA
		on pins BP and BM; $V_{BP} = V_{BM}$ ; $R_{sc} \leq 1\ \Omega$ ; $t_{sc} \geq 1500\ \mu\text{s}$	[7][8]	-	-	60	mA
<b>Pin INH</b>							
$V_{OH}$	HIGH-level output voltage	$I_{INH} = -0.2\text{ mA}$ ; AS_Normal; AS_Standby; AS_Reset		$V_{BAT} - 0.8$	-	$V_{BAT}$	V
$I_L$	leakage current	AS_Sleep; AS_PowerOff		-3	-	+3	$\mu\text{A}$
$I_{O(sc)}$	short-circuit output current	$V_{INH} = 0\text{ V}$ ; AS_Normal; AS_Standby; AS_Reset		-7	-	-1	mA
<b>Pin LWU</b>							
$V_{th(wake)LWU}$	wake-up threshold voltage on pin LWU	AS_Sleep; AS_Standby		2	-	3.75	V
$V_{hys(wake)LWU}$	wake-up hysteresis voltage on pin LWU			0.3	-	1.2	V
$I_{IL}$	LOW-level input current	$V_{LWU} = 2\text{ V}$ for $t > t_{det(wake)(LWU)}$		3	-	11	$\mu\text{A}$
		$V_{LWU} = 0\text{ V}$		-2	-	-0.3	$\mu\text{A}$



**Table 15. Static characteristics ...continued**

All parameters are guaranteed for  $V_{BAT} = 4.45\text{ V to }60\text{ V}$ ;  $V_{CC} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{BUF} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{IO} = 2.55\text{ V to }5.25\text{ V}$ ;  $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$ ;  $C_{bus} = 100\text{ pF}$ ;  $R_{bus} = 40\text{ }\Omega\text{ to }55\text{ }\Omega$ ;  $C_{RXD} = 15\text{ pF}$  and  $C_{TRXD0} = C_{TRXD1} = 50\text{ pF}$  unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>IH</sub>	HIGH-level input current	$V_{LWU} = 3.75\text{ V}$ for $t > t_{det(wake)(LWU)}$ ; $4.75\text{ V} \leq V_{BAT} \leq +60\text{ V}$	-11	-	-3	$\mu\text{A}$
		$V_{LWU} = V_{BAT}$	0.2	-	1.2	$\mu\text{A}$
<b>Pin SDO</b>						
V <sub>OH</sub>	HIGH-level output voltage	$I_{OH(SDO)} = -0.5\text{ mA}$	$V_{IO} - 0.4$	-	$V_{IO}$	V
V <sub>OL</sub>	LOW-level output voltage	$I_{OL(SDO)} = 0.5\text{ mA}$	-	-	0.4	V
I <sub>OH</sub>	HIGH-level output current	$V_{SDO} = V_{IO} - 0.4\text{ V}$	-8	-2	-0.5	mA
I <sub>OL</sub>	LOW-level output current	$V_{SDO} = 0.4\text{ V}$	0.5	2	8	mA
I <sub>L</sub>	leakage current	SCSN HIGH	-5	-	+5	$\mu\text{A}$
V <sub>O</sub>	output voltage	when undervoltage on $V_{IO}$ ; $V_{CC} \geq 4.75\text{ V}$ ; $R_L = 100\text{ k}\Omega$ to GND	-	-	500	mV
		$V_{CC} = V_{BAT} = V_{BUF} = 0\text{ V}$ ; $R_L = 100\text{ k}\Omega$ to GND	-	-	500	mV
<b>Pin SDI</b>						
V <sub>IH</sub>	HIGH-level input voltage		$0.7V_{IO}$	-	5.5	V
V <sub>IL</sub>	LOW-level input voltage		-0.3	-	$0.3V_{IO}$	V
R <sub>pd</sub>	pull-down resistance	to GND	50	150	400	k $\Omega$
<b>Pin SCSN</b>						
V <sub>IH</sub>	HIGH-level input voltage		$0.7V_{IO}$	-	5.5	V
V <sub>IL</sub>	LOW-level input voltage		-0.3	-	$0.3V_{IO}$	V
I <sub>IH</sub>	HIGH-level input current	$V_{SCSN} = V_{IO}$	-1	-	+1	$\mu\text{A}$
I <sub>IL</sub>	LOW-level input current	$V_{SCSN} = 0.3V_{IO}$	-15	-	-3	$\mu\text{A}$
<b>Pin SCLK</b>						
V <sub>IH</sub>	HIGH-level input voltage		$0.7V_{IO}$	-	5.5	V
V <sub>IL</sub>	LOW-level input voltage		-0.3	-	$0.3V_{IO}$	V
R <sub>pd</sub>	pull-down resistance	to GND	50	150	400	k $\Omega$
<b>Pin INTN</b>						
V <sub>OL</sub>	LOW-level output voltage	$I_{OL(INTN)} = 0.5\text{ mA}$	-	-	0.4	V
V <sub>O</sub>	output voltage	when undervoltage on $V_{IO}$ ; $V_{CC} \geq 4.75\text{ V}$ ; $R_L = 100\text{ k}\Omega$ to GND	-	-	500	mV
		$V_{CC} = V_{BAT} = V_{BUF} = 0\text{ V}$ ; $R_L = 100\text{ k}\Omega$ to GND	-	-	500	mV
<b>Temperature protection</b>						
T <sub>j(warn)</sub>	warning junction temperature		155	-	190	$^{\circ}\text{C}$
T <sub>j(high)</sub>	high junction temperature		165	-	200	$^{\circ}\text{C}$
$\Delta T_{j(high-warn)}$	difference between high and warning junction temperature		10	-	45	$^{\circ}\text{C}$

[1] Specified current is the sum of currents I<sub>CC1</sub> and I<sub>CC2</sub>.

- [2] These values are guaranteed under the condition that the internal digital block is supplied from  $V_{BAT}$ .
- [3] Not tested in production; guaranteed by design.
- [4]  $V_{cm}$  is the BP/BM common mode voltage ( $V_{cm} = (V_{BP} + V_{BM})/2$ ).
- [5]  $Z_{O(eq)(TX)} = 50 \Omega \times (V_{bus(100)} - V_{bus(40)}) / (2.5 \times V_{bus(40)} - V_{bus(100)})$  where:
  - $V_{bus(100)}$  is the differential output voltage on a load of 100  $\Omega$  and 100 pF in parallel
  - $V_{bus(40)}$  is the differential output voltage on a load of 40  $\Omega$  and 100 pF in parallel when driving a DATA\_1.
- [6]  $R_{sc}$  is the short-circuit resistance; voltage difference between bus pins BP and BM is 60 V max.
- [7]  $R_{sc}$  is the short-circuit resistance between BP and BM.
- [8]  $t_{sc}$  is the minimum duration of the short-circuit

## 11. Dynamic characteristics

**Table 16. Dynamic characteristics**

All parameters are guaranteed for  $V_{BAT} = 4.45\text{ V to }60\text{ V}$ ;  $V_{CC} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{BUF} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{IO} = 2.55\text{ V to }5.25\text{ V}$ ;  $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$ ;  $R_{bus} = 40\ \Omega$ ,  $C_{bus} = 100\text{ pF}$ ;  $C_{RXD} = 15\text{ pF}$ ;  $C_{TRXD0} = C_{TRXD1} = 50\text{ pF}$  and  $C_{SDO} = 50\text{ pF}$  unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Undervoltage detection</b>						
$t_{det(uv)(VBAT)}$	undervoltage detection time on pin $V_{BAT}$	$V_{BAT} = 4.35\text{ V}$	5	-	150	$\mu\text{s}$
$t_{rec(uv)(VBAT)}$	undervoltage recovery time on pin $V_{BAT}$	$V_{BAT} = 4.85\text{ V}$	5	-	150	$\mu\text{s}$
$t_{det(uv)(VCC)}$	undervoltage detection time on pin $V_{CC}$	$V_{CC} = 4.35\text{ V}$	5	-	100	$\mu\text{s}$
$t_{rec(uv)(VCC)}$	undervoltage recovery time on pin $V_{CC}$	$V_{CC} = 4.85\text{ V}$	5	-	100	$\mu\text{s}$
$t_{det(uv)(VBUF)}$	undervoltage detection time on pin $V_{BUF}$	$V_{BUF} = 4.10\text{ V}$	5	-	100	$\mu\text{s}$
$t_{rec(uv)(VBUF)}$	undervoltage recovery time on pin $V_{BUF}$	$V_{BUF} = 4.6\text{ V}$	5	-	100	$\mu\text{s}$
$t_{det(uv)(VIO)}$	undervoltage detection time on pin $V_{IO}$	$V_{IO} = 2.45\text{ V}$	5	-	100	$\mu\text{s}$
$t_{rec(uv)(VIO)}$	undervoltage recovery time on pin $V_{IO}$	$V_{IO} = 2.9\text{ V}$	5	-	100	$\mu\text{s}$
$t_{to(ugd)(VCC)}$	undervoltage detection time-out time on pin $V_{CC}$		100	-	670	ms
$t_{to(ugd)(VIO)}$	undervoltage detection time-out time on pin $V_{IO}$		100	-	670	ms
$t_{to(ugr)(VCC)}$	undervoltage recovery time-out time on pin $V_{CC}$		1	-	5	ms
$t_{to(ugr)(VIO)}$	undervoltage recovery time-out time on pin $V_{IO}$		1	-	5	ms
<b>SPI</b>						
$t_{cy}(clk)$	clock cycle time		0.5	-	100	$\mu\text{s}$
$t_{SPILEAD}$	SPI enable lead time		250	-	-	ns
$t_{SPILAG}$	SPI enable lag time		250	-	-	ns
$t_{su}(D)$	data input set-up time		150	-	-	ns
$t_{h}(D)$	data input hold time		100	-	-	ns
$t_{d}(SCLK-SDO)$	delay time from SCLK to SDO		-	-	200	ns
$t_{WH}(S)$	chip select pulse width HIGH		10	-	-	$\mu\text{s}$
$t_{d}(SCSNHL-SDOL)$	SCSN falling edge to SDO LOW-level delay time		-	-	250	ns
$t_{d}(SCSNLH-SDOZ)$	SCSN rising edge to SDO three-state delay time		-	-	500	ns

**Table 16. Dynamic characteristics ...continued**

All parameters are guaranteed for  $V_{BAT} = 4.45\text{ V to }60\text{ V}$ ;  $V_{CC} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{BUF} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{IO} = 2.55\text{ V to }5.25\text{ V}$ ;  $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$ ;  $R_{bus} = 40\ \Omega$ ,  $C_{bus} = 100\text{ pF}$ ;  $C_{RXD} = 15\text{ pF}$ ;  $C_{TRXD0} = C_{TRXD1} = 50\text{ pF}$  and  $C_{SD0} = 50\text{ pF}$  unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Transmit path</b>						
$t_{d(\text{TXD-bus})}$	delay time from TXD to bus	AS_Normal; see <a href="#">Figure 10</a>	[1]			
		DATA_0	-	-	75	ns
		DATA_1	-	-	75	ns
$\Delta t_{d(\text{TXD-bus})}$	delay time difference from TXD to bus	between DATA_0 and DATA_1; AS_Normal	[1] [2]	-5	+5	ns
$t_{d(\text{TXD-TRXD})}$	delay time from TXD to TRXD	AS_Normal; see <a href="#">Figure 10</a>	[1]			
		DATA_0	-	-	60	ns
		DATA_1	-	-	60	ns
$\Delta t_{d(\text{TXD-TRXD})}$	delay time difference from TXD to TRXD	between DATA_0 and DATA_1; AS_Normal	[1]	-5	+5	ns
$t_{d(\text{TRXD-bus})}$	delay time from TRXD to bus	AS_Normal; see <a href="#">Figure 12</a>				
		DATA_0	-	-	75	ns
		DATA_1	-	-	75	ns
$\Delta t_{d(\text{TRXD-bus})}$	delay time difference from TRXD to bus	between DATA_0 and DATA_1; AS_Normal	[2]	-5	+5	ns
$t_{d(\text{TXEN-busact})}$	delay time from TXEN to bus active	AS_Normal; from idle to active	-	-	175	ns
$t_{d(\text{TXEN-busidle})}$	delay time from TXEN to bus idle	AS_Normal; from active to idle	-	-	150	ns
$t_{d(\text{TXEN-RXD})}$	delay time from TXEN to RXD		-	-	150	ns
$t_{d(\text{TRXD-busact})}$	delay time from TRXD to bus active	$t_{\text{det}(\text{act})(\text{TRXD})} + t_{d(\text{TRXD-bus})}$	-	-	275	ns
$t_{d(\text{TRXD-busidle})}$	delay time from TRXD to bus idle	$t_{\text{det}(\text{idle})(\text{TRXD})} + t_{d(\text{TRXD-bus})}$	-	-	275	ns
$t_{d(\text{busact-TRXD})}$	delay time from bus active to TRXD	$t_{\text{det}(\text{act})(\text{bus})} + t_{d(\text{bus-TRXD})}$	-	-	285	ns
$t_{d(\text{busidle-TRXD})}$	delay time from bus idle to TRXD	$t_{\text{det}(\text{idle})(\text{bus})} + t_{d(\text{bus-TRXD})}$	-	-	275	ns
$t_{d(\text{TRXDact-RXD})}$	delay time from TRXD activity detection to RXD	$t_{\text{det}(\text{act})(\text{TRXD})} + t_{d(\text{TRXD-RXD})}$	-	-	260	ns
$t_{d(\text{busact-bus})}$	delay time from bus active to bus	from one branch to another, including activity detection time; $t_{\text{det}(\text{act})(\text{bus})} + t_{d(\text{bus-bus})}$	-	-	330	ns
$t_{d(\text{busidle-bus})}$	delay time from bus idle to bus	from one branch to another, including idle detection time; $t_{\text{det}(\text{idle})(\text{bus})} + t_{d(\text{bus-bus})}$	-	-	320	ns
<b>Receive path</b>						
$t_{d(\text{bus-TRXD})}$	delay time from bus to TRXD	AS_Normal; see <a href="#">Figure 11</a>				
		DATA_0	-	-	75	ns
		DATA_1	-	-	75	ns
$\Delta t_{d(\text{bus-TRXD})}$	delay time difference from bus to TRXD	between DATA_0 and DATA_1 AS_Normal; $V_{cm} = 2.5\text{ V}$ $R_{pu} = 200\ \Omega$	[2] [3]	-5	+5	ns

**Table 16. Dynamic characteristics ...continued**

All parameters are guaranteed for  $V_{BAT} = 4.45\text{ V to }60\text{ V}$ ;  $V_{CC} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{BUF} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{IO} = 2.55\text{ V to }5.25\text{ V}$ ;  $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$ ;  $R_{bus} = 40\text{ }\Omega$ ,  $C_{bus} = 100\text{ pF}$ ;  $C_{RXD} = 15\text{ pF}$ ;  $C_{TRXD0} = C_{TRXD1} = 50\text{ pF}$  and  $C_{SDO} = 50\text{ pF}$  unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$t_{d(\text{bus-RXD})}$	delay time from bus to RXD	AS_Normal; see <a href="#">Figure 11</a>					
		DATA_0	-	-	75	ns	
		DATA_1	-	-	75	ns	
$\Delta t_{d(\text{bus-RXD})}$	delay time difference from bus to RXD	between DATA_0 and DATA_1 AS_Normal; $V_{cm} = 2.5\text{ V}$	<a href="#">[2]</a> <a href="#">[3]</a>	-5	-	+5	ns
$t_{d(\text{TRXD-RXD})}$	delay time from TRXD to RXD	AS_Normal; see <a href="#">Figure 12</a>					
		DATA_0	-	-	60	ns	
		DATA_1	-	-	60	ns	
$\Delta t_{d(\text{TRXD-RXD})}$	delay time difference from TRXD to RXD	between DATA_0 and DATA_1 AS_Normal		-5	-	+5	ns
$t_{d(\text{TXD-RXD})}$	delay time from TXD to RXD	AS_Normal; see <a href="#">Figure 10</a>	<a href="#">[1]</a>				
		DATA_0	-	30	60	ns	
		DATA_1	-	30	60	ns	
$t_{d(\text{bus-bus})}$	delay time from bus to bus	from one branch to another AS_Normal; see <a href="#">Figure 11</a>					
		DATA_0	-	-	120	ns	
		DATA_1	-	-	120	ns	
$\Delta t_{d(\text{bus-bus})}$	delay time difference from bus to bus	between DATA_0 and DATA_1 AS_Normal		-8	-	+8	ns
<b>Bus slope</b>							
$t_{r(\text{dif})(\text{bus})}$	bus differential rise time	DATA_0 to DATA_1; 20 % to 80 %	6	-	18.75	ns	
		DATA_0 to idle; -300 mV to -30 mV	-	-	30	ns	
$t_{f(\text{dif})(\text{bus})}$	bus differential fall time	DATA_1 to DATA_0; 20 % to 80 %	6	-	18.75	ns	
		DATA_1 to idle; 300 mV to 30 mV	-	-	30	ns	
		idle to DATA_0; -30 mV to -300 mV	-	-	30	ns	
$\Delta t_{(r-f)(\text{dif})}$	difference between differential rise and fall time	between DATA_0 and DATA_1		-3	-	+3	ns
<b>Pin RXD</b>							
$t_r$	rise time	20 % to 80 %	-	-	9	ns	
$t_f$	fall time	80 % to 20 %	-	-	9	ns	
$t_{(r+f)}$	sum of rise and fall time	20 % to 80 % and 80 % to 20 %	-	-	13	ns	
$\Delta t_{(r-f)}$	difference between rise and fall time	20 % to 80 %		-5	-	+5	ns
<b>Pin RSTN</b>							
$t_{\text{def}(\text{rst})}$	reset detection time		5	-	20	$\mu\text{s}$	
<b>Pin BGE</b>							
$t_{d(\text{BGE-busact})}$	delay time from BGE to bus active	activity detected on TXEN	-	-	100	ns	
$t_{d(\text{BGE-busidle})}$	delay time from BGE to bus idle	activity detected on TXEN	-	-	100	ns	

**Table 16. Dynamic characteristics ...continued**

All parameters are guaranteed for  $V_{BAT} = 4.45\text{ V to }60\text{ V}$ ;  $V_{CC} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{BUF} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{IO} = 2.55\text{ V to }5.25\text{ V}$ ;  $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$ ;  $R_{bus} = 40\ \Omega$ ,  $C_{bus} = 100\text{ pF}$ ;  $C_{RXD} = 15\text{ pF}$ ;  $C_{TRXD0} = C_{TRXD1} = 50\text{ pF}$  and  $C_{SDO} = 50\text{ pF}$  unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

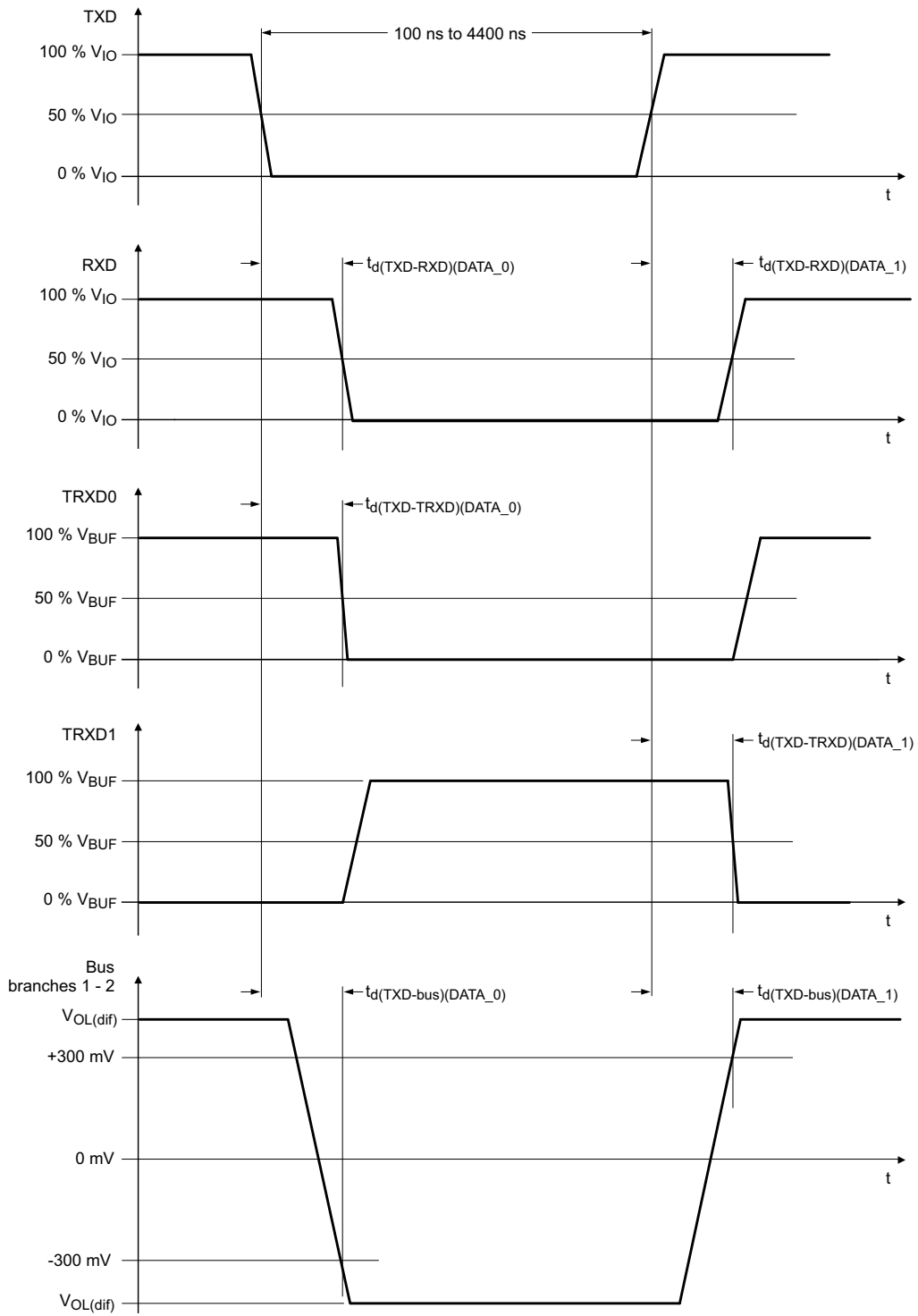
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Activity detection</b>							
$t_{det(act)}(TXEN)$	activity detection time on pin TXEN	AS_Normal; from idle to active	20	-	70	ns	
$t_{det(idle)}(TXEN)$	idle detection time on pin TXEN	AS_Normal; from active to idle	20	-	70	ns	
$\Delta t_{det(act-idle)}$	difference between active and idle detection time						
	on pin TXEN	AS_Normal	-25	-	+25	ns	
	on pin TRXD	pins TRXD0 and TRXD1; AS_Normal	-50	-	+50	ns	
	on bus	AS_Normal	-75	-	+75	ns	
$t_{det(act)}(TRXD)$	activity detection time on pin TRXD	pins TRXD0 and TRXD1; AS_Normal; from idle to active	100	-	200	ns	
$t_{det(idle)}(TRXD)$	idle detection time on pin TRXD	pins TRXD0 and TRXD1; AS_Normal; from active to idle	100	-	200	ns	
$t_{det(act)}(bus)$	activity detection time on bus pins	AS_Normal; from idle to active	100	-	210	ns	
$t_{det(idle)}(bus)$	idle detection time on bus pins	AS_Normal; from active to idle	50	-	200	ns	
$t_{det(int)}$	interrupt detection time	from interrupt detection to falling edge on INTN	-	-	100	$\mu\text{s}$	
$t_{INTNH(min)}$	minimum INTN HIGH time		10	-	40	$\mu\text{s}$	
<b>Wake-up detection</b>							
$t_{det(wake)}DATA\_0$	DATA_0 wake-up detection time	$-10\text{ V} \leq V_{cm} \leq +15\text{ V}$	[3] [4]	1	-	4	$\mu\text{s}$
$t_{det(wake)}idle$	idle wake-up detection time	$-10\text{ V} \leq V_{cm} \leq +15\text{ V}$	[3] [4]	1	-	4	$\mu\text{s}$
$t_{det(wake)}tot$	total wake-up detection time	$-10\text{ V} \leq V_{cm} \leq +15\text{ V}$	[3] [4]	50	-	115	$\mu\text{s}$
$t_{sup(int)}wake$	wake-up interruption suppression time	$-10\text{ V} \leq V_{cm} \leq +15\text{ V}$	[3]	130	-	1000	ns
$t_{d(bus)}(wake-act)$	bus delay time from wake-up to active		-	-	18	$\mu\text{s}$	
$t_{det(wake)}(LWU)$	wake-up detection time on pin LWU		2.9	-	175	$\mu\text{s}$	
$t_{det(wake)}(TRXD)$	wake-up detection time on pin TRXD	falling edge on TRXD_0 or TRXD_1	100	-	400	ns	
$t_{d(LWUwake-INHH)}$	delay time from LWU wake-up to INH HIGH	falling edge on LWU to INH HIGH AS_Sleep; $5.5\text{ V} < V_{BAT} < 27\text{ V}$ $R_{L(INH-GND)} = 100\text{ k}\Omega$	[5]	2.9	-	100	$\mu\text{s}$
		falling edge on LWU to INH HIGH AS_Sleep; $27\text{ V} < V_{BAT} < 60\text{ V}$ $R_{L(INH-GND)} = 100\text{ k}\Omega$	[5]	-	-	175	$\mu\text{s}$
$t_{d(buswake-INHH)}$	delay time from bus wake-up to INH HIGH	AS_Sleep; $V_{BAT} > 5.5\text{ V}$ $R_{L(INH-GND)} = 100\text{ k}\Omega$	[5]	-	-	55	$\mu\text{s}$
$t_{d(buswake-INTNL)}$	delay time from bus wake-up to INTN LOW	AS_Sleep; AS_Standby $V_{BAT} > 5.5\text{ V}$	-	-	10	$\mu\text{s}$	

**Table 16. Dynamic characteristics ...continued**

All parameters are guaranteed for  $V_{BAT} = 4.45\text{ V to }60\text{ V}$ ;  $V_{CC} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{BUF} = 4.45\text{ V to }5.25\text{ V}$ ;  $V_{IO} = 2.55\text{ V to }5.25\text{ V}$ ;  $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$ ;  $R_{bus} = 40\ \Omega$ ,  $C_{bus} = 100\text{ pF}$ ;  $C_{RXD} = 15\text{ pF}$ ;  $C_{TRXD0} = C_{TRXD1} = 50\text{ pF}$  and  $C_{SDO} = 50\text{ pF}$  unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(TRXDwake-INHH)}$	delay time from TRXD wake-up to INH HIGH	falling edge on TRXDx to INH HIGH AS_Sleep; $R_{L(INH-GND)} = 100\text{ k}\Omega$	[5]	-	55	$\mu\text{s}$
<b>Bus error diagnosis</b>						
$t_{to(BFT)}$	BFT time-out time		80	-	180	ns
<b>Clamp detection</b>						
$t_{detCL(bus)}$	bus clamp detection time		650	-	2600	$\mu\text{s}$
$t_{detCL(TRXD)}$	TRXD clamp detection time		650	-	2600	$\mu\text{s}$
$t_{detCL(TXEN)}$	TXEN clamp detection time		650	-	2600	$\mu\text{s}$
$t_{det(col)(TRXD)}$	TRXD collision detection time		40	-	120	ns
<b>Transition timing</b>						
$t_{to\_stargotosleep}$	dStarGoToSleep time-out time		640	-	6400	ms
$t_{t}(bnorm-bdis)$	branch normal to branch disabled transition time	AS_Normal; after a host 'Branch_Disabled' command; rising edge on SCSN to transmitter deactivated	-	-	1	$\mu\text{s}$
$t_{t}(bdis-bnorm)$	branch disabled to branch normal transition time	AS_Normal; after a host 'Branch_Normal' command; rising edge on SCSN to transmitter activated	-	-	1	$\mu\text{s}$
$t_{t}(bnorm-btx2)$	branch normal to branch TxOnly2 transition time	AS_Normal; after a host 'Branch_TxOnly' command; rising edge on SCSN to deactivating receive function	-	-	1	$\mu\text{s}$
$t_{t}(btx2-bnorm)$	branch TxOnly2 to branch normal transition time	AS_Normal; after a host 'Branch_Normal' command; rising edge on SCSN to activating receive function	-	-	1	$\mu\text{s}$
$t_{t}(moch)$	mode change transition time	after host command AS_Sleep to AS_Standby rising edge on SCSN to rising edge on INH	-	-	25	$\mu\text{s}$

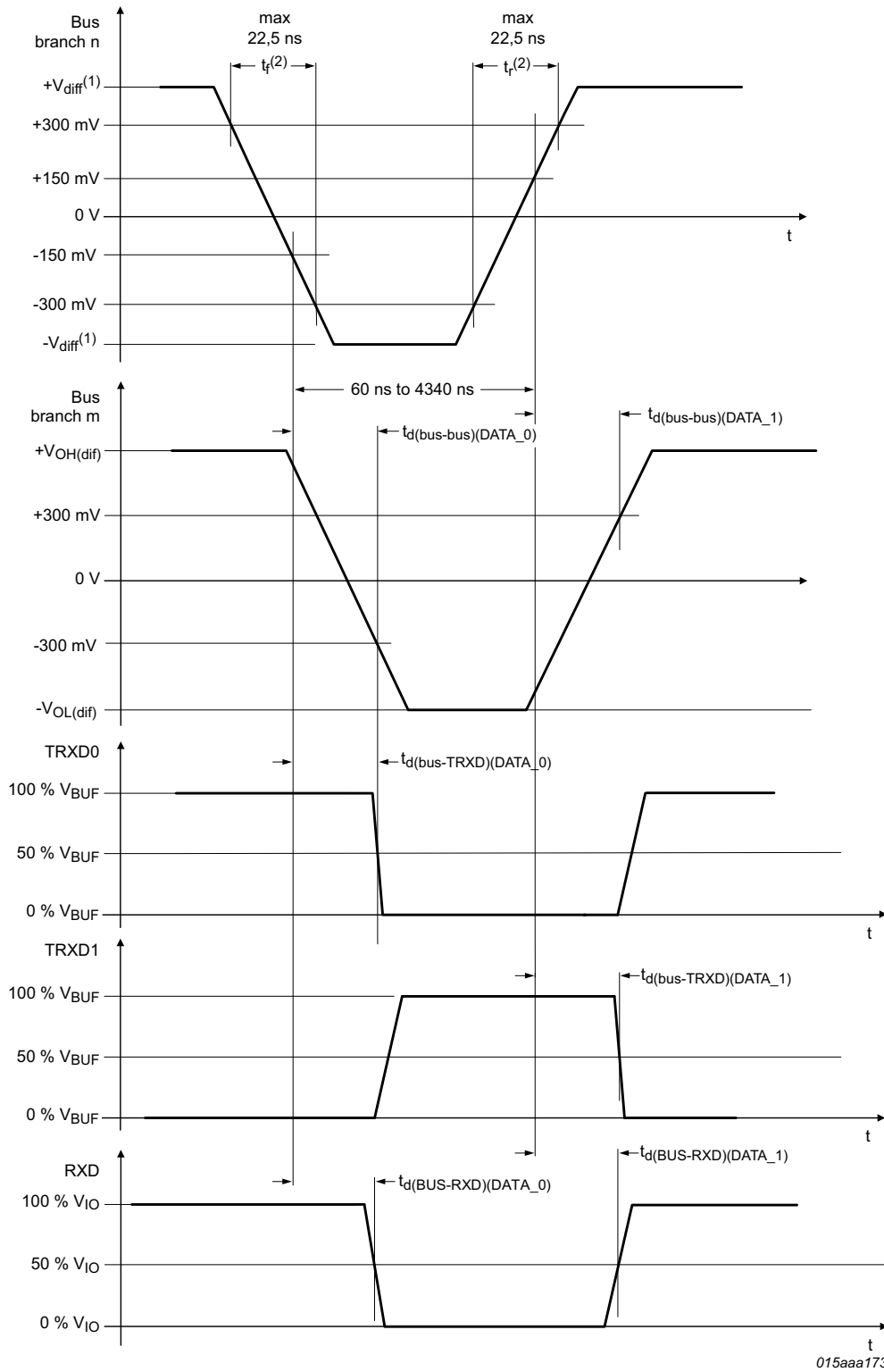
- [1] Sum of rise and fall times on TXD (20 % to 80 % on  $V_{IO}$ ) is 9 ns (max).
- [2] Guaranteed for  $V_{bus(dif)} = \pm 300\text{ mV}$  and  $V_{bus(dif)} = \pm 150\text{ mV}$ ;  $V_{bus(dif)}$  is the differential bus voltage,  $V_{BP} - V_{BM}$ .
- [3]  $V_{cm}$  is the BP/BM common mode voltage ( $V_{cm} = (V_{BP} + V_{BM})/2$ ).
- [4] See [Figure 3](#).
- [5] Defined for  $V_{INH} = 2\text{ V}$ .



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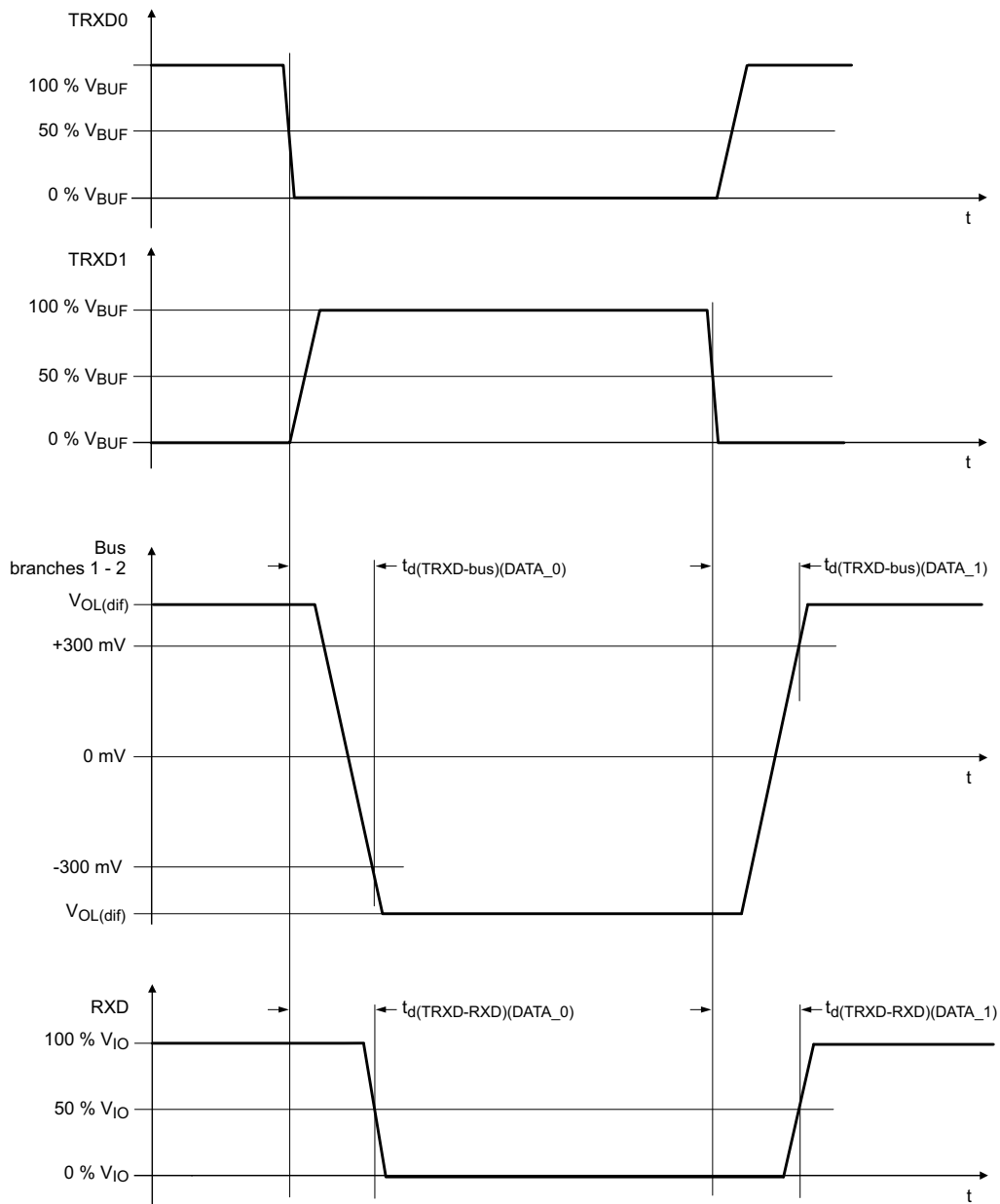
Fig 10. Timing diagram when the CC interface is the input channel





- (1)  $V_{diff} = 400 \text{ mV to } 3000 \text{ mV}$ .
- (2)  $t_r$  and  $t_f$ , defined between  $\pm 300 \text{ mV}$ , are both  $22.5 \text{ ns}$  for bus amplitudes of  $800 \text{ mV}$  (max), and lower for higher bus amplitudes.

**Fig 11. Timing diagram when one of the branches is the input channel**



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Fig 12. Timing diagram when the internal bus (TRXD0/1) is the input channel

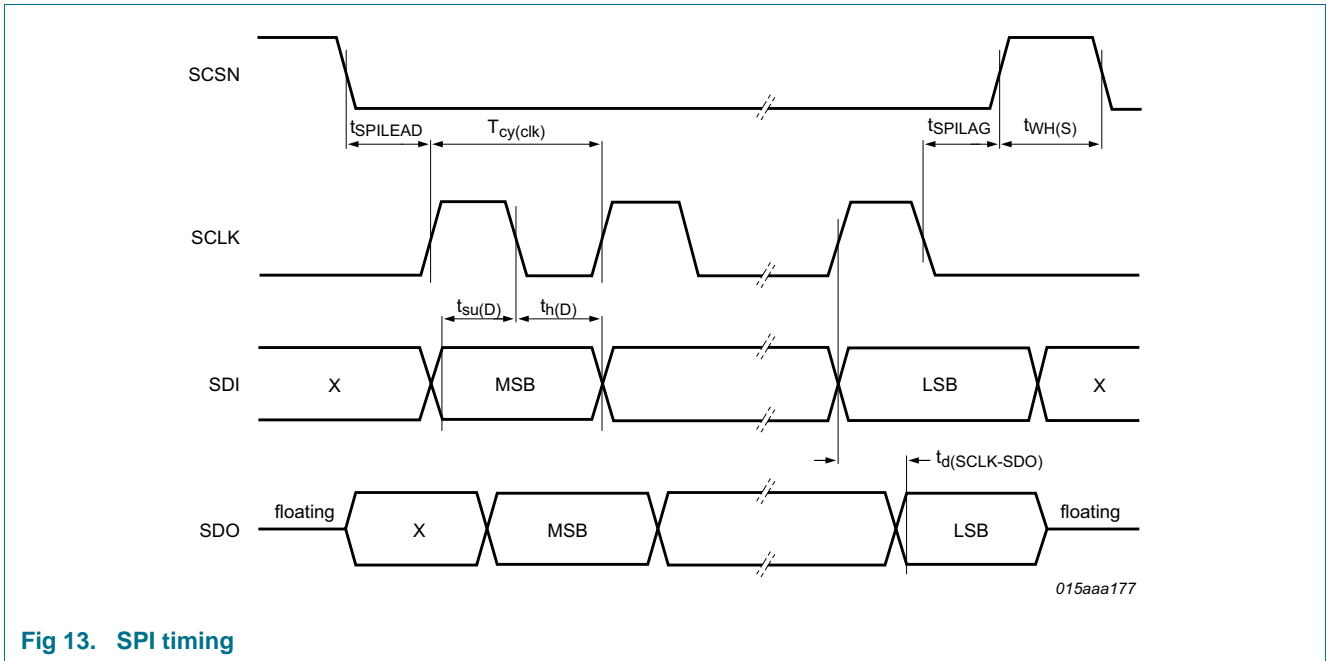


Fig 13. SPI timing

## 12. Application information

Further information on the application of the TJA1086G can be found in NXP application hints *AH1305\_TJA1086(G) FlexRay Active Star Coupler* ([Ref. 3](#)).

### 13. Test information

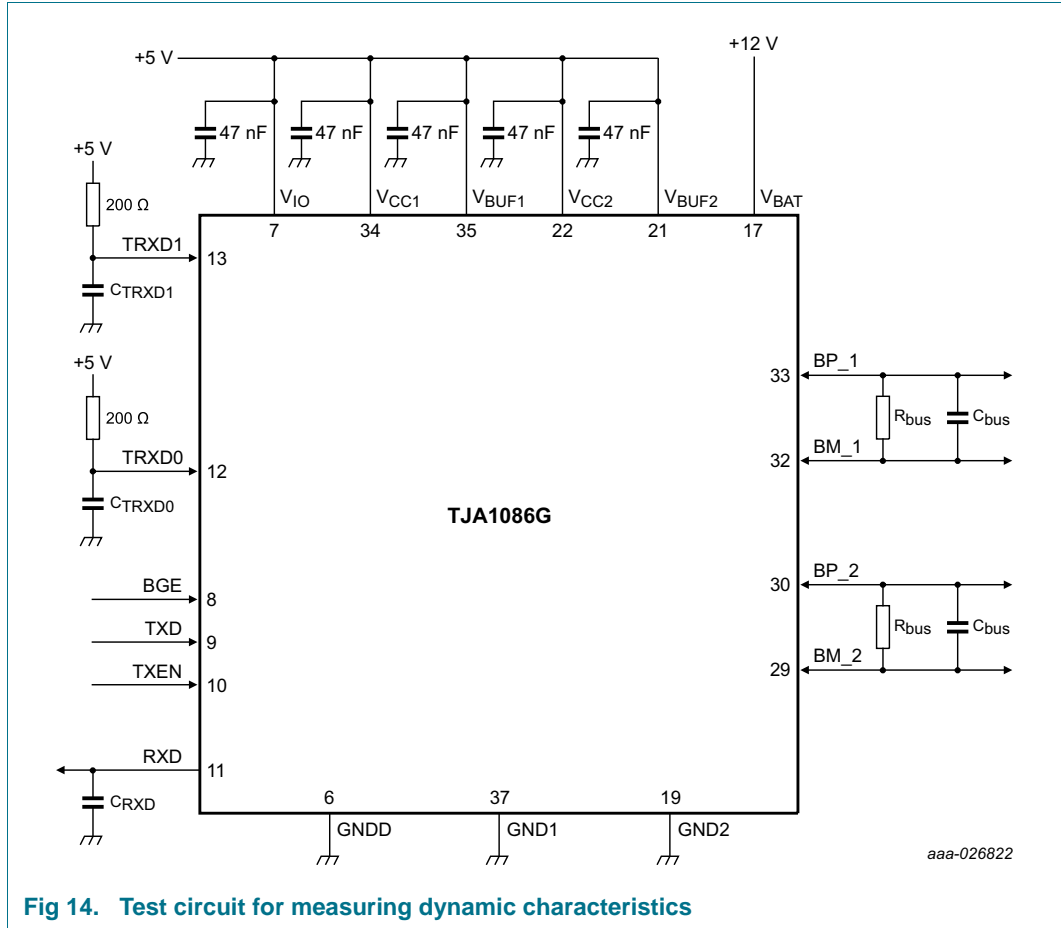


Fig 14. Test circuit for measuring dynamic characteristics

#### 13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 Rev-G - *Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

14. Package outline

HVQFN44: plastic thermal enhanced very thin quad flat package; no leads  
44 terminals; body 9 x 9 mm

SOT1113-1

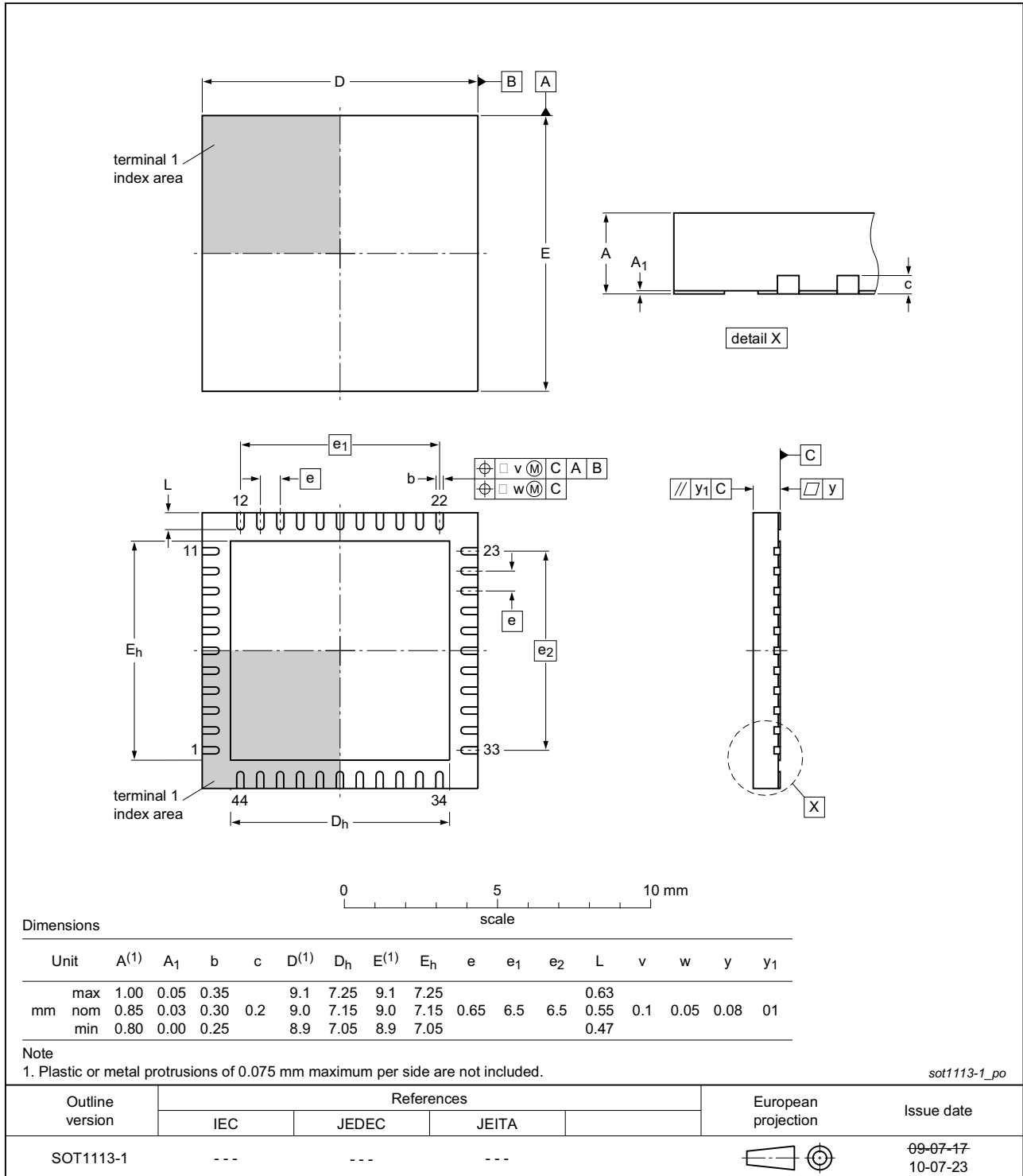


Fig 15. Package outline SOT1113-1 (HVQFN44)

## 15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 16](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 17](#) and [18](#)

**Table 17. SnPb eutectic process (from J-STD-020D)**

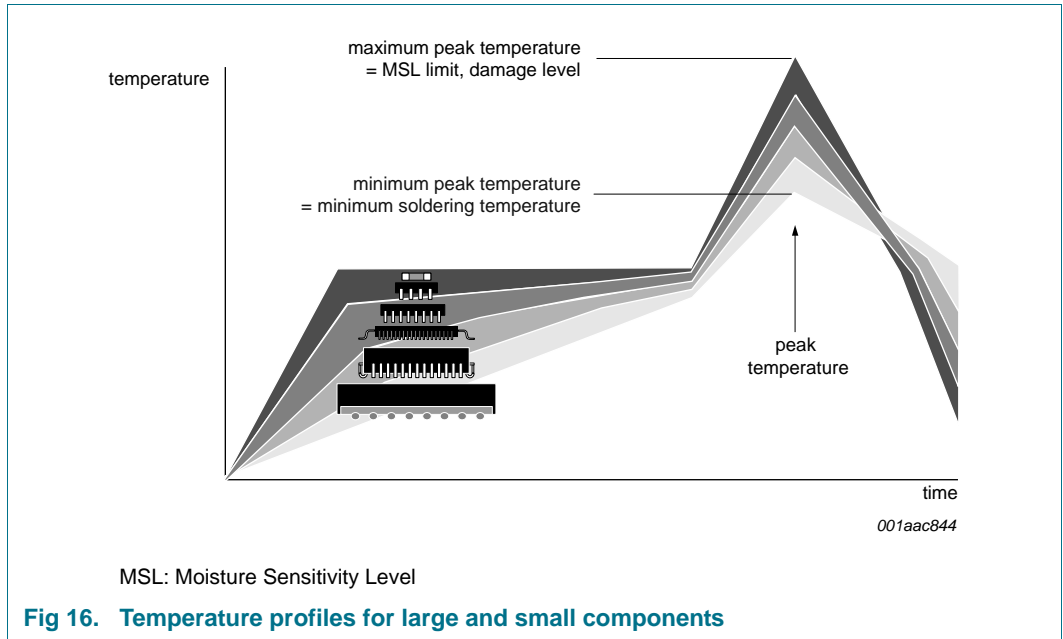
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 18. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 16](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.



## 16. Appendix: EPL 3.0.1/ISO17458-4 to TJA1086G parameter conversion

**Table 19. EPL 3.0.1/ISO17458-4 to TJA1086G conversion**

This table maps the EPL 3.0.1 parameters names to those in the TJA1086G. Values are provided for reference only (see the characteristics tables for comprehensive listings of guaranteed parameter values).

EPL 3.0.1				TJA1086G			
Symbol	Min	Max	Unit	Symbol	Min	Max	Unit
dBusTx01	6	18.75	ns	$t_{r(dif)(bus)}$	6	18.75	ns
dBusTx10	6	18.75	ns	$t_{f(dif)(bus)}$	6	18.75	ns
uStarTxactive	600	2000	mV	$ V_{OH(dif)} ,  V_{OL(dif)} $	600	2000	mV
uStarTxidle	0	30	mV	$ V_{o(idle)(dif)} $	0	25	mV
dBranchRxActiveMax	650	2600	$\mu$ s	$t_{detCL}(bus)$	650	2600	$\mu$ s
$R_{CM1}, R_{CM2}$	10	40	k $\Omega$	$R_i$ (pins BP and BM)	10	40	k $\Omega$
uCM	-10	+15	V	$V_{cm}$ [1]	-10	+15	V
uStarUVV <sub>BAT</sub>	4	5.5	V	$V_{uvd}(VBAT)$	4.45	4.715	V
uStarUVV <sub>CC</sub>	4	-	V	$V_{uvd}(VCC)$	4.45	4.715	V
dStarUVV <sub>CC</sub>	-	1000	ms	$t_{det(uv)}(VCC)$	5	100	$\mu$ s
iBP <sub>Leak</sub>	-	25	$\mu$ A	$ I_{LI}(BP) $	-	5	$\mu$ A
iBM <sub>Leak</sub>	-	25	$\mu$ A	$ I_{LI}(BM) $	-	5	$\mu$ A
iBM <sub>GNDShortMax</sub>	-	60	mA	$ I_{O(sc)} $ (pin BM)	-	60	mA
iBP <sub>GNDShortMax</sub>	-	60	mA	$ I_{O(sc)} $ (pin BP)	-	60	mA
iBM <sub>BAT48ShortMax</sub>	-	72	mA	$ I_{O(sc)} $ (pin BM)	-	60	mA
iBP <sub>BAT48ShortMax</sub>	-	72	mA	$ I_{O(sc)} $ (pin BP)	-	60	mA
iBM <sub>BAT27ShortMax</sub>	-	60	mA	$ I_{O(sc)} $ (pin BM)	-	60	mA
iBP <sub>BAT27ShortMax</sub>	-	60	mA	$ I_{O(sc)} $ (pin BP)	-	60	mA
functional class: Active Star - bus guardian interface				implemented (see <a href="#">Section 2.4</a> )			
dStarDelay10	-	150	ns	$t_{d(bus-TRXD)} + t_{d(TRXD-bus)}$	-	150	ns
dStarDelay01	-	150	ns	$t_{d(bus-TRXD)} + t_{d(TRXD-bus)}$	-	150	ns
dStarAsym	0	8	ns	$ \Delta t_{d(bus-bus)} $	-	8	ns
dStarAsym2	0	10	ns	$ \Delta t_{d(bus-TRXD)}  +  \Delta t_{d(TRXD-bus)} $	-	10	ns
dStarSetUpDelay	-	500	ns	$t_{det(act)}(TXEN) + t_{d}(TXD-TRXD)$	20	130	ns
				$t_{det(act)}(bus) + t_{d}(bus-TRXD)$	100	285	ns
dStarGoToSleep	640	6400	ms	$t_{to\_stargotosleep}$	640	6400	ms
dStarWakeupReactionTime	-	70	$\mu$ s	$t_{d}(bus)(wake-act)$	-	18	$\mu$ s
device qualification according to AEC-Q100 (Rev. F)				see <a href="#">Section 2.1</a>			
T <sub>AMB_Class1</sub>	-40	+125	$^{\circ}$ C	T <sub>amb</sub>	-40	+125	$^{\circ}$ C
iBM <sub>-5VshortMax</sub>	-	60	mA	$ I_{O(sc)} $ (pin BM)	-	60	mA
iBP <sub>-5VshortMax</sub>	-	60	mA	$ I_{O(sc)} $ (pin BP)	-	60	mA
functional class: Active Star - voltage regulator control				implemented (see <a href="#">Section 2.4</a> )			
iBM <sub>BPSHORTMax</sub>	-	60	mA	$ I_{O(sc)} $ (BP to BM)	-	60	mA
iBP <sub>BMSHORTMax</sub>	-	60	mA	$ I_{O(sc)} $ (BM to BP)	-	60	mA
iBM <sub>BAT60SHORTMax</sub>	-	90	mA	$ I_{O(sc)} $ (pin BP)	-	60	mA
iBP <sub>BAT60SHORTMax</sub>	-	90	mA	$ I_{O(sc)} $ (pin BM)	-	60	mA

Table 19. EPL 3.0.1/ISO17458-4 to TJA1086G conversion ...continued

This table maps the EPL 3.0.1 parameters names to those in the TJA1086G. Values are provided for reference only (see the characteristics tables for comprehensive listings of guaranteed parameter values).

EPL 3.0.1				TJA1086G			
Symbol	Min	Max	Unit	Symbol	Min	Max	Unit
uBias - Non-Low Power	1800	3200	mV	$V_{o(idle)(BP)}$ , $V_{o(idle)(BM)}$ [2]	1800	3150	mV
uBias - Low Power	-200	+200	mV	$V_{o(idle)(BP)}$ , $V_{o(idle)(BM)}$ [3]	-100	+100	mV
dStarUVV <sub>BAT</sub>	-	1000	ms	$t_{det(uv)(VBAT)}$	5	150	μs
uStarUVV <sub>IO</sub>	2	-	V	$V_{uvd}(VIO)$	2.55	2.765	V
dStarUVV <sub>IO</sub>	-	1000	ms	$t_{det(uv)(VIO)}$	5	100	μs
uINH1 <sub>Not_Sleep</sub>	uVBAT - 1 V	-	V	$V_{OH}$ (pin INH)	$V_{BAT} - 0.8 V$	$V_{BAT}$	V
iINH1 <sub>Leak</sub>	-	10	μA	$I_L$ (pin INH)	-3	+3	μA
dStarTSSLengthChange	-450	0	ns	$-(t_{det(act)(bus)} + t_{det(act)(TRXD)})$	-410	-	ns
				$-t_{det(act)(bus)}$	-	-100	ns
dStarFES1LengthChange	0	450	ns	$t_{det(idle)(bus)}$	50	-	ns
				$t_{det(idle)(bus)} + t_{det(idle)(TRXD)}$	-	400	ns
dStarUVV <sub>Supply</sub>	-	1	ms	$t_{det(uv)(VBUF)}$	5	100	μs
dStarRV <sub>Supply</sub>	-	10	ms	$t_{rec(uv)(VBUF)}$	5	100	μs
uStarUVV <sub>Supply</sub>	4	-	V	$V_{uvd}(VBUF)$	4.2	4.474	V
dStarRV <sub>BAT</sub>	-	10	ms	$t_{rec(uv)(VBAT)}$	5	150	μs
dStarRV <sub>CC</sub>	-	10	ms	$t_{rec(uv)(VCC)}$	5	100	μs
dStarRV <sub>IO</sub>	-	10	ms	$t_{rec(uv)(VIO)}$	5	100	μs
dWU <sub>Interrupt</sub>	0.13	1	μs	$t_{sup(int)wake}$	130	1000	ns
dWU <sub>0Detect</sub>	1	4	μs	$t_{det(wake)DATA\_0}$	1	4	μs
dWU <sub>IdleDetect</sub>	1	4	μs	$t_{det(wake)idle}$	1	4	μs
dWU <sub>Timeout</sub>	48	140	μs	$t_{det(wake)tot}$	50	115	μs
dStarWakePulseFilter	1	500	μs	$t_{det(wake)(LWU)}$	2.9	175	μs
iBP <sub>LeakGND</sub>	-	1600	μA	$ I_L(BP) $	-	1600	μA
iBM <sub>LeakGND</sub>	-	1600	μA	$ I_L(BM) $	-	1600	μA
dStarWakeupReaction <sub>local</sub>	-	100	μs	$t_d(LWUwake-INHH)$	0	100	μs
dStarSymbolLengthChange	-300	+450	ns	$\Delta t_{det(act-idle)(bus)} +$	-125	+125	ns
				$\Delta t_{det(act-idle)(TRXD)}$			
functional class: Active Star - logic level adaptation				implemented (see <a href="#">Section 2.4</a> )			
functional class: Active Star - increased voltage amplitude transmitter				implemented (see <a href="#">Section 2.4</a> )			
uESD <sub>EXT</sub>	6	-	kV	$ V_{ESD} $ : HBM on pins BP and BM to GND	8	-	kV
				$ V_{ESD} $ : HBM on pins LWU and V <sub>BAT</sub> to GND	6	-	kV
uESD <sub>INT</sub>	2	-	kV	$ V_{ESD} $ (HBM on any other pin)	4	-	kV
uESD <sub>IEC</sub>	6	-	kV	IEC61000-4-2 on pins BP and BM to GND	6	-	kV
uV <sub>BAT-WAKE</sub>	-	7	V	$V_{BAT}$	4.75	60	V
dBusTxai	-	30	ns	$t_r(dif)(bus)$ (DATA_0 to idle)	-	30	ns

**Table 19. EPL 3.0.1/ISO17458-4 to TJA1086G conversion ...continued**

This table maps the EPL 3.0.1 parameters names to those in the TJA1086G. Values are provided for reference only (see the characteristics tables for comprehensive listings of guaranteed parameter values).

EPL 3.0.1				TJA1086G			
Symbol	Min	Max	Unit	Symbol	Min	Max	Unit
dBusTxia	-	30	ns	$t_{f(dif)(bus)}$ (idle to DATA_0)	-	30	ns
valid operating modes when $V_{StarSupply} = \text{nominal}$ ; $V_{BAT} \geq 7\text{ V}$ ; $V_{CC} = \text{nominal}$				AS_Sleep, AS_Standby, AS_Normal			
valid operating modes when $V_{StarSupply} = \text{nominal}$ ; $V_{BAT} \geq 5.5\text{ V}$ ; $V_{CC} = \text{nominal}$				AS_Sleep, AS_Standby, AS_Normal			
dBusTxDif	-	3	ns	$ \Delta t_{(r-f)(dif)} $	-	3	ns
$R_{StarTransmitter}$	product-specific			$Z_{o(eq)(TX)}$	35	100	$\Omega$
dStarSymbolEndLengthChange	0	450	ns	$t_{det(idle)(bus)}$	50	-	ns
				$t_{det(idle)(bus)} + t_{det(idle)(TRXD)}$	-	400	ns
<b>Active star with communication controller interface</b>							
dStarRxAsym	-	10	ns	$ \Delta t_{d(bus-TRXD)}  +  \Delta t_{d(TRXD-RXD)} $	-	10	ns
dStarRx10	-	225	ns	$t_{d(bus-TRXD)} + t_{d(TRXD-RXD)}$	-	135	ns
dStarRx01	-	225	ns	$t_{d(bus-TRXD)} + t_{d(TRXD-RXD)}$	-	135	ns
dStarRxai	50	550	ns	$t_{det(idle)(bus)} + t_{d(bus-RXD)}$	50	-	ns
				$t_{det(idle)(bus)} + t_{d(bus-TRXD)} + t_{det(idle)(TRXD)} + t_{d(TRXD-RXD)}$	-	535	ns
dStarRxia	100	550	ns	$t_{det(act)(bus)} + t_{d(bus-RXD)}$	100	-	ns
				$t_{det(act)(bus)} + t_{d(bus-TRXD)} + t_{det(act)(TRXD)} + t_{d(TRXD-RXD)}$	-	545	ns
dStarTxAsym	-	10	ns	$ \Delta t_{d(TXD-TRXD)}  + \Delta  t_{d(TRXD-bus)} $	-	10	ns
dStarTx10	-	225	ns	$t_{d(TXD-TRXD)} + t_{d(TRXD-bus)}$	-	135	ns
dStarTx01	-	225	ns	$t_{d(TXD-TRXD)} + t_{d(TRXD-bus)}$	-	135	ns
dStarTxai	-	550	ns	$t_{det(idle)(TXEN)} + t_{d(TXD-TRXD)} + t_{det(idle)(TRXD)} + t_{d(TRXD-bus)}$	-	405	ns
dStarTxia	-	550	ns	$t_{det(act)(TXEN)} + t_{d(TXD-TRXD)} + t_{det(act)(TRXD)} + t_{d(TRXD-bus)}$	-	405	ns
$uV_{DIG-OUT-HIGH}$	80	100	%	$V_{OH}$ (pin RXD)	$V_{IO} - 0.4$	$V_{IO}$	V
$uV_{DIG-OUT-LOW}$	-	20	%	$V_{OL}$ (pin RXD)	-	0.4	V
$uV_{DIG-IN-HIGH}$	-	70	%	$V_{IH}$ (pins TXEN and BGE)	$0.7V_{IO}$	5.5	V
$uV_{DIG-IN-LOW}$	30	-	%	$V_{IL}$ (pins TXEN and BGE)	-0.3	$0.3V_{IO}$	V
uData0	-300	-150	mV	$V_{IL(dif)}$ (pins BP and BM)	-300	-150	mV
uData1	150	300	mV	$V_{IH(dif)}$ (pins BP and BM)	150	300	mV
$uData1 -  uData0 $	-30	+30	mV	$\Delta V_{i(dif)(H-L)}$	-30	+30	mV
uStarLogic_1	-	60	%	$V_{IH}$ (pin TXD)	$0.6V_{IO}$	5.5	V
uStarLogic_0	40	-	%	$V_{IL}$ (pin TXD)	-0.3	$0.4V_{IO}$	V
$dStarRxD_{R15} + dStarRxD_{F15}$	-	13	ns	$t_{(r+f)}$ (pin RXD)	-	13	ns
functional class: Active Star - communication controller interface				implemented			
dStarTxRxai	-	325	ns	$t_{d(TXEN-RXD)}$	-	150	ns
C_StarTxD	-	10	pF	$C_i$ (pin TXD)	-	10	pF

**Table 19. EPL 3.0.1/ISO17458-4 to TJA1086G conversion ...continued**

This table maps the EPL 3.0.1 parameters names to those in the TJA1086G. Values are provided for reference only (see the characteristics tables for comprehensive listings of guaranteed parameter values).

EPL 3.0.1				TJA1086G			
Symbol	Min	Max	Unit	Symbol	Min	Max	Unit
$uV_{DIG-OUT-UV}$	-	500	mV	$V_O$ (pin RXD) <sup>[4]</sup>	-	500	mV
$uData0\_LP$	-400	-100	mV	$V_{IL(dif)}$ (pins BP and BM)	-400	-125	mV
$uV_{DIG-OUT-OFF}$	product specific			$V_O$ (pin RXD) <sup>[5]</sup>	$V_{IO} - 500$	$V_{IO}$	mV
dStarTSSLengthChange_TxD_Bus	-450	0	ns	$-(t_{det(act)}(TXEN) + t_{det(act)}(TRXD))$	-270	-	ns
				$-t_{det(act)}(TXEN)$	-	-20	ns
dStarFES1LengthChange_TxD_Bus	0	450	ns	$t_{det(idle)}(TXEN)$	20	-	ns
				$t_{det(idle)}(TXEN) + t_{det(idle)}(TRXD)$	-	270	ns
dStarSymbolLengthChange_TxD_Bus	-300	+400	ns	$\Delta t_{det(act-idle)}(TXEN) + \Delta t_{det(act-idle)}(TRXD)$	-75	+75	ns
dStarTSSLengthChange_Bus_RxD	-450	0	ns	$-(t_{det(act)}(bus) + t_{det(act)}(TRXD))$	-410	-	ns
				$-t_{det(act)}(bus)$	-	-100	ns
dStarFES1LengthChange_Bus_RxD	0	450	ns	$t_{det(idle)}(bus)$	50	-	ns
				$t_{det(idle)}(bus) + t_{det(idle)}(TRXD)$	-	400	ns
dStarSymbolLengthChange_Bus_RxD	-300	+400	ns	$\Delta t_{det(act-idle)}(bus) + \Delta t_{det(act-idle)}(TRXD)$	-125	+125	ns
dStarActivityDetection	100	250	ns	$t_{det(act)}(bus)$	100	210	ns
dStarIdleDetection	50	200	ns	$t_{det(idle)}(bus)$	50	200	ns
$ dStarRxDR_{15} - dStarRxDF_{15} $	-	5	ns	$ \Delta t_{(r-f)} $ (pin RXD)	-	5	ns
dStarTxActiveMax	650	2600	$\mu s$	$t_{detCL}(TXEN)$	650	2600	$\mu s$
dStarTx <sub>reaction</sub>	-	75	ns	$t_{det(idle)}(TXEN)$	20	70	ns
<b>Active Star with host interface</b>							
dStarModeChange <sub>SPI</sub>	-	100	$\mu s$	$t_t(moch)$	-	25	$\mu s$
dStarReactionTime <sub>SPI</sub>	-	200	$\mu s$	$t_{det(int)}$	-	100	$\mu s$
$uV_{DIG-OUT-HIGH}$	80	100	%	$V_{OH}$ (pin SDO)	$V_{IO} - 0.4$	$V_{IO}$	V
$uV_{DIG-OUT-LOW}$	-	20	%	$V_{OL}$ (pins SDO, INTN)	-	0.4	V
$uV_{DIG-IN-HIGH}$	-	70	%	$V_{IH}$ (pins SDI, SCSN, SCLK)	$0.7V_{IO}$	5.5	V
$uV_{DIG-IN-LOW}$	30	-	%	$V_{IL}$ (pins SDI, SCSN, SCLK)	-0.3	$0.3V_{IO}$	V
Functional class: Active Star - host interface				implemented			
SPI	0.01	1	Mbit/s	$t_{cl}(clk)$	0.5	100	$\mu s$
$uV_{DIG-OUT-UV}$	-	500	mV	$V_O$ (pins SDO, INTN) <sup>[4]</sup>	-	500	mV
$uV_{DIG-OUT-OFF}$	product specific			$V_O$ (pins SDO, INTN) <sup>[5]</sup>	-	500	mV
behavior when SCK not connected				pull-down behavior on SCLK			
behavior when SDI not connected				pull-down behavior on SDI			
behavior when SCSN not connected				pull-up behavior on SCSN			

[1]  $V_{cm}$  is the BP/BM common mode voltage,  $(V_{BP} + V_{BM})/2$ , and is specified in conditions column for parameters  $V_{IH(dif)}$  and  $V_{IL(dif)}$  for pins BP and BM; see Table 15.  $V_{cm}$  is tested on a receiving bus driver with a transmitting bus driver that has a ground offset voltage in the range -12.5 V to +12.5 V and transmits a 50/50 pattern.

- [2] Min:  $V_{o(idle)(BP)} = V_{o(idle)(BM)} = 0.4V_{BUF} = 0.4 \cdot 4.5 \text{ V} = 1800 \text{ mV}$ ; max value:  $V_{o(idle)(BP)} = V_{o(idle)(BM)} = 0.6V_{BUF} = 0.6 \cdot 5.25 \text{ V} = 3150 \text{ mV}$ ; the nominal voltage is 2500 mV.
- [3] The nominal voltage is 0 mV.
- [4] When undervoltage on  $V_{IO}$
- [5] When  $V_{CC} = V_{BAT} = V_{BUF} = 0 \text{ V}$ .

## 17. Abbreviations

Table 20. Abbreviations

Abbreviation	Description
AS	Active Star
BSS	Byte Start Sequence
CC	Communication Controller
CDM	Charged Device Model
ECU	Engine Control Unit
EMC	Electro Magnetic Compatibility
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 18. References

- [1] **EPL** — FlexRay Communications System Electrical Physical Layer Specification Version 3.0.1, FlexRay Consortium
- [2] **ISO 17458-4:2013** — Road vehicles - FlexRay Communications System part 4: Electrical physical layer specification
- [3] **AH1305** — TJA1086(G) FlexRay Active Star Coupler application hints, available from NXP Semiconductors

## 19. Revision history

Table 21. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1086G v.1	20170713	Product data sheet	-	-

## 20. Legal information

### 20.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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