TJA1124

Quad LIN commander transceiver

Rev. 2 — 26 August 2022 Product data sheet

1 General description

The TJA1124 is a quad Local Interconnect Network (LIN) commander channel device. It provides the interface between a LIN commander protocol controller and the physical bus in a LIN network. Each of the four channels contains a LIN transceiver and LIN commander termination. The TJA1124 is primarily intended for in-vehicle subnetworks using baud rates up to 20 kBd and is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12 V LIN) and SAE J2602-1. It is available in three variants, TJA1124A, TJA1124B and TJA1124C; see Section 3 for details.

The transmit data streams generated by the LIN commander protocol controller are converted by the TJA1124 into optimized bus signals shaped to minimize ElectroMagnetic Emission (EME). The LIN bus output pins are pulled HIGH via internal LIN commander termination resistors. The receivers detect receive data streams on the LIN bus input pins and transfer them to the microcontroller via pins RXD1 to RXD4.

Power consumption is very low in Low Power mode. However, the TJA1124 can still be woken up via pins SLP and LIN1 to LIN4.

2 Features and benefits

2.1 General

- Four LIN commander channels in a single package:
  - LIN transceiver
  - LIN commander termination consisting of a diode and a pull-up resistor
- Compliant with:
  - LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A
  - ISO 17987-4:2016 (12 V LIN)
  - SAE J2602-1
- Very low current consumption in Low Power mode with wake-up via SLP or LIN pins
- Option to control an external voltage regulator via the INHN output
- Bus signal shaping optimized for baud rates up to 20 kBd
- VIO input for direct interfacing with 3.3 V and 5 V microcontrollers
- Passive behavior in unpowered state
- Undervoltage detection
- K-line compatible
- Leadless DHVQFN24 package (3.5 mm × 5.5 mm) supporting improved Automated Optical Inspection (AOI) capability

2.2 Protection

- Excellent ElectroMagnetic Immunity (EMI)

- Very high ESD robustness: ±6 kV according to IEC61000-4-2 for pins LIN1 to LIN4 and BAT
- Bus terminal and battery pin protected against transients in the automotive environment (ISO 7637)
- Bus terminal short-circuit proof to battery and ground
- TXD dominant timeout function
- LIN dominant timeout function
- Thermal protection

3 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TJA1124AHG[1]	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT 815-1
TJA1124BHG[2]			
TJA1124CHG[3]			

[1] The TJA1124A LIN commander termination consists of a diode and a pull-up resistor of 900 Ω to 1100 Ω, as specified in LIN 2.x, ISO 17987-4:2016 (12 V LIN) and SAE J2602-1.

[2] The TJA1124B LIN commander termination consists of a diode and a pull-up resistor of 900 Ω to 1100 Ω, as specified in LIN 2.x, ISO 17987-4:2016 (12 V LIN) and SAE J2602-1. Commander termination is switched off in Low Power mode.

[3] The TJA1124C LIN commander termination consists of a diode and a pull-up resistor of 900 Ω to 1010 Ω.

4 Block diagram

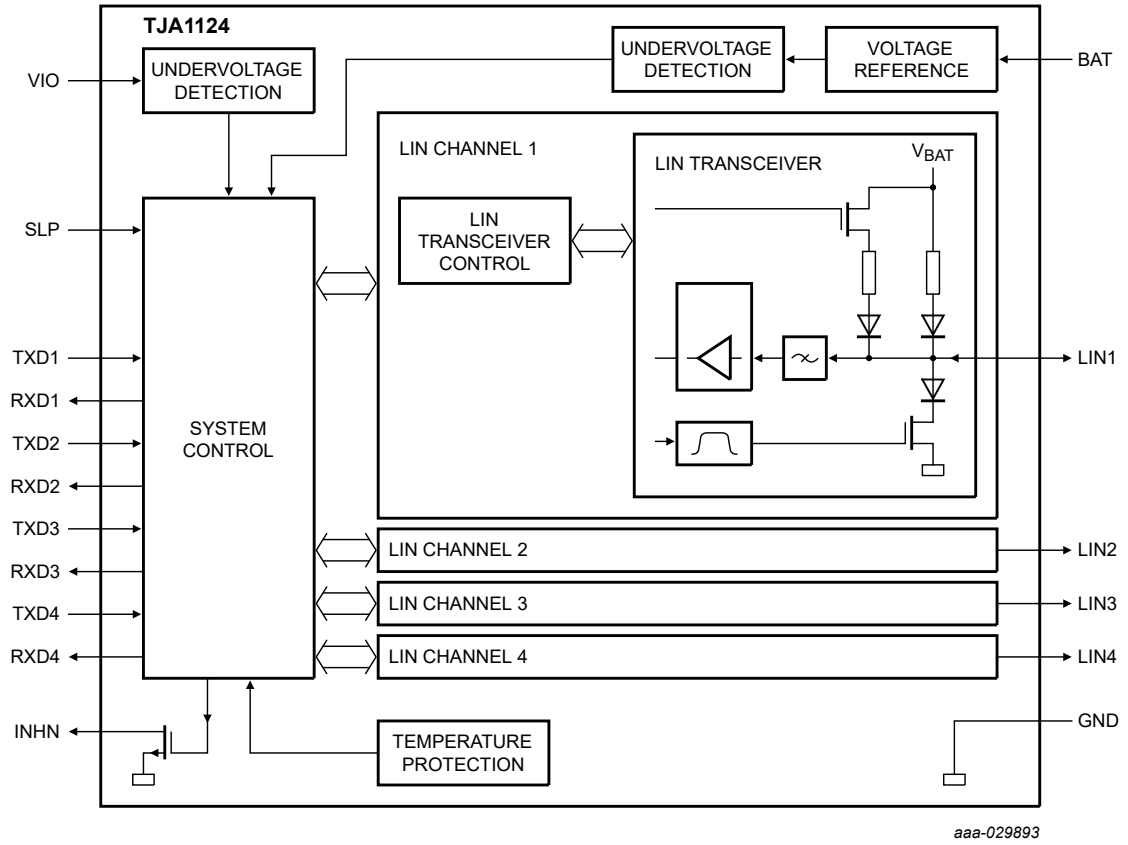


Figure 1. Block diagram

5 Pinning information

5.1 Pinning

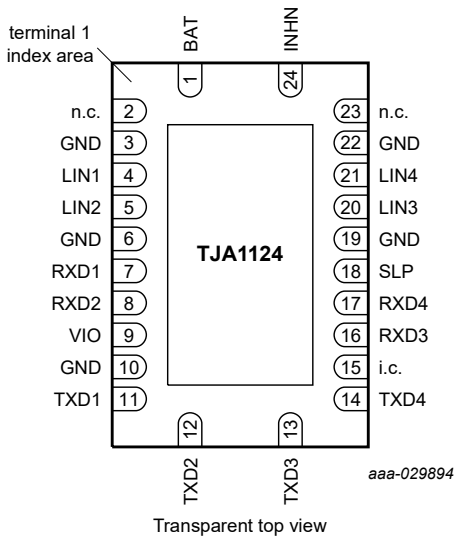


Figure 2. Pin configuration diagram

5.2 Pin description

Table 2. Pin description

Symbol	Pin[1]	Type[2]	Description
BAT	1	P	battery supply
n.c.	2	-	not connected
GND	3	G	ground
LIN1	4	AIO	LIN bus line 1 input/output
LIN2	5	AIO	LIN bus line 2 input/output
GND	6	G	ground
RXD1	7	O	receive data output 1; active LOW after a wake-up event on LIN1
RXD2	8	O	receive data output 2; active LOW after a wake-up event on LIN2
VIO	9	P	supply voltage for I/O level adapter
GND	10	G	ground
TXD1	11	I	transmit data input 1
TXD2	12	I	transmit data input 2
TXD3	13	I	transmit data input 3
TXD4	14	I	transmit data input 4
i.c.	15	-	internally connected; should be connected to ground

Table 2. Pin description...*continued*

Symbol	Pin[1]	Type[2]	Description
RXD3	16	O	receive data output 3; active LOW after a wake-up event on LIN3
RXD4	17	O	receive data output 4; active LOW after a wake-up event on LIN4
SLP	18	I	sleep control input; resets wake-up request on RXD
GND	19	G	ground
LIN3	20	AIO	LIN bus 3 input/output
LIN4	21	AIO	LIN bus 4 input/output
GND	22	G	ground
n.c.	23	-	not connected
INHN	24	O	inhibit output for controlling an external voltage regulator; open-drain; active LOW

[1] For enhanced thermal and electrical performance, solder the exposed center pad of the DHVQFN24 package to board ground.

[2] I: digital input; O: digital output; AIO: analog input/output; P: power supply; G: ground.

6 Functional description

The TJA1124 is the interface between the LIN commander protocol controller and the physical bus in a LIN network. Each of its four channels incorporates a LIN transceiver and LIN commander termination. According to the Open System Interconnect (OSI) model, this device comprises the LIN physical layer.

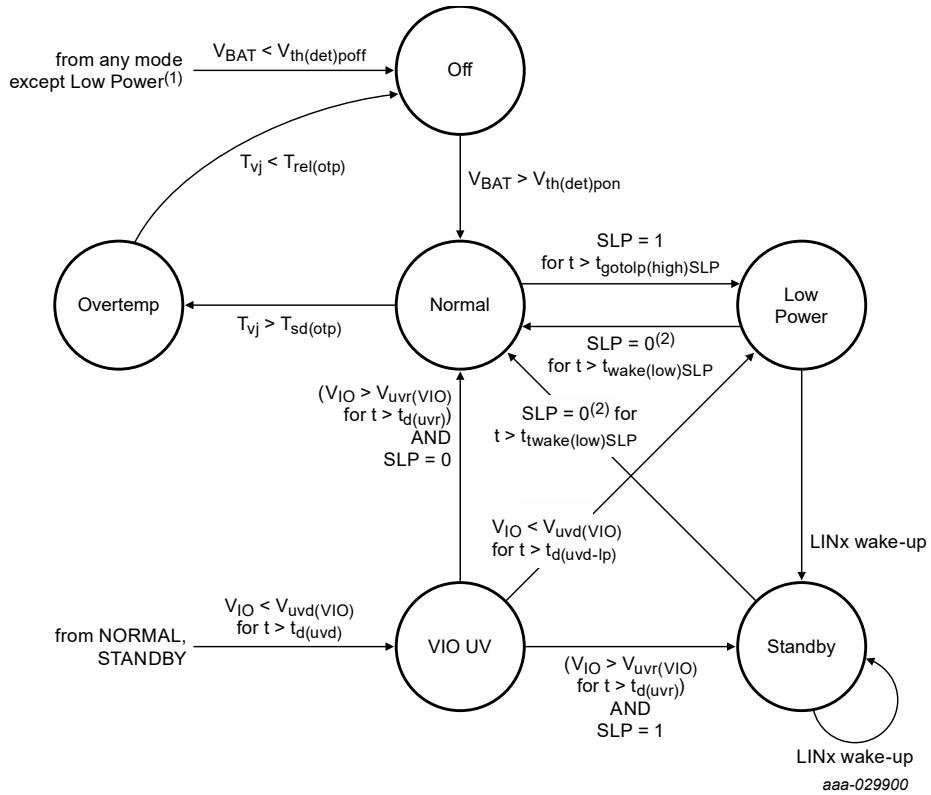
The TJA1124 is intended for, but not limited to, automotive LIN commander applications with multiple LIN commander channels. It provides excellent ElectroMagnetic Compatibility (EMC) performance.

6.1 ISO 17987/LIN 2.x/SAE J2602 compliance

The TJA1124 is fully compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12 V LIN) and SAE J2602-1.

6.2 Operating modes

The TJA1124 supports two main operating modes: Normal mode and Low Power mode. Additional battery supply undervoltage (Off), intermediate VIO undervoltage (VIO UV), intermediate wake-up signalling (Standby) and overtemperature protection (Overtemp) modes are supported. The TJA1124 state diagram is shown in Figure 3.



(1) A transition from Low Power mode to Off mode is triggered when V_{BAT} drops below typ. 2.4 V.
(2) The SLP input threshold depends on V_{IO}. This mode transition will not take place when $V_{SLP} > 0.75V_{IO}$.

Figure 3. State diagram

6.2.1 Off mode

When the TJA1124 is in Off mode, all input signals are ignored and all LIN output drivers are off. All pending LIN wake-up event flags are reset. The device is in a defined passive, low-power state in Off mode.

The TJA1124 switches to Off mode when the voltage on pin BAT drops below the power-off detection threshold, $V_{th(det)poff}$. When the TJA1124 is in Overtemp mode, it switches to Off mode when the junction temperature drops below $T_{rel(otp)}$.

6.2.2 Low Power mode

The TJA1124 consumes significantly less power in Low Power mode than in Normal mode. While current consumption is very low in Low Power mode, the TJA1124 can still detect remote wake-up events on pins LINx (see Section 6.3.1) and microcontroller wake-up events on pin SLP (see Section 6.3.2).

Pin INHN is set floating when the TJA1124 switches to Low Power mode.

A HIGH level on pin SLP in Normal mode lasting longer than $t_{gotolp(high)SLP}$ initiates a transition to Low Power mode. The LIN transmit path is disabled when pin SLP is HIGH. The transition to Low Power mode takes up to $t_{d(lp)}$.

The TJA1124 switches from VIO UV mode to Low Power mode if the voltage on pin VIO remains below $V_{uvd(VIO)}$ for longer than $t_{d(uvd-lp)}$.

6.2.3 Standby mode

In Standby mode, the LIN transmitter is off and the INHN output is LOW. The TJA1124 switches from Low Power mode to Standby mode when a remote wake-up is detected on one or more of the LIN pins (LIN1 to LIN4). The source of a wake-up event(s) is indicated to the microcontroller by a LOW level on the respective RXD pin(s) (RXD1 to RXD4), provided that the voltage on pin VIO is above $V_{uvr(VIO)}$.

The remaining LIN channels are still able to detect remote wake-up events during and after the transition to Standby mode. The transition to Standby mode takes t_{init}.

The TJA1124 switches from VIO UV mode to Standby mode when the voltage on pin VIO remains above $V_{uvr(VIO)}$ for longer than $t_{d(uvr)}$ and pin SLP is HIGH.

6.2.4 Normal mode

The TJA1124 can transmit and receive data via the LIN bus in Normal mode.

The receiver detects a data stream on a LIN bus input pin (LIN1 to LIN4) and transfers it to the microcontroller via the associated RXD pin (RXD1 to RXD4): HIGH for a recessive level and LOW for a dominant level on the bus. The receiver has a supply-voltage related threshold with hysteresis and an integrated filter to suppress bus line noise.

The transmitter converts a transmit data stream, received from the protocol controller and detected on pin TXDx, into optimized bus signals. The optimized bus signals are shaped to minimize EME. The LINx bus output pin is pulled HIGH via an internal commander termination resistor (see Section 6.8).

If pin SLP is pulled LOW for longer than $t_{wake(low)SLP}$ while the TJA1124 is in Low Power or Standby mode, the LIN transceiver switches to Normal mode. The transition to Normal mode from Low Power or Off modes takes t_{init}.

The TJA1124 switches from VIO UV mode to Normal mode when the voltage on pin VIO remains above $V_{uvr(VIO)}$ for longer than $t_{d(uvr)}$ and pin SLP is LOW.

6.2.5 VIO UV mode

In VIO UV mode, the LINx outputs are recessive, the INHN output is LOW and the digital inputs are ignored.

The TJA1124 switches from Normal or Standby mode to VIO UV mode when the voltage on pin VIO drops below the VIO undervoltage detection threshold, $V_{uvd(VIO)}$, for longer than $t_{d(uvd)}$.

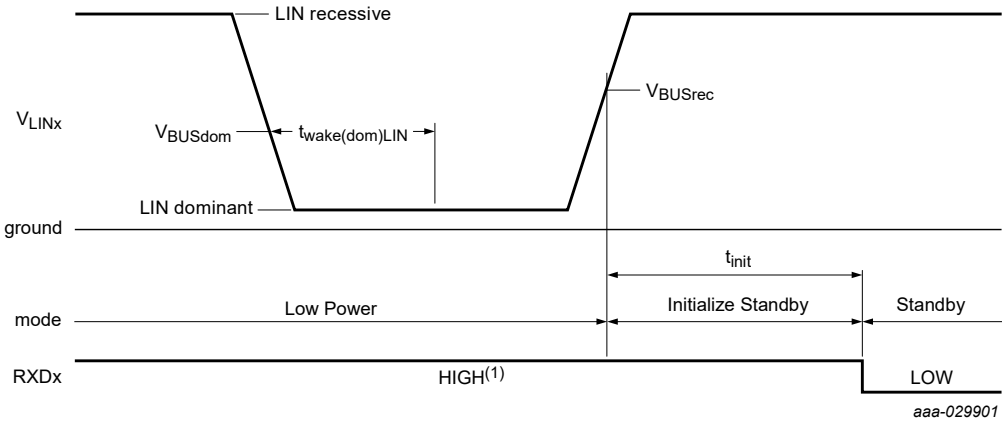
6.2.6 Overtemp mode

Overtemp mode prevents the TJA1124 from being damaged by excessive temperatures. If the junction temperature exceeds the shutdown threshold, $T_{sd(otp)}$, the thermal protection circuit disables the LIN channel output drivers and the LIN commander pull-up resistors (see Section 6.8) and pending wake-up events are cleared.

6.3 Device wake-up

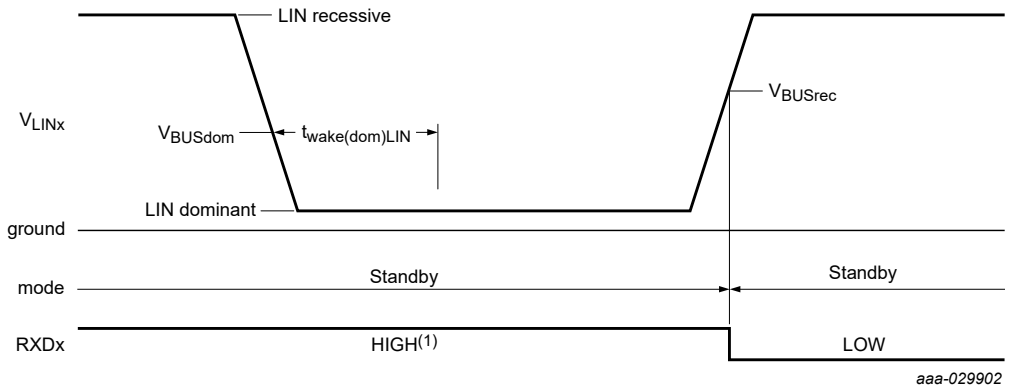
6.3.1 Remote wake-up via the LIN bus

The TJA1124 can detect remote LIN wake-up events in Low Power and Standby modes. A falling edge on pin LINx followed by a dominant level maintained for $t_{wake(dom)LIN}$, followed by a recessive level, is regarded as a remote wake-up request. The detection of a remote LIN wake-up event is signaled on pin RXDx (see Figure 4 and Figure 5), provided that the voltage on pin VIO is above $V_{uvr(VIO)}$.



(1) RXDx HIGH level depends on V_{IO}.

Figure 4. Principle of remote wake-up via LIN bus in Low Power mode



(1) RXDx HIGH level depends on V_{IO}.

Figure 5. Principle of remote wake-up via LIN bus in Standby mode

6.3.2 Local wake-up via pin SLP

A LOW level on pin SLP lasting at least $t_{wake(low)SLP}$ is interpreted as a local wake-up request.

6.4 Operation during automotive cranking pulses

The TJA1124 remains fully operational during automotive cranking pulses because it is specified down to V_{BAT} = 5 V.

6.5 Operation when supply voltage is outside specified operating range

If V_{BAT} > 28 V or V_{BAT} < 5 V, the TJA1124 may remain operational, but parameter values (as specified in Table 5 and Table 6) cannot be guaranteed.

If the voltage on pin BAT drops below the power-off detection threshold, $V_{th(det)poff}$, the TJA1124 switches to Off mode (see Section 6.2.1).

In Normal mode:

- If the input level on pin LINx is recessive, the respective receiver output on pin RXDx will be HIGH.
- If the input level on pin TXDx is HIGH, the respective LIN transmitter output on pin LINx will be recessive.

If $V_{uvd(VIO)(min)} < V_{IO} < V_{IO(min)}$, the TJA1124 will remain operational, but VIO-dependent parameter values cannot be guaranteed to remain within the operating ranges specified in Table 5 and Table 6.

6.6 TXD dominant time-out function

Once a transmitter has been enabled, its TXD dominant timeout timer is started every time the associated TXD pin goes LOW. If the LOW state on TXDx persists for longer than the TXD dominant timeout time ($t_{to(dom)TXD}$), the transmitter is disabled, releasing the bus line to recessive state. The TXD dominant timeout timer is reset when pin TXDx goes HIGH.

6.7 LIN dominant timeout function

Each LIN channel has an associated LIN dominant timeout function. This function switches off the LIN commander termination resistor, $R_{commander}$ or $R_{commander(lp)}$, if the LIN bus level remains dominant for longer than $t_{to(dom)LIN}$. LIN termination resistor $R_{responder}$ remains active as pull-up when $R_{commander}$ or $R_{commander(lp)}$ is switched off.

Once the LIN bus level is recessive again, the LIN commander termination is switched on and the LIN dominant timeout timer is reset.

6.8 LIN commander pull-up

The integrated LIN pull-up depends on the TJA1124 variant.

In Normal and Standby modes, the integrated LIN commander termination, $R_{commander}$, is a trimmed pull-up. See Table 5 for further details.

In Low Power mode, an untrimmed LIN commander termination, $R_{commander(lp)}$, is enabled in the TJA1124A and TJA1124C. In the TJA1124B, LIN commander termination is disabled and the LINx pins are terminated with the LIN termination resistor, $R_{responder}$.

6.9 Fail-safe features

A loss of power (pin BAT or GND) has no impact on the bus lines or on the microcontroller interface pins. When the battery supply is lost, reverse current $I_{BUS\_NO\_BAT}$ flows from the bus into pins LINx. When the ground connection is lost, current $I_{BUS\_NO\_GND}$ continues to flow from BAT to LINx via an integrated LIN termination resistor, $R_{responder}$. The current path through the LIN commander termination is disabled.

The output drivers on the LINx pins are protected against overtemperature conditions (see Section 6.2.6).

7 Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to pin GND; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	voltage on pin x[1]	pins BAT, INHN	-0.3	+43	V
		pin VIO	-0.3	+6	V
		pins SLP, RXDx, TXDx	-0.3	V_{IO} + 0.3	V
				+6	V
		pins LINx with respect to any other pin	-43	+43	V
I_{INHN}	input current on pin INHN		-	3	mA
V_{trt}	transient voltage	on pin BAT with inverse-polarity protection diode and 22 µF capacitor to ground; on pins LIN1, LIN2, LIN3, LIN4 coupled via 1 nF capacitor [2]			
		pulse 1	-100	-	V
		pulse 2a	-	+75	V
		pulse 3a	-150	-	V
		pulse 3b	-	+100	V
V_{ESD}	electrostatic discharge voltage	IEC61000-4-2 (150 pF, 330 Ω) discharge circuit [3]			
		on pins LIN1, LIN2, LIN3 and LIN4; on pin BAT with capacitor	-6	+6	kV
		Human Body Model (HBM)			
		on any pin [4]	-2	+2	kV
		on pin BAT, INHN [5]	-4	+4	kV
		on pins LIN1, LIN2, LIN3 and LIN4 [6]	-6	+6	kV
		Charged Device Model [7]			
		on any pin	-500	+500	V
T_{vj}	virtual junction temperature	[8]	-40	+150	°C
T_{stg}	storage temperature	[9]	-55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.
[2] Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO7637 part 2.
[3] Verified by an external test house according to IEC TS 62228, Section 4.3.
[4] According to AEC-Q100-002.
[5] Pins stressed to reference group containing all grounds, emulating the application circuit (Figure 7). HBM pulse as specified in AEC-Q100-002 used.
[6] Pins stressed to reference group containing all ground and supply pins, emulating the application circuit (Figure 7). HBM pulse as specified in AEC-Q100-002 used.
[7] According to AEC-Q100-011.
[8] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).
[9] T_{stg} in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.

8 Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	DHVQFN24; four-layer board	[1]	51	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer

9 Static characteristics

Table 5. Static characteristics

T_{vj} = −40 °C to +150 °C; V_{BAT} = 5.0 V to 28 V; V_{IO} = 2.97 V to 5.5 V; all voltages are referenced to pin GND; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V; unless otherwise specified [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{BAT}	battery supply voltage	operating range	5	-	28	V
V_{IO}	supply voltage for I/O level adapter	operating range	2.97	-	5.5	V
I_{BAT}	battery supply current	TJA1124A and TJA1124C; Low Power mode; $V_{SLP} = V_{IO}$; $V_{LINx} = V_{BAT}$; -40 °C < T_{vj} < 85 ° [2]	-	7.3	17.2	µA
		TJA1124B; Low Power mode; $V_{SLP} = V_{IO}$; $V_{LINx} = V_{BAT}$; -40 °C < T_{vj} < 85 ° [2]	-	6	15	µA
		Normal mode; bus recessive; $V_{TXDx} = V_{IO}$; V_{SLP} = 0 V; $V_{LINx} = V_{BAT}$	-	4.3	9	mA
		Normal mode; bus dominant; $V_{LINx} = V_{SLP}$ = 0 V; V_{BAT} = 12 V	-	66	87	mA
I_{IO}	supply current on pin VIO	Low Power mode; -40 °C < T_{vj} < 85 °C	-	6	9	µA
		Normal mode	-	-	1	mA
Supply undervoltage; pins BAT and VIO						
$V_{th(det)poff}$	power-off detection threshold voltage		4.0	-	4.51	V
$V_{th(det)pon}$	power-on detection threshold voltage		4.25	-	4.77	V
$V_{hys(det)pon}$	power-on detection hysteresis voltage		200	-	-	mV
$V_{uvd(VIO)}$	undervoltage detection voltage on pin VIO		2.7	2.8	2.9	V
$V_{uvr(VIO)}$	undervoltage recovery voltage on pin VIO		2.8	2.9	3.1	V

Table 5. Static characteristics...*continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 5.0 V to 28 V; V_{IO} = 2.97 V to 5.5 V; all voltages are referenced to pin GND; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V; unless otherwise specified [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{uvhys(VIO)}$	undervoltage hysteresis voltage on pin VIO		50	-	-	mV
Sleep control input and LIN transmit data inputs: SLP and TXDx; all measurements taken in Normal mode						
$V_{th(sw)}$	switching threshold voltage		$0.25V_{IO}$	-	$0.75V_{IO}$	V
$V_{th(sw)hys}$	switching threshold voltage hysteresis		$0.035V_{IO}$	-	-	V
R_{pu}	pull-up resistance	on pin SLP	38	60	88	kΩ
		on pins TXDx; $V_{TXD} > 0.75\ V_{IO}$	38	60	88	kΩ
R_{pd}	pull-down resistance	on pins TXDx; $V_{TXD} < 0.25\ V_{IO}$	38	60	88	kΩ
LIN receive data outputs; pins RXDx						
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA; Normal mode	V_{IO} – 0.4			V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; Normal mode			0.4	V
R_{pu}	pull-up resistance	Low Power mode	38	60	88	kΩ
$I_{LO(off)}$	off-state output leakage current	$V_{RXDx} = V_{IO}$; Low Power mode	−5		+5	µA
Inhibit output; pin INHN						
V_{OL}	LOW-level output voltage	I_{OL} = 0.2 mA			0.4	V
$I_{LO(off)}$	off-state output leakage current	V_O = 0 V to V_{BAT}	−5		+5	µA
LIN bus line; pins LIN1, LIN2, LIN3, LIN4						
$V_{O(dom)}$	dominant output voltage	Normal mode; V_{BAT} = 7.0 V	-	-	1.4	V
		Normal mode; V_{BAT} = 18.0 V	-	-	3.6	V
I_{BUS_LIM}	current limitation for driver dominant state	V_{BAT} = 18 V; V_{LINx} = 18 V; LIN driver on; $R_{commander}$ off	40	-	200	mA
$I_{BUS\_PAS\_dom}$	receiver dominant input leakage current including pull-up resistor	V_{BAT} = 12 V; V_{LINx} = 0 V; LIN driver off; $R_{commander}$ off	−1	-	-	mA
		V_{BAT} = 28 V; V_{LINx} = 0 V; LIN driver off; $R_{commander}$ off	−1.5	-	-	mA
$I_{BUS\_PAS\_rec}$	receiver recessive input leakage current	5 V < V_{BAT} < 18 V; 5 V < V_{LINx} < 18 V; $V_{LINx} \geq V_{BAT}$; LIN driver off	-	-	20	µA
		18 V < V_{BAT} < 28 V; 18 V < V_{LINx} < 28 V; $V_{LINx} \geq V_{BAT}$; LIN driver off	-	-	30	µA
$I_{BUS\_NO\_GND}$	loss-of-ground bus current	V_{BAT} = 12 V; $V_{GND} = V_{BAT}$; 0 V < V_{LINx} < 18 V [2]	-1	-	+1	mA
		V_{BAT} = 12 V; $V_{GND} = V_{BAT}$; 0 V < V_{LINx} < 28 V [2]	−1.5	-	+1.5	mA
$I_{BUS\_NO\_BAT}$	loss-of-battery bus current	V_{BAT} = 0 V; 0 V < V_{LINx} < 28 V [2]	-	-	30	µA

Table 5. Static characteristics...*continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 5.0 V to 28 V; V_{IO} = 2.97 V to 5.5 V; all voltages are referenced to pin GND; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V; unless otherwise specified [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BUSdom}	receiver dominant state		-	-	$0.4V_{BAT}$	V
V_{BUSrec}	receiver recessive state		$0.6V_{BAT}$	-	-	V
V_{BUS_CNT}	receiver center voltage	Normal mode; V_{BUS_CNT} = V_{th_rec} + V_{th_dom}) / 2; 7 V ≤ V_{BAT} < 28 V [3]	$0.475V_{BAT}$	$0.5V_{BAT}$	$0.525V_{BAT}$	V
		Normal mode; V_{BUS_CNT} = V_{th_rec} + V_{th_dom}) / 2; 5 V < V_{BAT} < 7 V	$0.45V_{BAT}$	$0.5V_{BAT}$	$0.55V_{BAT}$	V
		Low Power mode; V_{BUS_CNT} = (V_{th_rec} + V_{th_dom}) / 2	$0.47V_{BAT}$	$0.5V_{BAT}$	$0.54V_{BAT}$	V
V_{HYS}	receiver hysteresis voltage	V_{HYS} = (V_{th_rec} − V_{th_dom}) [3]	-	-	$0.175V_{BAT}$	V
$V_{SerDiode}$	voltage drop at the serial diodes	in pull-up path with $R_{commander}$; $I_{SerDiode}$ = 12 mA [2]	0.4	-	1.0	V
		in pull-up path with $R_{responder}$; $I_{SerDiode}$ = 0.9 mA [2]	0.4	-	1.0	V
$R_{commander}$	commander resistance	Normal mode; including $R_{responder}$				
		TJA1124A and TJA1124B	900	-	1100	Ω
		TJA1124C	900	-	1010	Ω
$R_{commander(lp)}$	low power commander resistance	TJA1124A and TJA1124 C only; Low Power mode; including $R_{responder}$	900	1200	1500	Ω
$R_{responder}$	responder resistance	$R_{commander}$ off	20	30	60	kΩ
C_{LIN}	capacitance on pin LINx	[2]	-	-	20	pF
Thermal shutdown						
$T_{sd(otp)}$	overtemperature protection shutsown temperature	[2]	150	165	179	°C
$T_{rel(otp)}$	overtemperature protection release temperature	[2]	122	137	150	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.
[2] Not tested in production; guaranteed by design.
[3] V_{th_dom}: receiver threshold of the recessive to dominant LIN bus edge. V_{th_rec}: receiver threshold of the dominant to recessive LIN bus edge.

10 Dynamic characteristics

Table 6. Dynamic characteristics

T_{vj} = -40 °C to +150 °C; V_{BAT} = 5.0 V to 28 V; V_{IO} = 2.97 V to 5.5V; all voltages are referenced to pin GND; positive currents flow into the IC; typical values are given at V_{BAT} = 12V; unless otherwise specified [1]

Symbols	Parameter	Conditions	Min	Typ	Max	Unit
Duty cycles; pins LIN1, LIN2, LIN3, LIN4						
δ1	duty cycle 1	$V_{th(rec)(max)}$ = 0.744 x V_{BAT}; $V_{th(dom)(max)}$ = 0.581 x V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 7 V to 28 V [2] [3] [4]	0.396	-	-	
		$V_{th(rec)(max)}$ = 0.744 x V_{BAT}; $V_{th(dom)(max)}$ = 0.581 x V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 5 V to 7 V [2] [3] [4]	0.37	-	-	
δ2	duty cycle 2	$V_{th(rec)(min)}$ = 0.422 x V_{BAT}; $V_{th(dom)(min)}$ = 0.284 x V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 7.6 V to 28 V [2] [3] [4]	-	-	0.581	
		$V_{th(rec)(min)}$ = 0.422 x V_{BAT}; $V_{th(dom)(min)}$ = 0.284 x V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 5.6 V to 7.6 V [2] [3] [4]	-	-	0.581	
δ3	duty cycle 3	$V_{th(rec)(max)}$ = 0.778 x V_{BAT}; $V_{th(dom)(max)}$ = 0.616 x V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 7 V to 28 V [2] [3] [4]	0.417	-	-	
		$V_{th(rec)(max)}$ = 0.778 x V_{BAT}; $V_{th(dom)(max)}$ = 0.616 x V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 5 V to 7 V [2] [3] [4]	0.417	-	-	
δ4	duty cycle 4	$V_{th(rec)(min)}$ = 0.389 x V_{BAT}; $V_{th(dom)(min)}$ = 0.251 x V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 7.6 V to 28 V [2] [3] [4]	-	-	0.590	
		$V_{th(rec)(min)}$ = 0.389 x V_{BAT}; $V_{th(dom)(min)}$ = 0.251 x V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 5.6 V to 7.6 V [2] [3] [4]	-	-	0.590	
LIN receiver; pins LIN1, LIN2, LIN3, LIN4						
t_{rx_pd}	receiver propagation delay	rising and falling edge; 7 V ≤ V_{BAT} < 28 V [4]	-	-	6	µs
		rising and falling edge; 5 V < V_{BAT} < 7 V	-	-	6.5	µs
t_{rx_sym}	receiver propagation delay symmetry	rising edge with respect to falling edge [4]	-2	-	+2	µs
$t_{wake(dom)LIN}$	LIN dominant wake-up time		30	80	150	µs
$t_{to(dom)LIN}$	LIN dominant time-out time	timer started at falling edge on LINx	17.5	20	23.5	ms
$t_{to(dom)TXD}$	TXD dominant time-out time	timer started at falling edge on TXDx	6	-	10	ms
Mode transition						
$t_{wake(low)SLP}$	sleep LOW wake-up timeout time	for wake-up from Low Power or Standby to Normal mode	1.75	-	4.65	µs

Table 6. Dynamic characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{BAT} = 5.0 V to 28 V; V_{IO} = 2.97 V to 5.5V; all voltages are referenced to pin GND; positive currents flow into the IC; typical values are given at V_{BAT} = 12V; unless otherwise specified [1]

Symbols	Parameter	Conditions	Min	Typ	Max	Unit
$t_{tgotolp(high)SLP}$	sleep HIGH to low power time	for transition form Normal to Low Power mode	5.2	6	6.7	µs
t_{init}	initialization time	Normal and Standby modes	-	-	2.5	ms
$t_{d(lp)}$	low power mode delay time		-	-	2	ms
$t_{d(uvd-lp)}$	delay time from VIO UV to low power mode		175	-	225	ms
$t_{d(uvd)}$	undervoltage detection delay time		5	-	10	µs
$t_{d(uvr)}$	undervoltage recovery delay time		485	-	630	µs

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.

[2]
$$\delta 1,\delta 3 = \frac{t_{bus(rec)min}}{2\times t_{bit}};\quad \delta 2,\delta 4 = \frac{t_{bus(rec)max}}{2\times t_{bit}}$$

[3] Bus load conditions: $R_{commander}$ = off; C_{LIN} = 1 nF and R_{LIN} = 1 kΩ; C_{LIN} = 6.8 nF and R_{LIN} = 660 Ω; C_{LIN} = 10 nF and R_{LIN} = 500 Ω.

[4] See timing diagram in Fig 10.

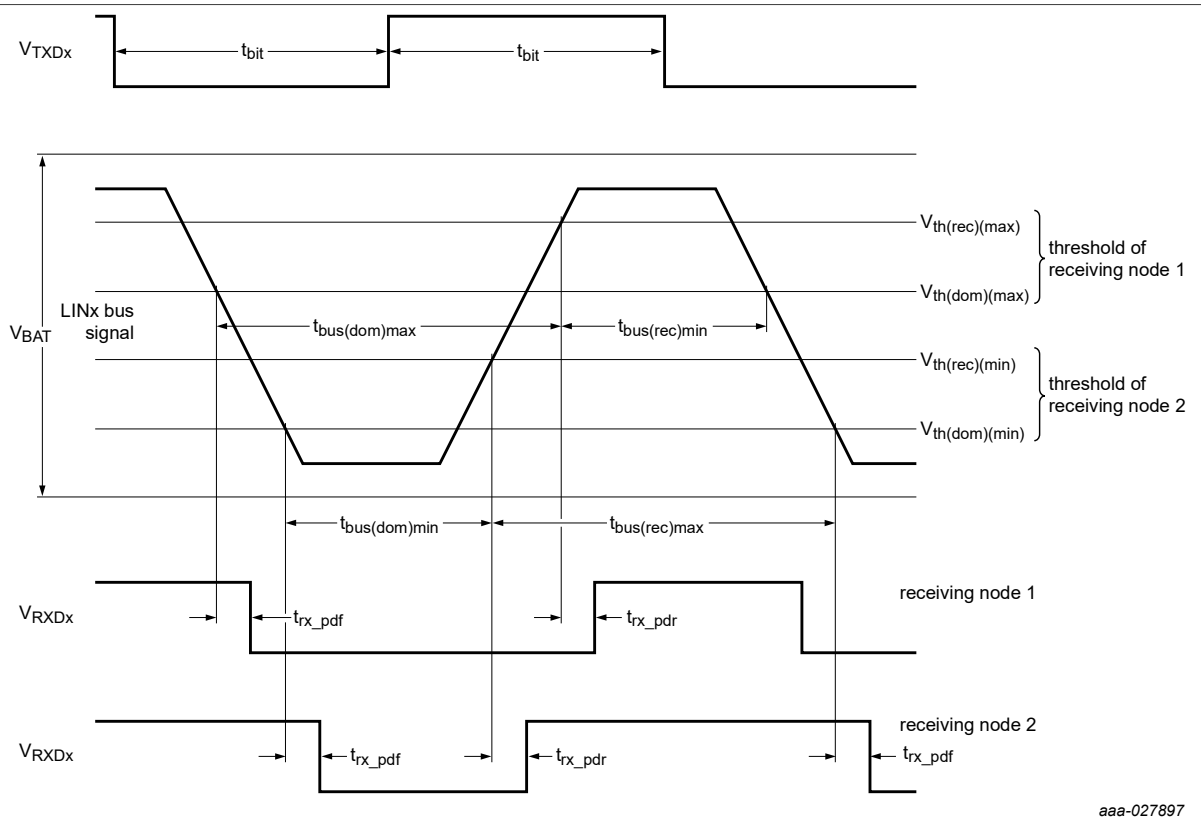
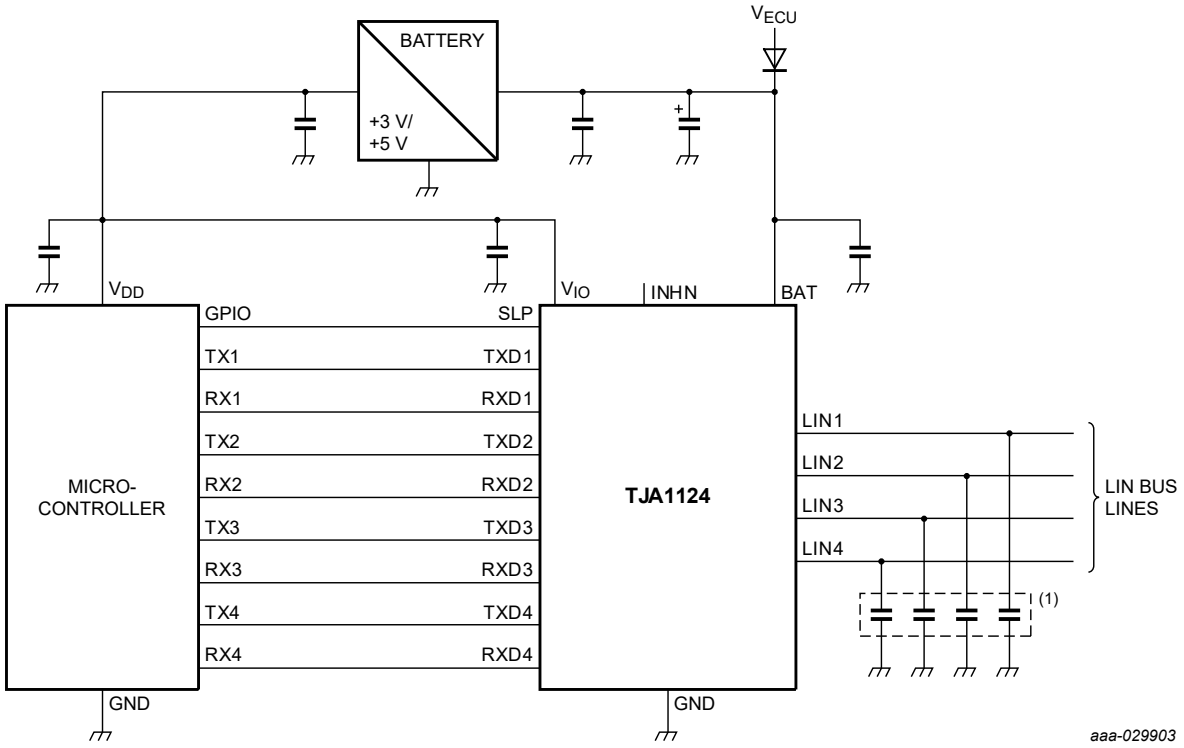


Figure 6. Timing diagram of LIN duty cycle

11 Application information

11.1 Application diagram

The minimum external circuitry needed with the TJA1124 is shown in Figure 7. Further information on external components and PCB layout can be found in the Application Hints document (see Section 11.3).



1. Typically specified by car manufacturer, e.g. 680pF

Figure 7. Application diagram

11.2 ESD robustness according to LIN EMC test specification

ESD robustness (IEC 61000-4-2) has been tested by an external test house according to the LIN EMC test specification (part of Conformance Test Specification Package for LIN 2.1, October 10th, 2008). The test report is available on request.

Table 7. ESD robustness (IEC 61000-4-2) according to LIN EMC test specification

Pin	Test configuration	Value	Unit
LINx	no capacitor connected to LINx pin	±8	kV
	220 pF capacitor connected to LINx pin	±8	kV
BAT	22 µF and 100 nF capacitors connected to pin BAT	>|15|	kV

11.3 Application hints

Further information on the application of the TJA1124 can be found in NXP application hints AH1705 *'Quad LIN commander transceiver SJA1124/TJA1124'*.

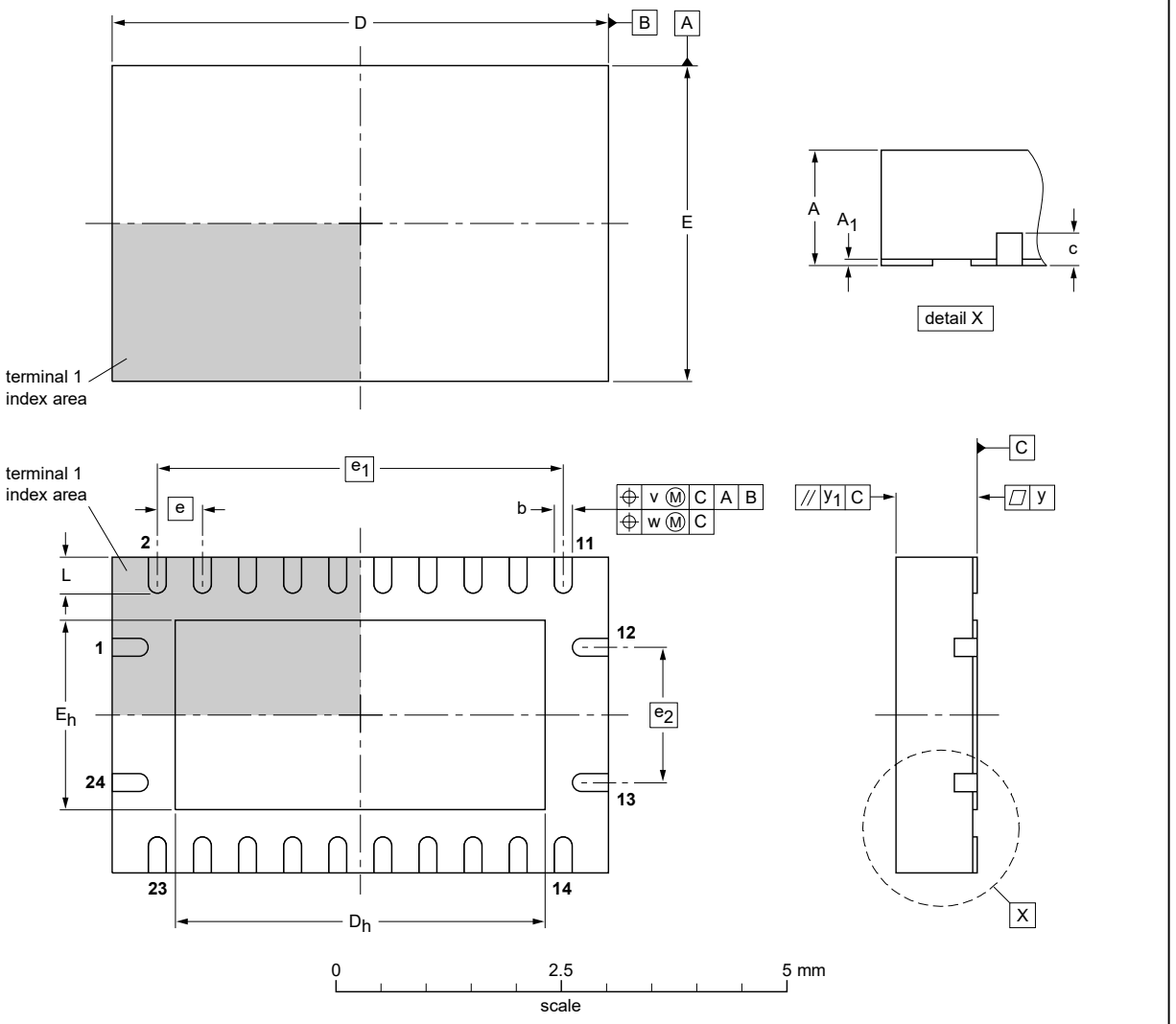
12 Test information

12.1 Quality information

After product release this product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 - *Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

13 Package outline

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm **SOT815-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.6 5.4	4.25 3.95	3.6 3.4	2.25 1.95	0.5	4.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT815-1	- - -	- - -	- - -			03-04-29

Figure 8. Package outline DHVQFN24

14 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

15 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 9) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 8 and Table 9

Table 8. SnPb eutectic process (from J-STD-020D)

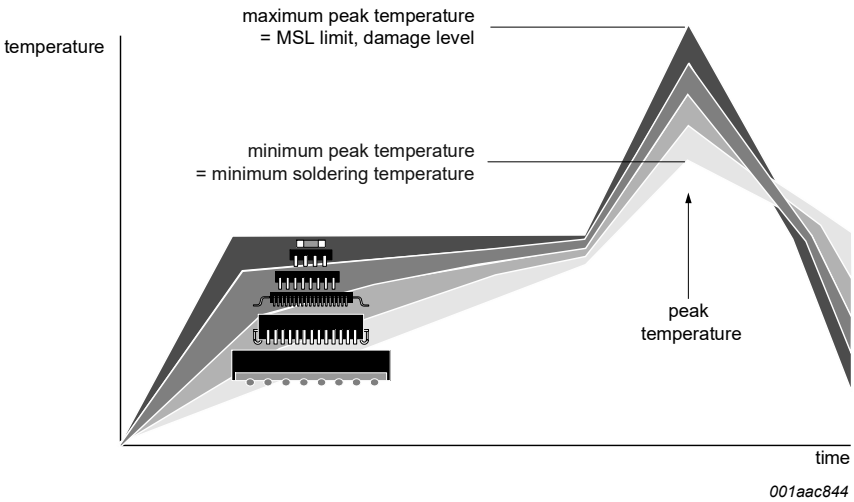
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 9. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 9.



MSL: Moisture Sensitivity Level

Figure 9. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16 Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1124 v.2.1	20220826	Product data sheet	-	TJA1124 v.2
Modifications:	• Section 6.5: behavior of V_{IO} when outside operating range but above undervoltage detection threshold clarified. • Table 3: V_{trt} conditions and values amended. • Table 6: values changed for parameters t_{init} and $t_{d(uvr)}$. • Section 17: *Suitability for use in Automotive applications* disclaimer revised; *Security* disclaimer added. • Terms master and slave replaced throughout with, respectively, commander and responder.			
TJA1124 v.2	20190925	Product data sheet	-	TJA1124 v.1
Modifications:	• TJA1124C variant added: Table 1, Section 6.8, parameters R_{master}, $R_{master(lp)}$ in Table 5. • Table 3: V_{ESD} section revised; tables notes added/amended; V_x specification for digital pins clarified. • Table 5: values changed for parameter I_{BAT} (Normal mode; bus recessive).			
TJA1124 v.1	20180508	Product data sheet	-	-

17 Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Suitability for use in automotive applications — This NXP product has been qualified for use in automotive applications. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as “Critical Applications”), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys’ fees) that NXP may incur related to customer’s incorporation of any product in a Critical Application.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer’s applications and products. Customer’s responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer’s applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

17.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.