TJA1128

LIN mini system basis chip

Rev. 1 — 29 March 2018 Product data sheet

1 General description

The TJA1128 is a LIN Mini System Basis Chip (SBC) with a LIN transceiver, a low-dropout voltage regulator (LDO), a window watchdog, two WAKE inputs, one general purpose input (GPI) and one high-voltage multipurpose (HVMPO) output. The voltage regulator delivers up to 85 mA and is available with 3.3 V and 5.0 V output voltages. The TJA1128 can be operated in very low-current STANDBY and SLEEP modes with bus and local wake-up capability.

2 Features and benefits

2.1 General

- Battery operating voltage range from (3.3 V) 5.0 V to 28 V
- Very low current consumption in SLEEP and STANDBY mode
  - SLEEP mode (voltage regulator off): typically 14 µA
  - STANDBY mode (voltage regulator on): typically 22 µA
- Remote wake-up capability via pin LIN
- Local wake-up via pins WAKE1 and WAKE2
  - Configurable level-sensitive wake-up detection
  - Cyclic sampled wake-up detection option with synchronized bias control via pin HVMPO
- Wake-up source recognition
- Configurable high-voltage multipurpose output (HVMPO)
  - Bias control output for cyclic wake-up
  - Limp home output
  - Bias control output for battery monitoring circuit
  - General purpose input (GPI) controlled output
- Limp home function on overtemperature, watchdog service fail, VCC undervoltage and RSTN short-circuit to ground
- Overtemperature shutdown
- Bidirectional reset pin with variable power-on reset length

2.2 Device customization

- Quasi one-time configuration via Serial Peripheral Interface (SPI)
- Initial mode to configure and disable
  - Functions (e.g., LIN, watchdog, Reset, WAKE)
  - Modes (e.g., SLEEP)

2.3 Low-dropout voltage regulator for 3.3 V/5.0 V microcontroller supply

- 5.0 V/3.3 V nominal output voltage, ±2 % accuracy
- 85 mA output current capability
- Undervoltage detection with reset output
- Excellent transient response with a small ceramic output capacitor
- Output is short-circuit proof to GND

2.4 LIN transceiver

- ISO 17987-4:2016 (12 V LIN) compliant
- LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A compliant
- SAE J2602-1 compliant
- K-line compatible
- Baud rate up to 20 kBd
- LIN high-speed mode with fast LIN slope to support high baud rates (> 20 kBd)
- Integrated termination resistor for LIN slave applications
- TXD dominant time-out function

2.5 Window watchdog

- Watchdog with Window, Timeout and Autonomous modes
- Microcontroller-independent clock source
- Watchdog period selectable between 16 ms and 128 ms
- Dedicated modes for software development and end-of-line flashing

2.6 Designed for automotive applications

- Qualified according to AEC-Q100
- Load dump pulse protected against up to 43 V
- ±8 kV Electrostatic Discharge (ESD) protection, according to the Human Body Model (HBM) on LIN-bus pin
- ±6 kV ESD protection according to IEC 61000-4-2 on pins BAT, WAKE1, WAKE2 and ±8 kV on pin LIN
- Bus terminal and battery pin protected against transients in the automotive environment (ISO 7637)
- LIN-bus pin short-circuit proof to battery and ground
- Leadless HVSON14 package (3.0 mm × 4.5 mm) supporting Automated Optical Inspection (AOI) capability and low thermal resistance

3 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TJA1128	14 pin HVSON	HVSON14; plastic, thermal enhanced very thin small outline package; no leads; 14 terminals, body 3 x 4.5 x 0.85 mm	SOT1086-2

3.1 Ordering options

Table 2. Overview of TJA1128 SBC family

Device	LDO supply	WAKE inputs	Watchdog	Initial CRC value
TJA1128A	5.0 V	1	No	6D
TJA1128B	3.3 V	1	No	C0
TJA1128C	5.0 V	2	No	C5
TJA1128D	3.3 V	2	No	68
TJA1128E	5.0 V	1	Yes	84
TJA1128F	3.3 V	1	Yes	29
TJA1128G	5.0 V	2	Yes	2C
TJA1128H	3.3 V	2	Yes	81

4 Block diagram

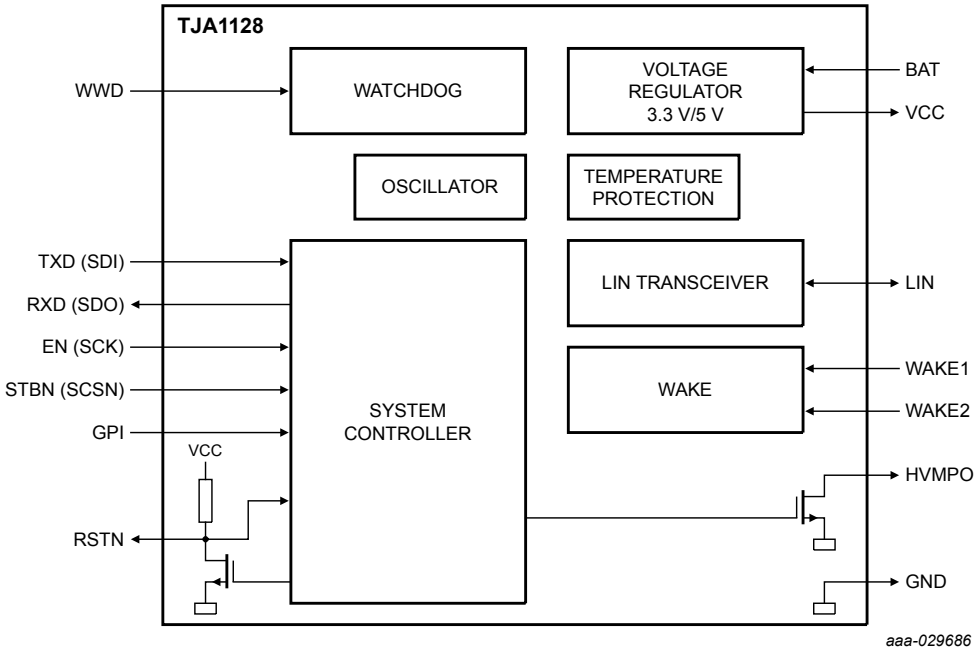


Figure 1. Block diagram

5 Pinning information

5.1 Pinning

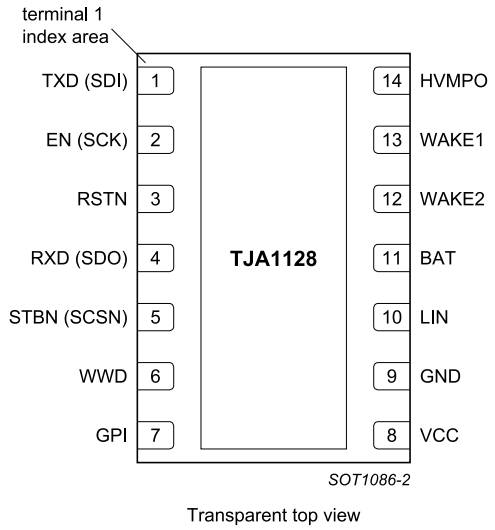


Figure 2. Pin configuration diagram

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
TXD (SDI)	1	LIN transmit data input (SPI data input in CONFIG mode)
EN (SCK)	2	Enable input (SPI clock input in CONFIG mode)
RSTN	3	Reset input/output; active-LOW
RXD (SDO)	4	LIN receive data output; wake-up event information (SPI data output in CONFIG mode)
STBN (SCSN)	5	Standby control input (SPI chip select input in CONFIG mode); active-LOW
WWD	6	Window watchdog trigger input
GPI	7	General purpose input
VCC	8	Voltage regulator output
GND	9	Ground
LIN	10	LIN bus line input/output
BAT	11	Battery supply
WAKE2	12	Local wake-up input 2
WAKE1	13	Local wake-up input 1
HVMPO	14	High-voltage multipurpose output (open-drain)

For enhanced thermal and electrical performance, the exposed center pad of the HVSON14 package should be soldered to board ground and not to any other voltage level.

6 Functional description

6.1 ISO 17987/LIN 2.x/SAE J2602 compliant

The TJA1128 is fully compliant with ISO 17987-4:2016 (12 V LIN), LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and SAE J2602. The LIN physical layer is independent of higher OSI model layers (e.g., the LIN protocol). Consequently, nodes containing an ISO 17987-compliant physical layer can be combined, without restriction, with LIN physical layer nodes that comply with earlier revisions (LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3, LIN 2.0, LIN 2.1, LIN 2.2 and LIN 2.2A).

6.2 Operating modes

The system controller contains a state machine that supports nine operating modes:

- NORMAL
- STANDBY
- PORT
- GOTOSLP
- SLEEP
- RESET
- CONFIG
- OVERTEMP
- OFF

The state transitions are illustrated in Figure 3.

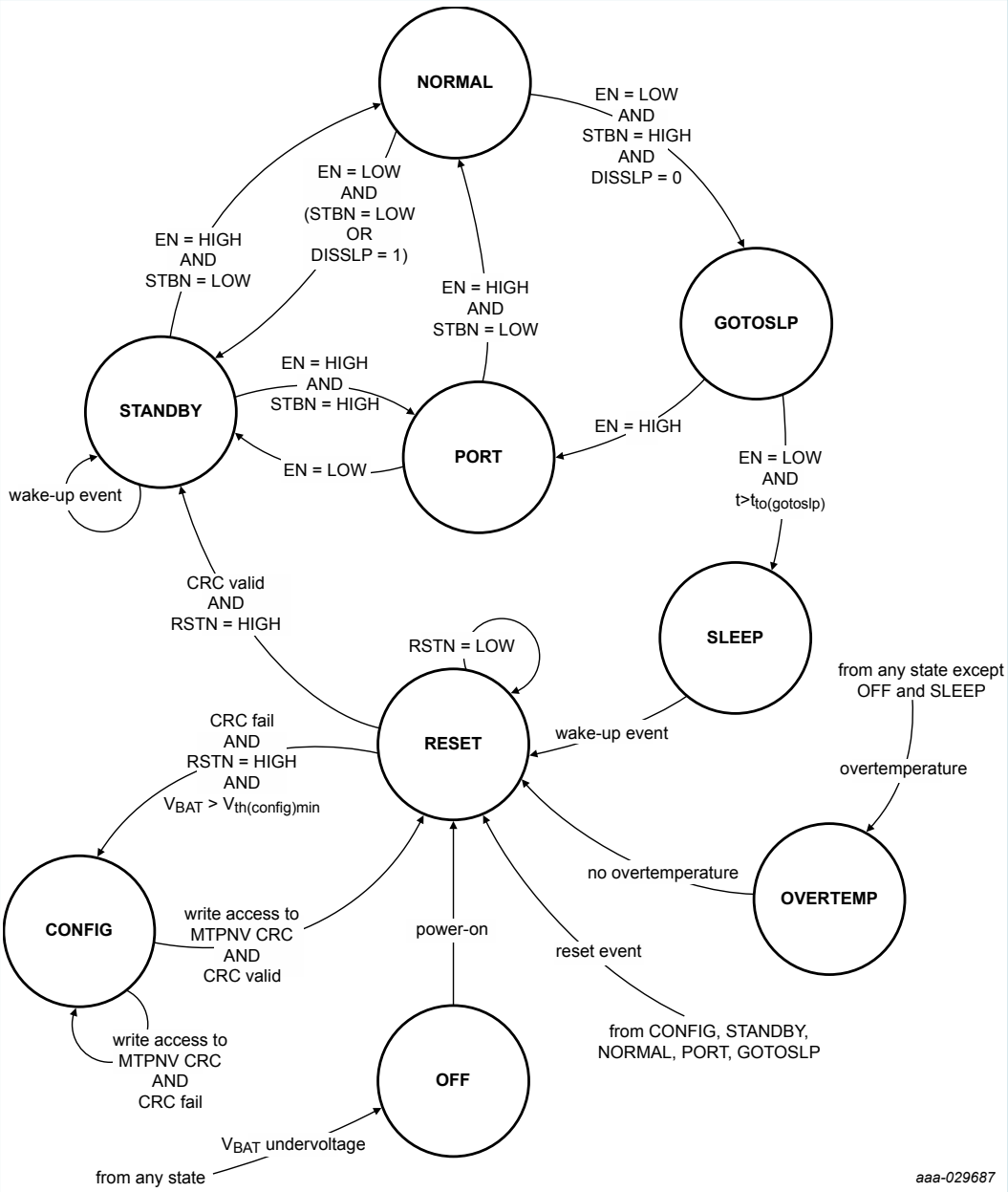


Figure 3. System controller state diagram

6.2.1 NORMAL mode

NORMAL mode is the active operating mode. In this mode, the voltage regulator VCC is enabled to supply a microcontroller. The LIN transceiver and the watchdog are active, provided that they are available and enabled. The LIN transceiver is enabled after its initialization time $t_{init(norm)}$.

Pending wake-up events are cleared in NORMAL mode.

The NORMAL mode can be entered from STANDBY mode and PORT mode. The TJA1128 switches from STANDBY mode to NORMAL mode when EN is pulled HIGH while STBN is LOW. The transition from PORT mode to NORMAL mode starts when STBN is pulled LOW, while EN is HIGH.

6.2.2 STANDBY mode

The STANDBY mode is a low-power mode with enabled voltage regulator VCC to supply a microcontroller. The LIN transceiver is disabled and the watchdog is either active or in autonomous mode, provided that the watchdog is available and enabled.

In STANDBY mode, wake-up event detection is provided. Depending on the device configuration, local wake-up events on WAKE1 and WAKE2 (if available) and remote LIN wake-up events can be detected. RXD is held LOW after detection of an enabled wake-up event.

The STANDBY mode can be entered from RESET mode, PORT mode and NORMAL mode. After RESET mode, the STANDBY mode is entered if the device is configured with a valid CRC value. A mode transition to STANDBY mode from NORMAL mode is initiated when EN is pulled LOW while STBN is LOW. If the SLEEP mode is disabled (DISSLP=1; see system register in Table 6), the NORMAL mode to STANDBY mode transition takes place when EN is pulled LOW, regardless of the STBN input level. The transition from PORT mode to STANDBY mode starts when EN is pulled LOW.

6.2.3 PORT mode

The PORT mode can be used to differentiate between PORT mode and CONFIG mode. Details are described in Section 6.2.10 "Differentiation between CONFIG and PORT modes". This is helpful during the software initialization phase to check whether the TJA1128 is already configured.

In addition, the TJA1128 provides in this mode, information about captured wake-up event sources, level status on WAKE1 and WAKE2 and limp home status. These status and capture flags can be read via a serial data format with a start bit encoded as LOW level and a stop bit encoded as HIGH level. Similar to UART data framing with 8N1-coding. When a 55h data is applied on TXD, the status and capture flags are transmitted on RXD. In Figure 4 the serial data format and the assignment of the status and capture flags are illustrated.

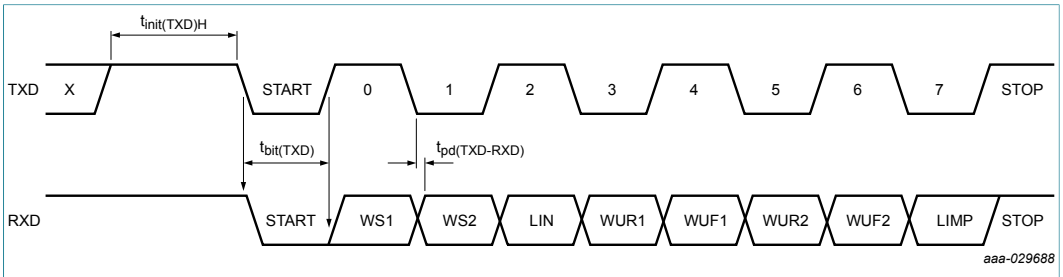


Figure 4. Serial data format in PORT mode

The wake-up event sources and limp home status are signaled as active LOW, see Table 4. These capture wake-up events and the limp home status will be cleared on the rising edge of stop bit.

The level status on WAKE1 and WAKE2 as well as the capture flag status is sampled on falling edge of start bit. However, after the falling edge of the start bit, new wake and limp home events will be captured and not cleared on the rising edge of the associated stop bit.

Table 4. PORT mode capture and status information

Bit	Symbol	Value	Description
7	LIMP	—	Limp home
		0	Limp home event detected
		1	No limp home event detected
6	WUF2	—	Wake-up on falling edge on WAKE2
		0	Falling edge detected on WAKE2
		1	No falling edge detected on WAKE2
5	WUR2	—	Wake-up on rising edge on WAKE2
		0	Rising edge detected on WAKE2
		1	No rising edge detected on WAKE2
4	WUF1	—	Wake-up on falling edge on WAKE1
		0	Falling edge detected on WAKE1
		1	No falling edge detected on WAKE1
3	WUR1	—	Wake-up on rising edge on WAKE1
		0	Rising edge detected on WAKE1
		1	No rising edge detected on WAKE1
2	LIN	—	LIN wakeup
		0	LIN wake-up event detected
		1	No LIN wake-up event detected
1	WS2	—	WAKE2 status
		0	Voltage on WAKE2 is below switching threshold ($V_{th(sw)}$)
		1	Voltage on WAKE2 is above switching threshold ($V_{th(sw)}$)
0	WS1	—	WAKE1 status
		0	Voltage on WAKE1 is below switching threshold ($V_{th(sw)}$)
		1	Voltage on WAKE1 is above switching threshold ($V_{th(sw)}$)

The PORT mode can be entered from STANDBY mode, and GOTOSLP mode. A TJA1128 mode transition to PORT mode is initiated either from GOTOSLP mode when EN is pulled HIGH or from STANDBY mode when EN is pulled HIGH while STBN is HIGH.

6.2.4 GOTOSLP mode

The GOTOSLP mode is a temporary mode with enabled voltage regulator VCC. The LIN transceiver is disabled and the watchdog is either active or in autonomous mode, provided that the watchdog is available and enabled.

In GOTOSLP mode, wake-up event detection is provided. Depending on the device configuration local wake-up events on WAKE1 and WAKE2 (if available) and remote LIN

wake-up events can be detected. RXD is held LOW after detection of an enabled wake-up event.

The GOTOSLP mode can be entered from NORMAL mode. A mode transition is initiated when EN is pulled LOW while STBN is HIGH, provided the SLEEP mode is enabled.

6.2.5 SLEEP mode

The SLEEP mode is the low-power mode with the lowest power consumption. The low-dropout voltage regulator, the LIN transceiver and the watchdog are disabled. Pin RSTN is forced LOW.

In SLEEP mode, wake-up event detection is provided. Depending on the device configuration, local wake-up events on WAKE1 and WAKE2 (if available) and remote LIN wake-up events can be detected.

The SLEEP mode is entered from GOTOSLP mode, when the GOTOSLP mode time-out $t_{to(gotoslp)}$ has been exceeded, while EN is LOW.

6.2.6 RESET mode

The RESET mode is a temporary mode to ensure that pin RSTN is pulled down for a defined time to allow the microcontroller to start up in a controlled manner.

The TJA1128 switches to RESET mode in response to a reset event. See Section 6.5 "System reset".

6.2.7 OFF mode

In OFF mode the power-on detection is enabled; all other functions are inactive. The TJA1128 starts to boot up when the battery voltage exceeds the power-on detection threshold $V_{th(det)pon}$ (triggering a start-up process). The start-up process from OFF mode via RESET mode to either STANDBY mode or CONFIG mode is completed after the start-up time, $t_{startup}$.

The TJA1128 switches to OFF mode when the battery supply is first connected or from any mode when the battery voltage drops below the power-off detection threshold $V_{th(det)poff}$.

6.2.8 OVERTEMP mode

The OVERTEMP mode is provided to prevent the TJA1128 from being damaged by excessive temperatures. The low-dropout voltage regulator, the LIN transceiver and the watchdog are disabled. Pin RSTN is forced LOW. No wake-up event will be detected.

The TJA1128 switches immediately to OVERTEMP mode from any mode (other than OFF mode or SLEEP mode) when the global chip temperature exceeds the overtemperature protection activation threshold, $T_{th(act)otp}$.

6.2.9 CONFIG mode

The CONFIG mode is provided for device configuration via SPI. Only in this mode device pins 1, 2, 4 and 5 are used as SPI. See pinning information in Section 5 "Pinning information". In CONFIG mode the low-dropout voltage regulator is enabled; LIN transceiver, watchdog and wake-up detection are disabled.

The SBC configuration options are described in Section 6.3.3 "SBC configuration register". The nonvolatile SBC configuration is described in Section 6.3.4 "Nonvolatile SBC configuration".

The CONFIG mode can be entered from RESET mode. After RESET mode, the CONFIG mode is entered if the device is not configured with a valid CRC value and the supply voltage is above minimum configuration threshold $V_{th(config)min}$. Based on the signal sequence it can be checked whether the SBC is in CONFIG mode. Details are described in Section 6.2.10 "Differentiation between CONFIG and PORT modes".

6.2.10 Differentiation between CONFIG and PORT modes

The CONFIG mode can be distinguished from the PORT mode via the RXD (SDO) output level. As illustrated in Figure 5, after the transition to PORT mode the RXD (SDO) output turns to HIGH. Whereas, in CONFIG mode the SDO (RXD) output turns to LOW after SCSN (STBN) is pulled HIGH.

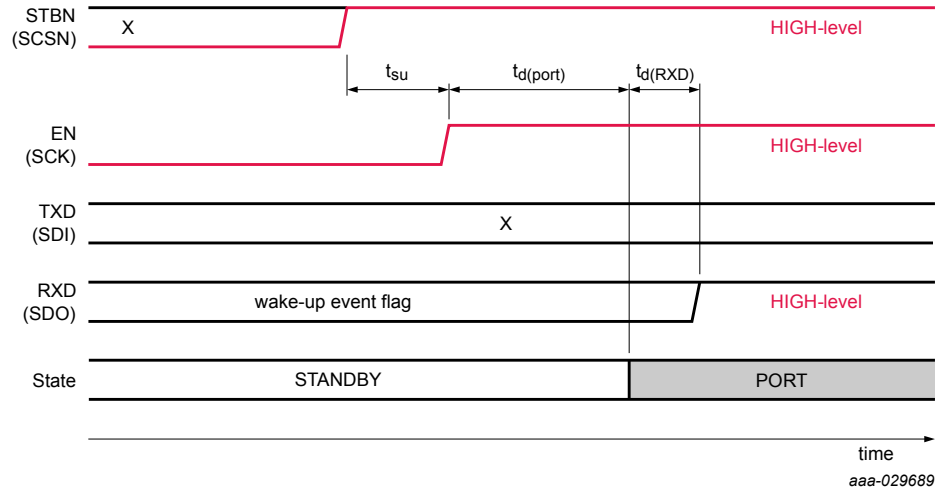


Figure 5. RXD (SDO) output after transition to PORT mode

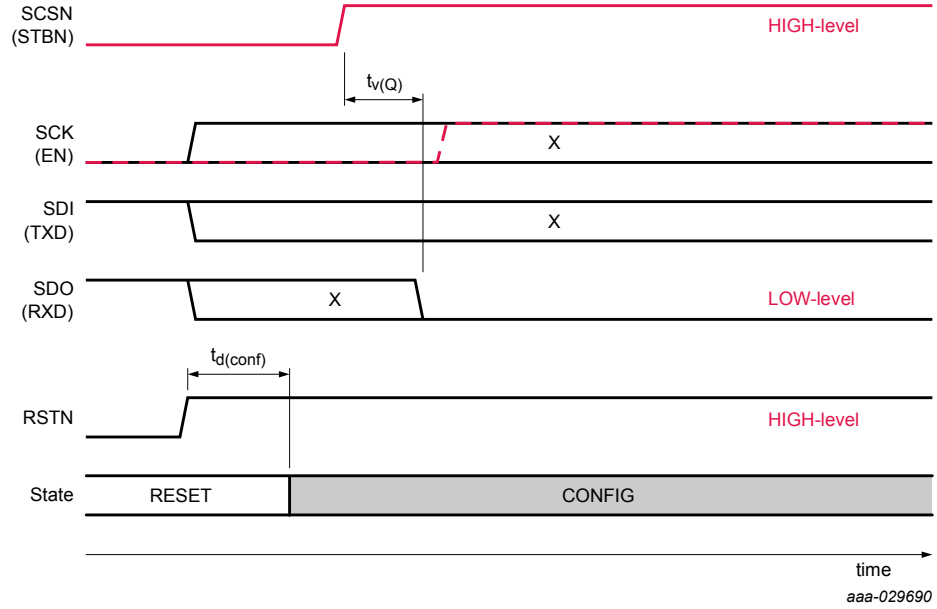


Figure 6. SDO (RXD) output after SCSN (STBN) turns to HIGH-level

In Figure 6 it is illustrated, that with the same pattern on STBN (SCSN) and EN (SCK) as shown in Figure 5, on the RXD (SDO) output level the TJA1128 modes CONFIG and PORT can be determined.

6.3 SBC configuration

6.3.1 SPI

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller for the SBC configuration. The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing the application to read back registers without changing the register content.

The SPI uses four interface signals for synchronization and data transfer: SCSN (STBN), SCK (EN), SDI (TXD) and SDO (RXD). For detail pinning information see Section 5 "Pinning information".

Bit sampling is performed on the falling edge of the clock and data is shifted in/out on the rising edge, as illustrated in Figure 12.

The SPI data in the TJA1128 is stored in a number of dedicated 8-bit registers. Each register is assigned a unique 7-bit address. Two bytes (16 bits) must be transmitted to the SBC for a single register read or write operation. The first byte contains the 7-bit address along with a read-only bit (the LSB). The read-only bit must be 0 to indicate a write operation (if this bit is 1, a read operation is assumed and any data on the SDI pin is ignored). The second byte contains the data to be written to the register.

24-bit read and write operations is also supported. The register address is automatically incremented, as illustrated in Figure 7.

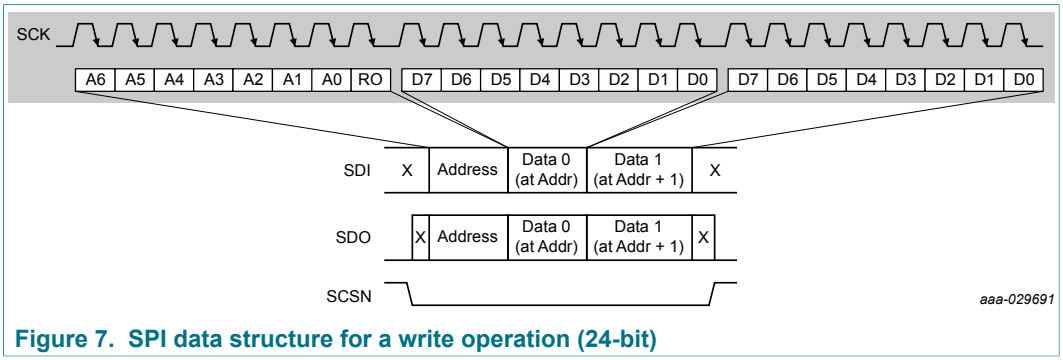


Figure 7. SPI data structure for a write operation (24-bit)

The content of the addressed registers is returned via pin SDO (RXD) during a SPI data read or write operation, i.e., the prior register content before the new value is set.

The TJA1128 tolerates attempts to write to registers that do not exist. If the available address space is exceeded during a write operation, the data above the valid address range is ignored. During a write operation, the TJA1128 monitors the number of SPI bits transmitted. If the number recorded is not 16 or 24, then the write operation is aborted.

A SPI access must not be attempted for at least $t_{d(conf)}$ after a positive edge on RSTN. Any earlier access may be ignored.

6.3.2 Register map overview

The addressable register space is 128 registers with addresses from 0x00 to 0x7F. Of these, 8 registers are available for SPI access. An overview of the register mapping is provided in Table 5. Further details are provided in Section 6.3.3 "SBC configuration register" and Section 6.3.4 "Nonvolatile SBC configuration".

Table 5. Register map overview

Address	Register name	Bits							
		7	6	5	4	3	2	1	0
10h	System	reserved			RSTTIM	reserved			DISSLP
11h	Wake	reserved			BUSWKE	LC2WKE		LC1WKE	
12h	LDO	reserved							DISVCCUV
13h	LIN	reserved				DISLIN	HSMODE		DISTXTO
14h	Watchdog	WDSDM	reserved	WDPER		reserved	WDAUTO	WDMOD	
15h	HVMPO	reserved		WKBSET	WKBPER	MPOINV	MPOMOD		
30h	MTPNV CRC	CRC							
31h	MTPNV status	NVMPS	NVERR	WRCNTS					

6.3.3 SBC configuration register

In Table 6, the system register bit assignment is listed. In this register the output reset pulse (see Section 6.5 "System reset") can be selected and the SLEEP mode (see Section 6.2.5 "SLEEP mode") can be disabled.

Table 6. System register (address 10h)

*Legend: * factory preset value*

Bit	Symbol	Access	Value	Description
7 to 5	reserved	R	—	—
4	RSTTIM	R/W	—	RSTN output reset pulse width
			0*	$t_{w(rst)}$ = 4 ms
			1	$t_{w(rst)}$ = 700 µs
3 to 1	reserved	R	—	—
0	DISSLP	R/W	—	disable SLEEP mode
			0*	SLEEP enabled
			1	SLEEP disabled

In the wake register the wake detection configuration bits for the local wake-up inputs WAKE1 and WAKE2 (see Section 6.9 "Local wake-up inputs") and for the LIN transceiver (Section 6.8 "LIN transceiver") are provided. The bit assignment is listed in Table 7.

Table 7. Wake register (address 11h)

*Legend: * factory preset value*

Bit	Symbol	Access	Value	Description
7 to 5	reserved	R	—	—
4	BUSWKE[1][2]	R/W	—	remote LIN bus wake-up enable
			0*	LIN wake-up disabled
			1	LIN wake-up enabled
3 to 2	LC2WKE[1]	R/W	—	local WAKE2 configuration
			00*	local disabled
			01	local wake-up on rising edge
			10	local wake-up on falling edge
			11	local wake-up on both edges
1:0	LC1WKE[1]	R/W	—	local WAKE1 configuration
			00*	local disabled
			01	local wake-up on rising edge
			10	local wake-up on falling edge
			11	local wake-up on both edges

[1] Do not disable all wake sources when the SLEEP mode is enabled. In this case only a power-on event can cause a transition out of SLEEP mode.
[2] The LIN wake-up is disabled irrespective of the BUSWKE bit setting, if the LIN transceiver is disabled (DISLIN = 1).

The LDO register can be used to disable the VCC undervoltage detection. See Section 6.7.2 "Low-dropout voltage regulator (pin VCC)". In Table 8 the LDO register bit assignment is listed.

Table 8. LDO register (address 12h)

*Legend: * factory preset value*

Bit	Symbol	Access	Value	Description
7 to 1	reserved	R	—	—
0	DISVCCUV	R/W	—	disable VCC undervoltage detection
			0*	VCC undervoltage detection enabled
			1	VCC undervoltage detection disabled

The LIN register in Table 9 provides the LIN transceiver configuration options. In this register LIN high-speed mode can be enabled and the TXD dominant time-out can be disabled. Furthermore, the LIN transceiver can be disabled. Details are provided in Section 6.8 "LIN transceiver".

Table 9. LIN register (address 13h)

*Legend: * factory preset value*

Bit	Symbol	Access	Value	Description
7 to 4	reserved	R	—	—
3	DISLIN	R/W	—	disable LIN transceiver
			0*	LIN transceiver enabled
			1	LIN transceiver disabled
2 to 1	HSMODE	R/W	—	LIN high-speed mode
			00*	LIN high-speed mode disabled
			01	LIN high speed mode enabled until next BAT power-on event
			10	LIN high speed mode enabled
			11	LIN high-speed mode disabled
0	DISTXTO	R/W	—	disable LIN TXD dominant time-out
			0*	LIN TXD dominant time-out enabled
			1	LIN TXD dominant time-out disabled

In the watchdog register the watchdog (see Section 6.4 "Watchdog") configuration options are provided. The watchdog mode and period can be chosen. In addition, the software development mode can be enabled. In Table 10 the watchdog register bit assignment is listed.

Table 10. Watchdog register (address 14h)

*Legend: * factory preset value*

Bit	Symbol	Access	Value	Description
7	WDSDM	R/W	—	watchdog software development mode
			0*	software development mode disabled
			1	software development mode enabled
6	reserved	R	—	—

Bit	Symbol	Access	Value	Description
5 to 4	WDPER	R/W	—	watchdog nominal period
			00*	16 ms
			01	32 ms
			10	64 ms
			11	128 ms
3	reserved	R	—	—
2	WDAUTO	R/W	—	watchdog autonomous mode
			0*	autonomous mode disabled
			1	autonomous mode enabled
1 to 0	WDMOD	R/W	—	watchdog operation mode
			00*	watchdog disabled
			01	window mode
			10	timeout mode
			11	watchdog disabled

With the HVMPO register the use of the HVMPO can be configured. It can be used to enable and configure the cyclic wake function. Furthermore, the HVMPO can be configured as LIMP home output, as state controlled output and as GPI controlled output. In Table 11 the HVMPO register bit assignment is listed.

Table 11. HVMPO register (address 15h)

*Legend: * factory preset value*

Bit	Symbol	Access	Value	Description
7 to 6	reserved	R	—	—
5	WKBSET	R/W	—	cyclic wake nominal settle time
			0*	$t_{set(cyclicwk)}$ = 70 µs
			1	$t_{set(cyclicwk)}$ = 134 µs
4	WKBPER	R/W	—	cyclic wake nominal period time
			0*	$t_{per(cyclicwk)}$ = 16 ms
			1	$t_{per(cyclicwk)}$ = 64 ms
3	MPOINV	R/W	—	inverted HVMPO
			0*	HVMPO not inverted
			1	HVMPO inverted

Bit	Symbol	Access	Value	Description
2 to 0	MPOMOD	R/W	—	HVMPO operation mode
			000*	disabled
			001	GPI controlled output
			010	bias control output for cyclic wake-up
			011	LIMP home output
			100	state controlled output: NORMAL
			101	state controlled output: NORMAL + STANDBY + PORT
			110	state controlled output: NORMAL + STANDBY+ PORT + GOTOSLP
			111	state controlled output: SLEEP

6.3.4 Nonvolatile SBC configuration

The TJA1128 has multiple time programmable (MTP) nonvolatile memory (NVM) cells to support programming of default device configuration. The MTPNVM address range is from 10h to 15h. For details. See Section 6.3.3 "SBC configuration register".

6.3.4.1 Programming of MTPNVM

NXP delivers the TJA1128 in the CONFIG mode as initial mode, also referred to as the *factory preset* configuration. The CONFIG mode is described in Section 6.2.9 "CONFIG mode".

If the TJA1128 has been programmed previously, the factory presets may need to be restored before reprogramming can begin. See Section 6.3.4.2 "Restoring factory preset values". When the factory presets have been restored successfully, a system reset is generated automatically and TJA1128 switches back to CONFIG mode.

Programming of the SBC configuration register listed in Section 6.3.3 "SBC configuration register" is performed in two steps. First, the required SBC configuration values are written to registers. In a second step, the programming is confirmed by writing the correct CRC value to register MTPNV CRC. See Table 13. The MTPNVM will be programmed with the SBC configuration values, provided these configuration values in conjunction with the initial CRC value (see Table 2) matches with the correct CRC value. If the CRC value is not correct, programming is aborted. After a successful MTPNVM programming a system reset of the TJA1128 is generated to indicate that the MTPNVM has been programmed successfully.

During MTPNVM programming the supply voltage must continue in the battery supply voltage operating range. MTPNVM programming shall not be done at cold or hot temperature conditions (see T_{vj} when programming the MTPNVM). MTPNVM programming time takes up to $t_{prog(MTPNV)}$.

The MTPNV status register contains the MTPNVM write counter value WRCNTS, the error status bit NVERR and the MTPNVM programming status bit NVMPS. The WRCNTS value is increased with each MTPNVM program cycle until 3Fh is reached (no overflow). Note the purpose of this counter is to provide information and not to prevent reprogramming if the maximum limit is reached. The error status bit NVERR indicates whether a MTPNVM fault was detected. Table 12 lists the MTPNV status register.

Table 12. MTPNV status (address 31h)

Bit	Symbol	Access	Value	Description
7	NVMPS	R	—	nonvolatile memory programming status
			0	MTPNVM cannot be overwritten
			1	MTPNVM write access enabled
6	NVERR	R	—	error status
			0	error detected
			1	no error
5 to 0	WRCNTS	R	—	write counter status
			xxxxxx[1]	Number of MTPNVM write accesses

[1] Value depends on number of MTPNVM program cycles. Initial value is 00h.

The cyclic redundancy check value stored in the MTPNV CRC register (see Table 13) is calculated using the data written to SBC configuration registers from Section 6.3.3 "SBC configuration register" (address 10h to 15h) and adding at the end two bytes: 1st byte with 00h and 2nd byte with 01h. All reserved bits shall be interpreted as 0 during CRC calculation.

Table 13. MTPNV CRC (address 30h)

Bit	Symbol	Access	Value	Description
7 to 0	CRC	R/W	—	cyclic redundancy check
			—	CRC value

The CRC value is sequentially calculated using the data in the SBC configuration registers in an incremental address order and the modulo-2 division with the generator polynomial: X8 + X5 + X3 +X2 + X + 1. The result of this operation must be bitwise inverted.

The following parameters can be used to calculate the CRC value (e.g., via the AUTOSAR method):

Table 14. Parameter for CRC coding

Parameter	Value
CRC value	8 bits
Polynomial	2Fh
Initial CRC value	depends on TJA1128 variant; see Table 2
Input data reflected	no
Result data reflected	no
XOR value	FFh

Alternatively, the following algorithm can be used:

```
data = 0 // unsigned byte
crc = initial_CRC // depends on TJA1128 variant
sbc_register(0) = system_register_content
sbc_register(1) = wake_register_content
sbc_register(2) = ldo_register_content
sbc_register(3) = lin_register_content
sbc_register(4) = watchdog_register_content
sbc_register(5) = hvmpo_register_content
sbc_register(6) = 0 // additional fixed value to be used for
 calculation
sbc_register(7) = 1 // additional fixed value to be used for
 calculation
for i = 0 to 7
  data = sbc_register(i) EXOR crc
  for j = 0 to 7
    if data ≥ 128
      data = data * 2 // shift left by 1
      data = data EXOR 0x2F
    else
      data = data * 2 // shift left by 1
    next jcrc = data
next i
crc = crc EXOR 0xFF
```

6.3.4.2 Restoring factory preset values

Factory preset values are restored, if the following conditions apply continuously for at least $t_{d(MTPNV)rst}$ during battery power-up:

- $V_{BAT} > V_{th(config)min}$
- pin RSTN is held LOW
- LIN is held dominant

After the factory preset values have been restored and LIN is recessive again, the TJA1128 performs a system reset and enters the CONFIG mode.

During factory restore the supply voltage must continue in the battery supply voltage operating range. The restoring takes up to $t_{prog(MTPNV)}$.

Note that the write counter, WRCNTS, in the register MTPNV status is incremented every time the factory presets are restored.

6.4 Watchdog

The TJA1128 contains a watchdog that supports two operating modes: window and timeout. In window mode, a watchdog trigger event within a defined watchdog window triggers and resets the watchdog timer. In timeout mode, the watchdog runs continuously and can be triggered and reset at any time within the watchdog period by a watchdog trigger. The watchdog mode bits WDMOD are listed in the watchdog register. See Table 10.

In addition, the TJA1128 provides a watchdog autonomous mode. In this mode, the watchdog switches off after a transition from NORMAL mode to either STANDBY mode or GOTOSLP mode. The watchdog is switched on again after a wake-up event or a

transition to NORMAL mode. The watchdog autonomous bit WDAUTO is listed in the watchdog register, See Table 10.

Four watchdog periods are supported, from 16 ms to 128 ms. The watchdog period is programmed via bits WDPER in the watchdog register. See Table 10. The selected period is valid for both window and timeout modes.

Independent of the watchdog setting the watchdog start-up behavior is always identical. For the first trigger the watchdog mode is timeout mode with the maximum watchdog nominal period. Afterwards the watchdog mode and period is according to the watchdog setting.

A watchdog trigger event resets the watchdog timer. A watchdog trigger event is a LOW pulse on the WWD pin for $t_{trig(d)low}$ at least.

The TJA1128 supports also a watchdog software development mode. It is provided for test and development purposes only and is not a dedicated SBC operating mode. The TJA1128 can be in any functional operating mode with watchdog software development mode enabled. This mode is enabled and disabled via bit WDSDM in the watchdog register. See Table 10. In the watchdog software development mode, the watchdog can be disabled or activated for test and software debugging purposes. During the transition from RESET to STANDBY the input level on the WWD pin is checked; with HIGH-level the watchdog is enabled and with LOW-level the watchdog is disabled.

6.5 System reset

When a system reset occurs, the SBC switches to RESET mode and initiates a process that generates a low-level pulse on pin RSTN. The TJA1128 can distinguish up to 10 different reset sources, as detailed in Table 15.

Table 15. Reset sources

Reset sources	Description
power-on	mode transition from OFF to RESET when $V_{BAT} > V_{th(det)pon}$
LIN wake	mode transition from SLEEP to RESET after LIN wake-up
WAKE1 wake	mode transition from SLEEP to RESET after WAKE1 wake-up
WAKE2 wake	mode transition from SLEEP to RESET after WAKE2 wake-up
device configured	mode transition from CONFIG to RESET after device configuration
watchdog overflow	watchdog timer overflow in timeout mode or window mode
watchdog trigger fault	watchdog triggered too early in window mode
RSTN LOW	RSTN pulled LOW externally
VCC undervoltage	VCC undervoltage detection when $V_{O(VCC)} < V_{uvd(VCC)}$
overtemperature	overtemperature detection when $T_{vj} > T_{th(act)otp}$
factory restore	factory preset values are restored

6.5.1 Characteristics of pin RSTN

Pin RSTN is a bidirectional open-drain low side driver with integrated pull-up resistor, as shown in Figure 1. With this configuration, the SBC can detect the pin being pulled down externally, e.g., by the microcontroller. The input reset pulse width must be at least $t_{w(rst)}$ to guarantee that external reset events are detected correctly.

6.5.2 Selecting the output reset pulse time width

The duration of the output reset pulse can be configured in the CONFIG mode via bit RSTTIM in the System register. See Table 6.

6.6 Temperature protection

The temperature of the TJA1128 is monitored, except in SLEEP and OFF modes. The SBC switches to OVERTEMP mode if the global chip temperature exceeds the overtemperature protection activation threshold, $T_{th(act)otp}$. In Section 6.2.8 "OVERTEMP mode" the OVERTEMP mode is described.

When the global chip temperature drops below the overtemperature protection release threshold, $T_{th(rel)otp}$, the SBC switches to STANDBY mode via RESET mode.

6.7 Power supplies

6.7.1 Battery supply voltage (pin BAT)

The internal circuitry is supplied from the battery via pin BAT. The device must be protected against negative supply voltages, e.g., by using an external series diode.

The TJA1128 starts up when the battery voltage exceeds the power-on detection threshold, $V_{th(det)pon}$. If V_{BAT} drops below the power-off detection threshold, $V_{th(det)poff}$, the SBC switches to OFF mode. In Section 6.2.7 "OFF mode" the OFF mode is described.

6.7.2 Low-dropout voltage regulator (pin VCC)

The TJA1128 provides a 5 V or 3.3 V supply (VCC), depending on the variant. Pin VCC can deliver up to 85 mA load current. It is designed to supply the microcontroller and its peripherals.

LDO supply current depends on VCC load current. As VCC load current increases, LDO supply current increases. For a battery supply voltage on pin BAT of 16 V and a VCC load current of 70 mA, the typical LDO supply current increases by 0.8 mA.

The output voltage on VCC is monitored. A system reset is generated, if the voltage on VCC drops below the VCC undervoltage detection threshold, $V_{uvd(VCC)}$, provided VCC undervoltage detection is enabled (DISVCCUV = 0; see LDO register in Table 8).

6.8 LIN transceiver

The LIN transceiver is the interface between the LIN master/slave protocol controller and the physical bus in a LIN network. According to the Open System Interconnect (OSI) model, this interface makes up the LIN physical layer. The LIN transceiver is optimized for, but not limited to, automotive applications with excellent ElectroMagnetic Compatibility (EMC) performance.

The LIN transceiver can be disabled (via bit DISLIN; see LIN register in Table 9) to support applications where a LIN transceiver is not used.

6.8.1 Remote wake-up via the LIN bus

The TJA1128 detects a remote wake-up via the LIN bus in GOTOSLP, PORT, RESET, STANDBY and SLEEP mode, provided remote LIN bus wake-up is enabled (BUSWKE = 1; see Wake register in Table 7.

A falling edge on pin LIN, followed by a LOW level maintained for $t_{wake(dom)LIN}$, followed by a rising edge on pin LIN, triggers a remote wake-up. See Figure 8 and Figure 9. Note that the time period $t_{wake(dom)LIN}$ is measured either in NORMAL mode while TXD is HIGH, or in GOTOSLP, PORT, RESET, STANDBY and SLEEP mode irrespective of the status of pin TXD.

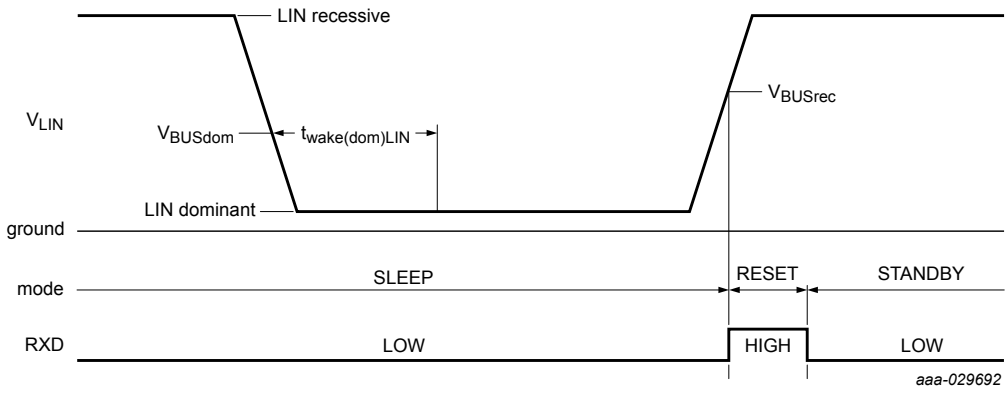


Figure 8. Principle of remote wake-up via LIN bus during SLEEP mode

The remote LIN bus wake-up request is communicated to the microcontroller in STANDBY (see Section 6.2.2 "STANDBY mode") and GOTOSLP (see Section 6.2.4 "GOTOSLP mode") mode by a continuous LOW level on pin RXD.

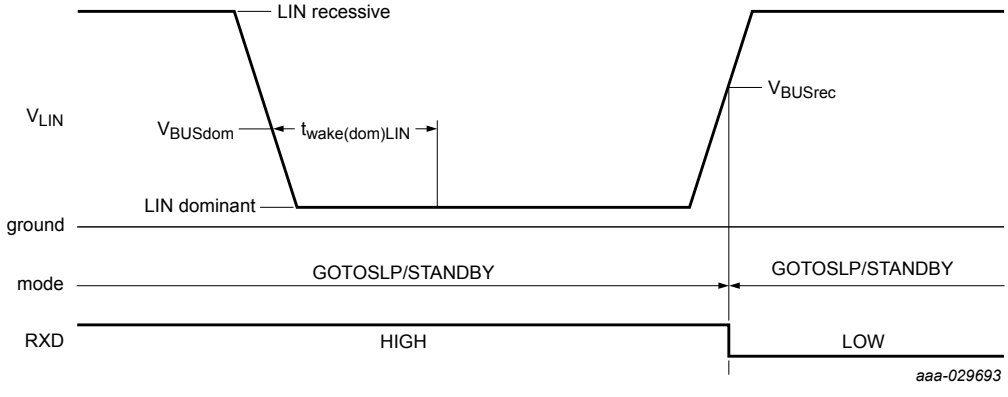


Figure 9. Principle of remote wake-up via LIN bus during GOTOSLP and STANDBY mode

6.8.2 Initial TXD dominant check

An initial TXD dominant check prevents the bus line being driven to a permanent dominant state (blocking all network communications) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The TXD input level is checked after a transition to NORMAL mode. If TXD is LOW, the transmit path remains disabled and is only enabled when TXD goes HIGH.

6.8.3 TXD dominant time-out

A TXD dominant time-out timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communications) if pin TXD is forced permanently LOW by a hardware and/or software application failure. This timer is started every time pin TXD goes LOW. If the LOW state on pin TXD persists for longer than the TXD dominant time-out time ($t_{to(dom)TXD}$), the transmitter is disabled, releasing the bus line to recessive state. The TXD dominant time-out timer is reset when pin TXD goes HIGH.

This function can be disabled (via bit DISTXTO; see LIN register in Table 9) to allow the TJA1128 to be used in applications requiring the transmission of long LOW sequences.

6.8.4 LIN high-speed mode

The TJA1128 provides two LIN high-speed mode configuration options (via bits HSMODE). See LIN register in Table 9.

- A temporary LIN high-speed mode. After the SBC configuration with bits HSMODE = 01 the LIN high speed mode is enabled until next BAT power-on event.
- A permanent LIN high-speed mode. With bits HSMODE = 10 the LIN transmitter will always transmit in LIN high-speed mode.

In the LIN high-speed mode, the curve shaping of the LIN output signal is disabled, i.e., the LIN output driver switches fast on and off to support higher baud rates than 20 kBd. The actual maximum baud rate depends on the LIN bus load: Total LIN pull-up resistance and total LIN capacitance.

6.9 Local wake-up inputs

The TJA1128 provides 1 or 2 local wake-up pins (WAKE1 and WAKE2). The edge sensitivity (falling, rising or both) of the wake-up pins can be configured independently via the LC1WKE and LC2WKE bits in the Wake register. See Table 7. These bits can also be used to disable wake-up via the wake-up pins. When wake-up is enabled, a valid wake-up event on either of these pins will be detected in RESET, STANDBY, PORT, GOTOSLP and SLEEP modes.

WAKE1 and WAKE2 can be used in two sampling modes: Continuous or cyclic. With cyclic sampling the wake pins are synchronized with the HVMPO output. Further details about the cyclic sampled wake-up detection option can be found in section Section 6.10.2 "Bias control output for cyclic wake-up". In Figure 13, a typical circuit for cyclic sampling with WAKE1 and WAKE2 is shown.

6.10 High-voltage multipurpose output

The high-voltage multipurpose output (HVMPO) pin is a battery-robust, active-LOW, open-drain output. It can be configured via the HVMPO register for multi purposes. See Table 11.

6.10.1 GPI controlled output

The HVMPO can be controlled via GPI by setting the HVMPO operation mode to MPOMOD = 001. The GPI input has an internal pull-up and with bit MPOINV = 0 the GPI

is an active-LOW input, i.e., if GPI is LOW then HVMPO is driving actively LOW. The HVMPO level is inverted if MPOINV = 1.

6.10.2 Bias control output for cyclic wake-up

The HVMPO can be configured as bias control output for cyclic wake-up sampling. The cyclic sampling is enabled by setting the HVMPO operation mode in the HVMPO register to MPOMOD = 010. Figure 13 shows a typical application circuit with the HVMPO for the cyclic sampling bias control.

Two cyclic wake nominal period times $t_{per(cyclicwk)}$ are supported. It can be selected via the WKBPER bit in the HVMPO register.

The cyclic wake nominal setting time $t_{set(cyclicwk)}$ is available in two configurations. The setting time can be selected via the WKBSET bit in the HVMPO register. The cyclic bias timing is illustrated in Figure 10.

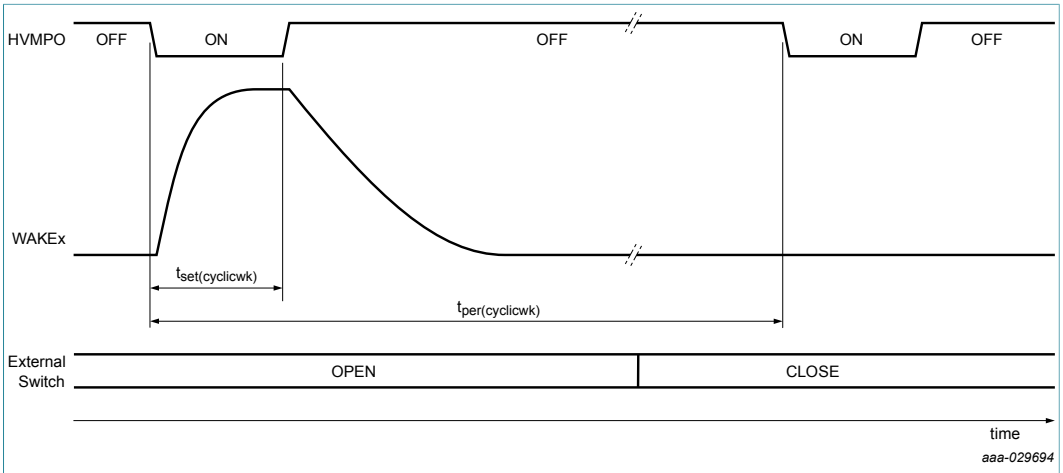


Figure 10. Cyclic bias timing with HVMPO

6.10.3 LIMP home output

This HVMPO function is used to enable so-called *limp home* hardware in the event of a serious ECU failure. Detectable failure conditions are VCC undervoltage and LOW-level on RSTN input while system controller is in the STANDBY, PORT, GOTOSLP or NORMAL mode and watchdog failure and SBC overtemperature.

After limp home event detection, the internal limp home flag is set. If the limp-home flag is set, HVMPO is held LOW while the TJA1128 is in RESET, STANDBY, PORT, GOTOSLP, SLEEP, OVERLOAD or NORMAL mode. The internal limp home flag can be read and cleared in PORT mode. See Section 6.2.3 "PORT mode". In OFF mode, the flag is also cleared.

The LIMP home output function of the HVMPO can be configured by setting the HVMPO operation mode to MPOMOD = 011.

6.10.4 State controlled output

As state controlled output the HVMPO drives active LOW as a function of the current TJA1128 mode. Four state controlled output functions are available. It can be configured with HVMPO operation modes MPOMOD = 1xx in the HVMPO register.

6.11 Test mode

The TJA1128 has a factory test mode. This test mode is not for customer use.

To avoid entering this test mode it should be prevented to apply more than 13 pulses on pin TXD within the time window of 25 ms after BAT power-on detection, while pin RSTN is LOW.

7 Limiting values

Table 16. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_X	voltage on pins BAT, HVMPO	—	–0.3	+43	V
	voltage on pins WAKE1, WAKE2	—	–18	+43	V
	voltage on pin LIN	with respect to GND and BAT	–43	+43	V
	voltage on pin VCC	—	–0.3	+6	V
	Voltage on logic pins TXD, RXD, RSTN, EN, STBN, WWD, GPI	—	–0.3	V_{VCC}+0.3	V
I_{HVMPO}	input current on pin HVMPO	—	—	20	mA
V_{trt}	transient voltage on pin BAT	with inverse-polarity protection diode and 22 µF capacitor to ground	–150	+100	V
	transient voltage on WAKE1, WAKE2	with 2.2 kΩ series resistor	–150	+100	V
	transient voltage on LIN	coupling via 1 nF capacitor	–150	+100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 [1]	—	—	—
		on pin BAT with capacitor	–6	+6	kV
		on pins WAKE1, WAKE2 with 47 pF capacitor and 2.2 kΩ series resistor	–6	+6	kV
		on pin LIN	–8	+8	kV
		Human Body Model [2]	—	—	—
		on pins BAT, WAKE1, WAKE2, HVMPO	–4	+4	kV
		on pin LIN	–8	+8	kV
		on any other pin	–2	+2	kV
		Charge Device Model [3]	—	—	—
		on any pin	–500	+500	V
T_{vj}	virtual junction temperature	—	–40	+150	°C
		when programming the MTPNVM	0	+85	°C
T_{stg}	storage temperature	—	–55	+150	°C

[1] Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor.
[2] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor. According AEC-Q100-002 Rev-D.
[3] According to AEC-Q100-011 Rev-C1. The classification level is C4B.

8 Thermal characteristics

Table 17. Thermal characteristics

Symbol	Parameter	Condition	Typ	Unit
$R_{th(vj-a)}$	Thermal resistance from virtual junction to ambient	Dual-layer board [1]	76	K/W
		Four-layer board [1]	40	K/W
$R_{th(vj-c)}$	Thermal resistance from virtual junction to case		5	K/W

[1] According to JEDEC JESD51-2, JESD51-3 and JESD51-5 at natural convection on 1s board with thermal via array under the exposed pad connected to the second copper layer.

9 Static characteristics

Table 18. Static characteristics

V_{BAT} = 3.0 V to 28 V; T_{vj} = –40 °C to +150 °C; $R_{L(LIN-BAT)}$ = 500 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V and T_{vj} = 25 °C; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin BAT						
I_{BAT}	battery supply current	SLEEP mode; BUSWKE = 0; V_{BAT} = 5 V to 14 V; $V_{LIN} = V_{WAKE1} = V_{WAKE2} = V_{BAT}$; $V_{TXD} = V_{WWD} = V_{GPI} = V_{EN} = V_{STBN}$ = 0 V; I_{VCC} = 0 µA; T_{vj} = –40 °C to +50 °C	—	14	22	µA
		STANDBY mode; BUSWKE = 0; WDMOD = 0h; V_{BAT} = 10.8 V to 14 V; $V_{LIN} = V_{WAKE1} = V_{WAKE2} = V_{BAT}$; $V_{TXD} = V_{WWD} = V_{GPI} = V_{VCC}$; $V_{EN} = V_{STBN}$ = 0 V; I_{VCC} = 0 µA; T_{vj} = –40 °C to +50 °C	—	22	32	µA
		additional current with LIN wake detection enabled; BUSWKE = 1; V_{BAT} = 5 V to 14 V; $V_{LIN} = V_{BAT}$; T_{vj} = –40 °C to +50 °C [2]	—	—	2	µA
		additional current with active watchdog; V_{BAT} = 5 V to 14 V; T_{vj} = –40 °C to +50 °C [2]	—	—	2	µA
		additional current with WAKE1 input pulled down; V_{BAT} = 5 V to 14 V; V_{WAKE1} = 0 V; T_{vj} = –40 °C to +50 °C [2]	—	—	2	µA
		additional current with WAKE2 input pulled down; V_{BAT} = 5 V to 14 V; V_{WAKE2} = 0 V; T_{vj} = –40 °C to +50 °C [2]	—	—	2	µA
		NORMAL mode; bus recessive; V_{BAT} = 10.8 V to 28 V; $V_{LIN} = V_{WAKE1} = V_{WAKE2} = V_{BAT}$; $V_{TXD} = V_{WWD} = V_{GPI} = V_{EN} = V_{VCC}$; V_{STBN} = 0 V; I_{VCC} = 0 µA; T_{vj} = –40 °C to +150 °C [2]	—	1.2	1.7	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		NORMAL mode; bus dominant; [2] V_{BAT} = 14 V; V_{WAKE1} = V_{WAKE2} = V_{BAT}; V_{WWD} = V_{GPI} = V_{EN} = V_{VCC}; V_{TXD} = V_{STBN} = 0 V; I_{VCC} = 0 µA; T_{vj} = –40 °C to +150 °C	—	3.5	4.2	mA
		additional current at low battery; [2] V_{BAT} = 3.8 V to 10.8 V; T_{vj} = –40 °C to +150 °C	—	170	369	µA
$V_{th(det)pon}$	power-on detection threshold	V_{BAT} rising	4.0	—	4.8	V
$V_{th(det)poff}$	power-off detection threshold	V_{BAT} falling	3.0	—	3.3	V
$V_{uvd(LIN)(WAKE)}$	LIN and WAKE undervoltage detection voltage	on pin BAT with V_{BAT} falling	4.0	—	4.5	V
$V_{uvr(LIN)(WAKE)}$	LIN and WAKE undervoltage recovery voltage	on pin BAT with V_{BAT} rising	4.5	—	5.0	V
$V_{th(config)min}$	minimum configuration threshold	on pin BAT	10.8	—	—	V
Voltage regulator; pin VCC						
V_O	output voltage	$V_{O(VCC)nom}$ = 3.3 V; V_{BAT} = 3.8 V to 28 V; I_{VCC} = –70 mA to 0.25 mA	3.234	3.3	3.366	V
		$V_{O(VCC)nom}$ = 3.3 V; V_{BAT} = 4.5 V to 28 V; I_{VCC} = –85 mA to 0.25 mA	3.234	3.3	3.366	V
		$V_{O(VCC)nom}$ = 3.3 V; V_{BAT} = 3.8 V to 28 V; I_{VCC} < 0.25 mA	3.201	3.3	3.399	V
		$V_{O(VCC)nom}$ = 5.0 V; V_{BAT} = 5.5 V to 28 V; I_{VCC} = –70 mA to 0.25 mA	4.9	5.0	5.1	V
		$V_{O(VCC)nom}$ = 5.0 V; V_{BAT} = 6.0 V to 28 V; I_{VCC} = –85 mA to 0.25 mA	4.9	5.0	5.1	V
		$V_{O(VCC)nom}$ = 5.0 V; V_{BAT} = 5.5 V to 28 V; I_{VCC} < 0.25 mA	4.85	5.0	5.15	V
$R_{ON(BAT–VCC)}$	ON resistance between pin BAT and pin VCC	$V_{O(VCC)nom}$ = 3.3 V; V_{BAT} = 3.0 V to 3.8 V	—	—	9	Ω
		$V_{O(VCC)nom}$ = 5.0 V; V_{BAT} = 3.0 V to 5.5 V	—	—	9	Ω
$V_{uvd(VCC)}$	VCC undervoltage detection voltage	$V_{O(VCC)nom}$ = 3.3 V	2.75	—	3.00	V
		$V_{O(VCC)nom}$ = 5.0 V	4.2	—	4.6	V
$V_{uvr(VCC)}$	VCC undervoltage recovery voltage	$V_{O(VCC)nom}$ = 3.3 V	2.875	—	3.135	V
		$V_{O(VCC)nom}$ = 5.0 V	4.35	—	4.75	V
$I_{O(sc)}$	short-circuit output current	— [2]	–200	—	–85	mA
$C_{O(VCC)}$	VCC output capacitance	MLC capacitor	375	1000	—	nF
LIN bus line; pin LIN						
I_{BUS_LIM}	current limitation for driver dominant state	NORMAL mode; LIN = 00h; V_{BAT} = V_{LIN} = 18 V; V_{TXD} = 0 V	40	—	200	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{BUS\_PAS\_dom}$	Receiver dominant input leakage current including LIN slave pull-up resistor	V_{BAT} = 12 V; V_{LIN} = 0 V; LIN driver off	–1	—	—	mA
		V_{BAT} = 28 V; V_{LIN} = 0 V; LIN driver off	–1.5	—	—	mA
$I_{BUS\_PAS\_rec}$	Receiver recessive input leakage current	5 V < V_{BAT} < 18 V; 5 V < V_{LIN} < 18 V; $V_{LIN} \geq V_{BAT}$; LIN driver off	—	—	20	µA
		18 V < V_{BAT} < 28 V; 18 V < V_{LIN} < 28 V; $V_{LIN} \geq V_{BAT}$; LIN driver off	—	—	30	µA
$I_{BUS\_NO\_GND}$	loss-of-ground current	V_{BAT} = 12 V; V_{LIN} = 0 V to 18 V; $V_{GND} = V_{BAT}$ [2]	–1000	—	+10	µA
$I_{BUS\_NO\_BAT}$	loss-of-battery current	V_{BAT} = 0 V; V_{LIN} = 0 V to 18 V	—	—	30	µA
V_{BUSdom}	receiver dominant state	V_{BAT} = 5 V to 28 V	—	—	0.4 × V_{BAT}	V
V_{BUSrec}	receiver recessive state	V_{BAT} = 5 V to 28 V	0.6 × V_{BAT}	—	—	V
V_{BUS_CNT}	receiver center voltage	V_{BAT} = 5 V to 28 V; $V_{BUS\_CNT} = (V_{th\_rec} + V_{th\_dom}) / 2$ [3]	0.475 × V_{BAT}	0.5 × V_{BAT}	0.525 × V_{BAT}	V
V_{HYS}	receiver hysteresis voltage	V_{BAT} = 5 V to 28 V; $V_{HYS} = (V_{th\_rec} - V_{th\_dom})$ [3]	—	—	0.175 × V_{BAT}	V
$V_{SerDiode}$	voltage drop at the serial diode	internal pull-up path with R_{SLAVE}; $I_{SerDiode}$ = 0.9 mA	0.4	0.7	1.0	V
$V_{O(dom)}$	dominant output voltage	NORMAL mode; LIN = 00h; V_{BAT} = 7.0 V; V_{TXD} = 0 V	—	—	1.4	V
		NORMAL mode; LIN = 00h; V_{BAT} = 18.0 V; V_{TXD} = 0 V	—	—	3.6	V
R_{SLAVE}	slave resistance	—	20	30	60	kΩ
C_{LIN}	capacitance on pin LIN	with respect to ground [2]	—	—	20	pF
Digital input; pins EN (SCK), GPI, STBN (SCSN), TXD (SDI), WWD						
$V_{th(sw)}$	switching threshold voltage	—	0.25 × V_{VCC}	—	0.75 × V_{VCC}	V
R_{pu}	pull-up resistance on pin GPI, TXD, WWD	—	15	—	50	kΩ
R_{pd}	pull-down resistance on pin EN, STBN	—	15	—	50	kΩ
Digital output; pin RXD (SDO)						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	—	—	0.4	V
R_{pu}	pull-up resistance	—	8	10	12	kΩ
Reset input/output; pin RSTN						
$Vt_{h(sw)}$	switching threshold voltage	—	0.25 × V_{VCC}	—	0.75 × V_{VCC}	V
V_{OL}	LOW-level output voltage	V_{VCC} = 1.0 V to 5.5 V; external pull-up resistor with ≥ 3 kΩ to V_{CC}	—	—	0.2 × V_{VCC}	V
R_{pu}	pull-up resistance	—	15	—	50	kΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Local wake input; pins WAKE1, WAKE2						
$V_{th(sw)}$	switching threshold voltage	—	0.25 × V_{BAT}	0.5 × V_{BAT}	0.75 × V_{BAT}	V
$V_{hys(i)}$	input hysteresis voltage	—	0.1 × V_{BAT}	—	—	V
I_i	Input current	LCxWKE > 0h; V_{BAT} = 12 V; V_{WAKE} = 0 V to V_{BAT}	–1	—	+1	µA
High-voltage multipurpose output; pin HVMPO						
V_{OL}	LOW-level output voltage	HVMPO on; I_{HVMPO} = 0.8 mA	—	—	0.4	V
I_{LO}	output leakage current	HVMPO off; V_{BAT} = 12 V; V_{HVMPO} = 0 V to 28 V	—	—	1	µA
Temperature protection						
$T_{th(act)otp}$	overtemperature protection activation threshold temperature	— [2]	155	165	175	°C
$T_{th(rel)otp}$	overtemperature protection release threshold temperature	— [2]	130	140	150	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.
[2] Not tested in production; guaranteed by design.
[3] V_{th_dom}: receiver threshold of the recessive to dominant LIN bus edge. V_{th_rec}: receiver threshold of the dominant to recessive LIN bus edge.

10 Dynamic characteristics

Table 19. Dynamic characteristics

V_{BAT} = 3.0 V to 28 V; T_{vj} = –40 °C to +150 °C; $R_{L(LIN-BAT)}$ = 500 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V and T_{vj} = 25 °C; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin BAT						
$t_{startup}$	start-up time	from OFF mode until CONFIG and STANDBY mode; RSTTIM = 0 ; C_{VCC} = 1 µF	—		5.7	ms
		from OFF mode until STANDBY mode; RSTTIM = 1 ; C_{VCC} = 1 µF	—	—	2.1	ms
Voltage regulator; pin VCC						
$t_{d(uvd)}$	undervoltage detection delay time	NORMAL mode ; V_{VCC} falling	15	—	30	µs
		STANDBY mode ; V_{VCC} falling	15	—	55	µs
LIN transmitter; pins LIN, TXD						
d1	duty cycle 1	$V_{th(rec)(max)}$ = 0.744 x V_{BAT}; $V_{th(dom)(max)}$ = 0.581 x V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 7 V to 28 V [2] [3] [4]	0.396	—	—	—
		$V_{th(rec)(max)}$ = 0.665 x V_{BAT}; $V_{th(dom)(max)}$ = 0.499 x V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 5 V to 7 V [2] [3] [4]	0.396	—	—	—
d2	duty cycle 2	$V_{th(rec)(min)}$ = 0.442 x V_{BAT}; $V_{th(dom)(min)}$ = 0.284 x V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 7.6 V to 28 V [2] [3] [5]	—	—	0.581	—
		$V_{th(rec)(min)}$ = 0.496 x V_{BAT}; $V_{th(dom)(min)}$ = 0.361 x V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 5.6 V to 7.6 V [2] [3] [5]	—	—	0.581	—
d3	duty cycle 3	$V_{th(rec)(max)}$ = 0.778 x V_{BAT}; $V_{th(dom)(max)}$ = 0.616 x V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 7 V to 28 V [2] [3] [4]	0.417	—	—	—
		$V_{th(rec)(max)}$ = 0.665 x V_{BAT}; $V_{th(dom)(max)}$ = 0.499 x V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 5 V to 7 V [2] [3] [4]	0.417	—	—	—
d4	duty cycle 4	$V_{th(rec)(min)}$ = 0.389 x V_{BAT}; $V_{th(dom)(min)}$ = 0.251 x V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 7.6 V to 28 V [2] [3] [5]	—	—	0.590	—
		$V_{th(rec)(min)}$ = 0.496 x V_{BAT}; $V_{th(dom)(min)}$ = 0.361 x V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 5.6 V to 7.6 V [2] [3] [5]	—	—	0.590	—
$t_{to(dom)TXD}$	TXD dominant time-out	timer started at falling edge on TXDx	6	—	8	ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN receiver; pins LIN, RXD						
t_{rx_pd}	receiver propagation delay	rising and falling edge	—	—	6	µs
t_{rx_sym}	receiver propagation delay symmetry	rising edge with respect to falling edge	–2	—	+2	µs
$t_{wake(dom)LIN}$	LIN dominant wake-up time		30	80	150	µs
$t_{d(RXD)}$	RXD delay time	STANDBY mode or GOTOSLP mode	—	—	10	µs
Mode transition; pins STBN, EN						
$t_{deglitch}$	deglitch time		3.6	—	10	µs
t_{su}	set-up time	NORMAL mode and PORT mode	30	—	—	µs
		STANDBY mode	50	—	—	µs
t_h	hold time	NORMAL mode and PORT mode	30	—	—	µs
		STANDBY mode	50	—	—	µs
$t_{d(stb)}$	standby mode delay time		—	—	25	µs
$t_{d(port)}$	port mode delay time		—	—	50	µs
$t_{d(norm)}$	normal mode delay time		—	—	50	µs
$t_{init(norm)}$	LIN initialization time		—	—	50	µs
$t_{to(gotoslp)}$	gotoslp mode time-out		0.9	—	1.1	ms
$t_{d(conf)}$	config mode delay time		—	—	25	µs
Local wake input; pins WAKE1, WAKE2						
t_{wake}	wake-up time		45	—	95	µs
$t_{init(wake)}$	wake initialization time	after rising $V_{BAT} > V_{uvr(LIN)(WAKE)}$	—	—	80	µs
$t_{d(WAKE-RXDL)}$	WAKE to RXD LOW delay time	STANDBY mode or GOTOSLP mode; after wake-up event detection	—	—	110	µs
High-voltage multipurpose output; pin HVMPO						
$t_{per(cyclicwk)}$	cyclic wake period time	WKBPER = 0	14.4	16	17.6	ms
		WKBPER = 1	57.6	64	70.4	ms
$t_{set(cyclicwk)}$	cyclic wake settle time	WKBSET = 0	62	70	78	µs
		WKBSET = 1	120	134	149	µs
$t_{d(GPI-HVMPO)}$	GPI to HVMPO delay time	MPOMOD = 1h	—	—	4	µs
$t_{d(limp-HVMPO)}$	limp to HVMPO delay time	MPOMOD = 3h	—	—	60	µs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PORT mode; pins TXD, RXD						
$t_{init(TXD)H}$	HIGH-level TXD initialization time	PORT mode	30	—	—	µs
$t_{bit(TXD)}$	TXD bit time	PORT mode	30	—	—	µs
$t_{pd(TXD-RXD)}$	TXD to RXD propagation delay time	PORT mode	—	—	16	µs
$t_{sym(TXD-RXD)}$	TXD to RXD propagation delay symmetry time	PORT mode	–2	—	+2	µs
Serial peripheral interface timing; pins EN (SCK), STBN (SCSN), TXD (SDI), RXD (SDO)						
$t_{cy(clk)}$	clock cycle time		10	—	—	µs
$t_{SPILEAD}$	SPI enable lead time		500	—	—	ns
t_{SPILAG}	SPI enable lag time		500	—	—	ns
$t_{clk(H)}$	clock HIGH time		5	—	—	µs
$t_{clk(L)}$	clock LOW time		5	—	—	µs
$t_{su(D)}$	data input set-up time		500	—	—	ns
$t_{h(D)}$	data input hold time		500	—	—	ns
$t_{v(Q)}$	data output valid time		—	—	1	µs
$t_{WH(S)}$	chip select pulse width HIGH		20		—	µs
$t_{d(SCKL-SCSNL)}$	delay time from SCK LOW to SCSN LOW		500	—	—	ns
Watchdog; pin WWD						
$t_{deglitch}$	deglitch time		3.6	—	10	µs
$t_{trig(wd)low}$	watchdog trigger low time		60	—	—	µs
$t_{trig(wd)1}$	watchdog trigger time 1		0.45× WDPER	—	0.55× WDPER	ms
$t_{trig(wd)2}$	watchdog trigger time 2		0.9× WDPER	—	1.1× WDPER	ms
Reset; pin RSTN						
$t_{w(rst)}$	reset pulse width time	RSTTIM = 0	3.6	4	4.4	ms
		RSTTIM = 1	600	700	800	µs
$t_{d(MTPNV)rst}$	reset MTPNVM restore delay time	RESET mode	0.9	1	1.1	s

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
MTP nonvolatile memory						
$t_{prog(MTPNV)}$	MTPNVM programming time	propagation delay from CONFIG mode to RESET mode	—	—	80	ms

[1] Parameters not tested in production; guaranteed by design.
[2] Bus load conditions: C_{LIN} = 1 nF and R_{LIN} = 1 kΩ; C_{LIN} = 6.8 nF and R_{LIN} = 660 Ω; C_{LIN} = 10 nF and R_{LIN} = 500 Ω
[3] See timing diagram in Figure 11
[4] Equation 1

$$\delta 1, \delta 3 = \frac{t_{bus(rec)(\min)}}{2 \times t_{bit}}$$

[5] Equation 2

$$\delta 2, \delta 4 = \frac{t_{bus(rec)(\max)}}{2 \times t_{bit}}$$

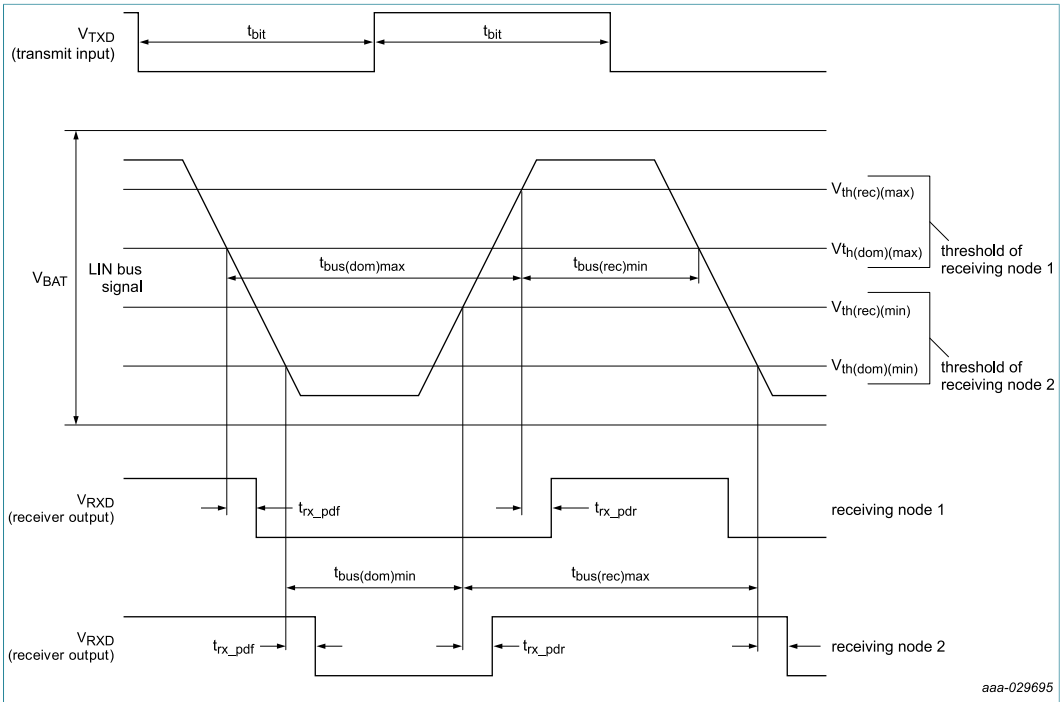


Figure 11. Timing diagram of LIN duty cycle

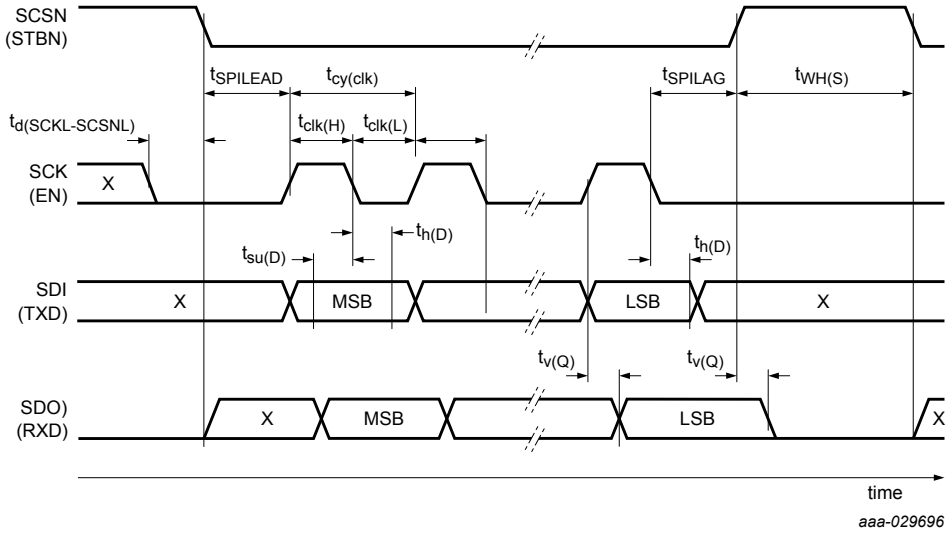


Figure 12. SPI timing diagram

11 Application information

11.1 Typical application diagram

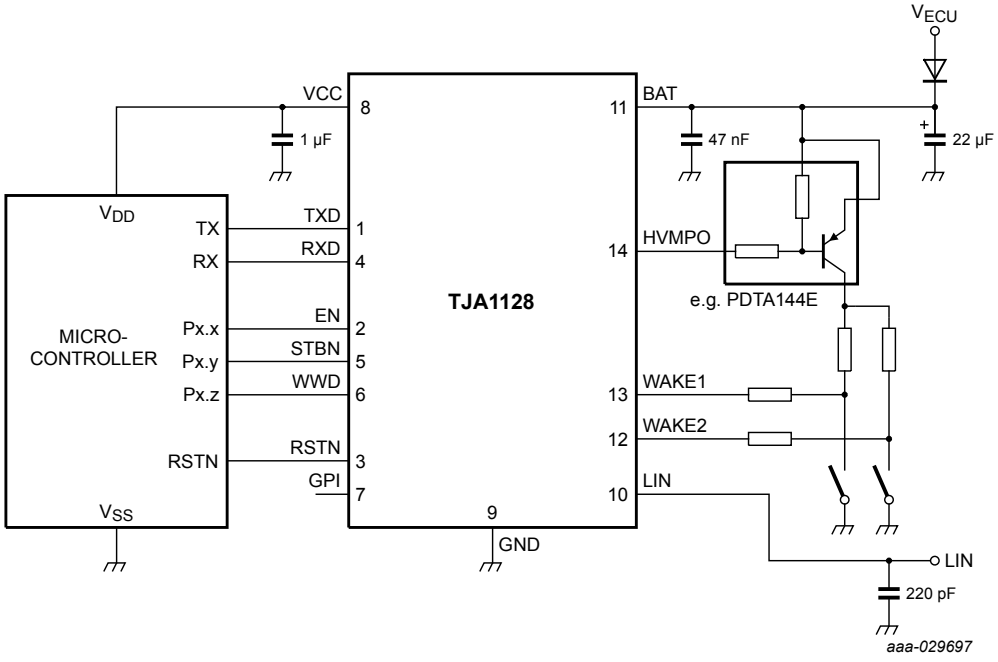


Figure 13. Typical application diagram

11.2 ESD robustness according to LIN EMC test specification

ESD robustness (IEC 61000-4-2) has been tested by an external test house according to the LIN EMC test specification (part of Conformance Test Specification Package for LIN 2.1, October 10th, 2008). The test report is available on request.

Table 20. ESD robustness (IEC 61000-4-2) according to LIN EMC test specification

Pin	Test configuration	Value	Unit
LIN	No capacitor connected to LIN pin	±10	kV
	220 pF capacitor connected to LIN pin	±11	kV
BAT	series diode and 47 nF and 22 µF capacitors connected to pin BAT	>|15|	kV

12 Packaging

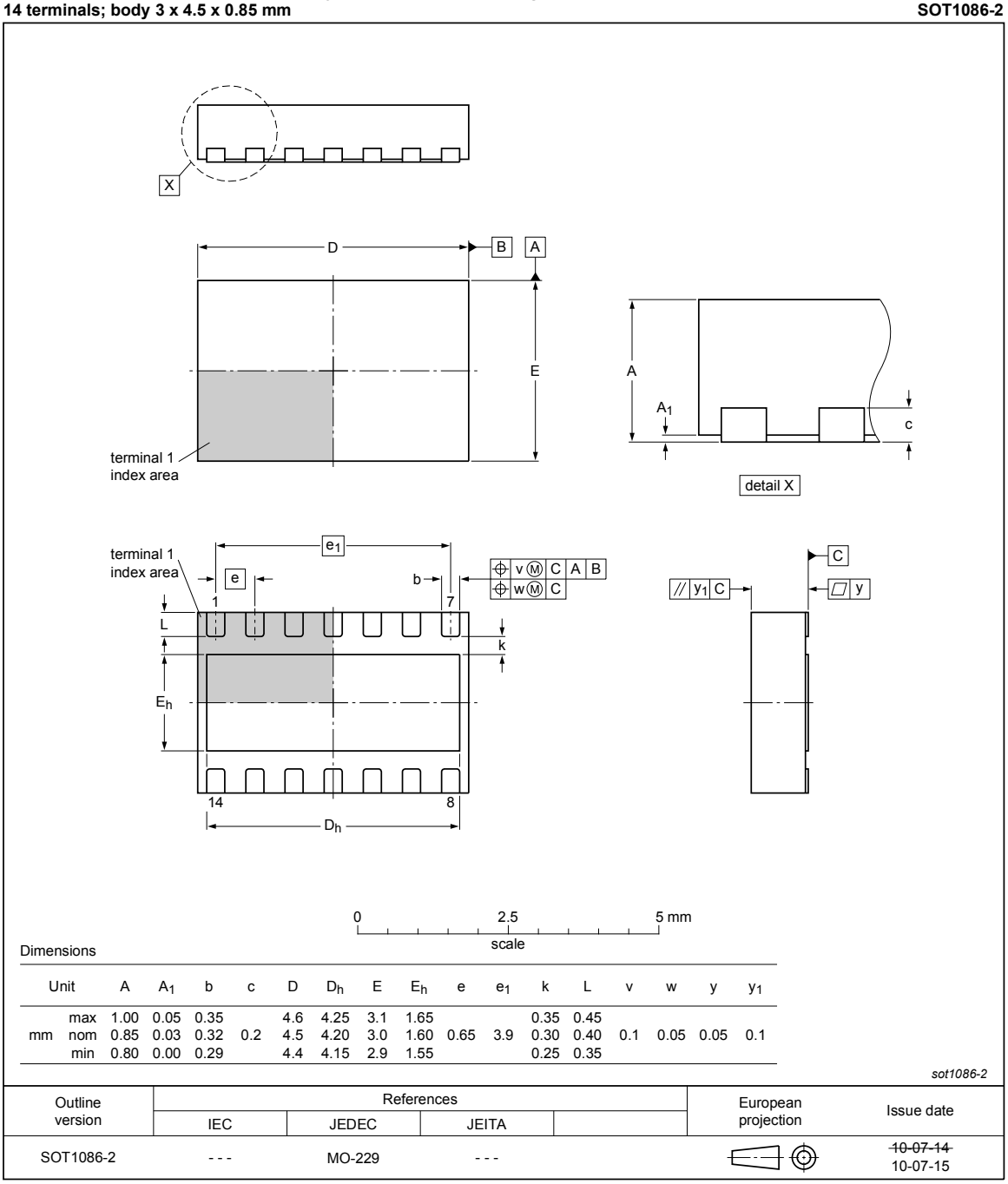
12.1 Package outline

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 21. Package outline

Package	Package outline drawing number
14 pin HVSON	SOT1086-2

HVSON14: plastic, thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 x 4.5 x 0.85 mm **SOT1086-2**



Dimensions

Unit		A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
mm	max	1.00	0.05	0.35		4.6	4.25	3.1	1.65			0.35	0.45				
	nom	0.85	0.03	0.32	0.2	4.5	4.20	3.0	1.60	0.65	3.9	0.30	0.40	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.29		4.4	4.15	2.9	1.55			0.25	0.35				

sot1086-2

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1086-2	- - -	MO-229	- - -			~~10-07-14~~ 10-07-15

Figure 14. Package outline

13 Revision history

Table 22. Revision history

Document ID	Release date	Data sheet status	Change notice	Supercedes
TJA1128 v.1	20180329	Product data sheet	—	—

14 Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Tables

Figures