

TJA1462

CAN FD signal improvement transceiver with Standby mode

Rev. 2 — 15 October 2021

Product data sheet

1 General description

The TJA1462 is a member of the TJA146x family of transceivers that provide an interface between a Controller Area Network (CAN) or CAN FD (Flexible Data rate) protocol controller and the physical two-wire CAN bus. TJA146x transceivers implement the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5, and are fully interoperable with high-speed Classical CAN and CAN FD transceivers.

The TJA1462 includes CAN Signal Improvement Capability (SIC), as defined in CiA 601-4:2019. CAN signal improvement significantly reduces signal ringing in a network, allowing reliable CAN FD communication to function in larger topologies. In addition, the TJA1462 features a much tighter bit timing symmetry performance to enable CAN FD communication up to 8 Mbit/s.

The TJA1462 is intended as a simple replacement for high-speed Classical CAN and CAN FD transceivers, such as the TJA1042 or TJA1044GT from NXP. It offers pin compatibility and is designed to avoid changes to hardware and software design, allowing the TJA1462 to be easily retrofitted to existing applications.

An AEC-Q100 Grade 0 variant, the TJR1462, is available for high temperature applications, supporting operation at 150 °C ambient temperature.

1.1 TJA1462 variants

The TJA1462 comes in two variants, each available in an SO8 or HVSON8 package:

- The TJA1462A is a high-speed CAN transceiver with Normal and Standby modes and a VIO supply pin. The VIO pin allows for direct interfacing with 3.3 V- and 5 V-supplied microcontrollers.
- The TJA1462B is a high-speed CAN transceiver with Normal and Standby modes.

2 Features and benefits

2.1 General

- ISO 11898-2:2016, SAE J2284-1 to SAE J2284-5 and SAE J1939-14 compliant
- Implements CAN Signal Improvement Capability as defined in CiA 601-4:2019 to significantly reduce signal ringing effects in a network
- Much tighter bit timing symmetry performance allowing more time to reduce signal ringing
- Low Electromagnetic Emission (EME) and high Electromagnetic Immunity (EMI)
- Qualified according to AEC-Q100 Grade 1
- TJA1462A only: VIO input for interfacing with 3.3 V to 5 V microcontrollers
- All variants are available in SO8 and leadless HVSON8 (3.0 mm x 3.0 mm) packages; HVSON8 with improved Automated Optical Inspection (AOI) capability.



- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

2.2 Predictable and fail-safe behavior

- Undervoltage detection with defined handling on all supply pins
- Full functionality guaranteed from the undervoltage detection thresholds up to the maximum limiting voltage values
- Defined behavior below the undervoltage detection thresholds
- Transceiver disengages from the bus (high-ohmic) when the supply voltage drops below the Off mode threshold
- Internal biasing of TXD and mode selection input pins, to enable defined fail-safe behavior

2.3 Low-power management

- Very low-current Standby mode with host and bus wake-up capability
- TJA1462A only: CAN wake-up receiver powered by V_{IO} allowing V_{CC} to be shut down
- CAN wake-up pattern filter time of 0.5 μ s to 1.8 μ s, meeting Classical CAN and CAN FD requirements

2.4 Protection

- High ESD handling capability on the bus pins (6 kV IEC and 8 kV HBM)
- Bus pins protected against transients in automotive environments
- Transmit Data (TXD) dominant time-out function
- Thermally protected

3 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		4.5	-	5.5	V
I _{CC}	supply current	Normal mode, dominant	-	42	70	mA
		Normal mode, recessive	-	7	10	mA
		Standby mode; TJA1462A	-	-	2	μA
		Standby mode; TJA1462B	-	8	21	μA
V _{uvd(stb)(VCC)}	standby undervoltage detection voltage on pin VCC		4	-	4.5	V
V _{uvhys(stb)(VCC)}	standby undervoltage hysteresis voltage on pin VCC		50	-	-	mV
V _{uvd(swoff)(VCC)}	switch-off undervoltage detection voltage on pin VCC	TJA1462B	2.65	-	2.95	V
V _{IO}	supply voltage on pin VIO		2.95	-	5.5	V
I _{IO}	supply current on pin VIO	Normal mode, dominant; V _{TXD} = 0 V	-	250	760	μA
		Normal mode, recessive; V _{TXD} = V _{IO}	-	150	460	μA
		Standby mode	-	8	19	μA
V _{uvd(swoff)(VIO)}	switch-off undervoltage detection voltage on pin VIO		2.65	-	2.95	V
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2 on pins CANH and CANL	-6	-	+6	kV
V _{CANH}	voltage on pin CANH	limiting value according to IEC 60134	-36	-	+40	V
V _{CANL}	voltage on pin CANL	limiting value according to IEC 60134	-36	-	+40	V
T _{vj}	virtual junction temperature		-40	-	+150	°C

4 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJA1462AT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TJA1462BT			
TJA1462ATK	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm	SOT782-1
TJA1462BTK			

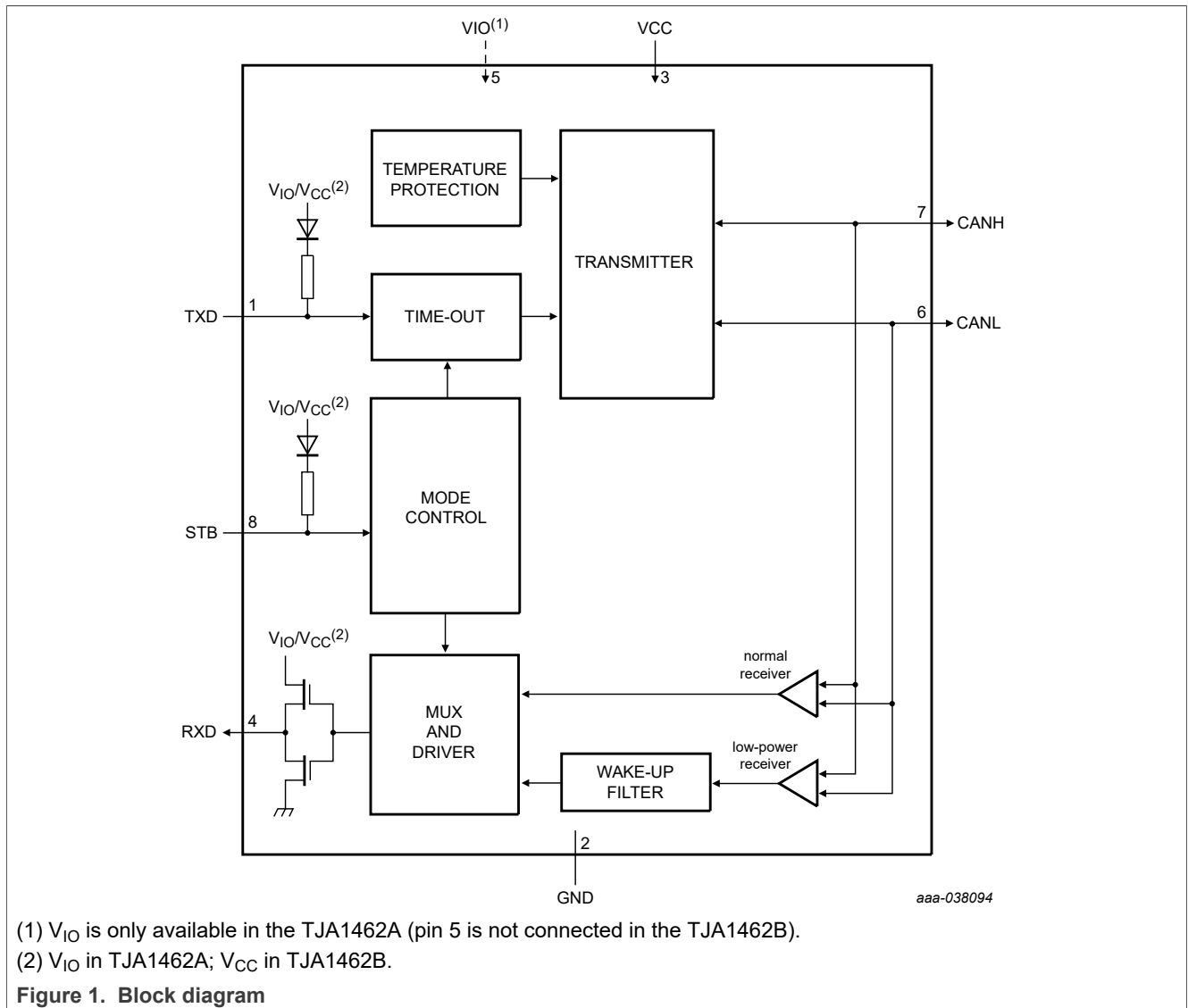
Table 3. TJA1462 feature overview

See [Section 19](#) for a feature overview of the complete TJx144x/TJx146x/TJF1441 family.

Device ^[1]	Modes					Supplies			Data rate		Additional features					
	Normal	Standby	Sleep	Silent/Listen-only	Selectable Off	VCC pin	VIO pin	VBAT pin	Up to 5 Mbit/s CAN FD	Up to 8 Mbit/s CAN FD	Signal improvement ^[2]	Wake-up source recognition ^[3]	Short WUP support [0.5 - 1.8 µs] ^[4]	Single supply pin wake-up ^[5]	TXD dominant timeout	Local diagnostics via ERR_N pin
TJA1462A	•	•				•	•		•	•	•		•	•	•	
TJx1462B	•	•				•			•	•	•		•		•	

[1] TJA1462 is AEC-Q100 Grade 1.
 [2] CAN FD Signal Improvement Capability (SIC) according to CiA 601-4:2019.
 [3] RXD is held LOW after wake-up request, enabling wake-up source recognition.
 [4] WUP = wake-up pattern according ISO11898-2:2016.
 [5] Only VIO supply needed for wake-up in TJA1462A.

5 Block diagram



6 Pinning information

6.1 Pinning

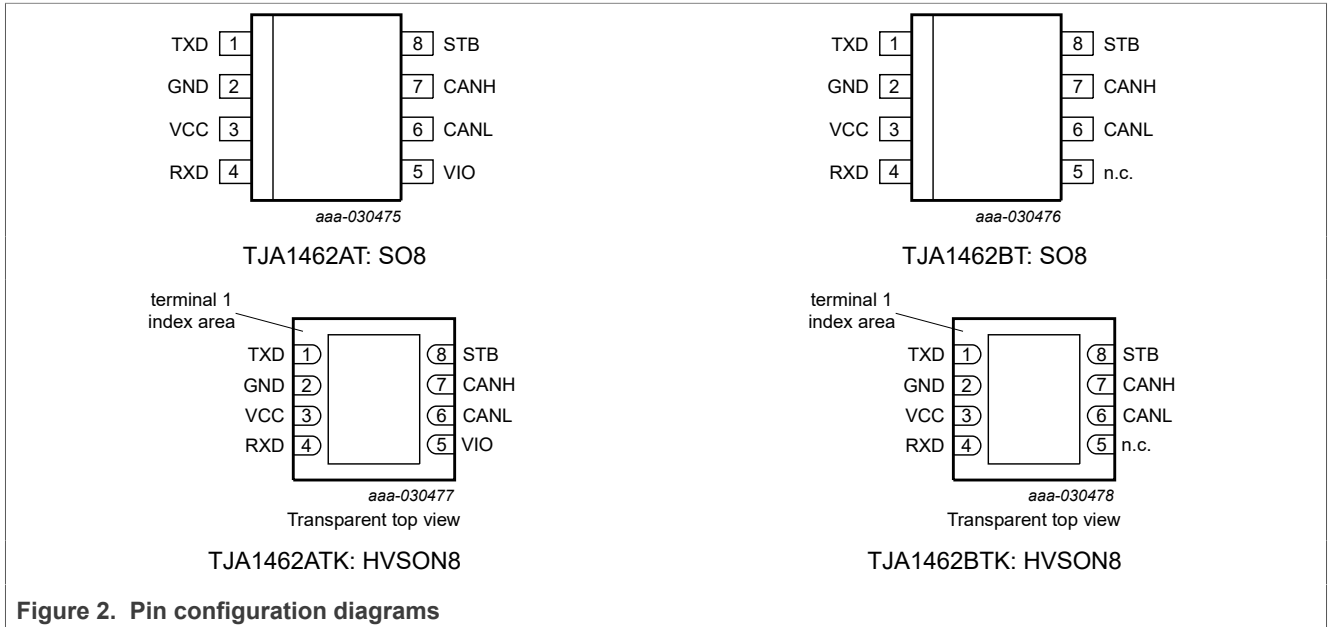


Figure 2. Pin configuration diagrams

6.2 Pin description

Table 4. Pin description

Symbol	Pin	Type ^[1]	Description
TXD	1	I	transmit data input; inputs data (from the CAN controller) to be written to the bus lines
GND ^[2]	2	G	ground
VCC	3	P	5 V supply voltage input
RXD	4	O	receive data output; outputs data read from the bus lines (to the CAN controller)
VIO	5	P	supply voltage input for I/O level adapter in TJA1462A
n.c.		-	not connected in TJA1462B
CANL	6	AIO	LOW-level CAN bus line
CANH	7	AIO	HIGH-level CAN bus line
STB	8	I	Standby mode control input; active-HIGH

[1] I: digital input; O: digital output; AIO: analog input/output; P: power supply; G: ground.

[2] HVSON package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is also recommended to solder the exposed center pad to board ground.

7 Functional description

7.1 Operating modes

The TJA1462 supports three operating modes, Normal, Standby and Off. The operating mode is selected via pin STB. See [Table 5](#) for a description of the operating modes under normal supply conditions. Mode changes are completed after transition time $t_{(moch)}$.

Table 5. Operating modes

Mode	Inputs		Outputs	
	Pin STB	Pin TXD	CAN driver	Pin RXD
Normal	LOW	LOW	dominant	LOW
		HIGH	recessive	LOW when bus dominant HIGH when bus recessive
Standby	HIGH	X	biased to ground	follows BUS when wake-up detected
				HIGH when no wake-up detected
Off ^[1]	X	X	high-ohmic state	high-ohmic state

[1] Off mode is entered when the voltage on pin VIO (TJA1462A) or pin VCC (TJA1462B) is below the switch-off undervoltage detection threshold.

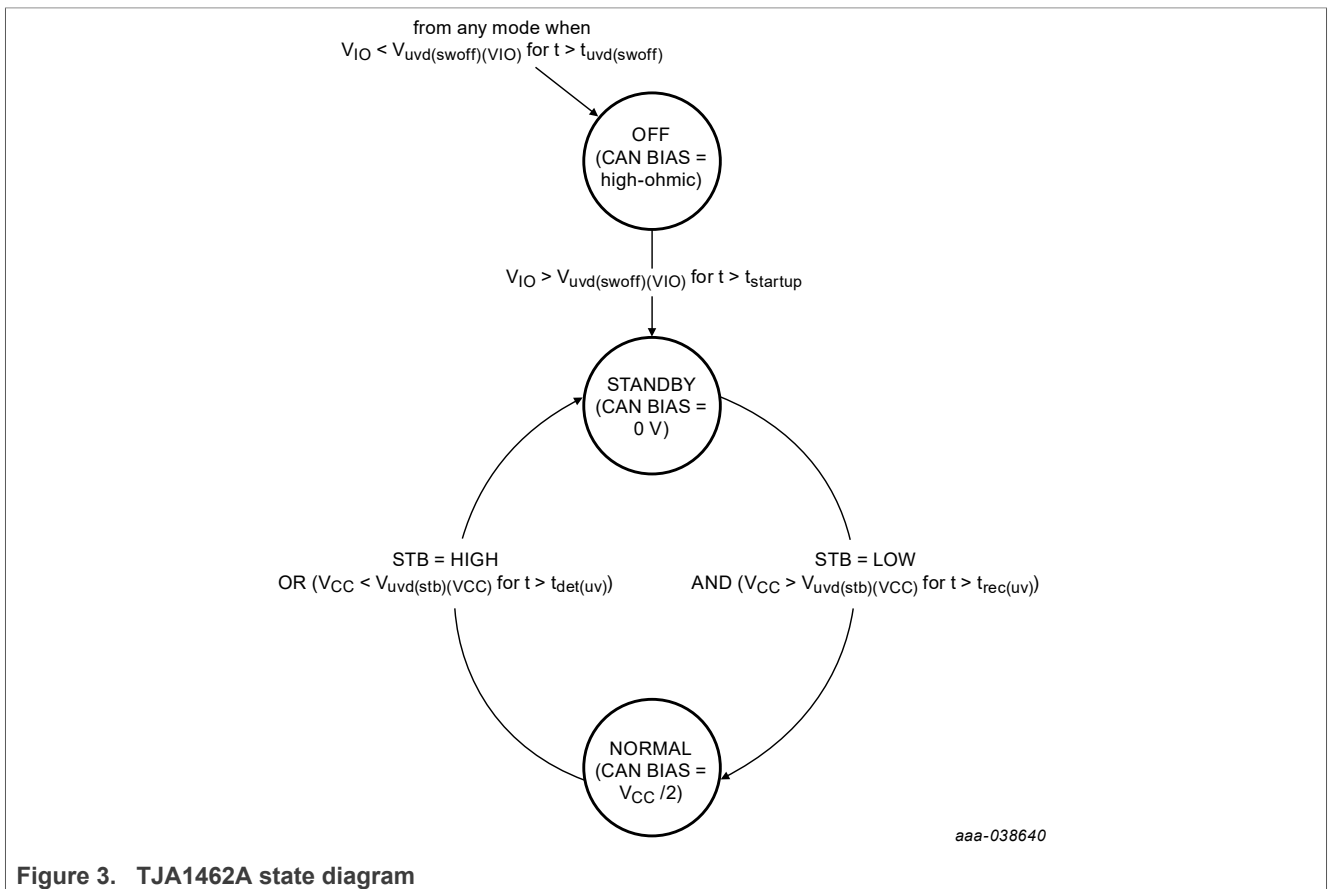


Figure 3. TJA1462A state diagram

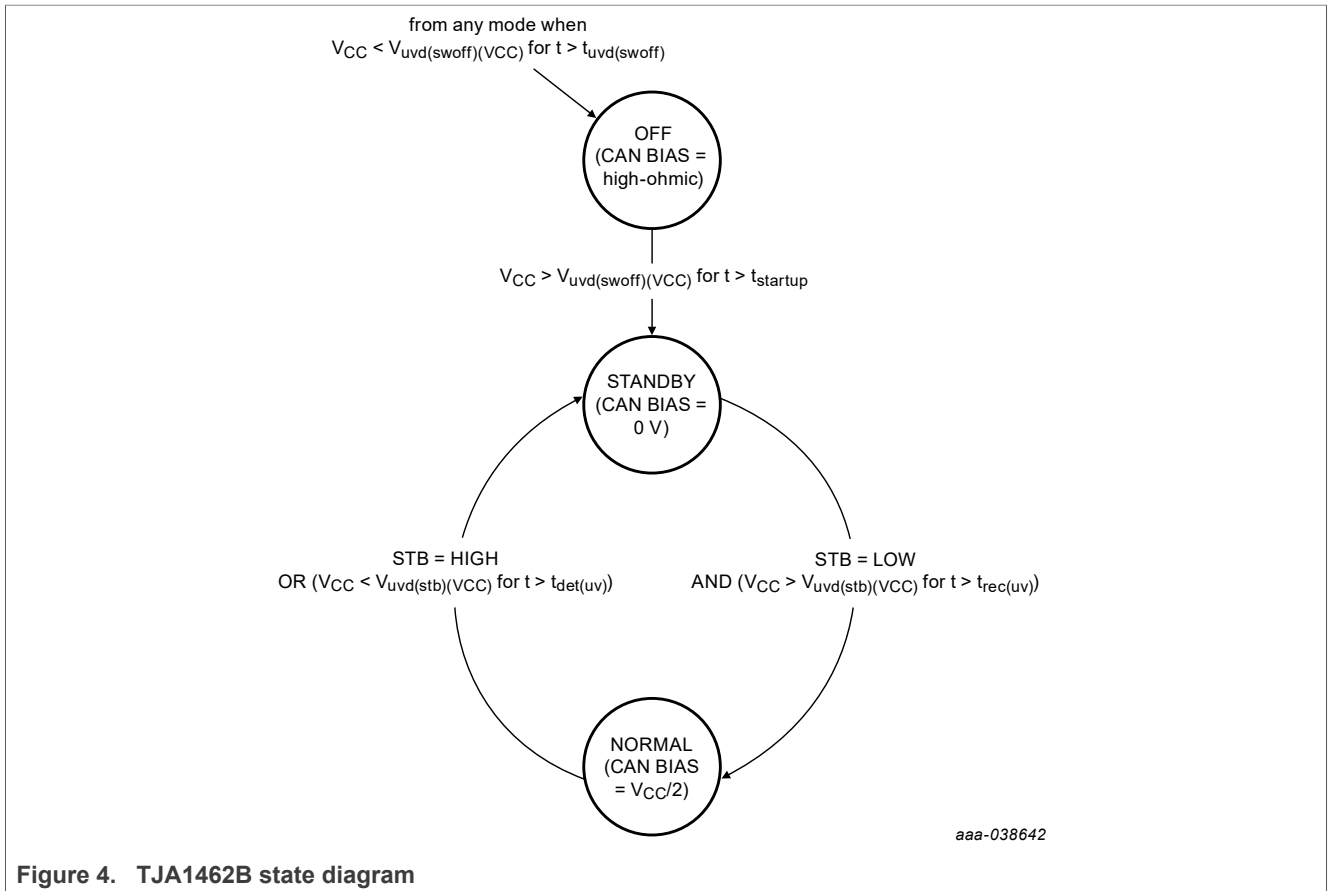


Figure 4. TJA1462B state diagram

7.1.1 Off mode

The TJA1462 switches to Off mode from any mode when the supply voltage (on pin V_{IO} in the TJA1462A and V_{CC} in the TJA1462B) falls below the switch-off undervoltage threshold ($V_{\text{uvd}(\text{swoff})}(V_{CC})$ or $V_{\text{uvd}(\text{swoff})}(V_{IO})$). This is the default mode when the supply is first connected.

In Off mode, the CAN pins and pin RXD are in a high-ohmic state.

7.1.2 Standby mode

When the supply voltage (V_{IO} for TJA1462A or V_{CC} for TJA1462B) rises above the switch-off undervoltage detection threshold, the TJA1462 starts to boot up, triggering an initialization procedure. The TJA1462 switches to the selected mode after t_{startup} .

Standby mode is selected when pin STB goes HIGH. In this mode, the transceiver is unable to transmit or receive data and a low-power receiver is activated to monitor the bus for a wake-up pattern. The transmitter and Normal-mode receiver blocks are switched off and the bus pins are biased to ground to minimize system supply current. Pin RXD follows the bus after a wake-up request has been detected.

A transition to Normal mode is triggered when STB is forced LOW (provided $V_{CC} > V_{\text{uvd}(\text{stb})}(V_{CC})$ and $V_{IO} > V_{\text{uvd}(\text{swoff})}(V_{IO})$ in the TJA1462A).

If V_{CC} is below $V_{\text{uvd}(\text{stb})}(V_{CC})$ when STB goes LOW (with $V_{IO} > V_{\text{uvd}(\text{swoff})}(V_{IO})$ in TJA1462A and $V_{CC} > V_{\text{uvd}(\text{swoff})}(V_{CC})$ in TJA1462B), the TJA1462 will remain in Standby mode.

Pending wake-up events will be cleared and differential data on the bus pins converted to digital data via the low-power receiver and output on pin RXD.

In the TJA1462A, the low-power receiver is supplied from V_{IO} and can detect CAN bus activity when V_{IO} is above $V_{\text{uvd}(\text{swoff})(V_{IO})}$ (even if V_{IO} is the only available supply voltage).

7.1.3 Normal mode

A LOW level on pin STB selects Normal mode, provided the supply voltage on pin VCC is above the standby undervoltage detection threshold, $V_{\text{uvd}(\text{stb})(VCC)}$.

In this mode, the transceiver can transmit and receive data via bus lines CANH and CANL. Pin TXD must be HIGH at least once in Normal Mode before transmission can begin. The differential receiver converts the analog data on the bus lines into digital data on pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME. In order to support high bit rates, especially in CAN FD systems, the Signal Improvement function largely eliminates topology-related reflections and impedance mismatches. In recessive state, the output voltage on the bus pins is $V_{CC}/2$.

7.1.4 Operating modes and gap-free operation

Gap-free operation guarantees defined behavior at all voltage levels. Supply voltage-to-operating mode mapping is detailed in [Figure 5](#) and in the state diagrams ([Figure 3](#) and [Figure 4](#)).

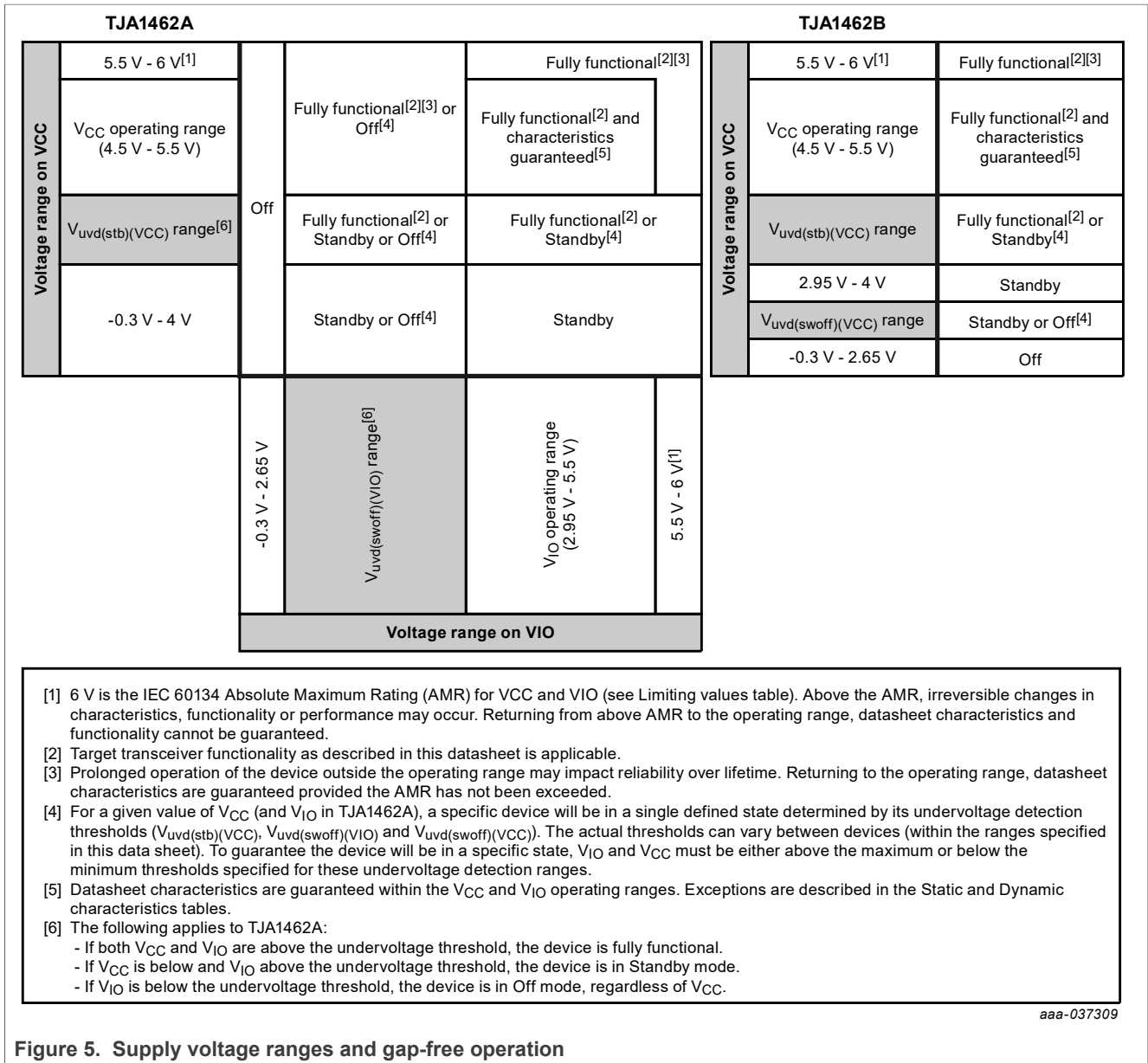


Figure 5. Supply voltage ranges and gap-free operation

7.2 Remote wake-up (via the CAN bus)

The TJA1462 wakes up from Standby mode when a dedicated wake-up pattern (specified in ISO 11898-2: 2016) is detected on the bus.

The wake-up pattern consists of:

- a dominant phase of at least $t_{wake(busdom)}$ followed by
- a recessive phase of at least $t_{wake(busrec)}$ followed by
- a dominant phase of at least $t_{wake(busdom)}$

Dominant or recessive bits between the above mentioned phases that are shorter than $t_{wake(busdom)}$ and $t_{wake(busrec)}$ respectively are ignored.

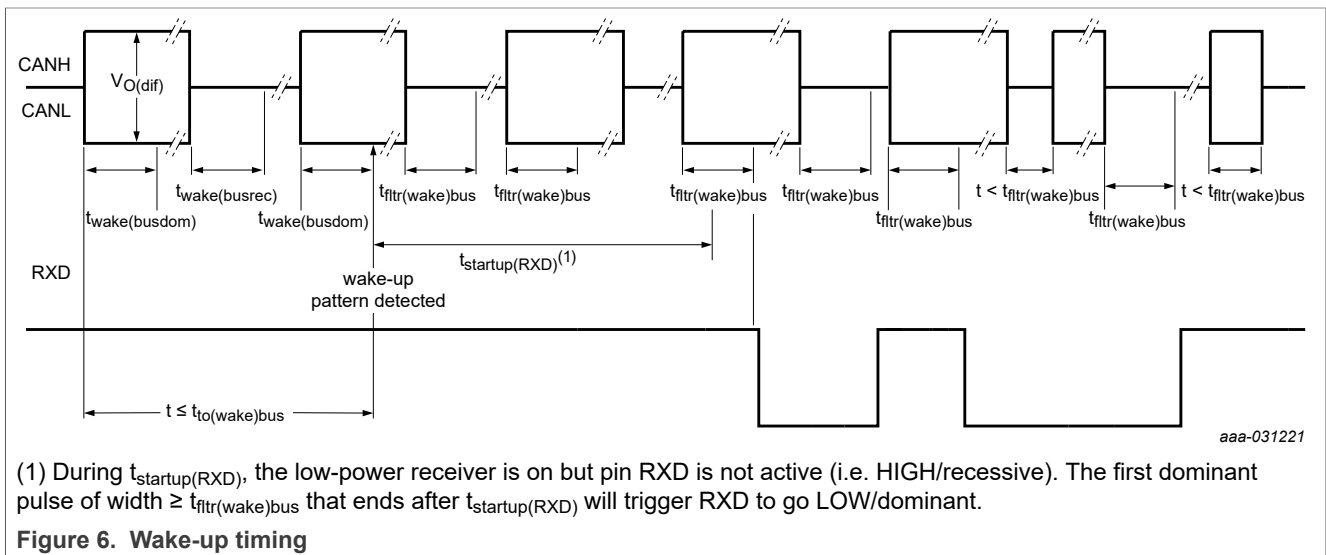
The complete dominant-recessive-dominant pattern must be received within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern (see Figure 6). Otherwise, the internal wake-up

logic is reset. The complete wake-up pattern then needs to be retransmitted to trigger a wake-up event. Pin RXD remains HIGH until the wake-up event has been triggered.

After a wake-up sequence has been detected, the TJA1462 remains in Standby mode with the bus signals reflected on RXD after $t_{startup(RXD)}$. Note that dominant or recessive phases lasting less than $t_{filtr(wake)bus}$ will not be detected by the low-power differential receiver and will not be reflected on RXD in Standby mode.

A wake-up event is not flagged on RXD if any of the following events occurs while a valid wake-up pattern is being received:

- The device switches to Normal mode
- The complete wake-up pattern was not received within $t_{to(wake)bus}$
- A V_{CC} or V_{IO} switch-off undervoltage is detected ($V_{CC} < V_{uvd(swoff)}(V_{CC})$ or $V_{IO} < V_{uvd(swoff)}(V_{IO})$; see [Section 7.3.3](#))



(1) During $t_{startup(RXD)}$, the low-power receiver is on but pin RXD is not active (i.e. HIGH/recessive). The first dominant pulse of width $\geq t_{filtr(wake)bus}$ that ends after $t_{startup(RXD)}$ will trigger RXD to go LOW/dominant.

Figure 6. Wake-up timing

7.3 Fail-safe features

7.3.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on this pin persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD goes HIGH.

7.3.2 Internal biasing of TXD and STB input pins

Pins TXD and STB have internal pull-ups to V_{CC}/V_{IO} to ensure a safe, defined state in case one, or both, of these pins is left or becomes floating. Pull-up resistors are active on these pins in all states; they should be held at the V_{CC}/V_{IO} level in Standby mode to minimize supply current.

7.3.3 Undervoltage detection on pins VCC and VIO

If V_{CC} drops below the standby undervoltage detection threshold ($V_{\text{uvd(stb)}}(V_{CC})$) for $t_{\text{det(uv)}}$, the transceiver switches to Standby mode. The logic state of pin STB is ignored until V_{CC} has recovered.

In the TJA1462A, if V_{IO} drops below the switch-off undervoltage detection threshold ($V_{\text{uvd(swoff)}}(V_{IO})$) for $t_{\text{uvd(swoff)}}$, the transceiver switches to Off mode and disengages from the bus (high-ohmic) until V_{IO} has recovered.

In the TJA1462B, if V_{CC} drops below the switch-off undervoltage detection threshold ($V_{\text{uvd(swoff)}}(V_{CC})$) for $t_{\text{uvd(swoff)}}$, the transceiver switches to Off mode and disengages from the bus (high-ohmic) until V_{CC} has recovered.

7.3.4 Overtemperature protection

The device is protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature, $T_{j(\text{sd})}$, the CAN bus drivers are disabled. When the junction temperature drops below $T_{j(\text{sd})\text{rel}}$, the CAN bus drivers recover once TXD has been reset to HIGH and Normal mode is selected (waiting for TXD to go HIGH prevents output driver oscillation due to small variations in temperature).

7.3.5 I/O levels

Pin VIO on the TJA1462A should be connected to the microcontroller supply voltage (see [Figure 12](#)). This adjusts the signal levels on pins TXD, RXD and STB to the I/O levels of the microcontroller, allowing for direct interfacing without additional glue logic. Pin VIO also provides the internal supply voltage for the low-power differential receiver. For applications running in low-power mode, this allows the bus lines to be monitored for activity even if there is no supply voltage on pin VCC.

All I/O levels are related to V_{CC} in the TJA1462B and are, therefore, compatible with 5 V microcontrollers. Spurious signals from the microcontroller on pin STB are filtered out with a filter time of $t_{\text{ftr(I/O)}}$.

8 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V _x	voltage on pin x ^[1]	pins VCC, VIO (TJA1462A), TXD, STB	-0.3	+6	V
			-	+7 ^[2]	V
		pins CANH, CANL	-36	+40	V
		pin RXD			
			TJA1462A	-0.3	V _{IO} +0.3 ^[3]
	TJA1462B	-0.3	V _{CC} +0.3 ^[3]	V	
V _(CANH-CANL)	voltage between pin CANH and pin CANL		-40	+40	V
V _{trt}	transient voltage	on pins CANH, CANL ^[4]			
		pulse 1	-100	-	V
		pulse 2a	-	+75	V
		pulse 3a	-150	-	V
		pulse 3b	-	+100	V
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω discharge circuit) ^[5]			
		on pins CANH, CANL	-6	+6	kV
		Human Body Model (HBM)			
		on any pin ^[6]	-4	+4	kV
		on pins CANH, CANL ^[7]	-8	+8	kV
		Charged Device Model (CDM) ^[8]			
		on corner pins	-750	+750	V
on any other pin	-500	+500	V		
T _{vj}	virtual junction temperature	^[9]	-40	+150	°C
T _{stg}	storage temperature	^[10]	-55	+150	°C

- [1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.
- [2] The device can withstand voltages between 6 V and 7 V for a total of 20 s over the product lifetime.
- [3] Subject to the qualifications detailed in Table notes 1 and 2 above for pins VCC, VIO, TXD and STB.
- [4] Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO7637.
- [5] Verified by an external test house according to IEC TS 62228, Section 4.3.
- [6] According to AEC-Q100-002.
- [7] Pins stressed to reference group containing all ground and supply pins, emulating the application circuits (Figure 12 and Figure 13). HBM pulse as specified in AEC-Q100-002 used.
- [8] According to AEC-Q100-011.
- [9] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value used in the calculation of T_{vj} . The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).
- [10] T_{stg} in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.

9 Thermal characteristics

Table 7. Thermal characteristics

Value determined for free convection conditions on a JEDEC 2S2P board.

Symbol	Parameter	Conditions ^[1]	Typ	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	SO8	100	K/W
		HVSON8	60	K/W
R _{th(j-c)}	thermal resistance from junction to case ^[2]	HVSON8	22	K/W
Ψ _{j-top}	thermal characterization parameter from junction to top of package	SO8	17	K/W
		HVSON8	16	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 μm).

[2] Case temperature refers to the center of the heatsink at the bottom of the package.

10 Static characteristics

Table 8. Static characteristics

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V (TJA1462A); R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.^[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Supply; pin VCC							
V _{CC}	supply voltage		4.5	-	5.5	V	
V _{uvd(stb)}	standby undervoltage detection voltage		^[2] 4	-	4.5	V	
V _{uvhys(stb)}	standby undervoltage hysteresis voltage		50	-	-	mV	
V _{uvd(swoff)}	switch-off undervoltage detection voltage	TJA1462B	^[2] 2.65	-	2.95	V	
I _{CC}	supply current	Normal mode					
		dominant; V _{TXD} = 0 V; t < t _{to(dom)TXD}	-	42	70	mA	
		dominant; V _{TXD} = 0 V; short circuit on bus lines; -3 V < (V _{CANH} = V _{CANL}) < +40 V	-	-	125	mA	
		recessive; V _{TXD} = V _{IO} ^[3]	-	7	10	mA	
		Standby mode					
		TJA1462A; T _{vj} < 85 °C	-	-	2	μA	
TJA1462B; T _{vj} < 85 °C	-	8	21	μA			
I/O level adapter supply; pin VIO (TJA1462A)							
V _{IO}	supply voltage		2.95	-	5.5	V	
V _{uvd(swoff)}	switch-off undervoltage detection voltage		^[2] 2.65	-	2.95	V	
I _{IO}	supply current	Normal mode, dominant; V _{TXD} = 0 V	-	250	760	μA	
		Normal mode, recessive; V _{TXD} = V _{IO}	-	150	460	μA	

CAN FD signal improvement transceiver with Standby mode

Table 8. Static characteristics...continued

$T_{vj} = -40\text{ °C to }+150\text{ °C}$; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$; $V_{IO} = 2.95\text{ V to }5.5\text{ V (TJA1462A)}$; $R_L = 60\ \Omega$ unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.^[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Standby mode; $T_{vj} < 85\text{ °C}$	-	8	19	μA
CAN transmit data input; pin TXD						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$ ^[3]	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{IO}$ ^[3]	V
$V_{hys(TXD)}$	hysteresis voltage on pin TXD		50	-	-	mV
R_{pu}	pull-up resistance		20	-	80	k Ω
C_i	input capacitance	^[4]	-	-	10	pF
CAN receive data output; pin RXD						
I_{OH}	HIGH-level output current	$V_{RXD} = V_{IO}$ ^[3] - 0.4 V	-10	-	-1	mA
I_{OL}	LOW-level output current	$V_{RXD} = 0.4\text{ V}$; bus dominant	1	-	10	mA
Standby control input; pin STB						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$ ^[3]	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{IO}$ ^[3]	V
V_{hys}	hysteresis voltage		50	-	-	mV
R_{pu}	pull-up resistance		20	-	80	k Ω
C_i	input capacitance	^[4]	-	-	10	pF
Bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	$V_{TXD} = 0\text{ V}$; $t < t_{to(dom)TXD}$; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$				
		pin CANH; $R_L = 50\ \Omega$ to $65\ \Omega$	2.89	3.5	4.26	V
		pin CANL; $R_L = 50\ \Omega$ to $65\ \Omega$	0.77	1.5	2.13	V
V_{TXsym}	transmitter voltage symmetry	$V_{TXsym} = V_{CANH} + V_{CANL}$; $C_{SPLIT} = 4.7\text{ nF}$; $f_{TXD} = 250\text{ kHz, }1\text{ MHz or }2.5\text{ MHz}$	^[4] ^[5] 0.9 V_{CC}	-	1.1 V_{CC}	V
$V_{cm(step)}$	common mode voltage step		^[4] ^[5] ^[6] -150	-	+150	mV
$V_{cm(p-p)}$	peak-to-peak common mode voltage		^[4] ^[5] ^[6] -300	-	+300	mV
$V_{O(dif)}$	differential output voltage	dominant; Normal mode; $V_{TXD} = 0\text{ V}$; $t < t_{to(dom)TXD}$; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$				
		$R_L = 50\ \Omega$ to $65\ \Omega$	1.5	-	2.75	V
		$R_L = 45\ \Omega$ to $70\ \Omega$	1.4	-	3.3	V
		$R_L = 2240\ \Omega$	^[4] 1.5	-	5	V
		recessive; no load				
	Normal mode; $V_{TXD} = V_{IO}$ ^[3]		-50	-	+50	mV

CAN FD signal improvement transceiver with Standby mode

Table 8. Static characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; $V_{IO} = 2.95\text{ V}$ to 5.5 V (TJA1462A); $R_L = 60\text{ }\Omega$ unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.^[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Standby mode	-0.2	-	+0.2	V
$V_{O(rec)}$	recessive output voltage	Normal mode; $V_{TXD} = V_{IO}$ ^[3] ; no load	2	2.5	3	V
		Standby mode; no load	-0.1	-	+0.1	V
$V_{th(RX)dif}$	differential receiver threshold voltage	$-12\text{ V} \leq V_{CANH} \leq +12\text{ V}$; $-12\text{ V} \leq V_{CANL} \leq +12\text{ V}$				
		Normal mode	0.5	-	0.9	V
		Standby mode	0.4	-	1.1	V
$V_{rec(RX)}$	receiver recessive voltage	$-12\text{ V} \leq V_{CANH} \leq +12\text{ V}$; $-12\text{ V} \leq V_{CANL} \leq +12\text{ V}$				
		Normal mode	-4	-	+0.5	V
		Standby mode	-4	-	+0.4	V
$V_{dom(RX)}$	receiver dominant voltage	$-12\text{ V} \leq V_{CANH} \leq +12\text{ V}$; $-12\text{ V} \leq V_{CANL} \leq +12\text{ V}$				
		Normal mode	0.9	-	9	V
		Standby mode	1.1	-	9	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	$-12\text{ V} \leq V_{CANH} \leq +12\text{ V}$; $-12\text{ V} \leq V_{CANL} \leq +12\text{ V}$; Normal mode	100	-	-	mV
$I_{O(sc)}$	short-circuit output current	$-15\text{ V} \leq V_{CANH} \leq +40\text{ V}$; $-15\text{ V} \leq V_{CANL} \leq +40\text{ V}$	-	-	115	mA
$I_{O(sc)rec}$	recessive short-circuit output current	$-27\text{ V} \leq V_{CANH} \leq +32\text{ V}$; $-27\text{ V} \leq V_{CANL} \leq +32\text{ V}$; Normal mode; $V_{TXD} = V_{IO}$ ^[3] for $t > t_{d(TXD-busrec)end}$ ^[7]	-3	-	+3	mA
I_L	leakage current	$V_{CC} = V_{IO} = 0\text{ V}$ or pins shorted to GND via $47\text{ k}\Omega$; $V_{CANH} = V_{CANL} = 5\text{ V}$	-10	-	+10	μA
R_i	input resistance	$-2\text{ V} \leq V_{CANL} \leq +7\text{ V}$; $-2\text{ V} \leq V_{CANH} \leq +7\text{ V}$	25	40	50	k Ω
ΔR_i	input resistance deviation	$0\text{ V} \leq V_{CANL} \leq +5\text{ V}$; $0\text{ V} \leq V_{CANH} \leq +5\text{ V}$	-3	-	+3	%
$R_{i(dif)}$	differential input resistance	$-2\text{ V} \leq V_{CANL} \leq +7\text{ V}$; $-2\text{ V} \leq V_{CANH} \leq +7\text{ V}$	50	80	100	k Ω
$C_{i(cm)}$	common-mode input capacitance		[4] -	-	30	pF
$C_{i(dif)}$	differential input capacitance		[4] -	-	15	pF
Signal Improvement function on CANH or CANL; $+4.75\text{ V} \leq V_{CC} \leq +5.25\text{ V}$; see Figure 10 and Figure 11						
$R_{i(dom)}$	dominant phase input resistance	bus dominant; $V_{CC} - 1.6\text{ V} \leq V_{CANH} \leq V_{CC} - 1.2\text{ V}$; $+1.2\text{ V} \leq V_{CANL} \leq +1.6\text{ V}$;	-	-	30	Ω
$R_{i(dif)dom}$	dominant phase differential input resistance	$R_{i(dif)dom} = R_{i(dom)CANH} + R_{i(dom)CANL}$	-	-	60	Ω

Table 8. Static characteristics...continued

$T_{vj} = -40\text{ °C to }+150\text{ °C}$; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$; $V_{IO} = 2.95\text{ V to }5.5\text{ V (TJA1462A)}$; $R_L = 60\text{ }\Omega$ unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.^[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{i(\text{extdom})}$	extended dominant phase input resistance ^[8]	bus dominant-to-recessive transition; $+2.3\text{ V} \leq V_{\text{CANH}} \leq V_{\text{CC}} - 2.3\text{ V}$;	-	-	25	Ω
$R_{i(\text{dif})\text{extdom}}$	extended dominant phase differential input resistance ^[8]	$+2.3\text{ V} \leq V_{\text{CANL}} \leq V_{\text{CC}} - 2.3\text{ V}$; $R_{i(\text{dif})\text{extdom}} = R_{i(\text{extdom})\text{CANH}} + R_{i(\text{extdom})\text{CANL}}$	-	-	50	Ω
$R_{i(\text{actrec})}$	active recessive phase input resistance ^[8]	bus dominant-to-recessive transition; $+1.5\text{ V} \leq V_{\text{CANH}} \leq V_{\text{CC}} - 1.5\text{ V}$;	37.5	-	62.5	Ω
$R_{i(\text{dif})\text{actrec}}$	active recessive phase differential input resistance ^[8]	$+1.5\text{ V} \leq V_{\text{CANL}} \leq V_{\text{CC}} - 1.5\text{ V}$; $R_{i(\text{dif})\text{actrec}} = R_{i(\text{actrec})\text{CANH}} + R_{i(\text{actrec})\text{CANL}}$	75	-	125	Ω
Temperature detection						
$T_{j(\text{sd})}$	shutdown junction temperature		[4] 180	-	200	$^{\circ}\text{C}$
$T_{j(\text{sd})\text{rel}}$	release shutdown junction temperature		[4] 175	-	195	$^{\circ}\text{C}$

- [1] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.
- [2] Undervoltage is detected between min and max values. Undervoltage is guaranteed to be detected below min value and guaranteed not to be detected above max value.
- [3] V_{CC} in TJA1462B
- [4] Not tested in production; guaranteed by design.
- [5] The test circuit used to measure the bus output voltage symmetry and the common-mode voltages (which includes C_{SPLIT}) is shown in [Figure 15](#).
- [6] See [Figure 9](#)
- [7] This parameter is defined in CiA specification CiA 601-4:2019 as $t_{\text{SIC_TX_base}}$ and is specified in the Dynamic Characteristics table (see [Table 9](#) and [Figure 10](#)).
- [8] Extended dominant and active recessive phases are not DC states and are only valid for a limited time after a dominant-to-recessive transition on pin TXD.

11 Dynamic characteristics

Table 9. Dynamic characteristics

$T_{vj} = -40\text{ °C to }+150\text{ °C}$; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$; $V_{IO} = 2.95\text{ V to }5.5\text{ V (TJA1462A)}$; $R_L = 60\ \Omega$ unless specified otherwise; all voltages are defined with respect to ground.^[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN timing characteristics; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $t_{bit(TXD)} \geq 125\text{ ns}$; see Figure 7 , Figure 8 , Figure 10 , Figure 11 and Figure 14						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	Normal mode	-	-	80	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	Normal mode	-	-	80	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	Normal mode	-	-	110	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	Normal mode	-	-	110	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	Normal mode	-	-	190	ns
		Normal mode; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	255	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	Normal mode	-	-	190	ns
		Normal mode; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	255	ns
$t_{d(TXD-busrec)end}$	delay time from TXD to bus recessive end	Normal mode	^[2] ^[3] 415	-	530	ns
$t_{d(TXD-busdom)end}$	delay time from TXD to bus dominant end	Normal mode	^[2] -	-	115	ns
$t_{d(TXD-extbusdom)end}$	delay time from TXD to extended bus dominant end	Normal mode	^[2] 55	-	-	ns
$t_{d(TXD-busactrec)start}$	delay time from TXD to bus active recessive start	Normal mode	^[2] 70	-	120	ns
$t_{d(TXD-busactrec)end}$	delay time from TXD to active recessive end	Normal mode	^[2] 335	-	480	ns
CAN FD timing characteristics according to CiA 601-4:2019; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $t_{bit(TXD)} \geq 125\text{ ns}$; see Figure 8 and Figure 14 ^[4]						
$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation	$\Delta t_{bit(bus)} = t_{bit(bus)} - t_{bit(TXD)}$	-10	-	+10	ns
Δt_{rec}	receiver timing symmetry	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$	-20	-	+15	ns
$\Delta t_{bit(RXD)}$	received recessive bit width deviation	$\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$	-30	-	+20	ns
CAN FD timing characteristics according to ISO 11898-2:2016 ^[5] ; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; see Figure 8 and Figure 14 . ^[4]						
$t_{bit(bus)}$ ^[6]	transmitted recessive bit width	2 Mbit/s ($t_{bit(TXD)} = 500\text{ ns}$)				
		$V_{CC} = 4.75\text{ V to }5.25\text{ V}$	490	-	510	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	435	-	530	ns
		5 Mbit/s ($t_{bit(TXD)} = 200\text{ ns}$)				
		$V_{CC} = 4.75\text{ V to }5.25\text{ V}$	190	-	210	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	^[7] 170	-	230	ns
		8 Mbit/s ($t_{bit(TXD)} = 125\text{ ns}$)				
$V_{CC} = 4.75\text{ V to }5.25\text{ V}$	115	-	135	ns		

CAN FD signal improvement transceiver with Standby mode

Table 9. Dynamic characteristics...continued

$T_{vj} = -40\text{ °C to }+150\text{ °C}$; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$; $V_{IO} = 2.95\text{ V to }5.5\text{ V}$ (TJA1462A); $R_L = 60\text{ }\Omega$ unless specified otherwise; all voltages are defined with respect to ground.^[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Δt_{rec}	receiver timing symmetry	$V_{CC} = 4.75\text{ V to }5.25\text{ V}$; for 2 Mbit/s, 5 Mbit/s and 8 Mbit/s	-20	-	+15	ns	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$; 2 Mbit/s	-65	-	+40	ns	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$; 5 Mbit/s	-45	-	+15	ns	
$t_{bit(RXD)}^{[8]}$	bit time on pin RXD	2 Mbit/s ($t_{bit(TXD)} = 500\text{ ns}$)					
		$V_{CC} = 4.75\text{ V to }5.25\text{ V}$	470	-	520	ns	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	400	-	550	ns	
		5 Mbit/s ($t_{bit(TXD)} = 200\text{ ns}$)					
		$V_{CC} = 4.75\text{ V to }5.25\text{ V}$	170	-	220	ns	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ^[7]	150	-	240	ns	
		8 Mbit/s ($t_{bit(TXD)} = 125\text{ ns}$)					
	$V_{CC} = 4.75\text{ V to }5.25\text{ V}$	95	-	145	ns		
Dominant time-out time; pin TXD							
$t_{to(dom)TXD}$	TXD dominant time-out time	$V_{TXD} = 0\text{ V}$; Normal mode ^[2] ^[9]	0.8	-	9	ms	
Bus wake-up times; pins CANH and CANL; see Figure 6							
$t_{wake(busdom)}$	bus dominant wake-up time	Standby mode ^[2] ^[10]	0.5	-	1.8	μs	
$t_{wake(busrec)}$	bus recessive wake-up time	Standby mode ^[2] ^[10]	0.5	-	1.8	μs	
$t_{to(wake)bus}$	bus wake-up time-out time	Standby mode ^[2] ^[9]	0.8	-	9	ms	
$t_{ftr(wake)bus}$	bus wake-up filter time	Standby mode ^[2]	-	-	1.8	μs	
Mode transitions							
$t_{t(moch)}$	mode change transition time		^[2]	-	50	μs	
$t_{startup}$	start-up time		^[2]	-	1.5	ms	
$t_{startup(RXD)}$	RXD start-up time	after wake-up detected	^[2] ^[11]	4	-	20	μs
IO filter; pin STB							
$t_{ftr(IO)}$	IO filter time		^[12]	1	-	5	μs
Undervoltage detection; Figure 3 and Figure 4							
$t_{det(uv)}$	undervoltage detection time	on pin VCC	^[2]	-	30	μs	
$t_{uvd(swoff)}$	switch-off undervoltage detection time	on pin VCC; TJA1462B	^[2]	-	30	μs	
		on pin VIO; TJA1462A	^[2]	-	30	μs	
$t_{rec(uv)}$	undervoltage recovery time	on pin VCC	^[2]	-	50	μs	

[1] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Not tested in production; guaranteed by design.

CAN FD signal improvement transceiver with Standby mode

- [3] If TXD goes LOW before the recessive transition has been completed, the bus switches to dominant.
- [4] TJA1462 fully meets CiA 601-4:2019 which sets tighter limits for $t_{bit(bus)}$, Δt_{rec} and $\Delta t_{bit(RXD)}$ than ISO 11898-2:2016, which TJA1462 therefore also fully meets.
- [5] 8 Mbit/s specification extends the timing characteristics of ISO 11898-2:2016 and CiA 601-4:2019.
- [6] $t_{bit(bus)} = \Delta t_{bit(bus)} + t_{bit(TXD)}$.
- [7] For reasons related to CAN FD bit timing symmetry, these values are centered around the nominal bit length. Details can be found in document AH2002 'TJx144x/TJx146x Application Hints', available on request from NXP Semiconductors.
- [8] $t_{bit(RXD)} = \Delta t_{bit(RXD)} + t_{bit(TXD)}$.
- [9] Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.
- [10] A dominant/recessive phase shorter than the min value is guaranteed not to be seen as a dominant/recessive bit; a dominant/recessive phase longer than the max value is guaranteed to be seen as a dominant/recessive bit.
- [11] When a wake-up is detected, RXD start-up time is between the min and max values. RXD cannot be relied on below the min value; RXD can be relied on above the max value; see [Figure 6](#).
- [12] Pulses shorter than the min value are guaranteed to be filtered out; pulses longer than the max value are guaranteed to be processed.

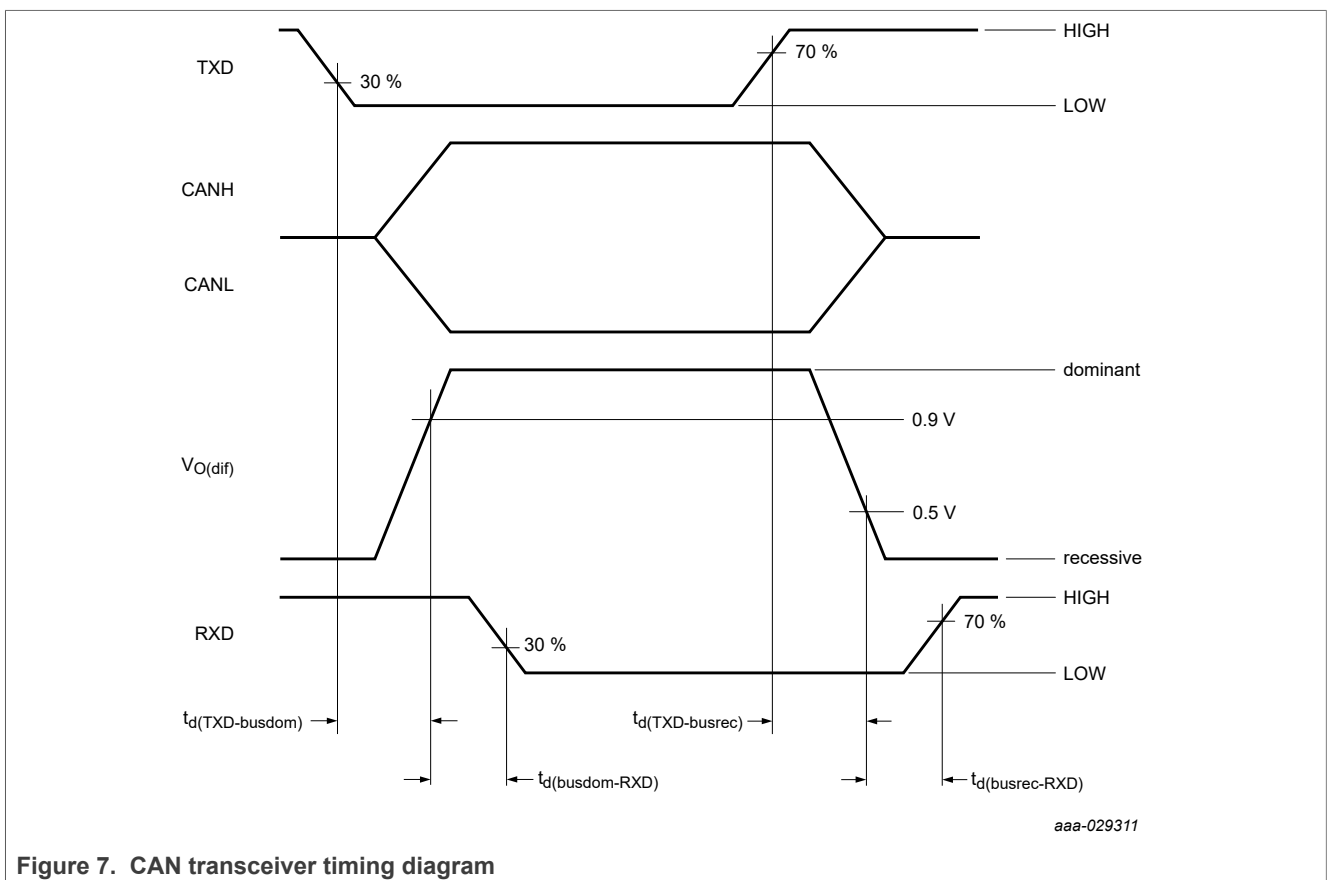


Figure 7. CAN transceiver timing diagram

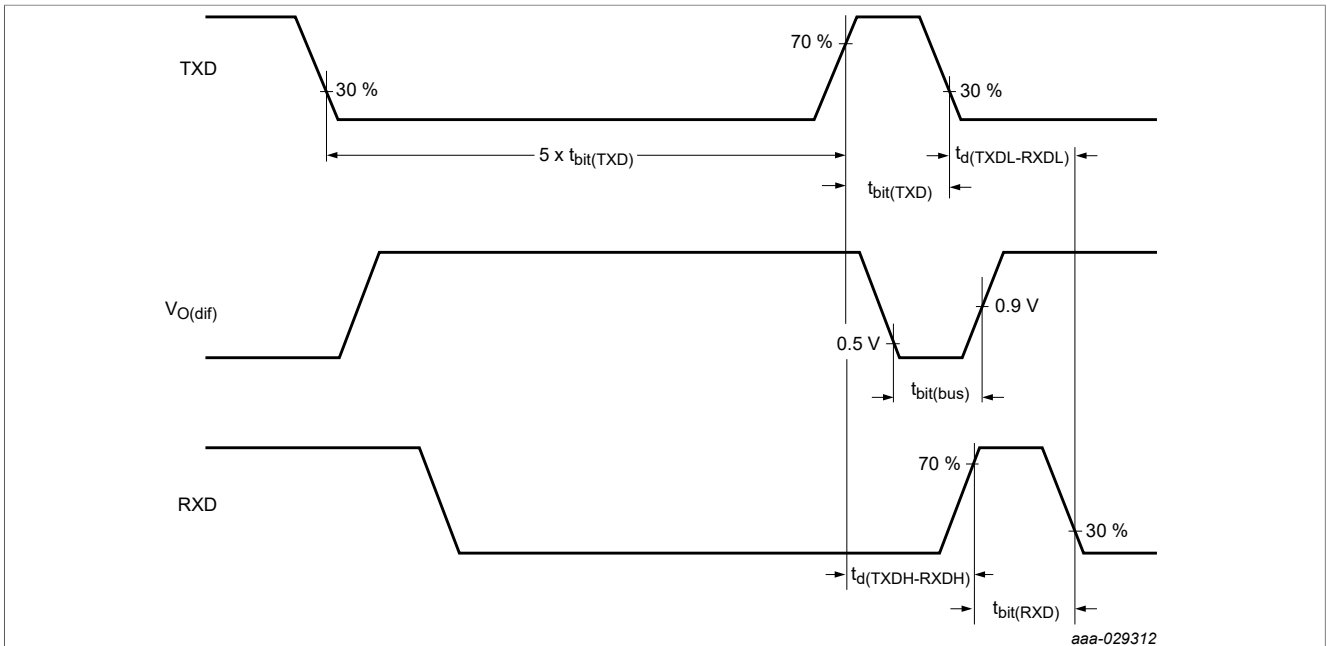


Figure 8. CAN FD timing definitions according to ISO 11898-2:2016

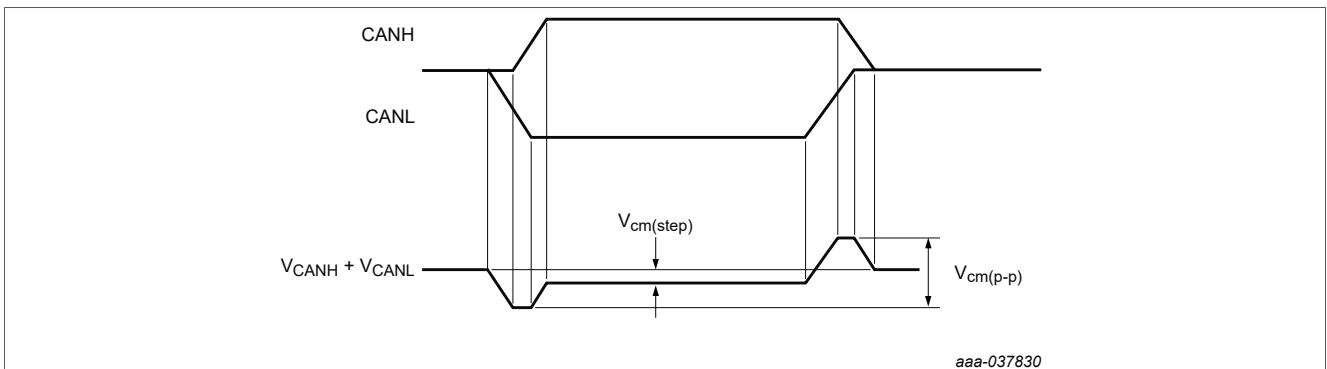


Figure 9. CAN bus common-mode voltage according to SAE 1939-14

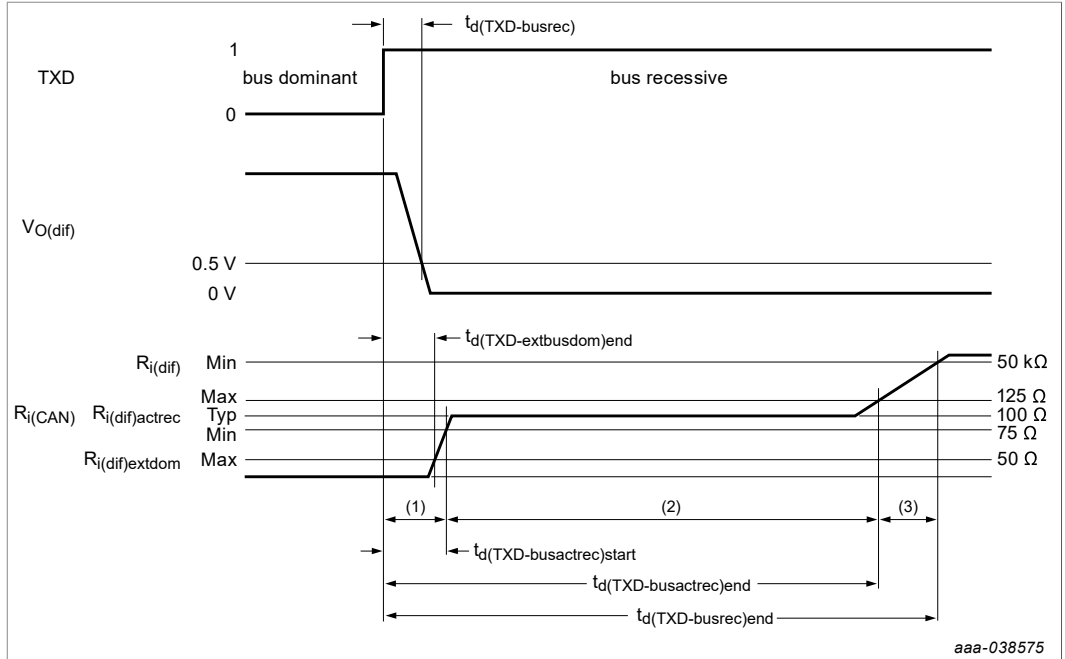


Figure 10. TJA1462 transmitter impedance and timing diagram for dominant-to-passive recessive transition

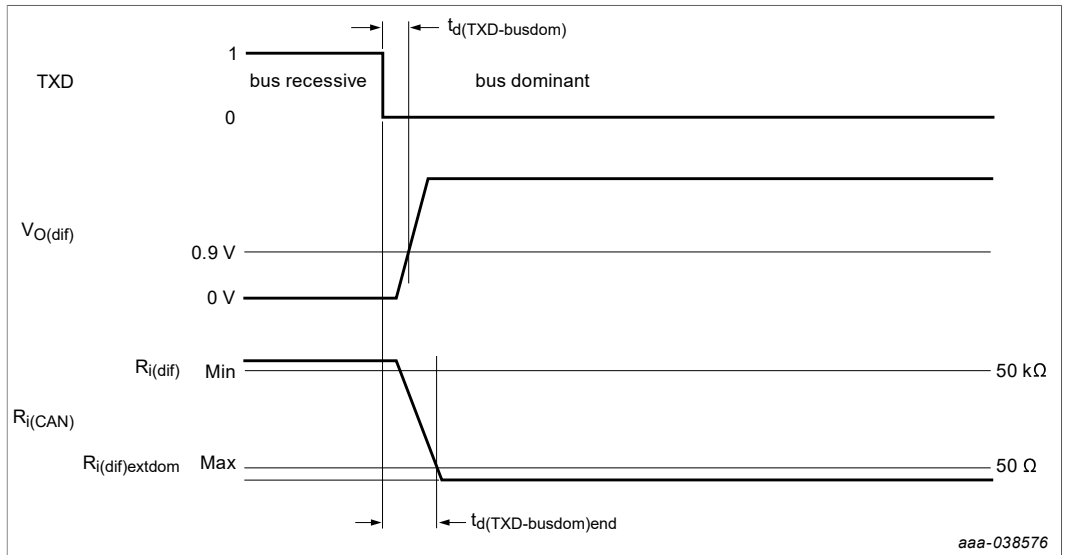
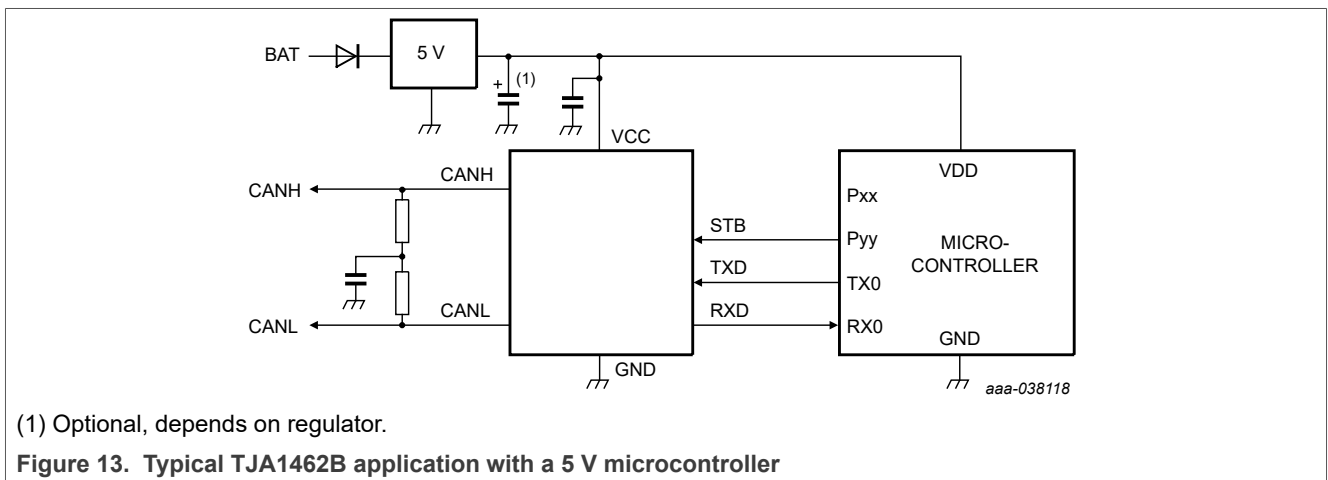
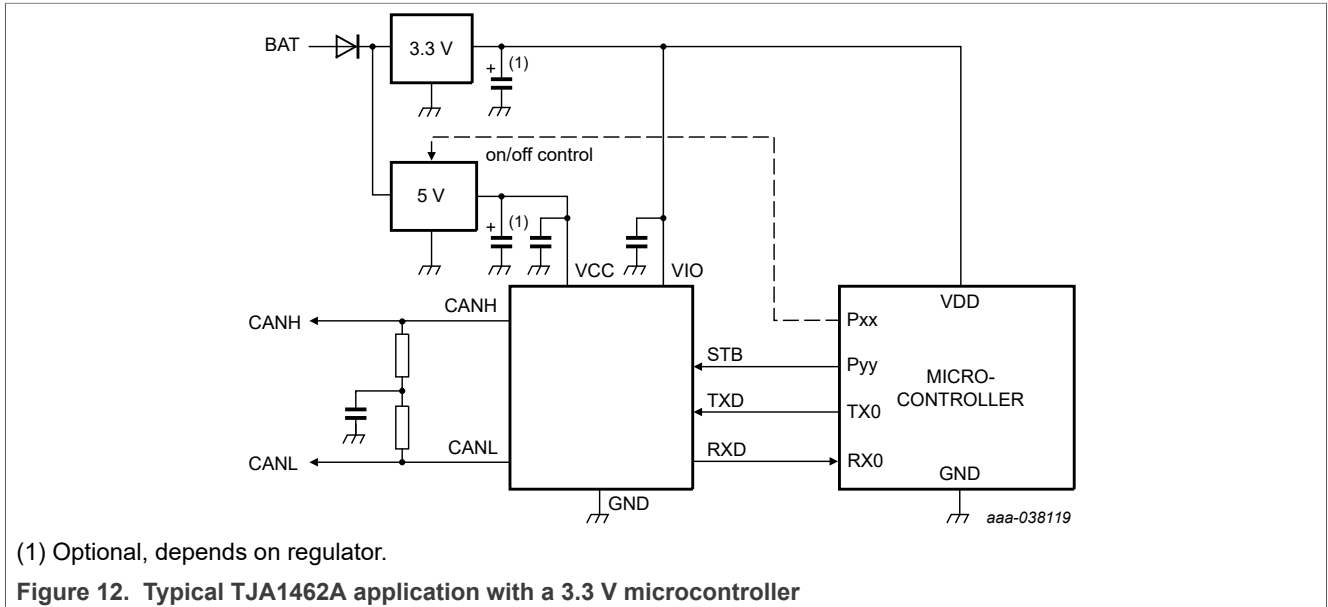


Figure 11. TJA1462 transmitter impedance and timing diagram for passive recessive-to-dominant transition

12 Application information

12.1 Application diagrams



12.2 Application hints

Further information on the application of the TJA1462 can be found in NXP application hints AH2002 '*TJx144x/TJx146x Application Hints*', available on request from NXP Semiconductors.

13 Test information

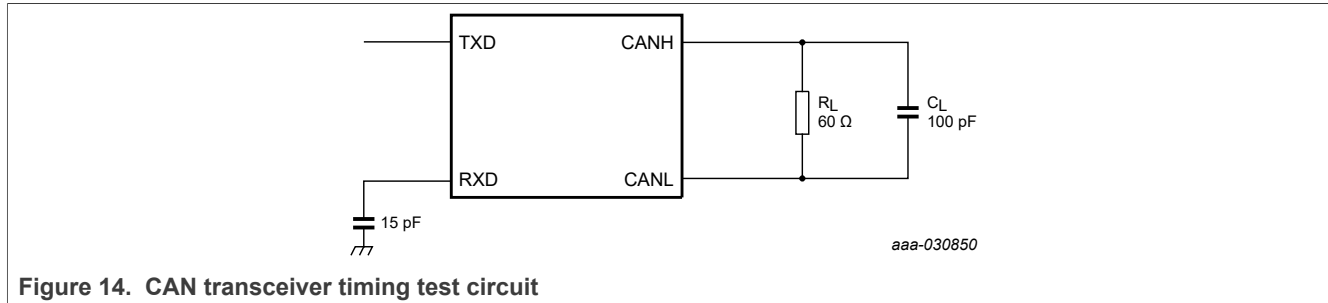


Figure 14. CAN transceiver timing test circuit

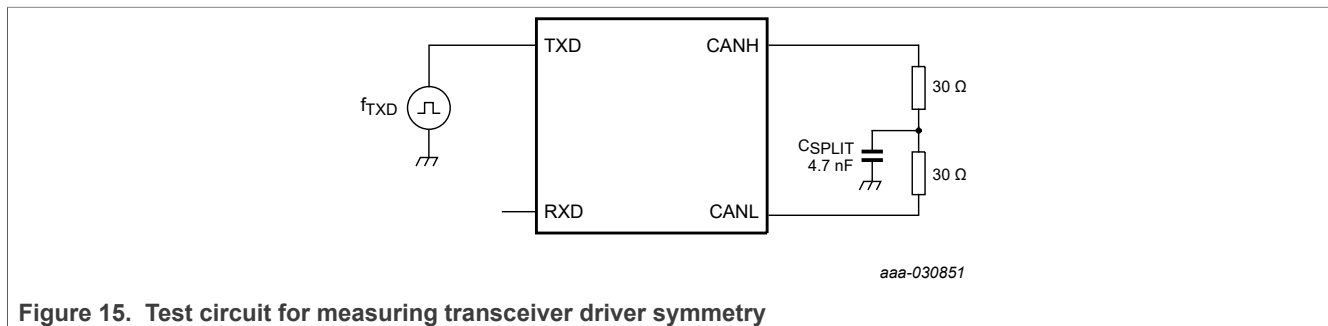


Figure 15. Test circuit for measuring transceiver driver symmetry

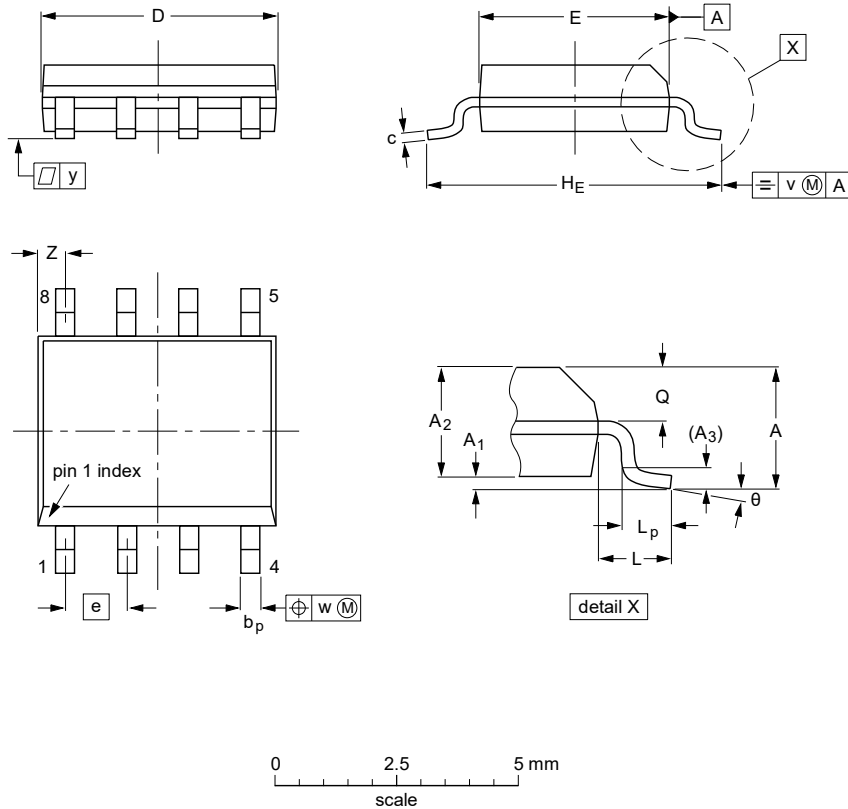
13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 Rev-H - *Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

14 Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

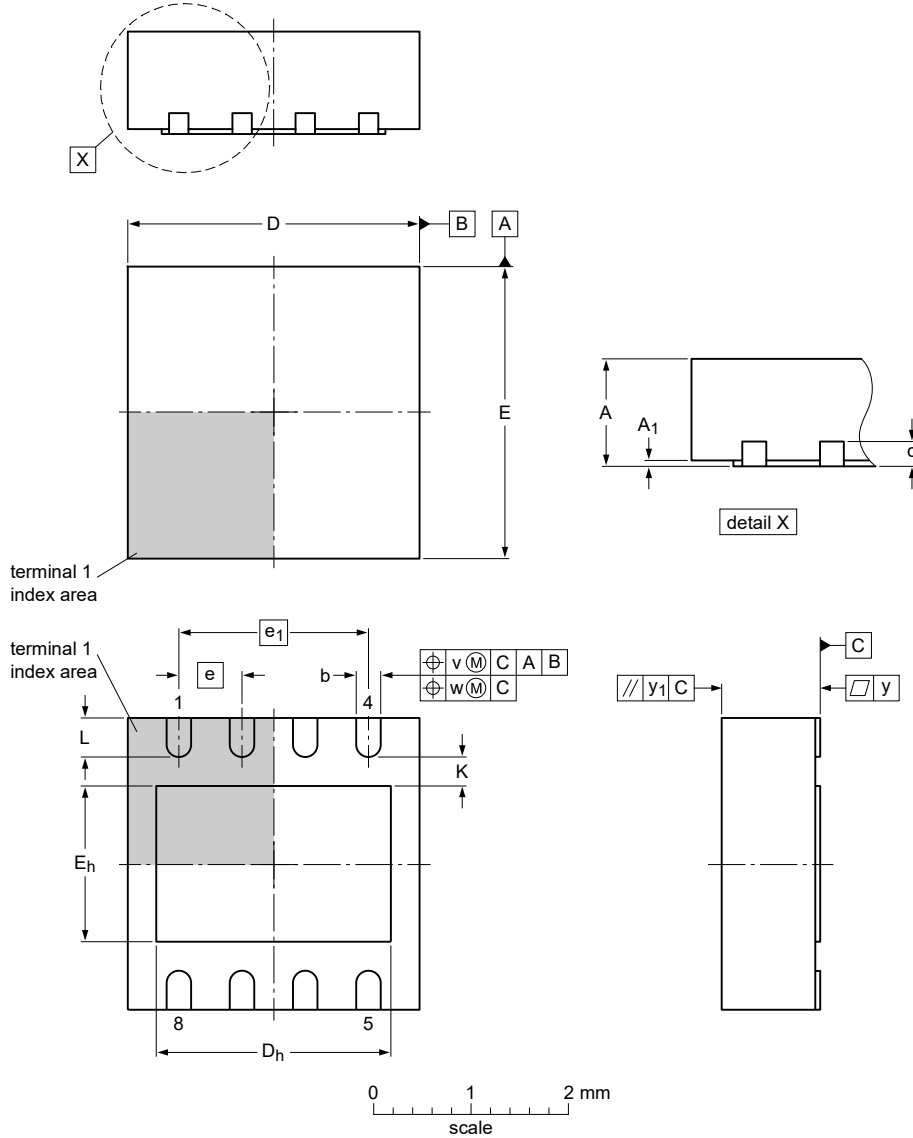
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT96-1	076E03	MS-012			99-12-27 03-02-18

Figure 16. Package outline SOT96-1 (SO8)

HVSON8: plastic thermal enhanced very thin small outline package; no leads;
8 terminals; body 3 x 3 x 0.85 mm

SOT782-1



Dimensions

Unit ⁽¹⁾	A	A ₁	b	c	D	D _h	E	E _h	e	e ₁	K	L	v	w	y	y ₁
max	1.00	0.05	0.35		3.10	2.45	3.10	1.65			0.35	0.45				
mm nom	0.85	0.03	0.30	0.2	3.00	2.40	3.00	1.60	0.65	1.95	0.30	0.40	0.1	0.05	0.05	0.1
min	0.80	0.00	0.25		2.90	2.35	2.90	1.55			0.25	0.35				

Note

1. Plastic or metal protrusions of 0.075 maximum per side are not included.

sot782-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT782-1	---	MO-229	---			-09-08-25- 09-08-28

Figure 17. Package outline SOT782-1 (HVSON8)

15 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 18](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 10](#) and [Table 11](#)

Table 10. SnPb eutectic process (from J-STD-020D)

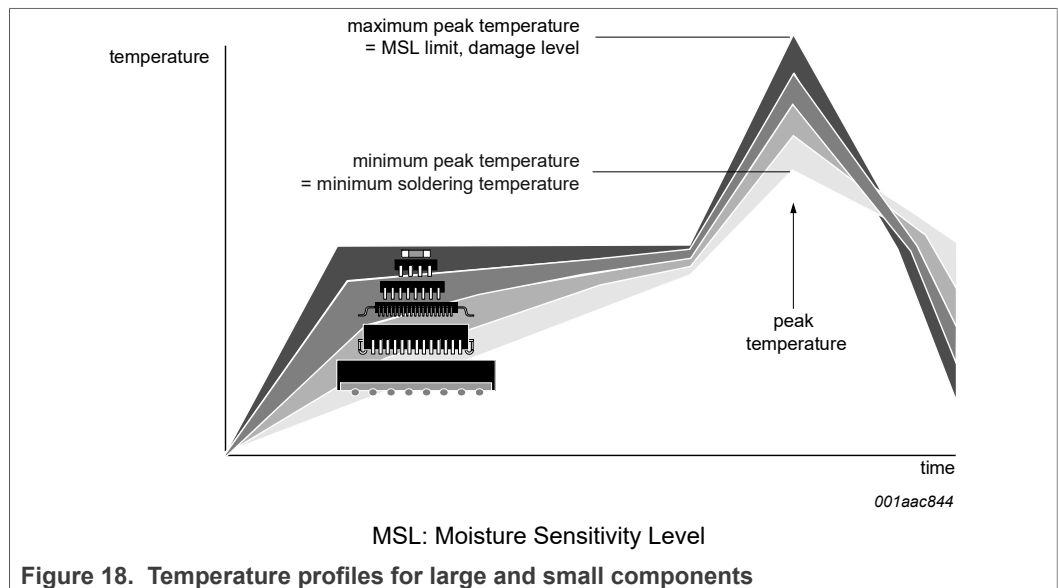
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 18](#).



For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.

17 Soldering of HVSON packages

[Section 16](#) contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering HVSON leadless package ICs can be found in the following application note:

- AN10365 “Surface mount reflow soldering description”

18 Appendix: ISO 11898-2:2016 and CiA 601-4:2019 parameter cross-reference lists

Table 12. ISO 11898-2:2016 to NXP data sheet parameter conversion

ISO 11898-2:2016		NXP data sheet	
Parameter	Notation	Symbol	Parameter
HS-PMA dominant output characteristics			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{O(dom)}$	dominant output voltage
Single ended voltage on CAN_L	V_{CAN_L}		
Differential voltage on normal bus load	V_{Diff}	$V_{O(dif)}$	differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
HS-PMA driver symmetry			
Driver symmetry	V_{SYM}	V_{TXsym}	transmitter voltage symmetry
Maximum HS-PMA driver output current			
Absolute current on CAN_H	I_{CAN_H}	$I_{O(sc)}$	short-circuit output current
Absolute current on CAN_L	I_{CAN_L}		
HS-PMA recessive output characteristics, bus biasing active/inactive			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{O(rec)}$	recessive output voltage
Single ended output voltage on CAN_L	V_{CAN_L}		
Differential output voltage	V_{Diff}	$V_{O(dif)}$	differential output voltage
Optional HS-PMA transmit dominant time-out			
Transmit dominant time-out, long	t_{dom}	$t_{to(dom)TXD}$	TXD dominant time-out time
Transmit dominant time-out, short			
HS-PMA static receiver input characteristics, bus biasing active/inactive			
Recessive state differential input voltage range	V_{Diff}	$V_{th(RX)dif}$	differential receiver threshold voltage
Dominant state differential input voltage range		$V_{rec(RX)}$	receiver recessive voltage
		$V_{dom(RX)}$	receiver dominant voltage
HS-PMA receiver input resistance (matching)			
Differential internal resistance	R_{Diff}	$R_{i(dif)}$	differential input resistance
Single ended internal resistance	R_{CAN_H} R_{CAN_L}	R_i	input resistance
Matching of internal resistance	MR	ΔR_i	input resistance deviation
HS-PMA implementation loop delay requirement			
Loop delay	t_{Loop}	$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH
		$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW

CAN FD signal improvement transceiver with Standby mode

Table 12. ISO 11898-2:2016 to NXP data sheet parameter conversion...continued

ISO 11898-2:2016		NXP data sheet	
Parameter	Notation	Symbol	Parameter
Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s up to 2 Mbit/s and above 2 Mbit/s up to 5 Mbit/s			
Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended	$t_{Bit(Bus)}$	$t_{bit(bus)}$	transmitted recessive bit width
Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s	$t_{Bit(RXD)}$	$t_{bit(RXD)}$	bit time on pin RXD
Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s	Δt_{Rec}	Δt_{rec}	receiver timing symmetry
HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}			
Maximum rating V_{Diff}	V_{Diff}	$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL
General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H}	V_x	voltage on pin x
Optional: Extended maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_L}		
HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered			
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_L	leakage current
HS-PMA bus biasing control timings			
CAN activity filter time, long	t_{Filter}	$t_{wake(busdom)}^{[1]}$	bus dominant wake-up time
CAN activity filter time, short		$t_{wake(busrec)}$	bus recessive wake-up time
Wake-up time-out, short	t_{Wake}	$t_{to(wake)bus}$	bus wake-up time-out time
Wake-up time-out, long			

[1] $t_{filtr(wake)bus}$ - bus wake-up filter time, in devices with basic wake-up functionality

Table 13. CiA 601-4:2019 to NXP data sheet parameter conversion

CiA 601-4:2019		NXP data sheet	
Parameter	Notation	Symbol	Parameter
Optional HS-PMA implementation data signal timing requirements			
Signal improvement time TX-based	$t_{SIC_TX_base}$	$t_{d(TXD-busrec)end}$	delay time from TXD to bus recessive end
Signal improvement time RX-based	$t_{SIC_RX_base}$	N/A ^[1]	N/A
Transmitted bit width variation	$\Delta t_{Bit(Bus)}$	$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation
Received bit width variation	$\Delta t_{Bit(RxD)}$	$\Delta t_{bit(RXD)}$	received recessive bit width deviation
Receiver timing symmetry	Δt_{REC}	Δt_{rec}	receiver timing symmetry
Propagation delay from TXD to bus dominant	$t_{prop(TXD-busdom)}$	$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant
Propagation delay from TXD to bus recessive	$t_{prop(TXD-busrec)}$	$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive
Propagation delay from bus to RXD dominant	$t_{prop(busdom-RXD)}$	$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD
Propagation delay from bus to RXD recessive	$t_{prop(busrec-RXD)}$	$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD

[1] The NXP signal improvement implementation is TX-based; RX-based is not applicable.

19 Appendix: TJx144x/TJx146x/TJF1441 family overview

Table 14. Feature overview of the complete TJx144x/TJx146x/TJF1441 family

Device ^[1]	Modes					Supplies			Data rate		Additional features					
	Normal	Standby	Sleep	Silent/Listen-only	Selectable Off	VCC pin	VIO pin	VBAT pin	Up to 5 Mbit/s CAN FD	Up to 8 Mbit/s CAN FD ^[2]	Signal improvement ^[3]	Wake-up source recognition ^[4]	Short WUP support [0.5 - 1.8 μs] ^[5]	Single supply pin wake-up ^[6]	TXD dominant timeout	Local diagnostics via ERR_N pin
TJx1441A	•			•		•	•		•						•	
TJx1441B	•			•		•			•						•	
TJx1441D	•			•	•	•			•						•	
TJF1441A	•			•		•	•		•							[7]
TJx1442A	•	•				•	•		•				•	•	•	
TJx1442B	•	•				•			•				•		•	
TJx1443A	•	•	•	•		•	•	•	•			•	•	•	•	•
TJx1448A	•	•				•	•		•				•	•	•	
TJx1448B	•	•				•			•				•		•	
TJx1448C	•	•				•	•		•			•	•	•	•	
TJx1462A	•	•				•	•		•	•	•		•	•	•	
TJx1462B	•	•				•			•	•	•		•		•	
TJx1463A	•	•	•	•		•	•	•	•	•	•	•	•	•	•	•

[1] TJx: TJA14xxx is AEC-Q100 Grade 1; TJR14xxx is AEC-Q100 Grade 0; TJF1441A is non-automotive grade.

[2] Only guaranteed for TJA146x, AEC-Q100 Grade 1.

[3] CAN FD Signal Improvement Capability (SIC) according to CiA 601-4:2019.

[4] RXD is held LOW after wake-up request, enabling wake-up source recognition.

[5] WUP = wake-up pattern according ISO11898-2:2016.

[6] Only VIO supply needed for wake-up in TJA1442A, TJA1448A, TJA1448C, TJA1462A; only VBAT supply needed for wake-up in TJA1443A, TJA1463A.

[7] Not having TXD dominant timeout allows for very low data rates in non-automotive grade applications.

20 Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1462 v.2	20211015	Product data sheet	-	TJA1462 v.1
Modifications	<ul style="list-style-type: none"> • CAN FD communication up to 8 Mbit/s: Section 1 text revised, CAN FD parameters $t_{bit(TXD)}$, $t_{bit(BUS)}$, Δt_{rec} and $t_{bit(RXD)}$ updated in Table 9 and table note 5 added • Added device (Table 3) and family (Section 19) feature overviews • Table 6: table note 10 added • Table 9: measurement conditions for parameter $t_{startup(RXD)}$ revised • Section 21: <i>Suitability for use in Automotive applications</i> and <i>Security</i> disclaimers revised 			

Table 15. Revision history...continued

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1462 v.1	20200812	Product data sheet	-	-

21 Legal information

21.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

21.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

21.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without

notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Suitability for use in automotive applications — This NXP product has been qualified for use in automotive applications. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"),

then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible

for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

21.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.