

# TJA1463

## CAN FD signal improvement transceiver with Sleep mode

Rev. 2 — 15 October 2021

Product data sheet

## 1 General description

---

The TJA1463 is a member of the TJA146x family of transceivers that provide an interface between a Controller Area Network (CAN) or CAN FD (Flexible Data rate) protocol controller and the physical two-wire CAN bus. TJA146x transceivers implement the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5, and are fully interoperable with high-speed Classical CAN and CAN FD transceivers.

The TJA1463 includes CAN Signal Improvement Capability (SIC), as defined in CiA 601-4:2019. CAN signal improvement significantly reduces signal ringing in a network, allowing reliable CAN FD communication to function in larger topologies. In addition, the TJA1463 features a much tighter bit timing symmetry performance to enable CAN FD communication up to 8 Mbit/s.

The TJA1463 is intended as a simple replacement for high-speed Classical CAN and CAN FD transceivers, such as the TJA1043 from NXP. It offers pin compatibility and is designed to avoid changes to hardware and software design, allowing the TJA1463 to be easily retrofitted to existing applications.

An AEC-Q100 Grade 0 variant, the TJR1463, is available for high temperature applications, supporting operation at 150 °C ambient temperature.

## 2 Features and benefits

---

### 2.1 General

- ISO 11898-2:2016, SAE J2284-1 to SAE J2284-5 and SAE J1939-14 compliant
- Implements CAN Signal Improvement Capability as defined in CiA 601-4:2019 to significantly reduce signal ringing effects in a network
- Much tighter bit timing symmetry performance allowing more time to reduce signal ringing
- Low Electromagnetic Emission (EME) and high Electromagnetic Immunity (EMI)
- Qualified according to AEC-Q100 Grade 1
- VIO input for interfacing with 3.3 V to 5 V microcontrollers
- Listen-only mode for node diagnosis and failure containment
- Available in SO14 and leadless HVSON14 (3.0 mm x 4.5 mm) packages; HVSON14 with improved Automated Optical Inspection (AOI) capability.
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)



## 2.2 Predictable and fail-safe behavior

- Undervoltage detection with defined handling on all supply pins
- Full functionality guaranteed from the undervoltage detection thresholds up to the maximum limiting voltage values
- Defined behavior below the undervoltage detection thresholds
- Transceiver disengages from the bus (high-ohmic) when the battery voltage drops below the Off mode threshold
- Internal biasing of TXD and mode selection input pins, to enable defined fail-safe behavior

## 2.3 Low-power management

- Very low-current Standby and Sleep modes, with host, local and bus wake-up capability
- Entire node with TJA1463 can be powered down while still supporting local, bus and host wake-up
- CAN wake-up receiver powered by  $V_{BAT}$  allowing  $V_{IO}$  and  $V_{CC}$  to be shut down
- CAN wake-up pattern filter time of 0.5  $\mu$ s to 1.8  $\mu$ s, meeting Classical CAN and CAN FD requirements

## 2.4 Diagnosis & Protection

- Overtemperature diagnosis
- Transmit Data (TXD) dominant time-out and TXD-to-RXD short-circuit handler with diagnosis
- Bus dominant failure diagnosis
- Cold start diagnosis (first battery connection)
- High ESD handling capability on the bus pins (6 kV IEC and 8kV HBM)
- Bus pins and VBAT protected against transients in automotive environments
- Thermally protected

### 3 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{BAT}$	battery supply voltage		4.5	-	28	V
$I_{BAT}$	battery supply current	Normal or Listen-only mode	-	80	300	$\mu$ A
		Standby or Sleep mode	-	13	26	$\mu$ A
$V_{uvd(VBAT)}$	undervoltage detection voltage on pin VBAT		4	-	4.5	V
$V_{CC}$	supply voltage		4.5	-	5.5	V
$I_{CC}$	supply current	Normal mode, dominant	-	42	70	mA
		Normal mode, recessive	-	7	10	mA
		Listen-only mode	-	5	8	mA
		Standby or Sleep mode	-	-	2	$\mu$ A
$V_{uvd(VCC)}$	undervoltage detection voltage on pin VCC	$V_{BAT} > 4.5$ V	4	-	4.5	V
$V_{uvhys(VCC)}$	undervoltage hysteresis voltage on pin VCC		50	-	-	mV
$V_{IO}$	supply voltage on pin VIO		2.95	-	5.5	V
$I_{IO}$	supply current on pin VIO	Normal mode, dominant; $V_{TXD} = 0$ V	-	90	250	$\mu$ A
		Normal or Listen-only mode, recessive; $V_{TXD} = V_{IO}$	-	-	3	$\mu$ A
		Standby or Sleep mode	-	-	2	$\mu$ A
$V_{uvd(VIO)}$	undervoltage detection voltage on pin VIO	$V_{BAT} > 4.5$ V	2.65	-	2.95	V
$V_{uvhys(VIO)}$	undervoltage hysteresis voltage on pin VIO		50	-	-	mV
$V_{ESD}$	electrostatic discharge voltage	IEC 61000-4-2 on pins CANH and CANL	-6	-	+6	kV
$V_{CANH}$	voltage on pin CANH	limiting value according to IEC 60134	-36	-	+40	V
$V_{CANL}$	voltage on pin CANL	limiting value according to IEC 60134	-36	-	+40	V
$T_{vj}$	virtual junction temperature		-40	-	+150	$^{\circ}$ C

### 4 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJA1463AT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TJA1463ATK	HVSON14	plastic thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm	SOT1086-2

**Table 3. TJA1463 feature overview**

See [Section 19](#) for a feature overview of the complete TJx144x/TJx146x/TJF1441 family.

Device <sup>[1]</sup>	Modes					Supplies			Data rate		Additional features					
	Normal	Standby	Sleep	Silent/Listen-only	Selectable Off	VCC pin	VIO pin	VBAT pin	Up to 5 Mbit/s CAN FD	Up to 8 Mbit/s CAN FD	Signal improvement <sup>[2]</sup>	Wake-up source recognition <sup>[3]</sup>	Short WUP support [0.5 - 1.8 µs] <sup>[4]</sup>	Single supply pin wake-up <sup>[5]</sup>	TXD dominant timeout	Local diagnostics via ERR_N pin
TJA1463A	•	•	•	•		•	•	•	•	•	•	•	•	•	•	•

[1] TJA1463 is AEC-Q100 Grade 1.  
 [2] CAN FD Signal Improvement Capability (SIC) according to CiA 601-4:2019.  
 [3] RXD is held LOW after wake-up request, enabling wake-up source recognition.  
 [4] WUP = wake-up pattern according ISO11898-2:2016.  
 [5] Only VBAT supply needed for wake-up.

5 Block diagram

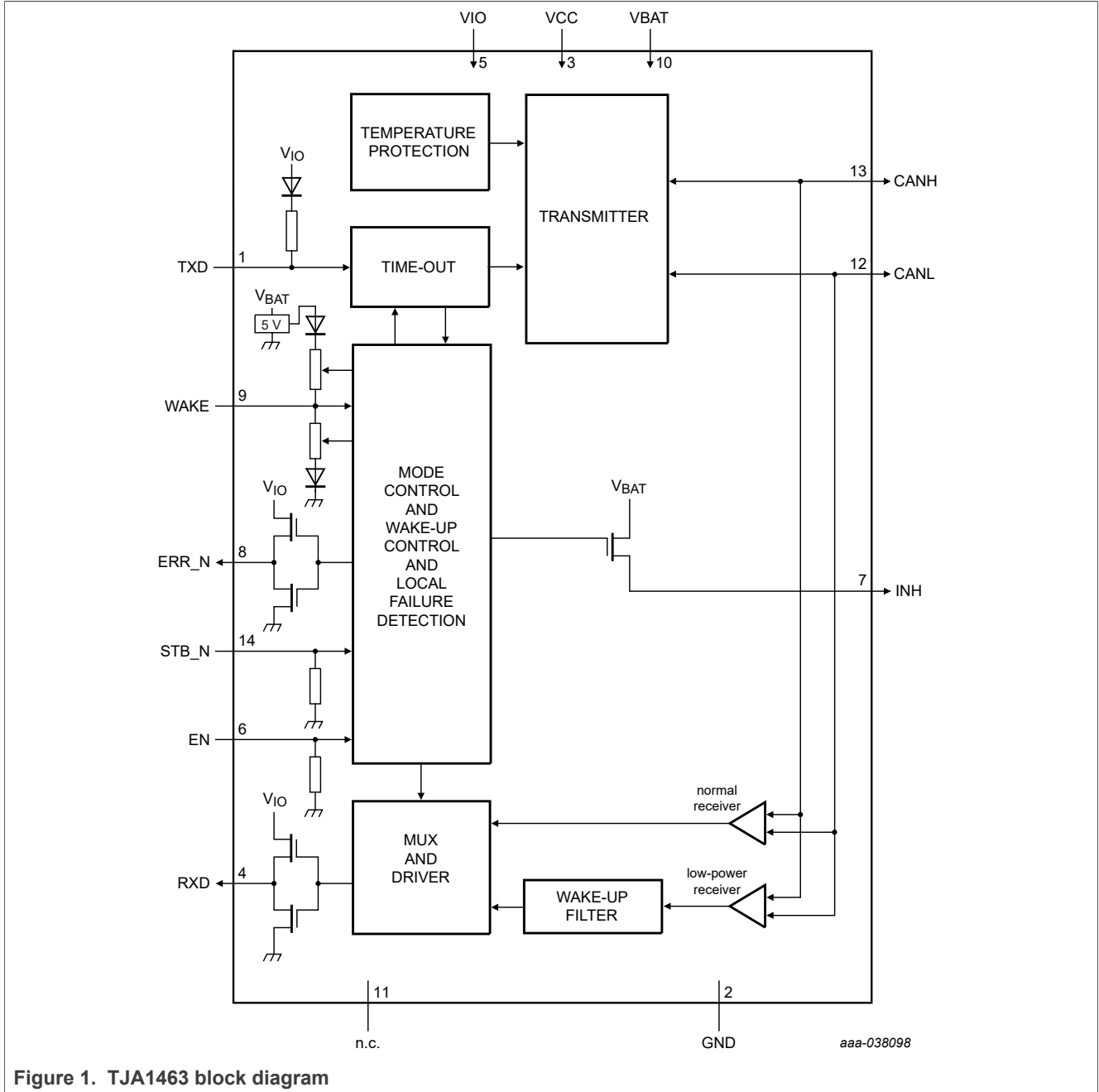
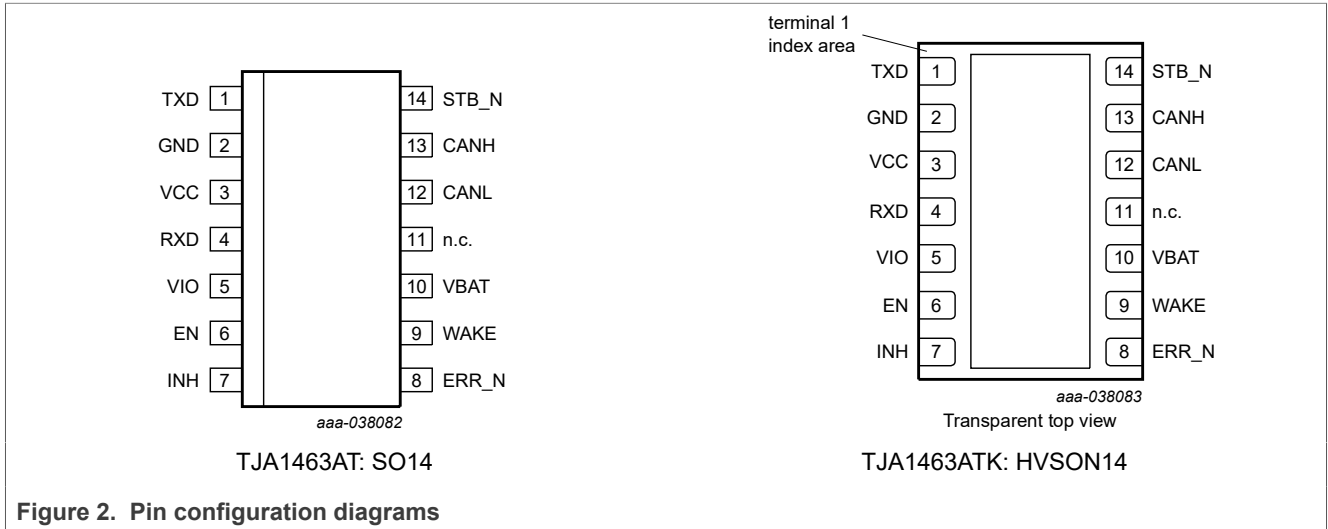


Figure 1. TJA1463 block diagram

## 6 Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 4. Pin description

Symbol	Pin	Type <sup>[1]</sup>	Description
TXD	1	I	transmit data input; inputs data (from the CAN controller) to be written to the bus lines
GND <sup>[2]</sup>	2	G	ground
VCC	3	P	5 V supply voltage input
RXD	4	O	receive data output; outputs data read from the bus lines (to the CAN controller)
VIO	5	P	supply voltage input for I/O level adapter
EN	6	I	enable control input
INH	7	AO	inhibit output for switching external voltage regulators
ERR_N	8	O	local failure detection; wake-up source recognition and power-on indication output (active-LOW)
WAKE	9	AI	local wake-up input
VBAT	10	P	battery supply voltage input
n.c.	11	-	not connected
CANL	12	AIO	LOW-level CAN bus line
CANH	13	AIO	HIGH-level CAN bus line
STB_N	14	I	Standby mode control input (active-LOW)

[1] I: digital input; O: digital output; AI: analog input; AO: analog output; AIO: analog input/output; P: power supply; G: ground.

[2] HVSON14 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is also recommended to solder the exposed center pad to board ground.

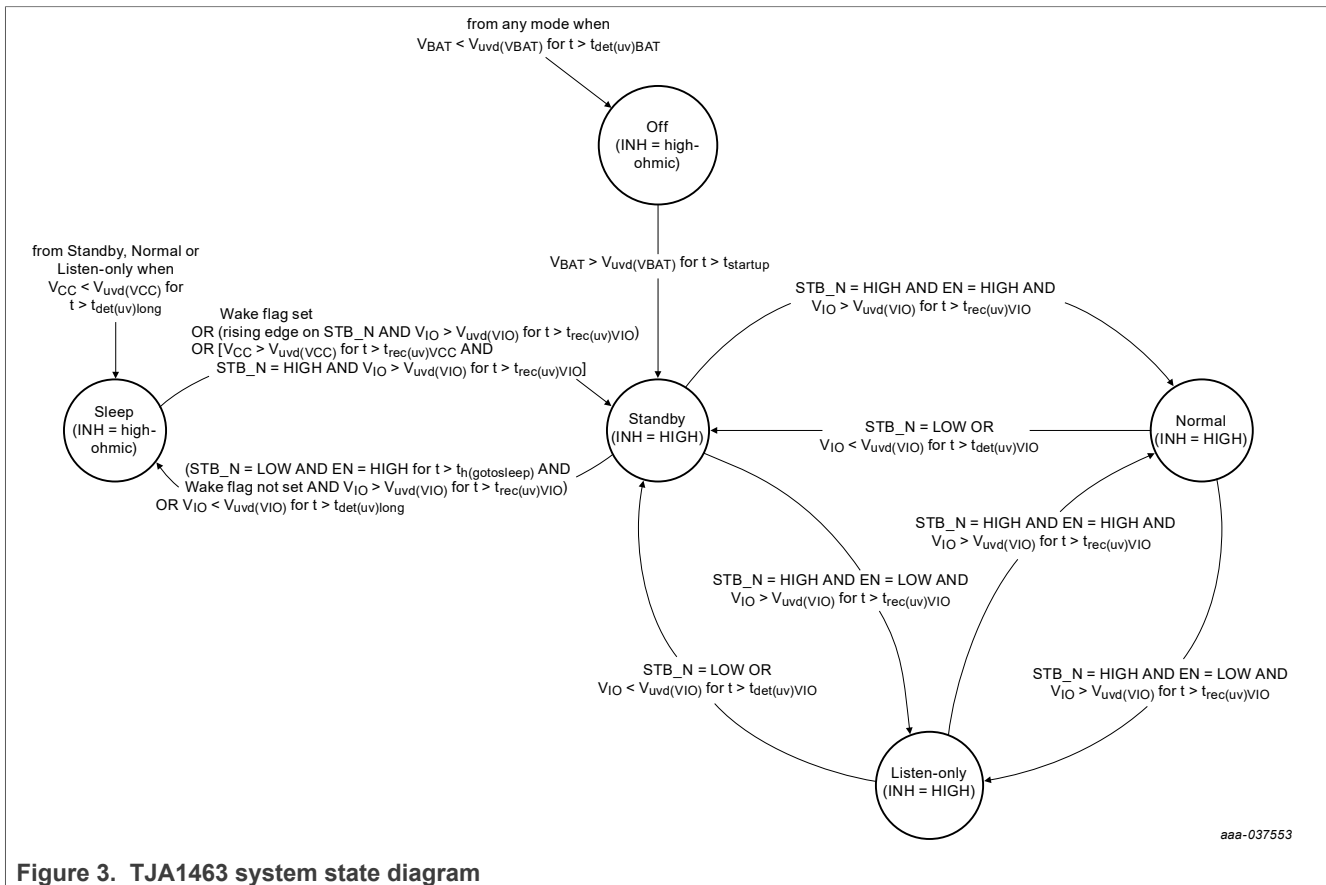
## 7 Functional description

### 7.1 Operating modes

The TJA1463 contains two independent state machines, a system state machine and a CAN state machine. Two state machines are needed to secure flag handling during undervoltage conditions. These state machines support a number of interdependent operating modes. The system state machine controls the CAN state machine, but both state machines are independently affected by the  $V_{CC}$  undervoltage status. For both state machines, undervoltage detection is defined as  $V_x < V_{uvd(x)}$  for  $t > t_{det(uv)}$  and undervoltage recovery is defined as  $V_x > V_{uvd(x)}$  for  $t > t_{rec(uv)}$ .

#### 7.1.1 System operating modes

The system state machine in the TJA1463 supports five system operating modes. Control pins STB\_N and EN are used to select the operating mode. Figure 3 describes how to switch between operating modes. Mode changes are completed after transition time  $t_{(moch)}$ . Fail-safe diagnostic information, as described in Section 7.2, is available on pin ERR\_N with a delay of  $t_{d(moch-ERR\_N)}$  after a mode change.



#### 7.1.1.1 Off mode

The TJA1463 switches to Off mode from any mode mode when the battery voltage falls below the undervoltage detection threshold,  $V_{uvd(VBAT)}$ . The device starts up in Off mode

when the battery is connected for the first time (cold start). Pins INH and ERR\_N are in a high-ohmic state in Off mode.

### 7.1.1.2 Standby mode

Standby mode is the first-level power-saving mode of the TJA1463. When  $V_{BAT}$  rises above the undervoltage detection threshold,  $V_{uvd(VBAT)}$ , the TJA1463 starts to boot up, triggering an initialization procedure. It switches to Standby mode after  $t_{startup}$ , resulting in a HIGH level on pin INH.

When  $V_{IO}$  rises above the undervoltage detection threshold,  $V_{uvd(VIO)}$ , the TJA1463 switches to Normal mode if pins STB\_N and EN are HIGH, and to Listen-only mode if STB\_N is HIGH and EN is LOW. It will remain in Standby mode if STB\_N is LOW.

The TJA1463 will switch to Sleep mode if  $V_{IO}$  remains below  $V_{uvd(VIO)}$  for  $t_{det(uv)long}$  and/or  $V_{CC}$  remains below  $V_{uvd(VCC)}$  for  $t_{det(uv)long}$ . A transition from Standby mode to Sleep mode can also be triggered by holding STB\_N LOW and EN HIGH for  $t_{h(gotosleep)}$  (also known as a 'go-to-sleep' command). This 'go-to-sleep' command is overruled if the Wake flag is set, in which case the device remains in Standby mode.

### 7.1.1.3 Normal mode

HIGH levels on pin STB\_N and pin EN selects Normal mode, provided the battery supply voltage,  $V_{BAT}$ , and  $V_{IO}$  are present. Pin INH remains HIGH, so voltage regulators controlled by pin INH will also be active (see [Figure 12](#)).

### 7.1.1.4 Listen-only mode

A HIGH level on pin STB\_N and a LOW level on pin EN selects Listen-only mode, provided  $V_{BAT}$  and  $V_{IO}$  are present. Pin INH remains HIGH, so voltage regulators controlled by pin INH will also be active.

In Listen-only mode the receiver is enabled, but the transmitter is disabled.

### 7.1.1.5 Sleep mode

Sleep mode is the second-level power-saving mode of the TJA1463. Sleep mode is entered in a number of ways:

- via Standby mode, in response to a 'go-to-sleep' command
- via Standby mode as a result of a  $V_{IO}$  undervoltage longer than  $t_{det(uv)long}$
- via all other modes, except Off mode, as a result of a  $V_{CC}$  undervoltage longer than  $t_{det(uv)long}$

In Sleep mode, the transceiver behaves as described for Standby mode, with the exception that pin INH is set high-ohmic. Voltage regulators controlled by this pin are switched off and the current into pin VBAT is reduced to a minimum.

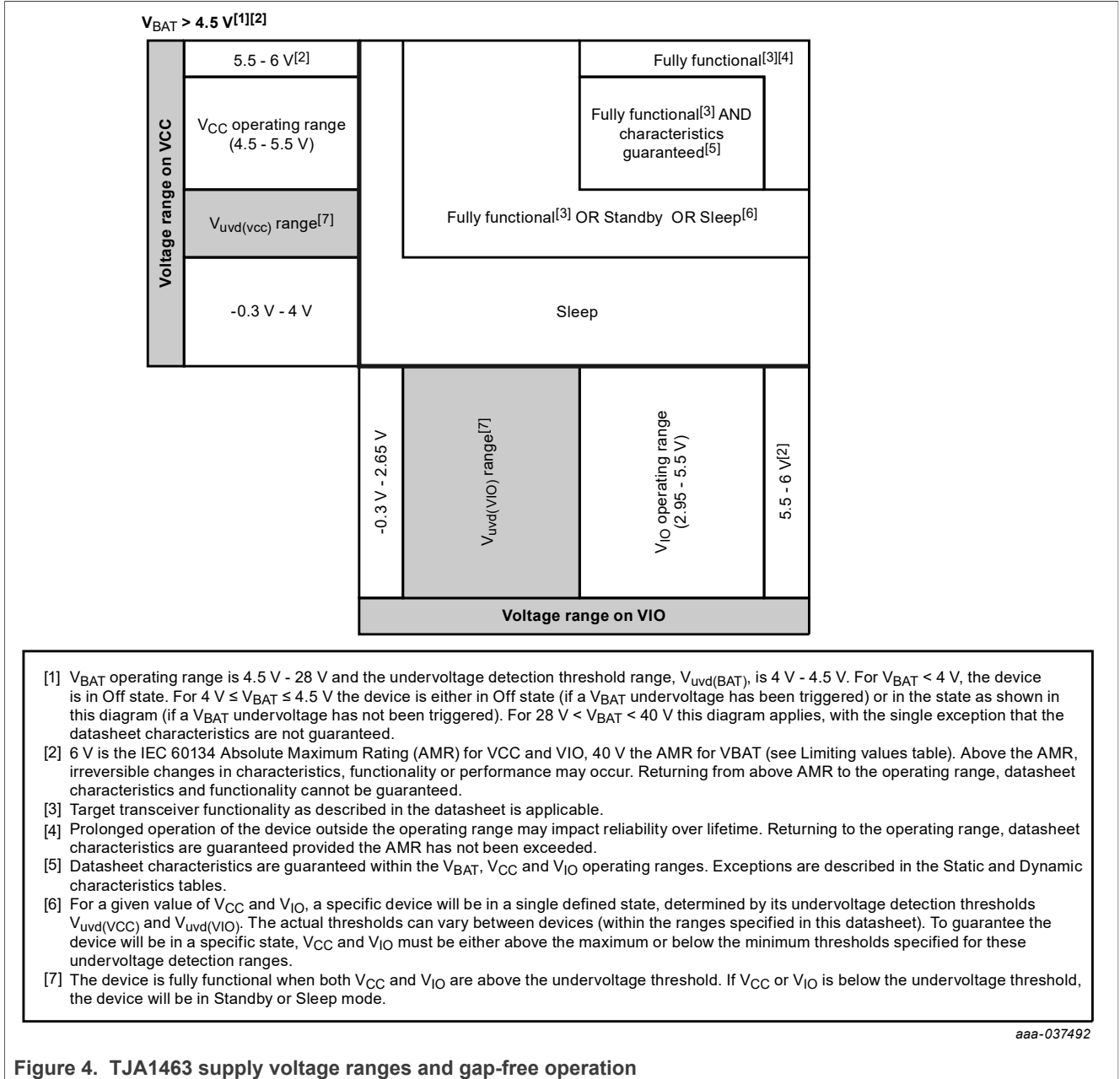
A number of events will cause the TJA1463 to exit Sleep mode, switching to Standby mode:

- setting the Wake flag
- a rising edge on pin STB\_N (if  $V_{IO} > V_{uvd(VIO)}$ )
- $V_{CC} > V_{uvd(VCC)}$ ,  $V_{IO} > V_{uvd(VIO)}$  and the 'go-to-sleep' command has not been activated. After entering Standby mode, the TJA1463 will enter Normal or Listen-Only if STB\_N is HIGH.



7.1.1.6 System operating modes and gap-free operation

Gap-free operation guarantees defined behavior at all voltage levels. Supply voltage-to-operating mode mapping is detailed in [Figure 4](#).



7.1.2 CAN operating modes

The CAN state machine supports six operating modes.

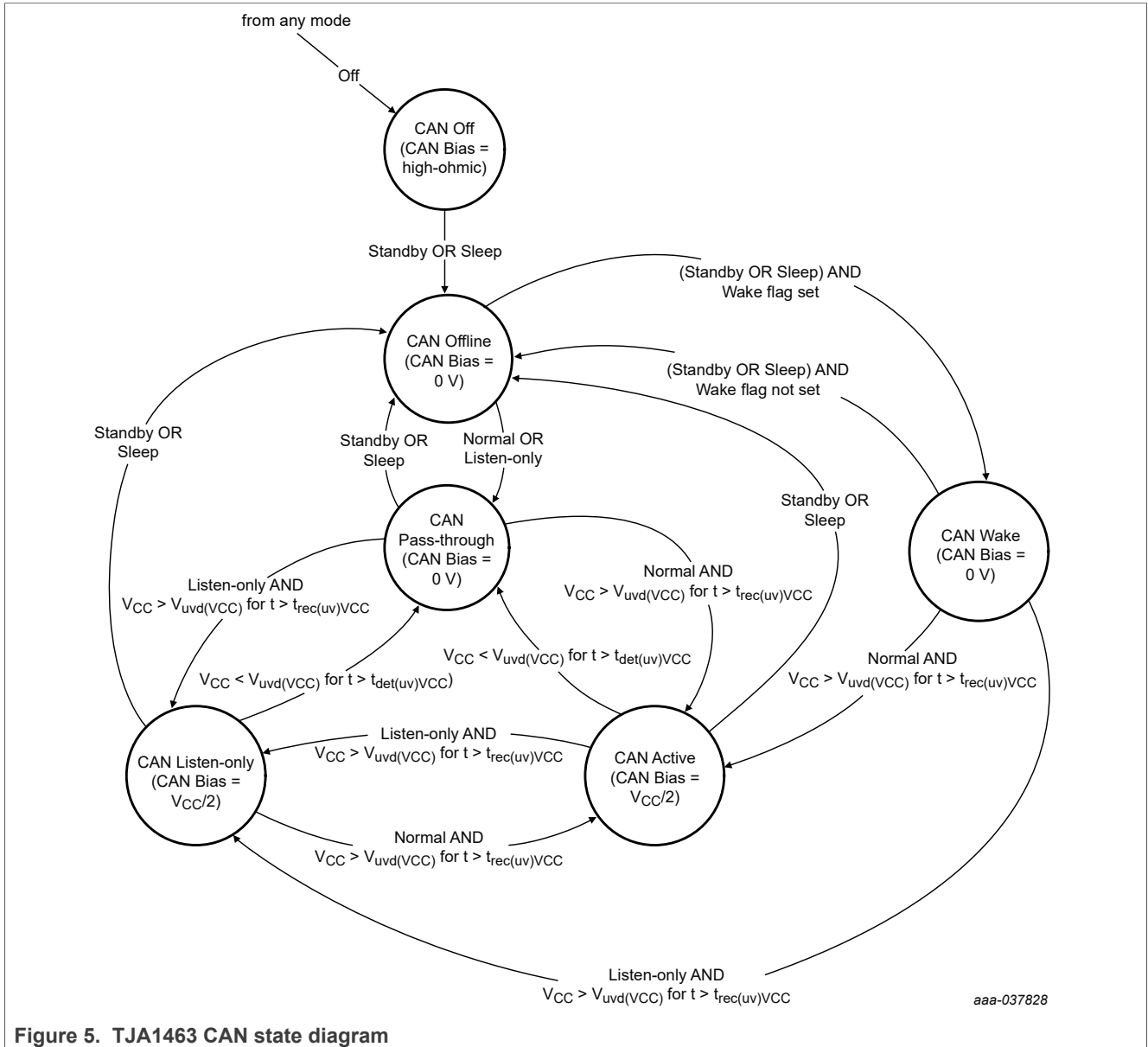


Figure 5. TJA1463 CAN state diagram

7.1.2.1 CAN Off mode

When the TJA1463 system state machine is in Off mode, the CAN state machine will be in CAN Off mode, with the bus pins and pin RXD in a high-ohmic state.

7.1.2.2 CAN Offline mode

When the TJA1463 system state machine is in Sleep or Standby mode and the Wake flag has not been set, the CAN state machine will be in CAN Offline mode. The bus pins are biased to ground.

The transceiver is unable to transmit or receive data and the low-power receiver is activated to monitor the bus for a wake-up pattern. Pin RXD is HIGH.

#### 7.1.2.3 CAN Wake mode

When the TJA1463 system state machine is in Sleep or Standby mode and the wake flag has been set, the CAN state machine will be in CAN Wake mode. Pin RXD will be LOW, reflecting the active wake-up request. The bus pins are biased to ground.

#### 7.1.2.4 CAN Pass-through mode

When the TJA1463 system state machine is in Normal or Listen-only mode and  $V_{CC}$  is below the undervoltage detection threshold,  $V_{uvd(VCC)}$ , the CAN state machine will be in CAN Pass-through mode.

The transceiver cannot transmit data via the bus lines in this mode. The output voltage on the bus pins is biased to ground. Differential data on the bus pins is converted to digital data via the low-power receiver and the results are output on pin RXD.

#### 7.1.2.5 CAN Active mode

When the TJA1463 system state machine is in Normal mode and  $V_{CC}$  is above the undervoltage detection threshold,  $V_{uvd(VCC)}$ , the CAN state machine will be in CAN Active mode. The transceiver can transmit and receive data via bus lines CANH and CANL. Pin TXD must be HIGH at least once in CAN Active mode before the first transmission can begin. The differential receiver converts the analog data on the bus lines into digital data on pin RXD. In order to support high bit rates, especially in CAN FD systems, the Signal Improvement function largely eliminates topology-related reflections and impedance mismatches. In recessive state, the output voltage on the bus pins is  $V_{CC}/2$ .

#### 7.1.2.6 CAN Listen-only mode

When the TJA1463 system state machine is in Listen-only mode and  $V_{CC}$  is above the undervoltage detection threshold,  $V_{uvd(VCC)}$ , the CAN state machine will be in CAN Listen-only mode. The transmitter is disabled. The differential receiver converts the analog data on the bus lines into digital data on pin RXD. As in CAN Active mode, the bus pins are biased to  $V_{CC}/2$ .

## 7.2 Internal flags

The device makes use of four internal flags for fail-safe fallback control and system diagnosis. These flags can be polled by the controller via pin ERR\_N while  $V_{IO}$  is active. Which flag is available on pin ERR\_N at any time depends on the current system operating mode; see [Table 5](#).

**Table 5. Accessing internal flags via pin ERR\_N**

Internal flag	Flag available on pin ERR_N <sup>[1]</sup>	Flag status: set <sup>[2]</sup>	Flag status: not set <sup>[2]</sup>	Flag cleared
Pwon	in Listen-only mode (coming from Standby or Sleep mode)	V <sub>BAT</sub> has risen above V <sub>uvd(VBAT)</sub>	V <sub>BAT</sub> has not risen above V <sub>uvd(VBAT)</sub>	on entering Normal mode
Wake	in Standby and Sleep modes (provided V <sub>IO</sub> and V <sub>BAT</sub> are present)	remote or local wake-up detected OR Pwon flag has been set	no remote or local wake-up detected	on entering Normal mode
Wake-up source	in Normal mode	local wake-up OR Pwon flag has been set	remote wake-up OR no wake-up	on leaving Normal mode
Local failure	in Listen-only mode (coming from Normal mode)	on occurrence of: - TXD dominant failure OR - TXD-RXD short circuit OR - Bus dominant failure OR - Overtemperature	none of the set conditions have been met	when Pwon flag is set or, provided all local failures have been resolved, when: - device enters Normal mode OR - RXD dominant while TXD recessive OR - bus dominant failure resolved AND no other local failure has set the flag

[1] Pin ERR\_N is an active-LOW output; a LOW level indicates a set flag and a HIGH level indicates the flag has not been set.

[2] Status since flag was last cleared.

### 7.2.1 Pwon flag

Pwon is the V<sub>BAT</sub> power-on flag. This flag is set when the voltage on pin VBAT recovers after previously dropping below V<sub>uvd(VBAT)</sub> (usually because the battery was disconnected). The Pwon flag can be used for cold start diagnosis. The Wake and Wake-up source flags are set to ensure consistent system power-up under all supply conditions. Coming from Sleep or Standby and entering Listen-Only mode, a LOW level on pin ERR\_N signals that the Pwon flag has been set. The flag is cleared when the transceiver enters Normal mode.

### 7.2.2 Wake flag

The Wake flag is set when the transceiver detects a local or remote wake-up request.

#### 7.2.2.1 Local wake-up (via WAKE pin)

A local wake-up request is registered when the logic level on pin WAKE changes and the new level remains stable for at least  $t_{wake}$ . The system state machine can set the Wake flag in Standby or Sleep mode. Setting the Wake flag clears the timers. Once set, the Wake flag status is immediately available on pins ERR\_N and RXD (provided V<sub>IO</sub> and V<sub>BAT</sub> are present). This flag is also set at power-on and cleared when the transceiver enters Normal mode.

#### 7.2.2.2 Remote wake-up (via the CAN bus)

The TJA1463 wakes up from Sleep to Standby mode when a dedicated wake-up pattern (specified in ISO 11898-2: 2016) is detected on the bus.

The wake-up pattern consists of:

- a dominant phase of at least  $t_{wake(busdom)}$  followed by
- a recessive phase of at least  $t_{wake(busrec)}$  followed by
- a dominant phase of at least  $t_{wake(busdom)}$

Dominant or recessive bits between the above mentioned phases that are shorter than  $t_{wake(busdom)}$  and  $t_{wake(busrec)}$  respectively are ignored.

The complete dominant-recessive-dominant pattern must be received within  $t_{to(wake)bus}$  to be recognized as a valid wake-up pattern (see [Figure 6](#)). Otherwise, the internal wake-

up logic is reset. The complete wake-up pattern then needs to be retransmitted to trigger a wake-up event. Pins RXD and ERR\_N remain HIGH until the wake-up event has been triggered and then switch LOW after  $t_{startup(RXD)}$ . Pin INH remains floating until the wake-up event has been triggered and then switches HIGH after  $t_{startup(INH)}$ .

A wake-up event is not flagged on RXD if any of the following events occurs while a valid wake-up pattern is being received:

- The device switches to Normal mode
- The complete wake-up pattern was not received within  $t_{to(wake)bus}$
- A  $V_{CC}$  or  $V_{IO}$  undervoltage is detected

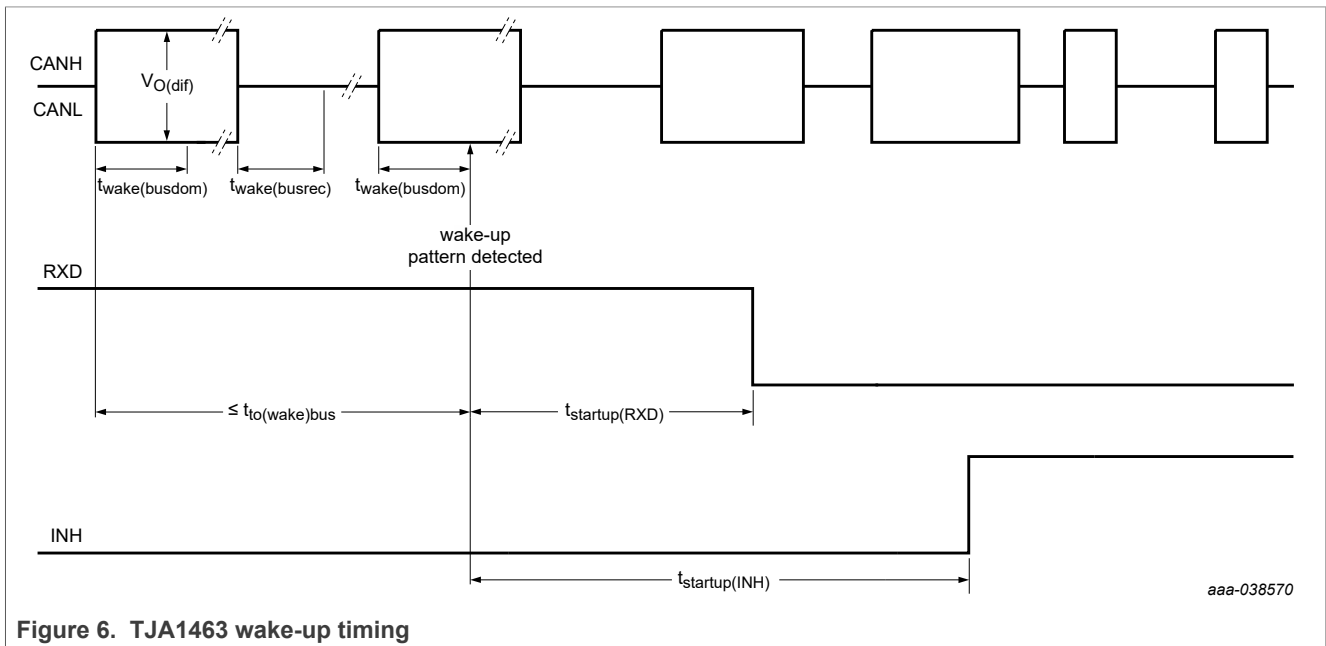


Figure 6. TJA1463 wake-up timing

### 7.2.3 Wake-up source flag

Wake-up source recognition is provided via the Wake-up source flag. It is set after the Wake flag has been set by a local wake-up request via the WAKE pin. The Wake-up source flag can be polled via the ERR\_N pin in Normal mode (see Table 5). This flag is also set at power-on and cleared when the transceiver leaves Normal mode.

### 7.2.4 Local failure flag

In Normal and Listen-only modes, the transceiver can distinguish four local failure events, any of which will cause the Local failure flag to be set. The four local failure events are:

- TXD dominant failures
- TXD-to-RXD short circuit
- Bus dominant failures
- Overtemperature

The nature and detection of these local failures is described in Section 7.3. The Local failure flag can be polled via the ERR\_N pin in Listen-only mode, when coming from Normal mode (see Table 5).

This flag is cleared at power-on when the Pwon flag is set or, provided all local failures have been resolved, when:

- The device enters Normal mode OR
- RXD is dominant while TXD is recessive OR
- Bus dominant failure has been resolved AND no other local failure has set the flag

### 7.3 Local failure events

The TJA1463 can detect four different local failure conditions, any of which will set the Local failure flag. In most cases, the transmitter is disabled.

#### 7.3.1 TXD dominant failures

A hardware and/or software application failure that caused pin TXD to be held LOW would drive the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out function prevents such a network lock-up. A 'TXD dominant time-out' timer is started when pin TXD goes LOW. If the LOW state on this pin persists for longer than  $t_{to(dom)TXD}$ , the transmitter is disabled, releasing the bus lines to recessive state. The transmitter remains disabled until the Local failure flag has been cleared. The TXD dominant time-out timer is reset when pin TXD is set HIGH.

#### 7.3.2 TXD-to-RXD short circuit

A short-circuit between pins RXD and TXD would lock the bus in a permanent dominant state once it had been driven dominant, because the low-side driver of RXD is typically stronger than the high-side driver of the controller connected to TXD. TXD-to-RXD short-circuit detection prevents such a network lock-up by disabling the transmitter. The transmitter remains disabled until the Local failure flag has been cleared.

#### 7.3.3 Bus dominant failures

A CAN bus short circuit (to  $V_{BAT}$ ,  $V_{CC}$  or GND) or a failure in one of the other network nodes could result in a differential voltage on the bus high enough to represent a bus dominant state. Because a node will not begin to transmit while the bus is dominant, the host controller would not be able to detect this failure condition. However, bus dominant clamping detection will detect the short circuit. The Local failure flag is set if the dominant state on the bus persists for longer than  $t_{to(dom)bus}$ . By checking this flag, the controller can determine if a clamped bus is blocking network communications. There is no need to disable the transmitter. Note that the Local failure flag is reset as soon as the bus returns to recessive state.

#### 7.3.4 Overtemperature

The device is protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature,  $T_{j(sd)}$ , the CAN bus drivers are disabled. The transmitter will remain disabled until the junction temperature drops below  $T_{j(sd)rel}$  and the Local failure flag has been cleared.

### 7.4 I/O levels

Pin VIO should be connected to the same supply voltage used to supply the microcontroller. This adjusts the signal levels on pins TXD, RXD, STB\_N, EN and

ERR\_N to the I/O levels of the microcontroller, allowing for direct interfacing without additional glue logic. Spurious signals from the microcontroller on pins STB\_N and EN are filtered out with a filter time of  $t_{\text{fltr(I/O)}}$ .

## 7.5 WAKE pin

A local wake-up event is triggered by a LOW-to-HIGH or HIGH-to-LOW transition on the WAKE pin when  $V_{\text{WAKE}}$  passes the wake-up threshold,  $V_{\text{th(wake)}}$ . After the transition, the new HIGH or LOW level should remain stable for at least  $t_{\text{wake}}$ . This allows for maximum flexibility when designing a local wake-up circuit.

A local wake-up is guaranteed in the case of:

- a LOW-to-HIGH transition from  $V_{\text{WAKE}} < V_{\text{th(wake)min}}$  to  $V_{\text{WAKE}} > V_{\text{th(wake)max}}$ , followed by  $V_{\text{WAKE}} > V_{\text{th(wake)max}}$  for  $t > t_{\text{wake(max)}}$
- a HIGH-to-LOW transition from  $V_{\text{WAKE}} > V_{\text{th(wake)max}}$  to  $V_{\text{WAKE}} < V_{\text{th(wake)min}}$ , followed by  $V_{\text{WAKE}} < V_{\text{th(wake)min}}$  for  $t > t_{\text{wake(max)}}$

A local wake-up is guaranteed not to occur if the HIGH/LOW level after the transition does not remain stable for at least  $t_{\text{(wake)min}}$ .

To minimize current consumption, the internal bias voltage follows the logic state on the pin after a delay of  $t_{\text{wake}}$ . A HIGH level on pin WAKE is followed by an internal pull-up to  $V_{\text{BAT}}$ . A LOW level on pin WAKE is followed by an internal pull-down towards GND. In applications that do not make use of the local wake-up facility, it is recommended to connect the WAKE pin to pin VBAT or GND for optimal EMI performance.

## 7.6 Internal biasing of TXD, STB\_N and EN input pins

Pin TXD has an internal pull-up to  $V_{\text{IO}}$  and pins STB\_N and EN have internal pull-downs to GND to ensure a safe, defined state in case one, or all, of these pins is left floating. Pull-up/pull-down resistors are present on these pins in all states. Pull-down on pin EN is only active when  $V_{\text{BAT}}$  is present.

## 8 Limiting values

**Table 6. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to pin GND, unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>x</sub>	Voltage on pin x <sup>[1]</sup>	pins VCC, VIO, TXD, STB_N, EN	-0.3	+6	V
			-	+7 <sup>[2]</sup>	V
		pin VBAT, load dump	-0.3	+40 <sup>[3]</sup>	V
		pin INH	-0.3	V <sub>BAT</sub> +0.3 <sup>[4]</sup>	V
		pins CANH, CANL, WAKE	-36	+40	V
		pins RXD, ERR_N	-0.3	V <sub>IO</sub> +0.3 <sup>[5]</sup>	V
I <sub>O(INH)</sub>	output current on pin INH		-2	-	mA
V <sub>(CANH-CANL)</sub>	voltage between pin CANH and pin CANL		-40	+40	V
V <sub>trt</sub>	transient voltage	on pins VBAT, WAKE, CANH, CANL <sup>[6]</sup>			
		pulse 1	-100	-	V
		pulse 2a	-	+75	V
		pulse 3a	-150	-	V
		pulse 3b	-	+100	V
V <sub>ESD</sub>	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω discharge circuit) <sup>[7]</sup>			
		on pins CANH, CANL	-6	+6	kV
		on pin VBAT with 100 nF capacitor; pin WAKE with 33 kΩ resistor	-8	+8	kV
		Human Body Model (HBM)			
		on any pin <sup>[8]</sup>	-4	+4	kV
		on pins CANH, CANL <sup>[9]</sup>	-8	+8	kV
		Charged Device Model (CDM) <sup>[10]</sup>			
		on corner pins	-750	+750	V
on any other pin	-500	+500	V		
T <sub>vj</sub>	virtual junction temperature	<sup>[11]</sup>	-40	+150	°C
T <sub>stg</sub>	storage temperature	<sup>[12]</sup>	-55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

[2] The device can withstand voltages between 6 V and 7 V for a total of 20 s over the product lifetime.

[3] For a maximum of 50 hours over the product lifetime.

[4] Absolute maximum of 40 V under the conditions defined in Table note 3 above.

[5] Subject to the qualifications detailed in Table notes 1 and 2 above for pins VCC, VIO, TXD, STB\_N and EN.

[6] Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO 7637, Part 2.

[7] Verified by an external test house according to IEC TS 62228, Section 4.3.

[8] According to AEC-Q100-002.

[9] Pins stressed to reference group containing all ground and supply pins, emulating the application circuit (Figure 12). HBM pulse as specified in AEC-Q100-002 used.

[10] According to AEC-Q100-011.

[11] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is:  $T_{vj} = T_{amb} + P \times R_{th(j-a)}$ , where  $R_{th(j-a)}$  is a fixed value used in the calculation of  $T_{vj}$ . The rating for  $T_{vj}$  limits the allowable combinations of power dissipation (P) and ambient temperature ( $T_{amb}$ ).

[12]  $T_{stg}$  in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.



## 9 Thermal characteristics

**Table 7. Thermal characteristics**

Value determined for free convection conditions on a JEDEC 2S2P board.

Symbol	Parameter	Conditions <sup>[1]</sup>	Typ	Unit
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	SO14	74	K/W
		HVSON14	46	K/W
R <sub>th(j-c)</sub>	thermal resistance from junction to case <sup>[2]</sup>	HVSON14	13	K/W
Ψ <sub>j-top</sub>	thermal characterization parameter from junction to top of package	SO14	13	K/W
		HVSON14	7	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 μm).

[2] Case temperature refers to the center of the heatsink at the bottom of the package.

## 10 Static characteristics

**Table 8. Static characteristics**

T<sub>vj</sub> = -40 °C to +150 °C; V<sub>CC</sub> = 4.5 V to 5.5 V; V<sub>IO</sub> = 2.95 V to 5.5 V; V<sub>BAT</sub> = 4.5 V to 28 V; R<sub>I</sub> = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.<sup>[1]</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin VCC						
V <sub>CC</sub>	supply voltage		4.5	-	5.5	V
V <sub>uvd</sub>	undervoltage detection voltage	<sup>[2]</sup>	4	-	4.5	V
V <sub>uvhys</sub>	undervoltage hysteresis voltage		50	-	-	mV
I <sub>CC</sub>	supply current	Normal mode				
		dominant; V <sub>TXD</sub> = 0 V; t < t <sub>to(dom)TXD</sub>	-	42	70	mA
		dominant; V <sub>TXD</sub> = 0 V; short circuit on bus lines; -3 V < (V <sub>CANH</sub> = V <sub>CANL</sub> ) < +40 V	-	-	125	mA
		Normal mode, recessive; V <sub>TXD</sub> = V <sub>IO</sub>	-	7	10	mA
		Listen-only mode	-	5	8	mA
		Standby or Sleep mode; T <sub>vj</sub> < 85 °C	-	-	2	μA
I/O level adapter supply; pin VIO						
V <sub>IO</sub>	supply voltage		2.95	-	5.5	V
V <sub>uvd</sub>	undervoltage detection voltage	<sup>[2]</sup>	2.65	-	2.95	V
V <sub>uvhys</sub>	undervoltage hysteresis voltage		50	-	-	mV
I <sub>IO</sub>	supply current	Normal mode, dominant; V <sub>TXD</sub> = 0 V	-	90	250	μA
		Normal mode, recessive, V <sub>TXD</sub> = V <sub>IO</sub> or Listen-only mode	-	-	3	μA

## CAN FD signal improvement transceiver with Sleep mode

Table 8. Static characteristics...continued

$T_{vj} = -40\text{ °C to }+150\text{ °C}$ ;  $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{IO} = 2.95\text{ V to }5.5\text{ V}$ ;  $V_{BAT} = 4.5\text{ V to }28\text{ V}$ ;  $R_L = 60\ \Omega$  unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.<sup>[1]</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Standby or Sleep mode; $T_{vj} < 85\text{ °C}$	-	-	2	$\mu\text{A}$
Supply; pin VBAT						
$V_{BAT}$	battery supply voltage		4.5	-	28	V
$V_{uvd}$	undervoltage detection voltage	<sup>[2]</sup>	4	-	4.5	V
$I_{BAT}$	battery supply current	Normal or Listen-only mode; pin INH left open	-	80	300	$\mu\text{A}$
		Normal or Listen-only mode; pin INH left open; $T_{vj} \leq 25\text{ °C}$ ; $V_{BAT} = 14.5\text{ V}$	-	80	100	$\mu\text{A}$
		Standby mode; pin INH left open; $V_{WAKE} = V_{BAT}$ ; $T_{vj} < 85\text{ °C}$	-	13	26	$\mu\text{A}$
		Sleep mode; $V_{WAKE} = V_{BAT}$ ; $T_{vj} < 85\text{ °C}$	-	13	26	$\mu\text{A}$
CAN transmit data input; pin TXD						
$V_{IH}$	HIGH-level input voltage		$0.7V_{IO}$	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	$0.3V_{IO}$	V
$V_{hys(TXD)}$	hysteresis voltage on pin TXD		50	-	-	mV
$R_{pu}$	pull-up resistance		20	-	80	k $\Omega$
$C_i$	input capacitance	<sup>[3]</sup>	-	-	10	pF
CAN receive data output; pin RXD						
$I_{OH}$	HIGH-level output current	$V_{RXD} = V_{IO} - 0.4\text{ V}$	-10	-	-1	mA
$I_{OL}$	LOW-level output current	$V_{RXD} = 0.4\text{ V}$	1	-	10	mA
Standby and enable control inputs; pins STB_N and EN						
$V_{IH}$	HIGH-level input voltage		$0.7V_{IO}$	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	$0.3V_{IO}$	V
$V_{hys}$	hysteresis voltage		50	-	-	mV
$R_{pd}$	pull-down resistance		<sup>[4]</sup> 20	-	80	k $\Omega$
$C_i$	input capacitance	<sup>[3]</sup>	-	-	10	pF
Local failure detection and power-on indication output; pin ERR_N						
$I_{OH}$	HIGH-level output current	$V_{ERR\_N} = V_{IO} - 0.4\text{ V}$	-50	-	-4	$\mu\text{A}$
$I_{OL}$	LOW-level output current	$V_{ERR\_N} = 0.4\text{ V}$	0.1	-	2	mA
Local wake-up input; pin WAKE						
$R_{pu}$	pull-up resistance	$V_{WAKE} > V_{th(wake)(max)}$ for $t > t_{wake(max)}$	100	-	400	k $\Omega$
$R_{pd}$	pull-down resistance	$V_{WAKE} < V_{th(wake)(min)}$ for $t > t_{wake(max)}$	100	-	400	k $\Omega$
$V_{th(wake)}$	wake-up threshold voltage	Sleep or Standby mode	1.8	-	2.6	V
$V_{hys}$	hysteresis voltage		90	-	-	mV

CAN FD signal improvement transceiver with Sleep mode

Table 8. Static characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$  to  $+150\text{ }^{\circ}\text{C}$ ;  $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$ ;  $V_{IO} = 2.95\text{ V}$  to  $5.5\text{ V}$ ;  $V_{BAT} = 4.5\text{ V}$  to  $28\text{ V}$ ;  $R_L = 60\text{ }\Omega$  unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.<sup>[7]</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Inhibit output; pin INH						
$\Delta V_H$	HIGH-level voltage drop	$\Delta V_H = V_{BAT} - V_{INH}$ ; $I_{INH} = -1\text{ mA}$	0	-	1	V
		$\Delta V_H = V_{BAT} - V_{INH}$ ; $I_{INH} = -2\text{ mA}$	0	-	2	V
$I_L$	leakage current	Sleep mode; Off mode	-2	-	+2	$\mu\text{A}$
$I_{O(sc)}$	short-circuit output current	$V_{INH} = 0\text{ V}$	-15	-	-	mA
Bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	$V_{TXD} = 0\text{ V}$ ; $t < t_{to(dom)TXD}$ ; $V_{CC} = 4.75\text{ V}$ to $5.25\text{ V}$				
		pin CANH; $R_L = 50\text{ }\Omega$ to $65\text{ }\Omega$	2.89	3.5	4.26	V
		pin CANL; $R_L = 50\text{ }\Omega$ to $65\text{ }\Omega$	0.77	1.5	2.13	V
$V_{TXsym}$	transmitter voltage symmetry	$V_{TXsym} = V_{CANH} + V_{CANL}$ ; $C_{SPLIT} = 4.7\text{ nF}$ ; $f_{TXD} = 250\text{ kHz}$ , $1\text{ MHz}$ or $2.5\text{ MHz}$	<sup>[3]</sup> <sup>[5]</sup> $0.9V_{CC}$	-	$1.1V_{CC}$	V
$V_{cm(step)}$	common mode voltage step		<sup>[3]</sup> <sup>[5]</sup> <sup>[6]</sup> -150	-	+150	mV
$V_{cm(p-p)}$	peak-to-peak common mode voltage		<sup>[3]</sup> <sup>[5]</sup> <sup>[6]</sup> -300	-	+300	mV
$V_{O(dif)}$	differential output voltage	dominant; Normal mode; $V_{TXD} = 0\text{ V}$ ; $t < t_{to(dom)TXD}$ ; $V_{CC} = 4.75\text{ V}$ to $5.25\text{ V}$	<sup>[5]</sup>			
		$R_L = 50\text{ }\Omega$ to $65\text{ }\Omega$	1.5	-	2.75	V
		$R_L = 45\text{ }\Omega$ to $70\text{ }\Omega$	1.4	-	3.3	V
		$R_L = 2240\text{ }\Omega$	<sup>[3]</sup> 1.5	-	5	V
		recessive; no load				
		Normal or Listen-only mode; $V_{TXD} = V_{IO}$	-50	-	+50	mV
$V_{O(rec)}$	recessive output voltage	Normal or Listen-only mode; $V_{TXD} = V_{IO}$ ; no load	2	2.5	3	V
		Standby or Sleep mode; no load	-0.1	0	+0.1	V
$V_{th(RX)dif}$	differential receiver threshold voltage	$-12\text{ V} \leq V_{CANH} \leq +12\text{ V}$ ; $-12\text{ V} \leq V_{CANL} \leq +12\text{ V}$				
		Normal or Listen-only mode	0.5	-	0.9	V
		Standby or Sleep mode	0.4	-	1.1	V
$V_{rec(RX)}$	receiver recessive voltage	$-12\text{ V} \leq V_{CANH} \leq +12\text{ V}$ ; $-12\text{ V} \leq V_{CANL} \leq +12\text{ V}$				
		Normal or Listen-only mode	-4	-	+0.5	V
		Standby or Sleep mode	-4	-	+0.4	V
$V_{dom(RX)}$	receiver dominant voltage	$-12\text{ V} \leq V_{CANH} \leq +12\text{ V}$ ; $-12\text{ V} \leq V_{CANL} \leq +12\text{ V}$				

CAN FD signal improvement transceiver with Sleep mode

Table 8. Static characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$  to  $+150\text{ }^{\circ}\text{C}$ ;  $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$ ;  $V_{IO} = 2.95\text{ V}$  to  $5.5\text{ V}$ ;  $V_{BAT} = 4.5\text{ V}$  to  $28\text{ V}$ ;  $R_i = 60\text{ }\Omega$  unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.<sup>[7]</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Normal or Listen-only mode	0.9	-	9	V
		Standby or Sleep mode	1.1	-	9	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	$-12\text{ V} \leq V_{CANH} \leq +12\text{ V}$ ; $-12\text{ V} \leq V_{CANL} \leq +12\text{ V}$ ; Normal or Listen-only mode	100	-	-	mV
$I_{O(sc)}$	short-circuit output current	$-15\text{ V} \leq V_{CANH} \leq +40\text{ V}$ ; $-15\text{ V} \leq V_{CANL} \leq +40\text{ V}$	-	-	115	mA
$I_{O(sc)rec}$	recessive short-circuit output current	$-27\text{ V} \leq V_{CANH} \leq +32\text{ V}$ ; $-27\text{ V} \leq V_{CANL} \leq +32\text{ V}$ ; Normal or Listen-only mode; $V_{TXD} = V_{IO}$ for $t > t_{d(TXD-busrec)end}$ <sup>[7]</sup>	-3	-	+3	mA
$I_L$	leakage current	$V_{CC} = V_{IO} = 0\text{ V}$ or pins shorted to GND via $47\text{ k}\Omega$ ; $V_{CANH} = V_{CANL} = 5\text{ V}$ ;	-10	-	+10	$\mu\text{A}$
$R_i$	input resistance	$-2\text{ V} \leq V_{CANL} \leq +7\text{ V}$ ; $-2\text{ V} \leq V_{CANH} \leq +7\text{ V}$	25	40	50	k $\Omega$
$\Delta R_i$	input resistance deviation	$0\text{ V} \leq V_{CANL} \leq +5\text{ V}$ ; $0\text{ V} \leq V_{CANH} \leq +5\text{ V}$	-3	-	+3	%
$R_{i(dif)}$	differential input resistance	$-2\text{ V} \leq V_{CANL} \leq +7\text{ V}$ ; $-2\text{ V} \leq V_{CANH} \leq +7\text{ V}$	50	80	100	k $\Omega$
$C_{i(cm)}$	common-mode input capacitance	<sup>[3]</sup>	-	-	30	pF
$C_{i(dif)}$	differential input capacitance	<sup>[3]</sup>	-	-	15	pF
Signal Improvement function on CANH or CANL; $+4.75\text{ V} \leq V_{CC} \leq +5.25\text{ V}$ ; see <a href="#">Figure 10</a> and <a href="#">Figure 11</a>						
$R_{i(dom)}$	dominant phase input resistance	bus dominant; $V_{CC} - 1.6\text{ V} \leq V_{CANH} \leq V_{CC} - 1.2\text{ V}$ ; $+1.2\text{ V} \leq V_{CANL} \leq +1.6\text{ V}$ ;	-	-	30	$\Omega$
$R_{i(dif)dom}$	dominant phase differential input resistance	$R_{i(dif)dom} = R_{i(dom)CANH} + R_{i(dom)CANL}$	-	-	60	$\Omega$
$R_{i(extdom)}$	extended dominant phase input resistance <sup>[8]</sup>	bus dominant-to-recessive transition; $+2.3\text{ V} \leq V_{CANH} \leq V_{CC} - 2.3\text{ V}$ ; $+2.3\text{ V} \leq V_{CANL} \leq V_{CC} - 2.3\text{ V}$ ;	-	-	25	$\Omega$
$R_{i(dif)extdom}$	extended dominant phase differential input resistance <sup>[8]</sup>	$R_{i(dif)extdom} = R_{i(extdom)CANH} + R_{i(extdom)CANL}$	-	-	50	$\Omega$
$R_{i(actrec)}$	active recessive phase input resistance <sup>[8]</sup>	bus dominant-to-recessive transition; $+1.5\text{ V} \leq V_{CANH} \leq V_{CC} - 1.5\text{ V}$ ; $+1.5\text{ V} \leq V_{CANL} \leq V_{CC} - 1.5\text{ V}$ ;	37.5	-	62.5	$\Omega$
$R_{i(dif)actrec}$	active recessive phase differential input resistance <sup>[8]</sup>	$R_{i(dif)actrec} = R_{i(actrec)CANH} + R_{i(actrec)CANL}$	75	-	125	$\Omega$
Temperature detection						
$T_{j(sd)}$	shutdown junction temperature	<sup>[3]</sup>	180	-	200	$^{\circ}\text{C}$
$T_{j(sd)rel}$	release shutdown junction temperature	<sup>[3]</sup>	175	-	195	$^{\circ}\text{C}$

[1] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.  
 [2] Undervoltage is detected between min and max values. Undervoltage is guaranteed to be detected below min value and guaranteed not to be detected above max value.  
 [3] Not tested in production; guaranteed by design.  
 [4] Pull-down on EN pin is only active when  $V_{BAT}$  is present.

- [5] The test circuit used to measure the bus output voltage symmetry and the common-mode voltages (which includes C<sub>SPLIT</sub>) is shown in [Figure 14](#).
- [6] See [Figure 9](#).
- [7] This parameter is defined in CiA specification CiA 601-4:2019 as  $t_{\text{SIC\_TX\_base}}$  and is specified in the Dynamic Characteristics table (see [Table 9](#) and [Figure 10](#)).
- [8] Extended dominant and active recessive phases are not DC states and are only valid for a limited time after a dominant-to-recessive transition on pin TXD.

## 11 Dynamic characteristics

**Table 9. Dynamic characteristics**

$T_{vj} = -40\text{ °C to }+150\text{ °C}$ ;  $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{IO} = 2.95\text{ V to }5.5\text{ V}$ ;  $V_{BAT} = 4.5\text{ V to }28\text{ V}$ ;  $R_L = 60\ \Omega$  unless specified otherwise; all voltages are defined with respect to ground.<sup>[1]</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN timing characteristics; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$ ; $t_{\text{bit(TXD)}} \geq 125\text{ ns}$ ; see <a href="#">Figure 7</a> , <a href="#">Figure 8</a> , <a href="#">Figure 10</a> , <a href="#">Figure 11</a> and <a href="#">Figure 13</a>						
$t_{\text{d(TXD-busdom)}}$	delay time from TXD to bus dominant	Normal mode	-	-	80	ns
$t_{\text{d(TXD-busrec)}}$	delay time from TXD to bus recessive	Normal mode	-	-	80	ns
$t_{\text{d(busdom-RXD)}}$	delay time from bus dominant to RXD	Normal or Listen-Only mode	-	-	110	ns
$t_{\text{d(busrec-RXD)}}$	delay time from bus recessive to RXD	Normal or Listen-Only mode	-	-	110	ns
$t_{\text{d(TXDL-RXDL)}}$	delay time from TXD LOW to RXD LOW	Normal mode	-	-	190	ns
		Normal mode; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	255	ns
$t_{\text{d(TXDH-RXDH)}}$	delay time from TXD HIGH to RXD HIGH	Normal mode	-	-	190	ns
		Normal mode; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	255	ns
$t_{\text{d(TXD-busrec)end}}$	delay time from TXD to bus recessive end	Normal mode	<sup>[2]</sup> <sup>[3]</sup> 415	-	530	ns
$t_{\text{d(TXD-busdom)end}}$	delay time from TXD to bus dominant end	Normal mode	<sup>[2]</sup> -	-	115	ns
$t_{\text{d(TXD-extbusdom)end}}$	delay time from TXD to extended bus dominant end	Normal mode	<sup>[2]</sup> 55	-	-	ns
$t_{\text{d(TXD-busactrec)start}}$	delay time from TXD to bus active recessive start	Normal mode	<sup>[2]</sup> 70	-	120	ns
$t_{\text{d(TXD-busactrec)end}}$	delay time from TXD to active recessive end	Normal mode	<sup>[2]</sup> 335	-	480	ns
CAN FD timing characteristics according to CiA 601-4:2019; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$ ; $t_{\text{bit(TXD)}} \geq 125\text{ ns}$ ; see <a href="#">Figure 8</a> and <a href="#">Figure 13</a> <sup>[4]</sup>						
$\Delta t_{\text{bit(bus)}}$	transmitted recessive bit width deviation	$\Delta t_{\text{bit(bus)}} = t_{\text{bit(bus)}} - t_{\text{bit(TXD)}}$	-10	-	+10	ns
$\Delta t_{\text{rec}}$	receiver timing symmetry	$\Delta t_{\text{rec}} = t_{\text{bit(RXD)}} - t_{\text{bit(bus)}}$	-20	-	+15	ns
$\Delta t_{\text{bit(RXD)}}$	received recessive bit width deviation	$\Delta t_{\text{bit(RXD)}} = t_{\text{bit(RXD)}} - t_{\text{bit(TXD)}}$	-30	-	+20	ns
CAN FD timing characteristics according to ISO 11898-2:2016 <sup>[5]</sup> ; see <a href="#">Figure 8</a> and <a href="#">Figure 13</a> <sup>[4]</sup>						
$t_{\text{bit(bus)}}^{[6]}$	transmitted recessive bit width	2 Mbit/s ( $t_{\text{bit(TXD)}} = 500\text{ ns}$ )				
		$V_{CC} = 4.75\text{ V to }5.25\text{ V}$	490	-	510	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	435	-	530	ns
		5 Mbit/s ( $t_{\text{bit(TXD)}} = 200\text{ ns}$ )				

CAN FD signal improvement transceiver with Sleep mode

Table 9. Dynamic characteristics...continued

$T_{vj} = -40\text{ °C to }+150\text{ °C}$ ;  $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ;  $V_{IO} = 2.95\text{ V to }5.5\text{ V}$ ;  $V_{BAT} = 4.5\text{ V to }28\text{ V}$ ;  $R_L = 60\ \Omega$  unless specified otherwise; all voltages are defined with respect to ground.<sup>[1]</sup>

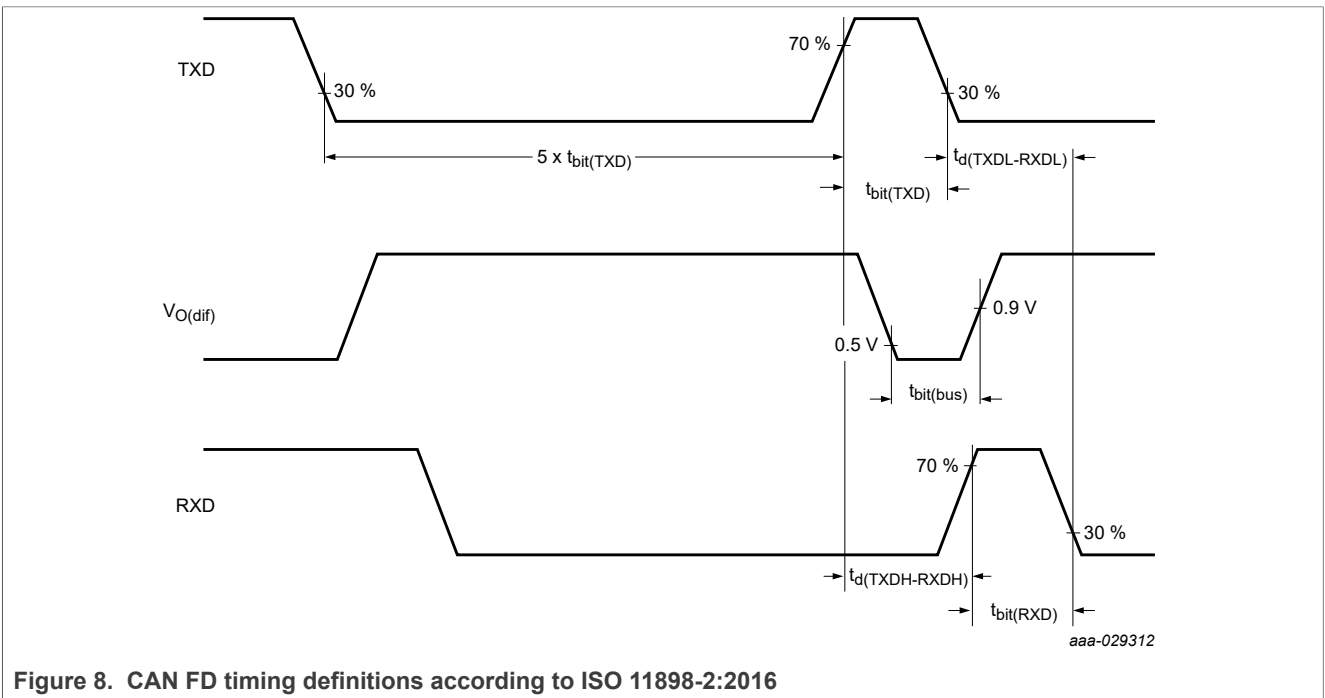
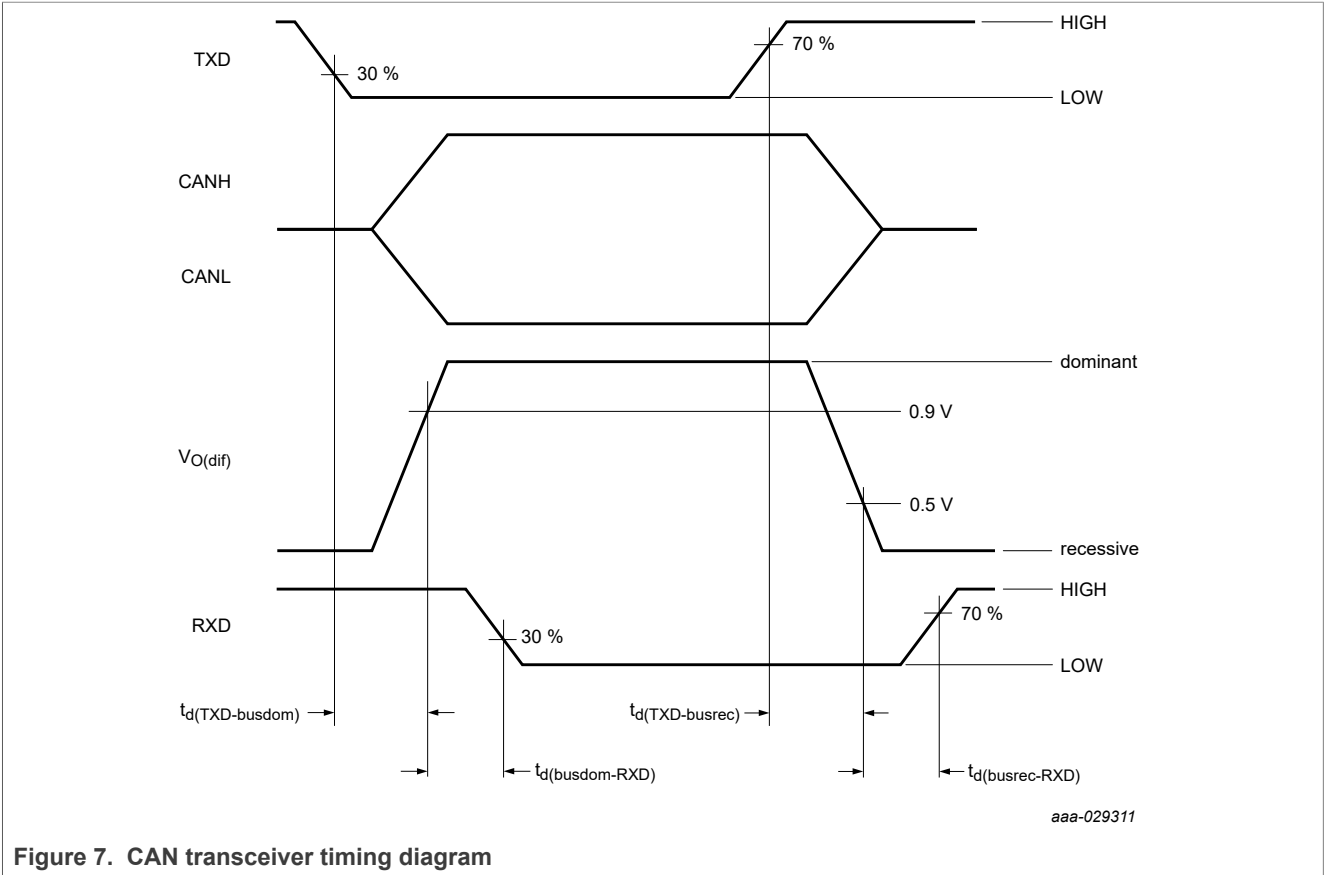
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_{CC} = 4.75\text{ V to }5.25\text{ V}$	190	-	210	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ <sup>[7]</sup>	170	-	230	ns
		8 Mbit/s ( $t_{bit(TXD)} = 125\text{ ns}$ )				
		$V_{CC} = 4.75\text{ V to }5.25\text{ V}$	115	-	135	ns
$\Delta t_{rec}$	receiver timing symmetry	$V_{CC} = 4.75\text{ V to }5.25\text{ V}$ ; for 2 Mbit/s, 5 Mbit/s and 8 Mbit/s	-20	-	+15	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ; 2 Mbit/s	-65	-	+40	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ; 5 Mbit/s	-45	-	+15	ns
$t_{bit(RXD)}$ <sup>[8]</sup>	bit time on pin RXD	2 Mbit/s ( $t_{bit(TXD)} = 500\text{ ns}$ )				
		$V_{CC} = 4.75\text{ V to }5.25\text{ V}$	470	-	520	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	400	-	550	ns
		5 Mbit/s ( $t_{bit(TXD)} = 200\text{ ns}$ )				
		$V_{CC} = 4.75\text{ V to }5.25\text{ V}$	170	-	220	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ <sup>[7]</sup>	150	-	240	ns
		8 Mbit/s ( $t_{bit(TXD)} = 125\text{ ns}$ )				
		$V_{CC} = 4.75\text{ V to }5.25\text{ V}$	95	-	145	ns
Dominant time-out times						
$t_{to(dom)TXD}$	TXD dominant time-out time	$V_{TXD} = 0\text{ V}$ ; Normal mode <sup>[2]</sup> <sup>[9]</sup>	0.8	-	9	ms
$t_{to(dom)bus}$	bus dominant time-out time	$V_{O(dif)} > 0.9\text{ V}$ ; Normal or Listen-Only mode <sup>[2]</sup> <sup>[9]</sup>	0.8	-	9	ms
Bus wake-up times; pins CANH and CANL; see <a href="#">Figure 6</a>						
$t_{wake(busdom)}$	bus dominant wake-up time	Standby or Sleep mode <sup>[2]</sup> <sup>[10]</sup>	0.5	-	1.8	$\mu\text{s}$
$t_{wake(busrec)}$	bus recessive wake-up time	Standby or Sleep mode <sup>[2]</sup> <sup>[10]</sup>	0.5	-	1.8	$\mu\text{s}$
$t_{to(wake)bus}$	bus wake-up time-out time	Standby or Sleep mode <sup>[2]</sup> <sup>[9]</sup>	0.8	-	9	ms
Mode transitions						
$t_{t(moch)}$	mode change transition time		-	-	50	$\mu\text{s}$
$t_{startup}$	start-up time		-	-	1.5	ms
$t_{startup(RXD)}$	RXD start-up time	after local or remote wake-up detected <sup>[2]</sup> <sup>[11]</sup>	4	-	20	$\mu\text{s}$
$t_{startup(INH)}$	INH start-up time	after local or remote wake-up detected; transition from Sleep to Standby <sup>[2]</sup> <sup>[12]</sup>	4	-	50	$\mu\text{s}$
$t_{h(gotosleep)}$	go-to-sleep hold time	STB_N = LOW and EN = HIGH hold time for entering Sleep mode <sup>[2]</sup> <sup>[13]</sup>	24	-	50	$\mu\text{s}$

**Table 9. Dynamic characteristics...continued**

$T_{vj} = -40\text{ }^{\circ}\text{C}$  to  $+150\text{ }^{\circ}\text{C}$ ;  $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$ ;  $V_{IO} = 2.95\text{ V}$  to  $5.5\text{ V}$ ;  $V_{BAT} = 4.5\text{ V}$  to  $28\text{ V}$ ;  $R_L = 60\text{ }\Omega$  unless specified otherwise; all voltages are defined with respect to ground.<sup>[1]</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<a href="#">t<sub>d(moch-ERR_N)</sub></a>	delay time from mode change to ERR_N	to ERR_N stable in response to a mode transition <sup>[2]</sup>	-	-	20	$\mu\text{s}$
Local wake-up input; pin WAKE						
<a href="#">t<sub>wake</sub></a>	wake-up time	in response to a falling or rising edge on pin WAKE; Standby or Sleep mode <sup>[14]</sup>	20	-	50	$\mu\text{s}$
IO filter; pins STB_N, EN						
<a href="#">t<sub>filtr(IO)</sub></a>	I/O filter time	<sup>[15]</sup>	1	-	5	$\mu\text{s}$
Undervoltage detection; see <a href="#">Figure 3</a> and <a href="#">Figure 5</a>						
<a href="#">t<sub>det(uv)</sub></a>	undervoltage detection time	on pin VBAT <sup>[2]</sup>	-	-	30	$\mu\text{s}$
		on pin VCC <sup>[2]</sup>	-	-	30	$\mu\text{s}$
		on pin VIO <sup>[2]</sup>	-	-	30	$\mu\text{s}$
<a href="#">t<sub>det(uv)long</sub></a>	long undervoltage detection time	on pins VCC and/or VIO <sup>[2]</sup> <sup>[16]</sup>	100	-	150	ms
<a href="#">t<sub>rec(uv)</sub></a>	undervoltage recovery time	on pin VCC <sup>[2]</sup>	-	-	50	$\mu\text{s}$
		on pin VIO <sup>[2]</sup>	-	-	50	$\mu\text{s}$

- [1] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.
- [2] Not tested in production; guaranteed by design.
- [3] If TXD goes LOW before the recessive transition has been completed, the bus switches to dominant.
- [4] The TJA1463 fully meets CiA 601-4:2019 which sets tighter limits for  $t_{bit(bus)}$ ,  $\Delta t_{rec}$  and  $\Delta t_{bit(RXD)}$  than ISO 11898-2:2016, which TJA1463 therefore also fully meets.
- [5] 8 Mbit/s specification extends the timing characteristics of ISO 11898-2:2016 and CiA 601-4:2019.
- [6]  $t_{bit(bus)} = \Delta t_{bit(bus)} + t_{bit(TXD)}$ .
- [7] For reasons related to CAN FD bit timing symmetry, these values are centered around the nominal bit length. Details can be found in document AH2002 'TJx144x/TJx146x Application Hints', available on request from NXP Semiconductors.
- [8]  $t_{bit(RXD)} = \Delta t_{bit(RXD)} + t_{bit(TXD)}$ .
- [9] Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.
- [10] A dominant/recessive phase shorter than the min value is guaranteed not to be seen as a dominant/recessive bit; a dominant/recessive phase longer than the max value is guaranteed to be seen as a dominant/recessive bit.
- [11] When a wake-up is detected, RXD start-up time is between the min and max values. RXD cannot be relied on below the min value; RXD can be relied on above the max value; see [Figure 6](#).
- [12] INH switches HIGH between the min and max values after a wake-up had been detected. INH is guaranteed to be floating below the min value and guaranteed to be HIGH above the max value; see [Figure 6](#).
- [13] The device is guaranteed to switch to Sleep mode when STB\_N = LOW and EN = HIGH for longer than max value, and guaranteed not to switch to Sleep mode when less than the min value.
- [14] The device is guaranteed to wake up above 50  $\mu\text{s}$  and guaranteed not to wake up below 20  $\mu\text{s}$ .
- [15] Pulses shorter than the min value are guaranteed to be filtered out; pulses longer than the max value are guaranteed to be processed.
- [16] An undervoltage longer than the max value is guaranteed to force a transition to Sleep mode; an undervoltage shorter than the min value is guaranteed not to force a transition to Sleep mode.





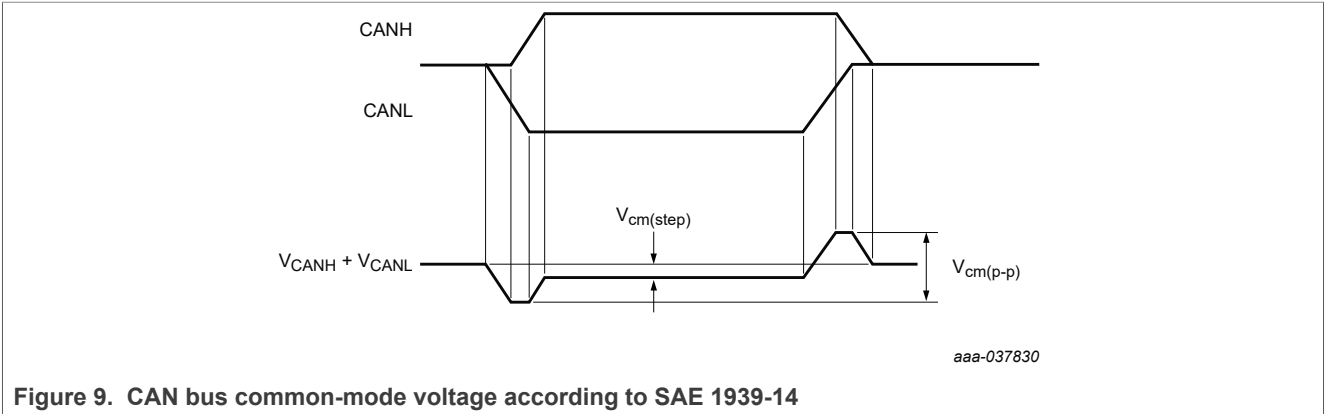
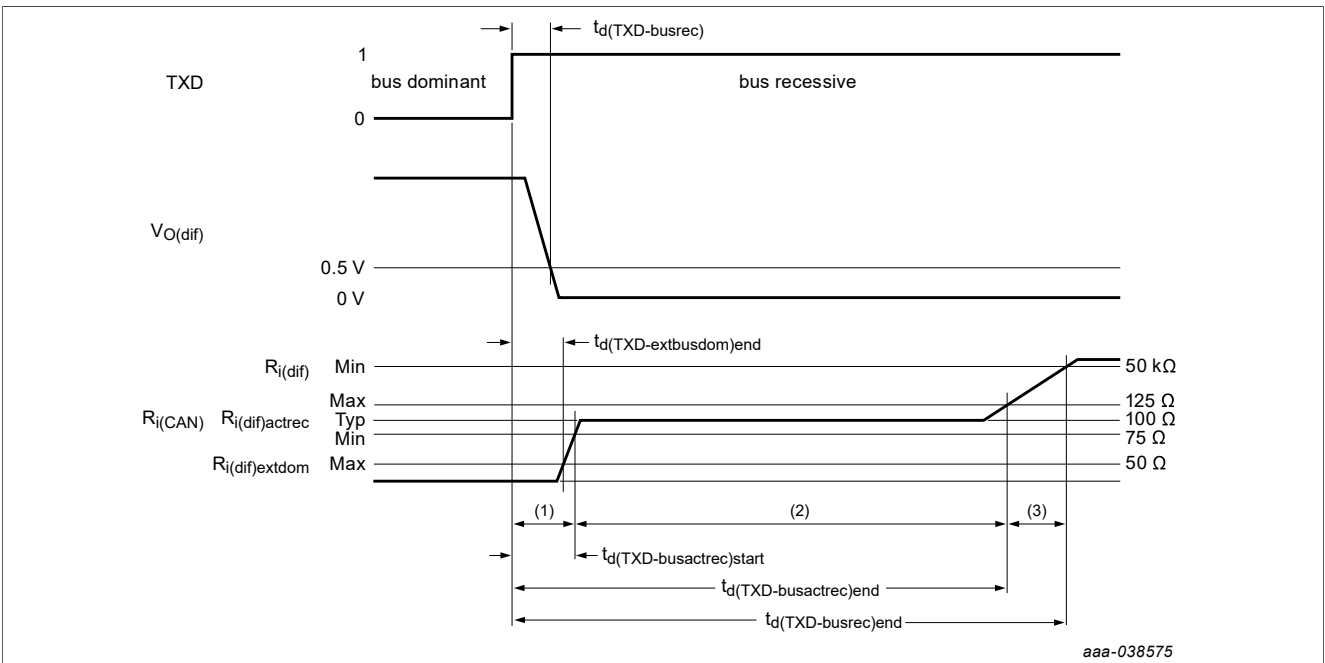


Figure 9. CAN bus common-mode voltage according to SAE 1939-14



(1) Extended dominant phase; (2) Active recessive phase; (3) Slow release phase.

Figure 10. TJA1463 transmitter impedance and timing diagram for dominant-to-passive recessive transition

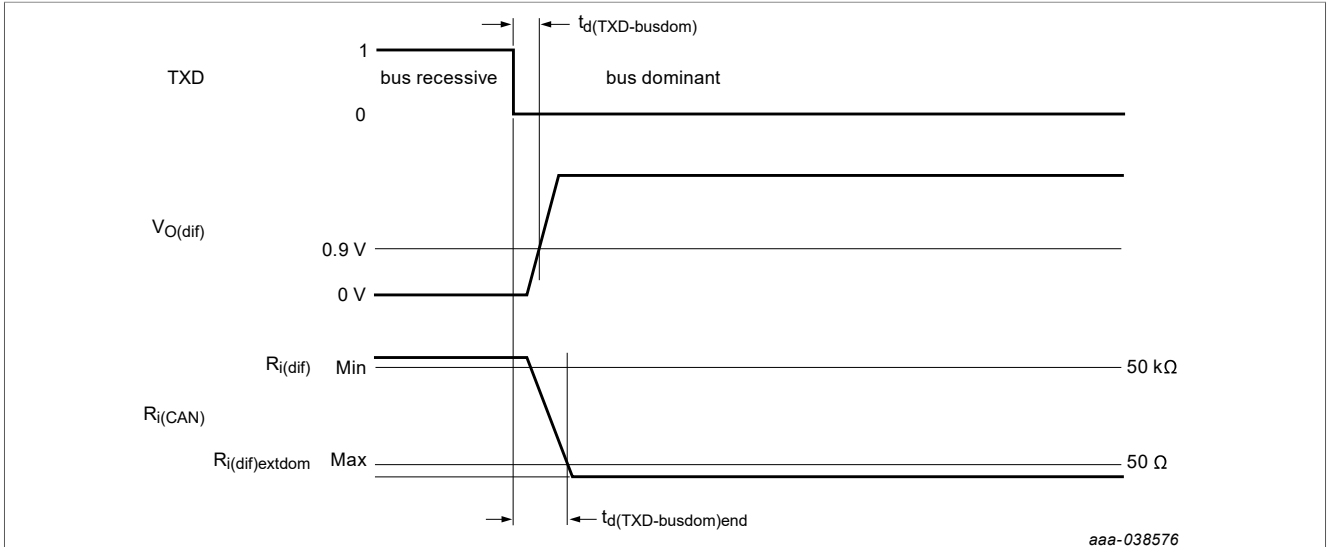
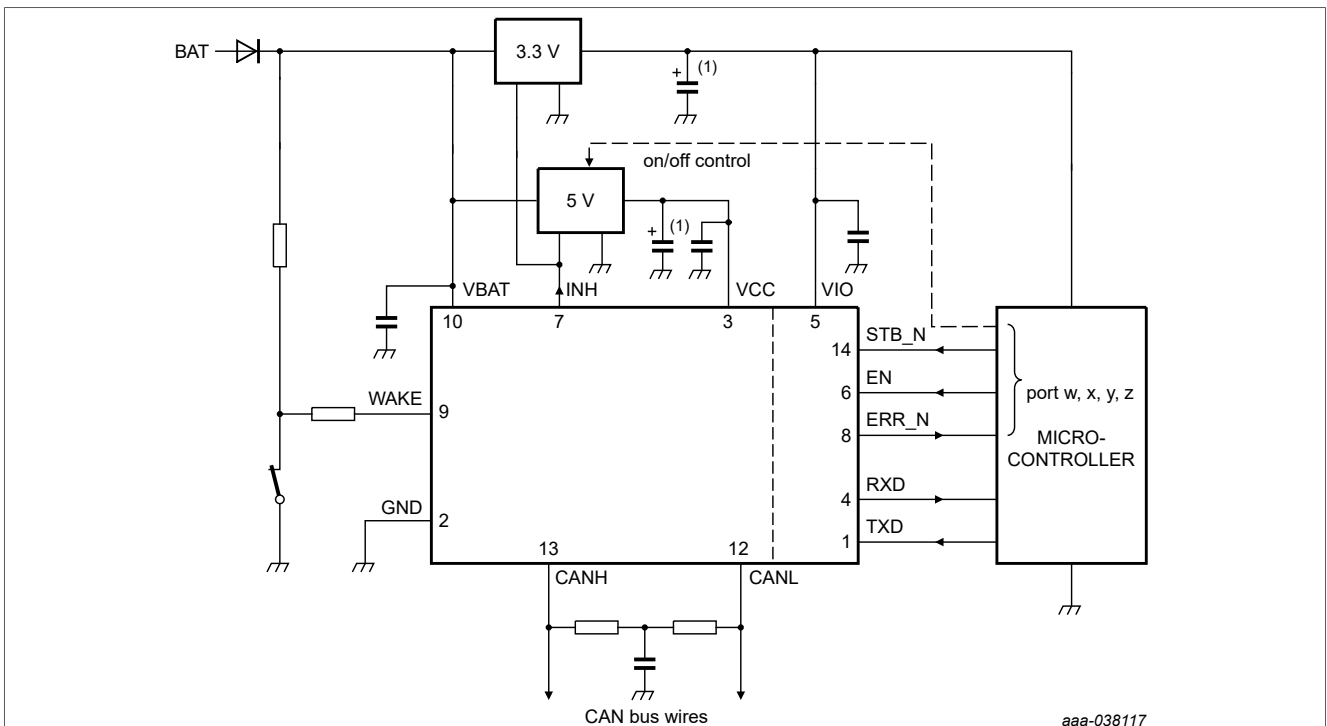


Figure 11. TJA1463 transmitter impedance and timing diagram for passive recessive-to-dominant transition

## 12 Application information

### 12.1 Application diagram



(1) Optional, depends on regulator.

Figure 12. Typical TJA1463 application with a 3.3 V microcontroller

## 12.2 Application hints

Further information on the application of the TJA1463 can be found in NXP application hints AH2002 '*TJx144x/TJx146x Application Hints*', available on request from NXP Semiconductors.

### 13 Test information

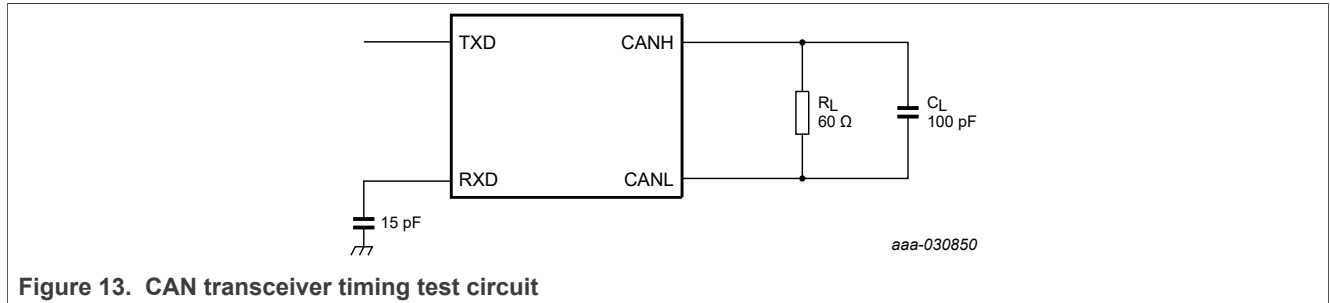


Figure 13. CAN transceiver timing test circuit

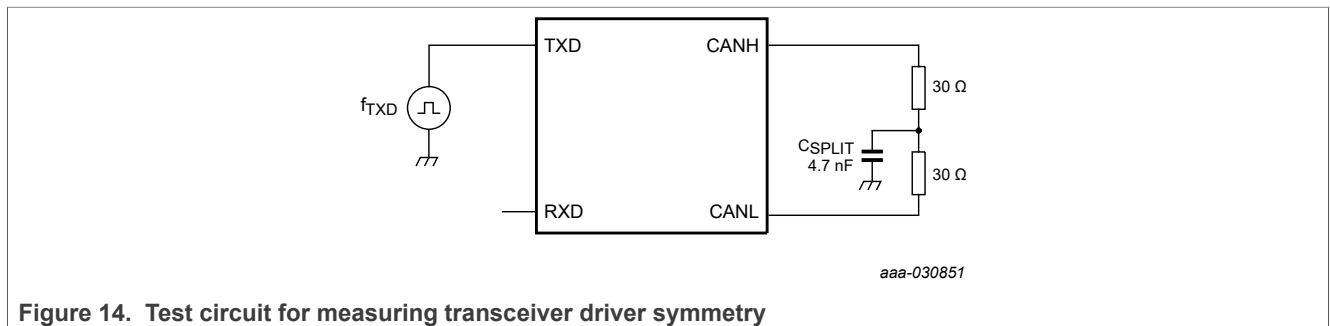


Figure 14. Test circuit for measuring transceiver driver symmetry

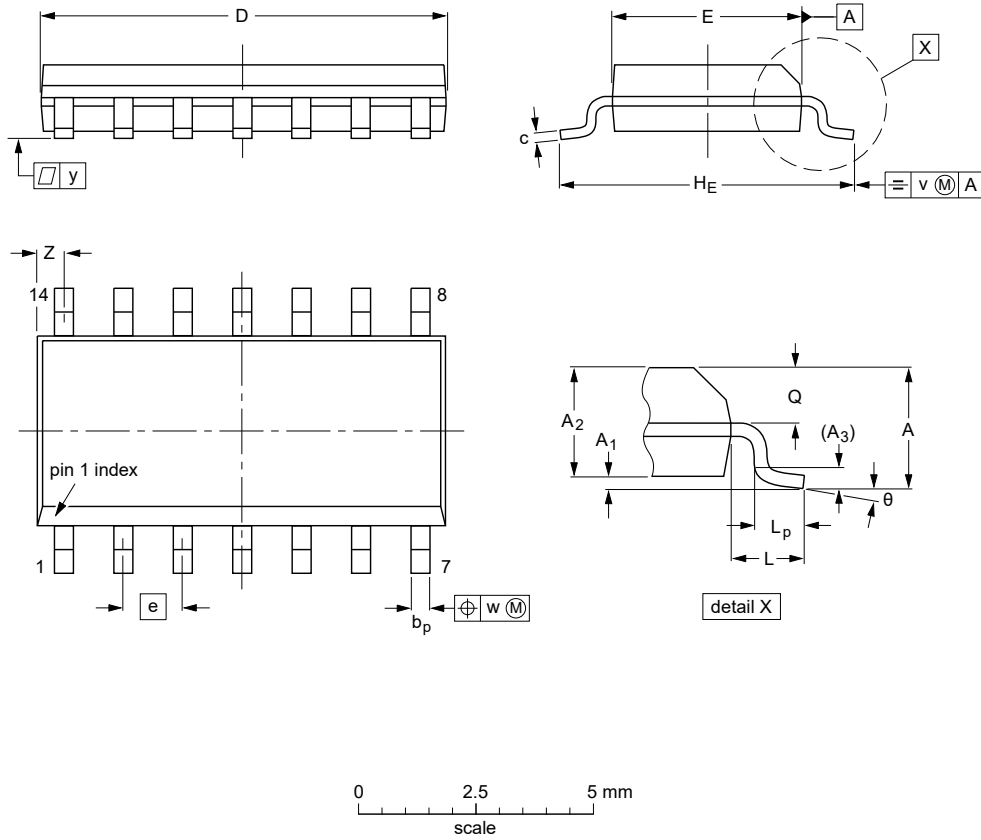
#### 13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 Rev-H - *Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

14 Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

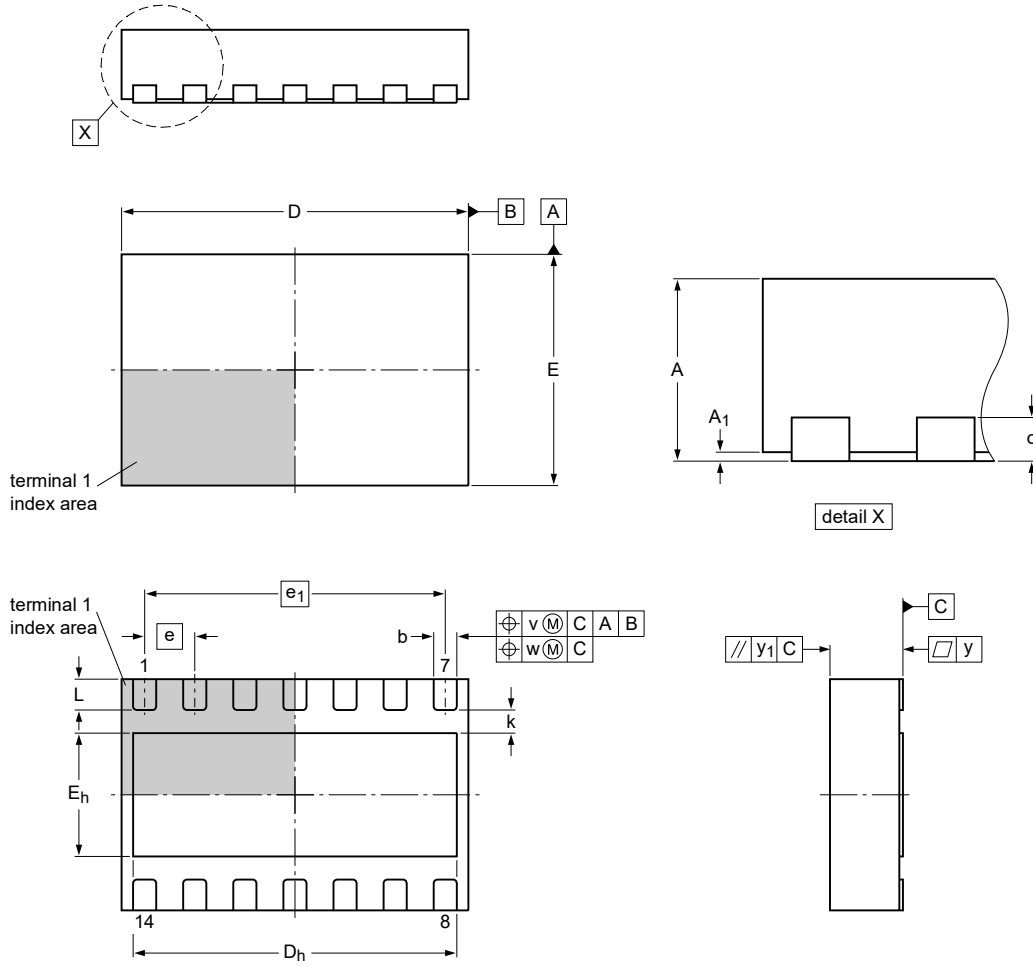
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT108-1	076E06	MS-012			99-12-27 03-02-19

Figure 15. Package outline SOT108-1 (SO14)

HVSON14: plastic, thermal enhanced very thin small outline package; no leads;  
14 terminals; body 3 x 4.5 x 0.85 mm

SOT1086-2



Dimensions

Unit	A	A <sub>1</sub>	b	c	D	D <sub>h</sub>	E	E <sub>h</sub>	e	e <sub>1</sub>	k	L	v	w	y	y <sub>1</sub>
max	1.00	0.05	0.35		4.6	4.25	3.1	1.65			0.35	0.45				
mm nom	0.85	0.03	0.32	0.2	4.5	4.20	3.0	1.60	0.65	3.9	0.30	0.40	0.1	0.05	0.05	0.1
min	0.80	0.00	0.29		4.4	4.15	2.9	1.55			0.25	0.35				

sot1086-2

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1086-2	---	MO-229	---			10-07-14 10-07-15

Figure 16. Package outline SOT1086-2 (HVSON14)

## 15 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

## 16 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

**16.4 Reflow soldering**

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 17](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 10](#) and [Table 11](#)

**Table 10. SnPb eutectic process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

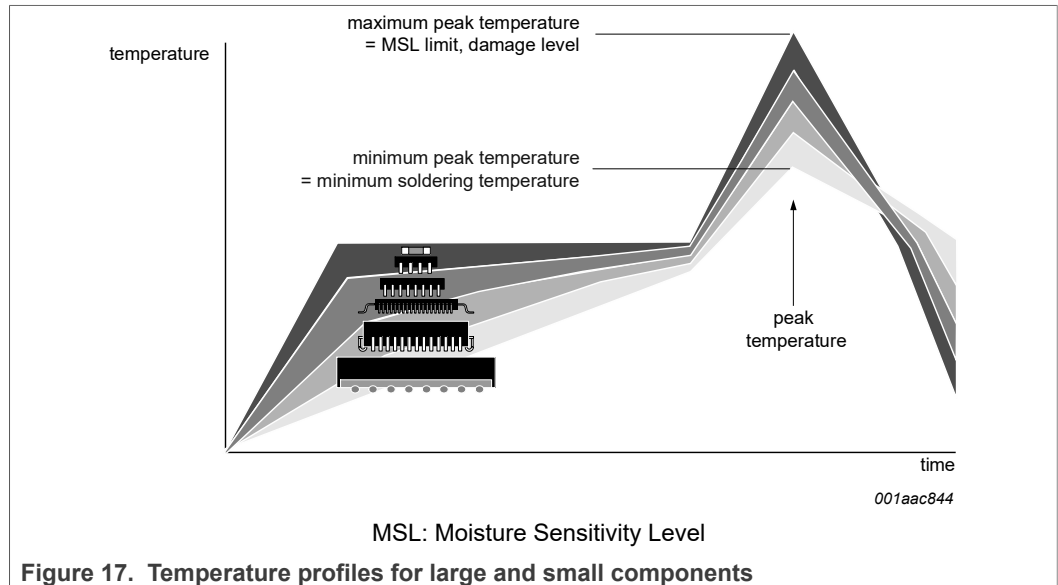
**Table 11. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 17](#).





For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.

## 17 Soldering of HVSON packages

[Section 16](#) contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering HVSON leadless package ICs can be found in the following application note:

- AN10365 “Surface mount reflow soldering description”

## 18 Appendix: ISO 11898-2:2016 and CiA 601-4:2019 parameter cross-reference lists

Table 12. ISO 11898-2:2016 to NXP data sheet parameter conversion

ISO 11898-2:2016		NXP data sheet	
Parameter	Notation	Symbol	Parameter
<b>HS-PMA dominant output characteristics</b>			
Single ended voltage on CAN_H	$V_{CAN\_H}$	$V_{O(dom)}$	dominant output voltage
Single ended voltage on CAN_L	$V_{CAN\_L}$		
Differential voltage on normal bus load	$V_{Diff}$	$V_{O(dif)}$	differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
<b>HS-PMA driver symmetry</b>			
Driver symmetry	$V_{SYM}$	$V_{TXsym}$	transmitter voltage symmetry
<b>Maximum HS-PMA driver output current</b>			
Absolute current on CAN_H	$I_{CAN\_H}$	$I_{O(sc)}$	short-circuit output current
Absolute current on CAN_L	$I_{CAN\_L}$		
<b>HS-PMA recessive output characteristics, bus biasing active/inactive</b>			
Single ended output voltage on CAN_H	$V_{CAN\_H}$	$V_{O(rec)}$	recessive output voltage
Single ended output voltage on CAN_L	$V_{CAN\_L}$		
Differential output voltage	$V_{Diff}$	$V_{O(dif)}$	differential output voltage
<b>Optional HS-PMA transmit dominant time-out</b>			
Transmit dominant time-out, long	$t_{dom}$	$t_{to(dom)TXD}$	TXD dominant time-out time
Transmit dominant time-out, short			
<b>HS-PMA static receiver input characteristics, bus biasing active/inactive</b>			
Recessive state differential input voltage range	$V_{Diff}$	$V_{th(RX)dif}$	differential receiver threshold voltage
Dominant state differential input voltage range		$V_{rec(RX)}$	receiver recessive voltage
		$V_{dom(RX)}$	receiver dominant voltage
<b>HS-PMA receiver input resistance (matching)</b>			
Differential internal resistance	$R_{Diff}$	$R_{i(dif)}$	differential input resistance
Single ended internal resistance	$R_{CAN\_H}$ $R_{CAN\_L}$	$R_i$	input resistance
Matching of internal resistance	MR	$\Delta R_i$	input resistance deviation
<b>HS-PMA implementation loop delay requirement</b>			
Loop delay	$t_{Loop}$	$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH
		$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW

CAN FD signal improvement transceiver with Sleep mode

Table 12. ISO 11898-2:2016 to NXP data sheet parameter conversion...continued

ISO 11898-2:2016		NXP data sheet	
Parameter	Notation	Symbol	Parameter
<b>Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s up to 2 Mbit/s and above 2 Mbit/s up to 5 Mbit/s</b>			
Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended	$t_{\text{Bit(Bus)}}$	$t_{\text{bit(bus)}}$	transmitted recessive bit width
Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s	$t_{\text{Bit(RXD)}}$	$t_{\text{bit(RXD)}}$	bit time on pin RXD
Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s	$\Delta t_{\text{Rec}}$	$\Delta t_{\text{rec}}$	receiver timing symmetry
<b>HS-PMA maximum ratings of <math>V_{\text{CAN\_H}}</math>, <math>V_{\text{CAN\_L}}</math> and <math>V_{\text{Diff}}</math></b>			
Maximum rating $V_{\text{Diff}}$	$V_{\text{Diff}}$	$V_{(\text{CANH-CANL})}$	voltage between pin CANH and pin CANL
General maximum rating $V_{\text{CAN\_H}}$ and $V_{\text{CAN\_L}}$	$V_{\text{CAN\_H}}$	$V_x$	voltage on pin x
Optional: Extended maximum rating $V_{\text{CAN\_H}}$ and $V_{\text{CAN\_L}}$	$V_{\text{CAN\_L}}$		
<b>HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered</b>			
Leakage current on CAN_H, CAN_L	$I_{\text{CAN\_H}}$ $I_{\text{CAN\_L}}$	$I_L$	leakage current
<b>HS-PMA bus biasing control timings</b>			
CAN activity filter time, long	$t_{\text{Filter}}$	$t_{\text{wake(busdom)}}^{[1]}$	bus dominant wake-up time
CAN activity filter time, short		$t_{\text{wake(busrec)}}$	bus recessive wake-up time
Wake-up time-out, short	$t_{\text{Wake}}$	$t_{\text{to(wake)bus}}$	bus wake-up time-out time
Wake-up time-out, long			

[1]  $t_{\text{filtr(wake)bus}}$  - bus wake-up filter time, in devices with basic wake-up functionality

Table 13. CiA 601-4:2019 to NXP data sheet parameter conversion

CiA 601-4:2019		NXP data sheet	
Parameter	Notation	Symbol	Parameter
<b>Optional HS-PMA implementation data signal timing requirements</b>			
Signal improvement time TX-based	$t_{\text{SIC\_TX\_base}}$	$t_{\text{d(TXD-busrec)end}}$	delay time from TXD to bus recessive end
Signal improvement time RX-based	$t_{\text{SIC\_RX\_base}}$	N/A <sup>[1]</sup>	N/A
Transmitted bit width variation	$\Delta t_{\text{Bit(Bus)}}$	$\Delta t_{\text{bit(bus)}}$	transmitted recessive bit width deviation
Received bit width variation	$\Delta t_{\text{Bit(RxD)}}$	$\Delta t_{\text{bit(RXD)}}$	received recessive bit width deviation
Receiver timing symmetry	$\Delta t_{\text{REC}}$	$\Delta t_{\text{rec}}$	receiver timing symmetry
Propagation delay from TXD to bus dominant	$t_{\text{prop(TXD-busdom)}}$	$t_{\text{d(TXD-busdom)}}$	delay time from TXD to bus dominant
Propagation delay from TXD to bus recessive	$t_{\text{prop(TXD-busrec)}}$	$t_{\text{d(TXD-busrec)}}$	delay time from TXD to bus recessive
Propagation delay from bus to RXD dominant	$t_{\text{prop(busdom-RXD)}}$	$t_{\text{d(busdom-RXD)}}$	delay time from bus dominant to RXD
Propagation delay from bus to RXD recessive	$t_{\text{prop(busrec-RXD)}}$	$t_{\text{d(busrec-RXD)}}$	delay time from bus recessive to RXD

[1] The NXP signal improvement implementation is TX-based; RX-based is not applicable.

## 19 Appendix: TJx144x/TJx146x/TJF1441 family overview

Table 14. Feature overview of the complete TJx144x/TJx146x/TJF1441 family

Device <sup>[1]</sup>	Modes					Supplies			Data rate		Additional features					
	Normal	Standby	Sleep	Silent/Listen-only	Selectable Off	VCC pin	VIO pin	VBAT pin	Up to 5 Mbit/s CAN FD	Up to 8 Mbit/s CAN FD <sup>[2]</sup>	Signal improvement <sup>[3]</sup>	Wake-up source recognition <sup>[4]</sup>	Short WUP support [0.5 - 1.8 μs] <sup>[5]</sup>	Single supply pin wake-up <sup>[6]</sup>	TXD dominant timeout	Local diagnostics via ERR_N pin
TJx1441A	•			•		•	•		•						•	
TJx1441B	•			•		•			•						•	
TJx1441D	•			•	•	•			•						•	
TJF1441A	•			•		•	•		•						[7]	
TJx1442A	•	•				•	•		•				•	•	•	
TJx1442B	•	•				•			•				•		•	
TJx1443A	•	•	•	•		•	•	•	•			•	•	•	•	•
TJx1448A	•	•				•	•		•				•	•	•	
TJx1448B	•	•				•			•				•		•	
TJx1448C	•	•				•	•		•			•	•	•	•	
TJx1462A	•	•				•	•		•	•	•		•	•	•	
TJx1462B	•	•				•			•	•	•		•		•	
TJx1463A	•	•	•	•		•	•	•	•	•	•	•	•	•	•	•

[1] TJx: TJA14xxx is AEC-Q100 Grade 1; TJR14xxx is AEC-Q100 Grade 0; TJF1441A is non-automotive grade.

[2] Only guaranteed for TJA146x, AEC-Q100 Grade 1.

[3] CAN FD Signal Improvement Capability (SIC) according to CiA 601-4:2019.

[4] RXD is held LOW after wake-up request, enabling wake-up source recognition.

[5] WUP = wake-up pattern according ISO11898-2:2016.

[6] Only VIO supply needed for wake-up in TJA1442A, TJA1448A, TJA1448C, TJA1462A; only VBAT supply needed for wake-up in TJA1443A, TJA1463A.

[7] Not having TXD dominant timeout allows for very low data rates in non-automotive grade applications.

## 20 Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1463 v.2	20211015	Product data sheet	-	TJA1463 v.1
Modifications	<ul style="list-style-type: none"> <li>• CAN FD communication up to 8 Mbit/s: <a href="#">Section 1</a> text revised, CAN FD parameters <math>t_{\text{bit(TXD)}}</math>, <math>t_{\text{bit(BUS)}}</math>, <math>\Delta t_{\text{rec}}</math> and <math>t_{\text{bit(RXD)}}</math> updated in <a href="#">Table 9</a> and table note 5 added</li> <li>• Added device (<a href="#">Table 3</a>) and family (<a href="#">Section 19</a>) feature overviews</li> <li>• <a href="#">Figure 3</a>: text defining transition from Sleep to Standby revised</li> <li>• <a href="#">Section 7.1.1.2</a>: typo corrected - STBN_N changed to STB_N</li> <li>• <a href="#">Table 6</a>: table notes 3 and 4 revised; table note 12 added; measurement conditions and table note changed for parameter <math>V_{\text{trt}}</math></li> <li>• <a href="#">Table 9</a>: measurement conditions for parameters <math>t_{\text{startup(RXD)}}</math> and <math>t_{\text{startup(INH)}}</math> revised; table note 14 added</li> <li>• <a href="#">Section 21</a>: <i>Suitability for use in Automotive applications</i> and <i>Security</i> disclaimers revised</li> </ul>			
TJA1463 v.1	20200812	Product data sheet	-	-

## 21 Legal information

### 21.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 21.2 Definitions

**Draft** — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 21.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without

notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Suitability for use in automotive applications** — This NXP product has been qualified for use in automotive applications. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"),

then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

**Security** — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible

for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

## 21.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**NXP** — wordmark and logo are trademarks of NXP B.V.