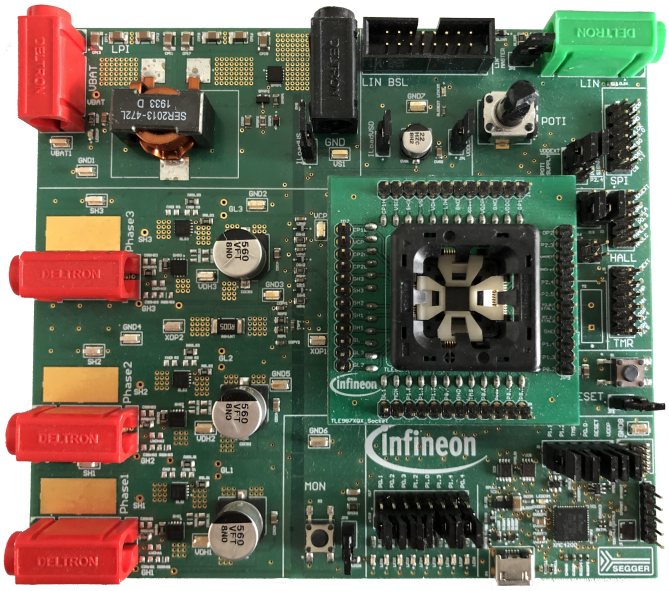
TLE987x EvalBoard



About this document

Scope and purpose

This user manual is intended to help users using the TLE987x EvalBoard. This EvalBoard is designed to evaluate hardware and software functionalities of the TLE987x device family.

This manual provides additional information about the layout, jumper settings, interface and debug options. It introduces the evaluation platform as well as how to write software and download it to the TLE987x.

The TLE987x is available in VQFN and a brand-new TQFP package, this document is valid for both.

Intended audience

This document is for everyone who works with the TLE987x EvalBoard.

Abbreviations and definitions

Abbreviation	Definition
BLDC	Brushless direct current
BSL	Bootstrap loader
COSN	Cosinusoidal TMR output negative
COSP	Cosinusoidal TMR output positive
CS	Chip Select
CSA	Current sense amplifier
GH1-3	Gate high-side MOSFETs for phases 1-3
GND	Ground
GL1,-3	Gate low-side MOSFETs for phase 1-3
GPIO	General Purpose Input / Output
ISP	In-system programmer
LED	Light Emitting Diode
LIN	Local Interconnect Network
MISO	Master Input Slave Output
MON	Monitor
MOSI	Master Output Slave Input
N.C.	Not connected
n/u	Not used
OP1	Negative operational amplifier input
OP2	Positive operational amplifier input
PORST	Power-on Reset
SCLK	Serial Clock
SH1-3	Source high-side MOSFET 1-3
SINN	Sinusoidal TMR output negative
SINP	Sinusoidal TMR output positive
SL	Source low-side MOSFET
SWD	Arm® serial wire debug
TMS	Test mode select
TMR	Tunnel Magneto Resistance
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VAREF	Reference voltage
VBAT	Battery voltage supply
VCOM	Virtual COM-port

Abbreviations and definitions

Abbreviation	Definition
VCP	Voltage charge pump
VDDC	Core supply
VDDEXT	External voltage supply output
VDDP	I/O port supply
VDH	Voltage drain high-side MOSFET
VS	Battery supply input
VSD	Battery supply input for MOSFET driver

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1 Concept

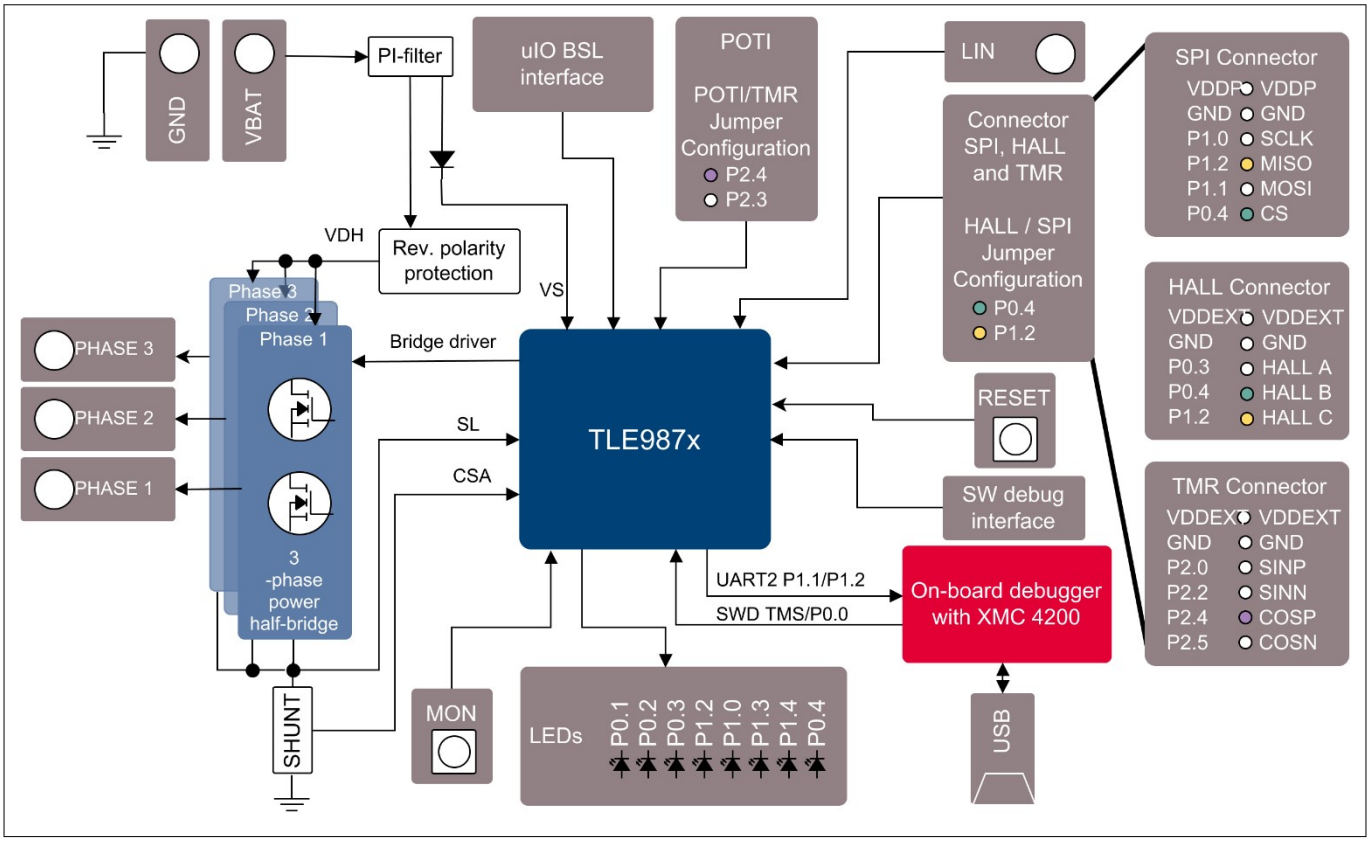

Figure 1 Board concept

This board is designed to provide a simple, easy-to-use tool for getting familiar with Infineon's Embedded Power IC TLE987x devices. A socket provides the possibility to test and evaluate all ICs of the TLE987x family. Every pin of the IC is connectable via rows of pin headers. The board is protected against reverse polarity of the input voltage supply.

Three MOSFET half bridges are placed on the board to drive a BLDC motor. The board is ready to be connected to a car supply or similar and offers an USB port to use the on-board SWD debugger.

The evaluation board can be operated by standard laboratory equipment, since the power supply and LIN communication are connected using via banana jacks.

A LED indicates that the board is connected correctly to the power supply. The integrated reverse polarity protection secures the board from damage by cross connection.

2 Interconnects

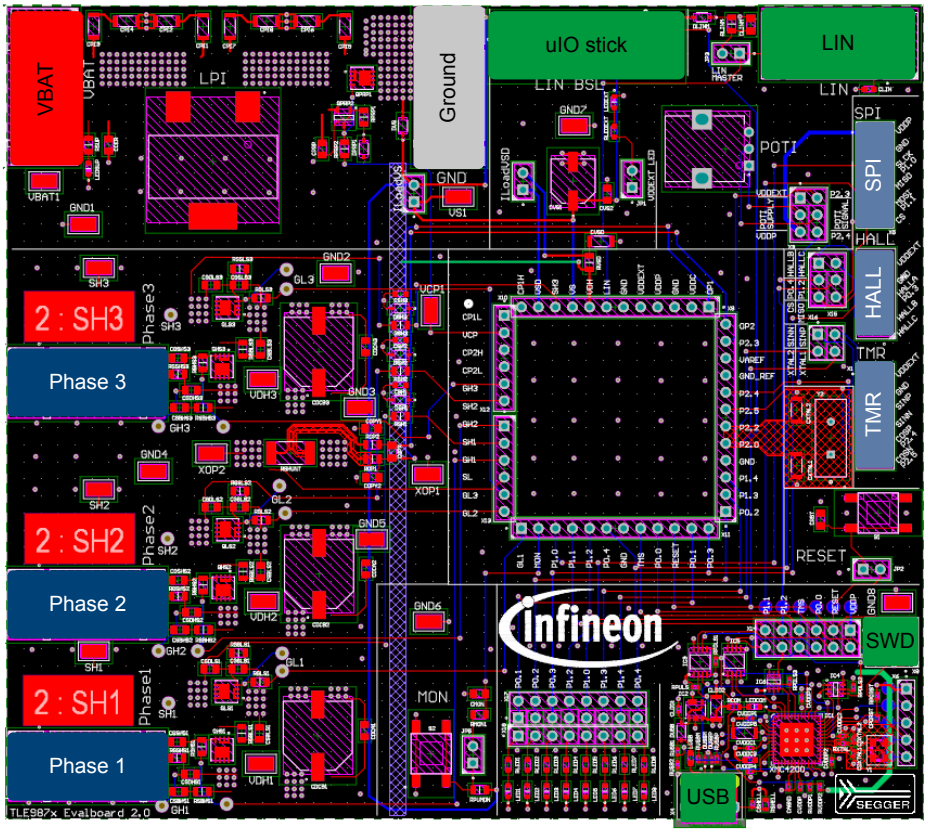

Figure 2 Interconnects

Banana jacks for ground, supply and LIN

Multiple jacks are available in different colors for ground, supply (max. 28 V) and LIN communication via banana jack.

Banana jacks for motor connection

The three jacks for Phase 1, Phase 2 and Phase 3 provide access to the three half bridges and for driving a brushless motor.

uIO Stick connector

The uIO bootstrap loader is a 16-pin header (2 × 8) with 2.54 mm pitch.

This interface can be used to programming the TLE987x via LIN (see ***www.infineon.com/uio*** or ***www.hitex.com/uio***).

N.C.	N.C.	N.C.	N.C.	RESET	LIN	N.C.	NC.
15	13	11	9	7	5	3	1
16	14	12	10	8	6	4	2
N.C.	N.C.	N.C.	N.C.	N.C.	VS	N.C.	GND

Figure 3 Pin configuration uIO BSL

USB for on-board debugger

The on-board connector can be accessed with a micro-USB cable, connected to a PC.

Pin header for SWD

The 10-pin header (2 × 5) with 1.27 mm can be used for debugging if the on-board debugger is not available or if it cannot be used.

TMS	P0.0	N.C.	N.C.	RESET
2	4	6	8	10
1	3	5	7	9
5V	GND	GND	N.C.	PORST

Figure 4 Pin configuration SWD interface

Pin header for SPI

The 12-pin header (2 × 6) with 2.54 mm pitch can be used for controlling an external IC with the SPI. In order to access the SPI, the jumpers P0.4 and P1.2 have to be set in position 2.

VDDP	GND	SCLK	MISO	MOSI	CS
2	4	6	8	10	12
1	3	5	7	9	11
VDDP	GND	SCLK	MISO	MOSI	CS

Figure 5 Pin configuration SPI

Pin header for Hall sensor interface

The 10-pin header (2 × 5) with 2.54 mm pitch can be used for controlling external Hall sensors. In order to access the Hall sensor interface, the jumpers P0.4 and P1.2 have to be set in position 1.

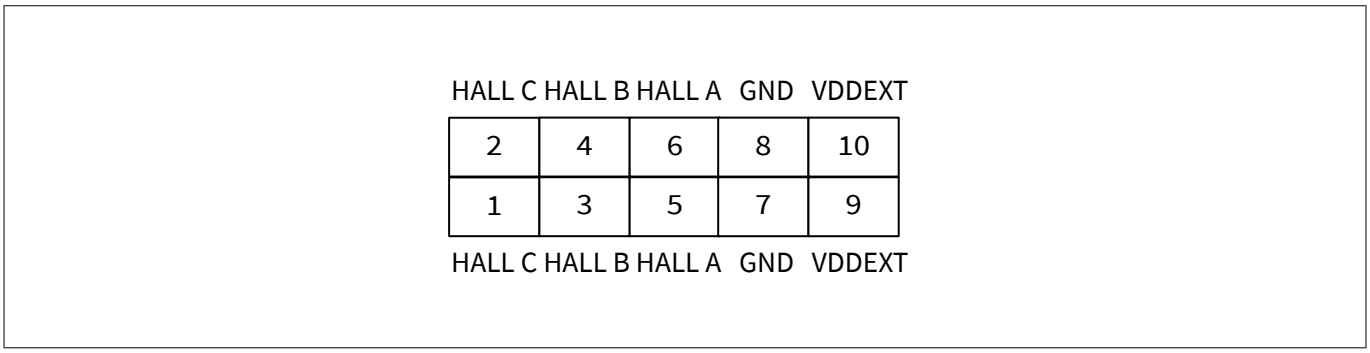

Figure 6 Pin configuration Hall sensor interface

Pin header for TMR sensor interface

The 10-pin header (2 × 5) with 2.54 mm pitch can be used for controlling external TMR sensors. In order to access the TMR sensor interface, the jumpers SINN and SINP have to be set.

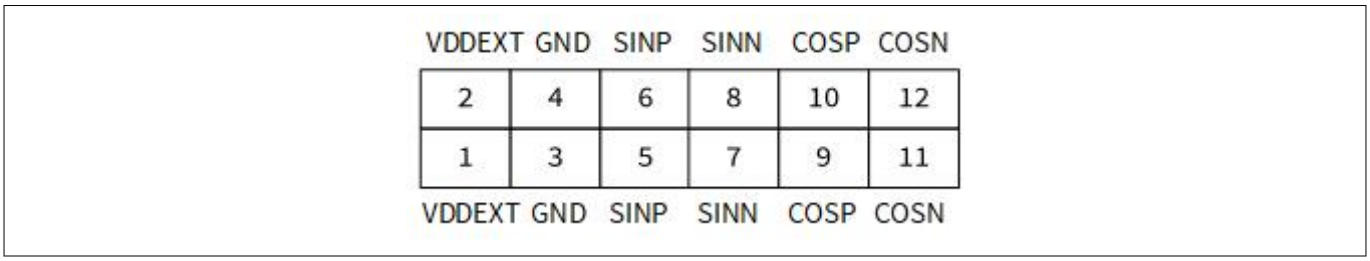

Figure 7 Pin configuration TMR sensor interface

3 Test points and LEDs

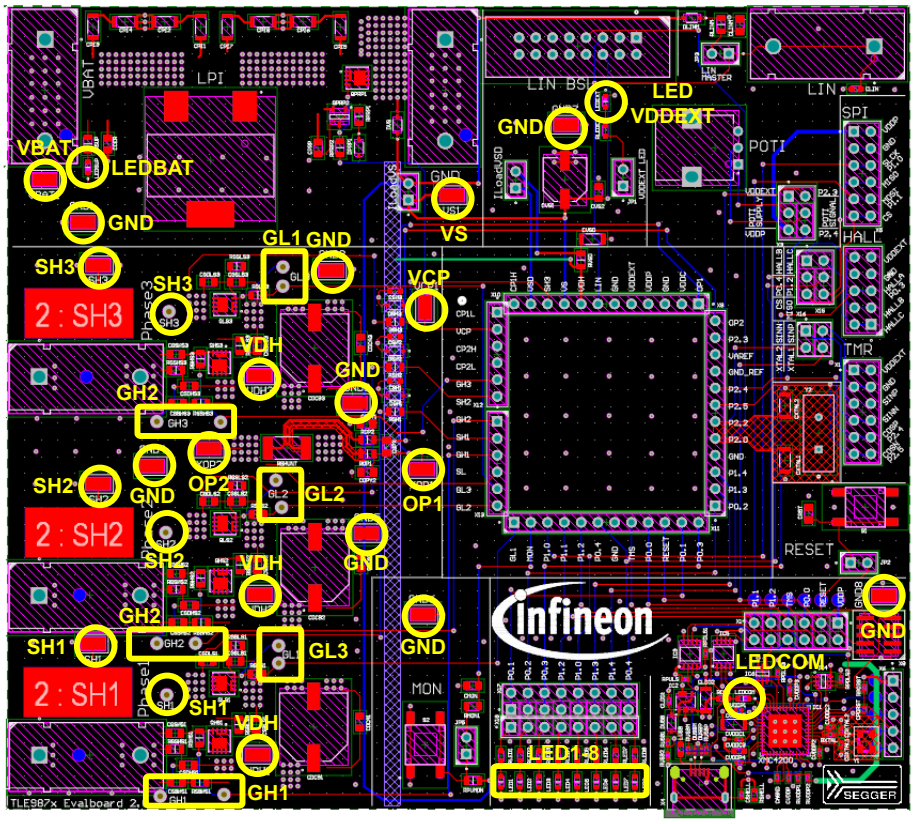

Figure 8 Test points

Test points

- 2× VBAT
- 1× VS
- 1× VCP
- 8× GND
- 2× SH1, 2× SH2, 2× SH3
- 2× GH1, 2× GH2, 2× GH3 (for gate-current supervision)
- 3× GH1, 3× GH2, 3× GH3 (for gate-current supervision).
- OP1, OP2
- 3× VDH

LEDs

- LEDBAT (supply voltage active)
- LEDCOM (on-board debugger communication active)
- LEDVDDEXT (VDDEXT active)
- LED1-8 can be connected to GPIOs (see ***Table 1***)

4 Jumper settings

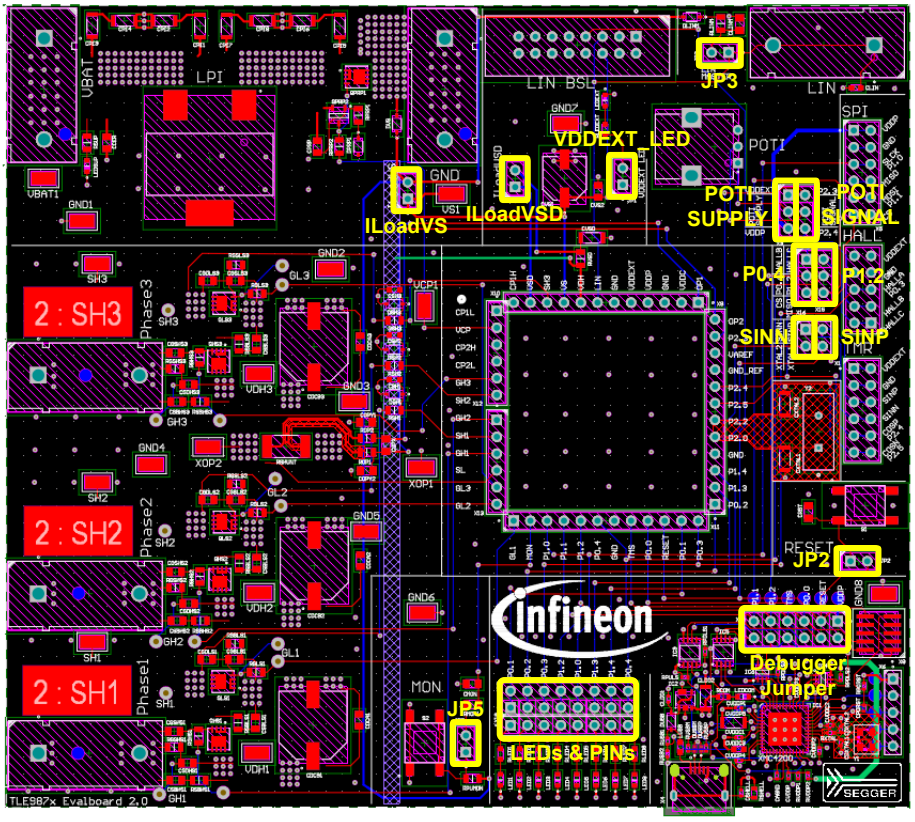

Figure 9 Jumpers

JP2	Set this jumper to connect RESET button to RESET pin. Open it to disconnect RESET button from RESET pin.
JP3	Set this jumper to terminate TLE987x in daughter board as LIN master. Open it to terminate TLE987x in daughter board as LIN slave.
JP5	Set this jumper to connect MON button to MON pin. Open it to disconnect MON button from MON pin.
VDDEXT_LED	Set this jumper to enable LED operation at VDDEXT.
ILoadVS	This jumper is closed by default. If this jumper is left open the device is not supplied. Target is to measure the current flowing into the TLE987x device.
ILoadVSD	This jumper is closed by default. If this jumper is left open the charge-pump is not supplied. Target is to measure the charge-pump current consumption.
SINN/P	Set to use TMR sensor interface.
Debugger Jumper	Open debugger jumper to use off-board SWD debugger.

4 Jumper settings

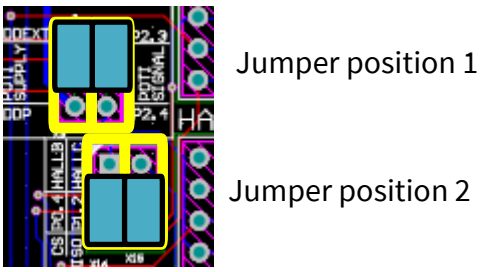

Figure 10 Jumper position

Jumper	Position 1	Position 2
POTI SUPPLY	VDDEXT	VDDP
POTI SIGNAL	P2.3	P2.4
P0.4	HALL B	CS
P1.2	HALL C	MISO

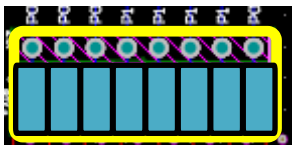

Figure 11 Jumper position for LEDs and PINs

Set jumper as shown in ***Figure 11*** to connect the according PINs and LEDs.

Table 1 LEDs and PORTs jumper

PIN	LED
P0.1	LED1
P0.2	LED2
P0.3	LED3
P1.2	LED4
P1.0	LED5
P1.3	LED6
P1.4	LED7
P0.4	LED8

5 Communication interfaces

5.1 LIN (via banana jack and uIO BSL)

The integrated LIN transceiver is connected to a banana jack and additionally to the uIO BSL interface. In order to integrate the device in a LIN network, it is sufficient to use the single wire banana interface. The BSL interface programs the device via LIN. For further information about the uIO interface is available at ***www.infineon.com/uio*** or ***www.hitex.com/uio***.

5.2 Debugging

Debugging is possible via the on-board debugger that can be connected via an USB cable and the SWD interface; the signals are routed through the 10-pin header SWD interface.

6 Software toolchain

The Software toolchain can be installed following the explanation bellow, or visiting ***www.infineon.com/tle987x*** and search for Tools & Software.

6.1 Keil µVision5

The recommended Integrated Software Development Environment is Keil® µVision5®.

Infineon's Embedded Power family is supported. More information about the installation process is available at ***www.keil.com***.

6.2 Infineon ConfigWizard

In addition to the IDE, Infineon provides a solution to speed-up the IC programming, called "ConfigWizard". This tool is designed for code configuration in combination with the IDE. Infineon ConfigWizard can be downloaded via the Infineon Toolbox. The Infineon Toolbox allows to download and update all your Infineon tools. It can be downloaded from ***www.infineon.com/toolbox***.

6.3 TLE987x SDK

All Embedded Power products can be installed to Keil® µVision5® via "Pack Installer". Browsing to the Infineon chapter in "All Devices" will lead to the "TLE98xx Series". The ".pack" file comes with several code examples to provide an easy start up and speed up software development.

6.4 Debug connection setup

For a proper Flash and Debug Connection, install V5.10 (or newer) from: ***www.segger.com/jlink-software.html***. Keil® µVision5® has to be configured in the IDE Menu "Options for Target". After connecting the USB cable and powering up the EvalBoard, go to the "Debug" register-card, choose "J-LINK / J-TRACE Cortex" and press "Settings".

6 Software toolchain

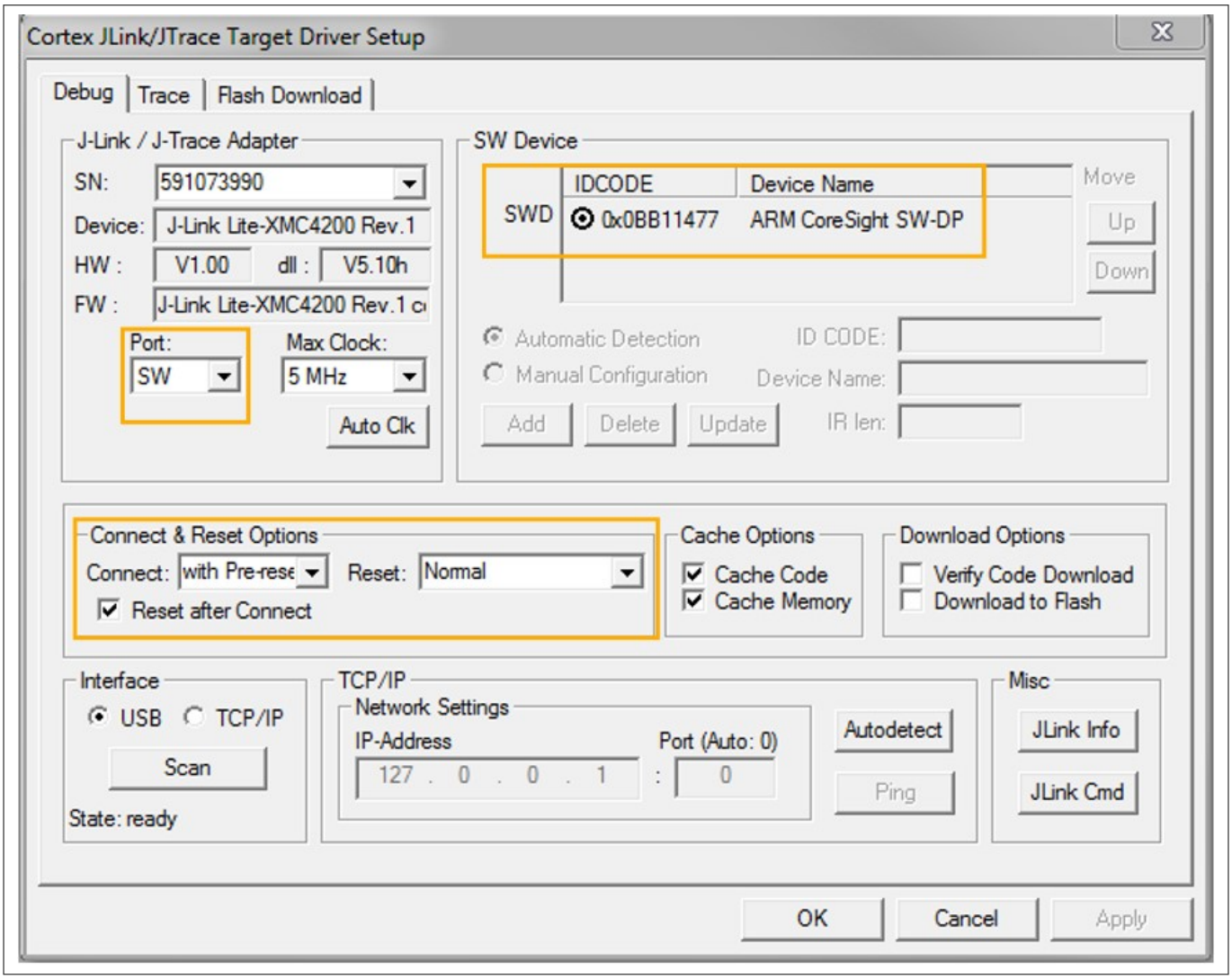

Figure 12 Debug and flash configuration

If the board is connected successfully, the Arm® IDCODE will be visible in the SW Device Window. If the connection fails, "Connect & Reset Options" and "Port" window has to be checked.

7 Technical data

Table 2 Technical data

Voltage supply	max. 28 V
Motor current	max. 30 A
Pin ports	5 V

8 Optional additional placements

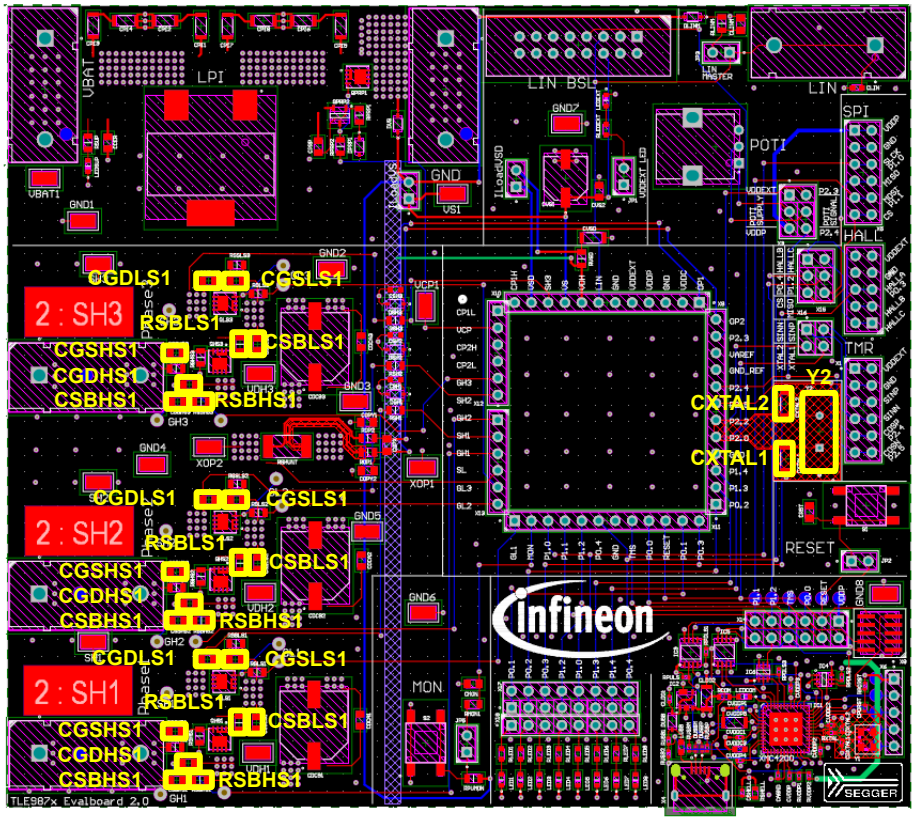

Figure 13 Additional placements' positions

Values for optional additional placements have to be determined depending on application.

Table 3 Additional placements

Component	Description
Y1	External oscillator
CXTAL1	Oscillator capacitor 1
CXTAL2	Oscillator capacitor 2
RSBHS1	Resistance snubber high-side MOSFET phase 1
CSBHS1	Capacitor snubber high-side MOSFET phase 1
CGDHS1	Gate-drain capacitor high-side MOSFET phase 1
CGSHS1	Gate-source capacitor high-side MOSFET phase 1
RSBLS1	Resistance snubber low-side MOSFET phase 1
CSBLS1	Capacitor snubber low-side MOSFET phase 1
CGDLS1	Gate-drain capacitor low-side MOSFET phase 1
CGSLS1	Gate-source capacitor low-side MOSFET phase 1
RSBHS2	Resistance snubber high-side MOSFET phase 2

8 Optional additional placements

Table 3 Additional placements (continued)

Component	Description
CSBHS2	Capacitor snubber high-side MOSFET phase 2
CGDHS2	Gate-drain capacitor high-side MOSFET phase 2
CGSHS2	Gate-source capacitor high-side MOSFET phase 2
RSBLS2	Resistance snubber low-side MOSFET phase 2
CSBLS2	Capacitor snubber low-side MOSFET phase 2
CGDLS2	Gate-drain capacitor low-side MOSFET phase2
CGSLS2	Gate-source capacitor low-side MOSFET phase 2
RSBHS3	Resistance snubber high-side MOSFET phase 3
CSBHS3	Capacitor snubber high-side MOSFET phase 3
CGDHS3	Gate drain capacitor high-side MOSFET phase 3
CGSHS3	Gate-source capacitor high-side MOSFET phase 3
RSBLS3	Resistance snubber low-side MOSFET phase 3
CSBLS3	Capacitor snubber low-side MOSFET phase 3
CGDLS3	Gate-drain capacitor low-side MOSFET phase 3
CGSLS3	Gate-source capacitor low-side MOSFET phase 3

9 Schematics and layout baseboard

9.1 Schematics baseboard

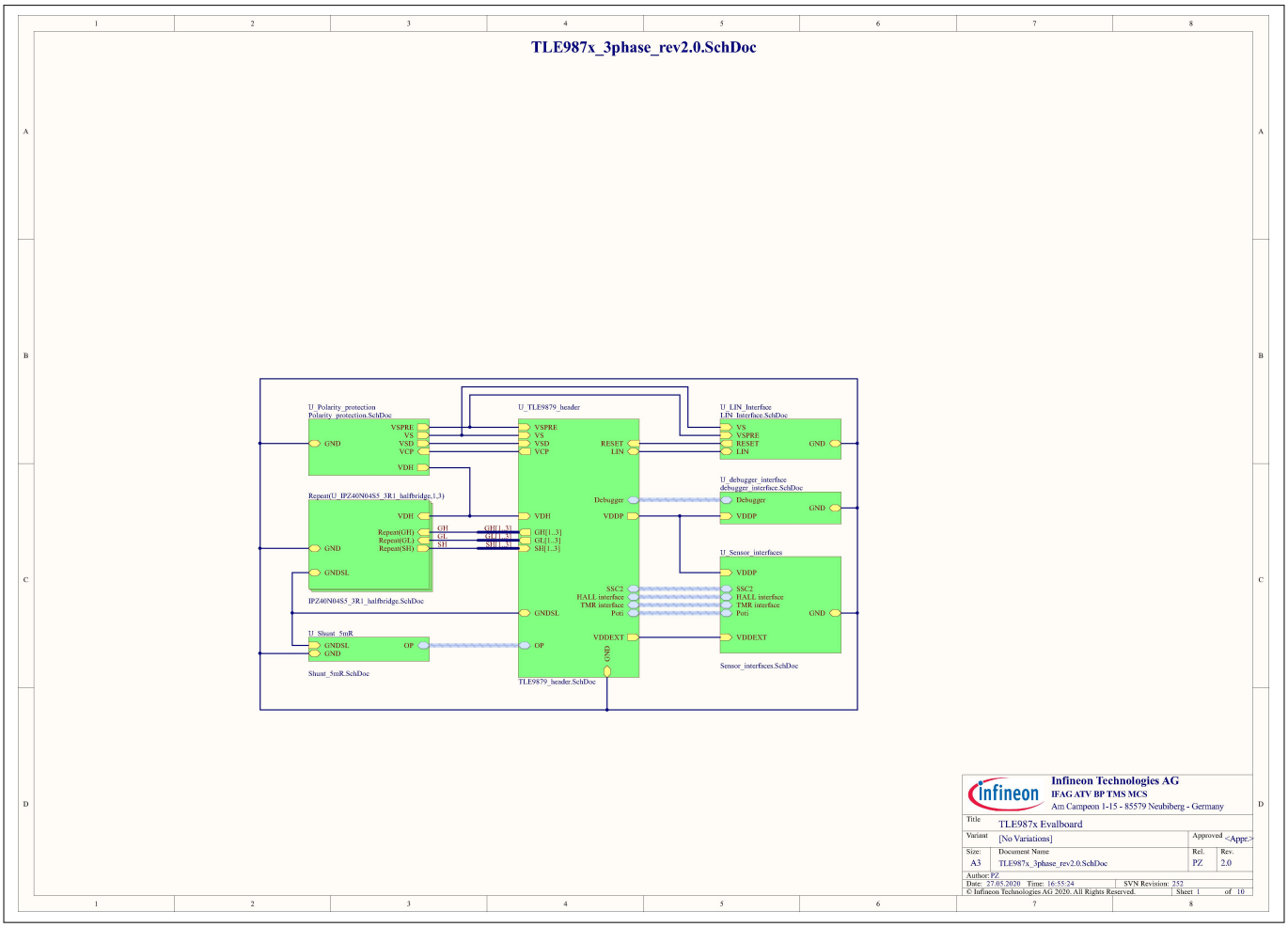

Figure 14 Schematics Sheet 1

9 Schematics and layout baseboard

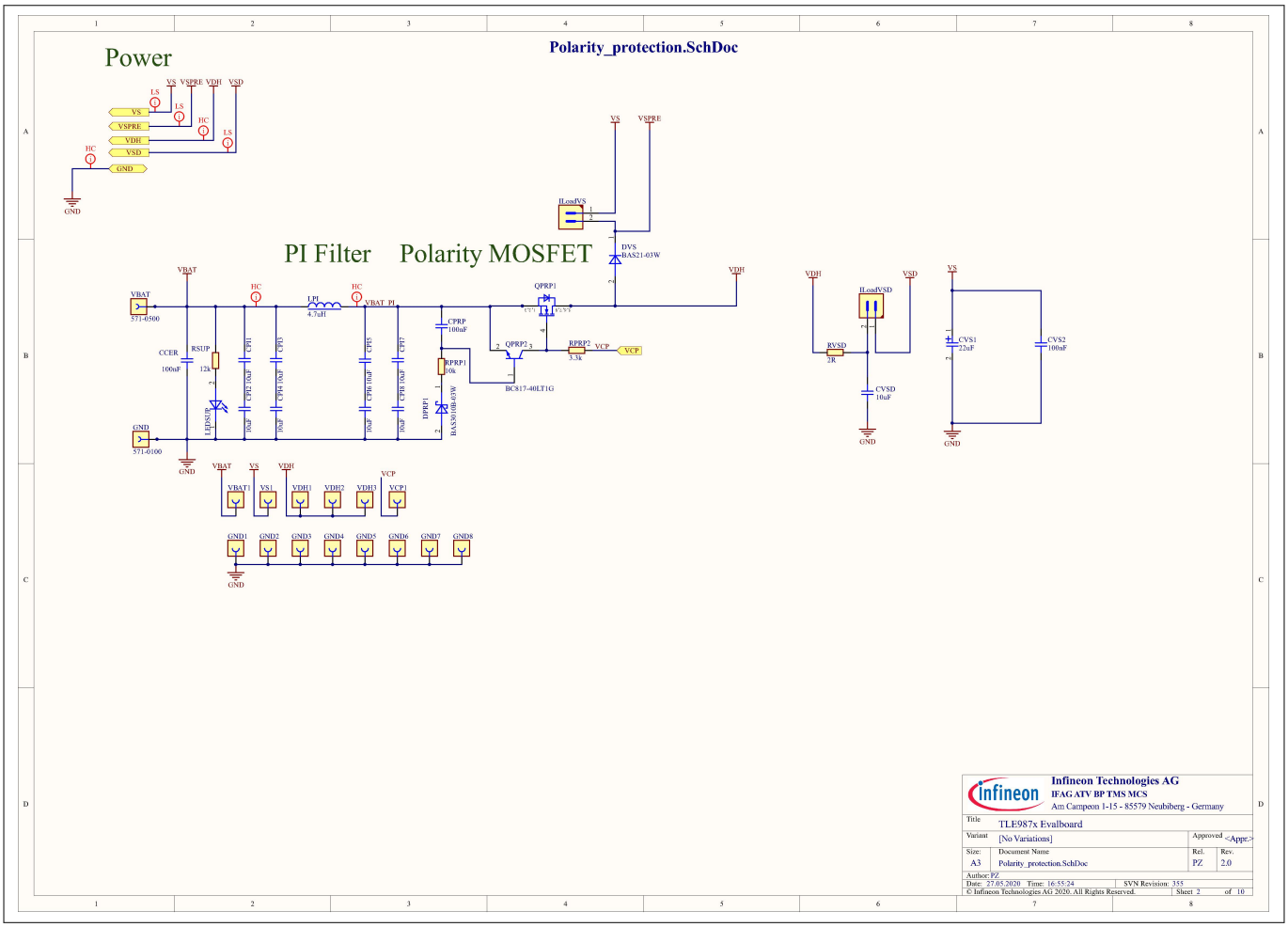

Figure 15 Schematics Sheet 2

9 Schematics and layout baseboard

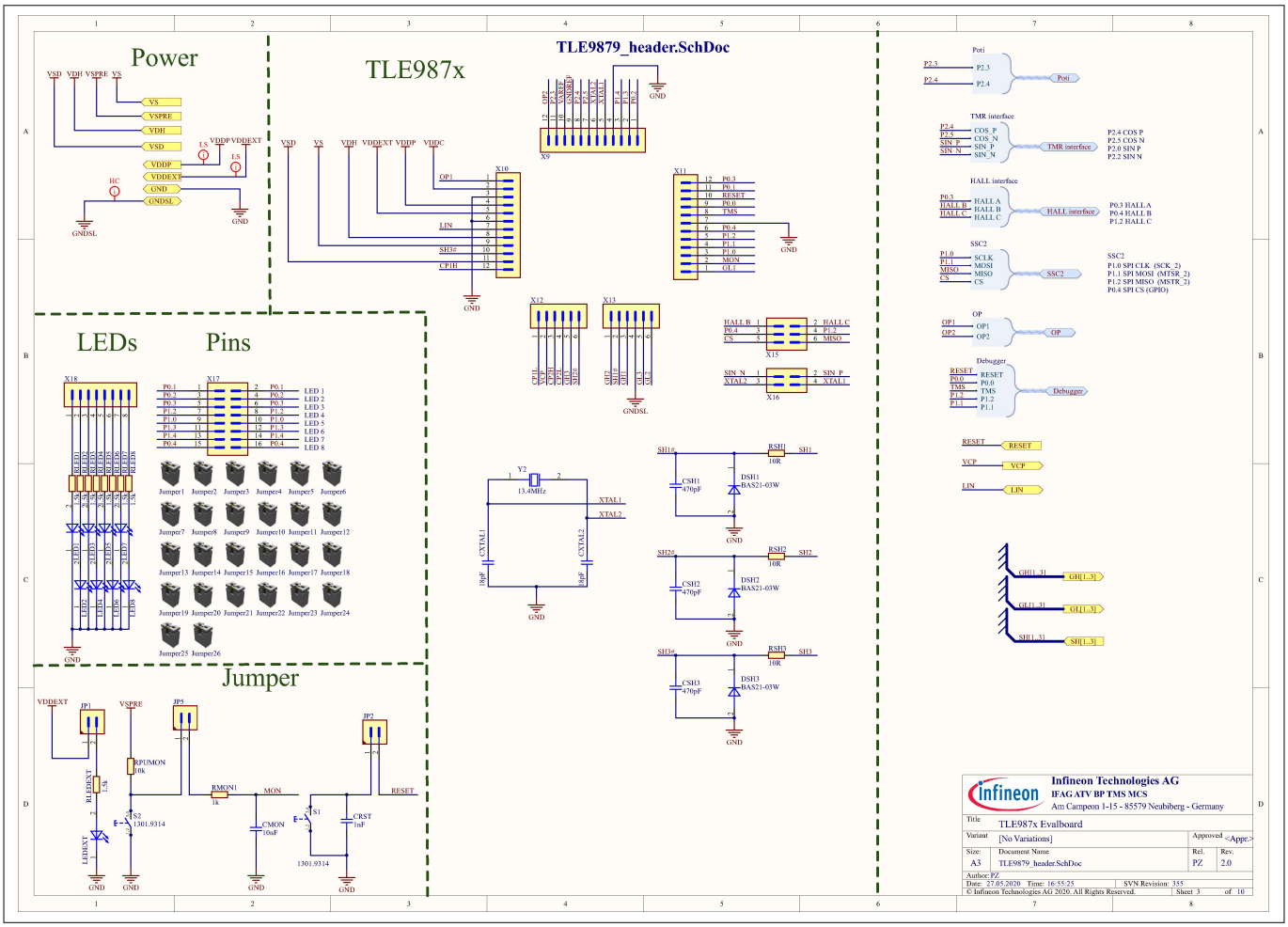

Figure 16 Schematics Sheet 3

9 Schematics and layout baseboard

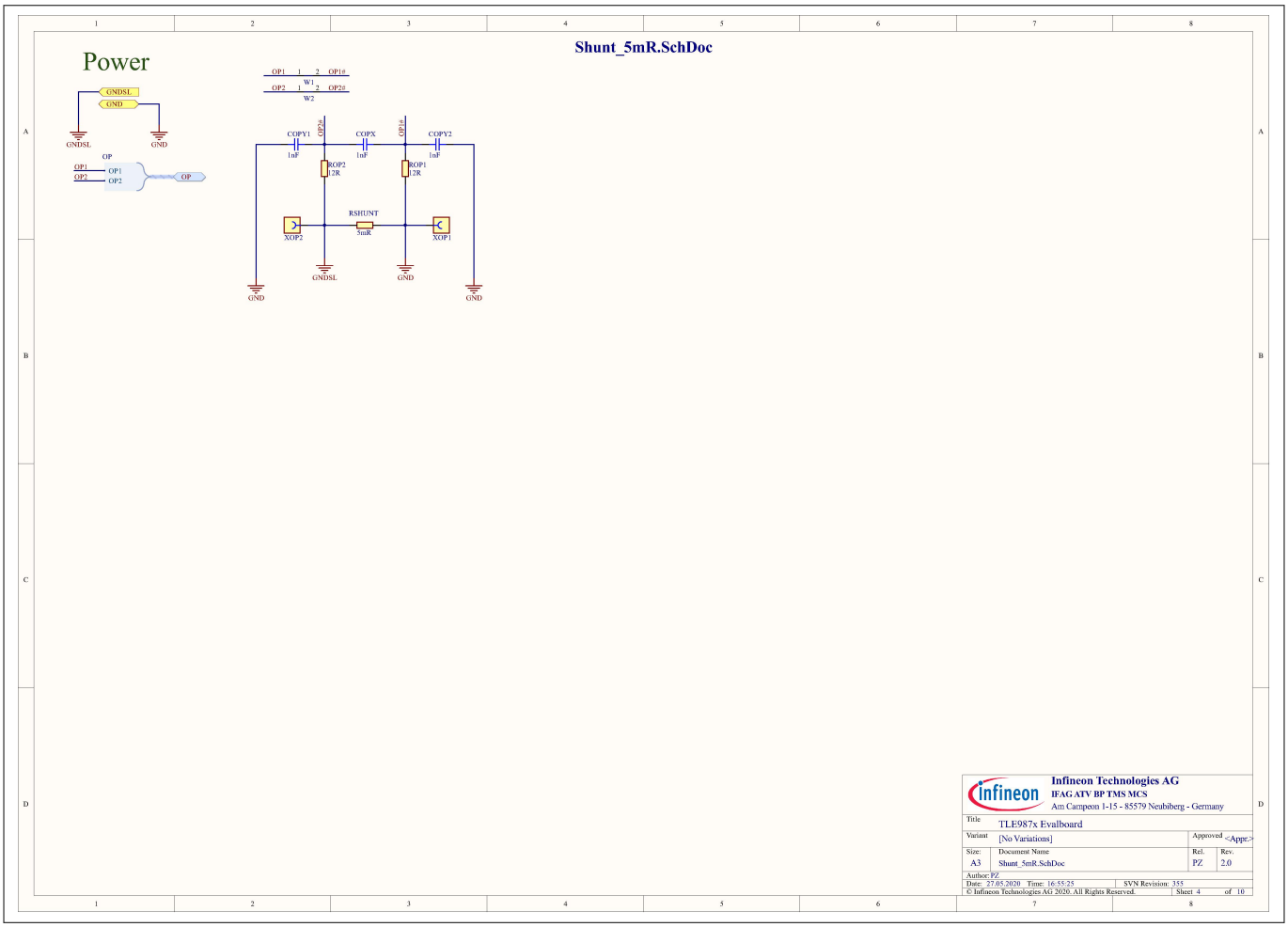

Figure 17 Schematics Sheet 4

9 Schematics and layout baseboard

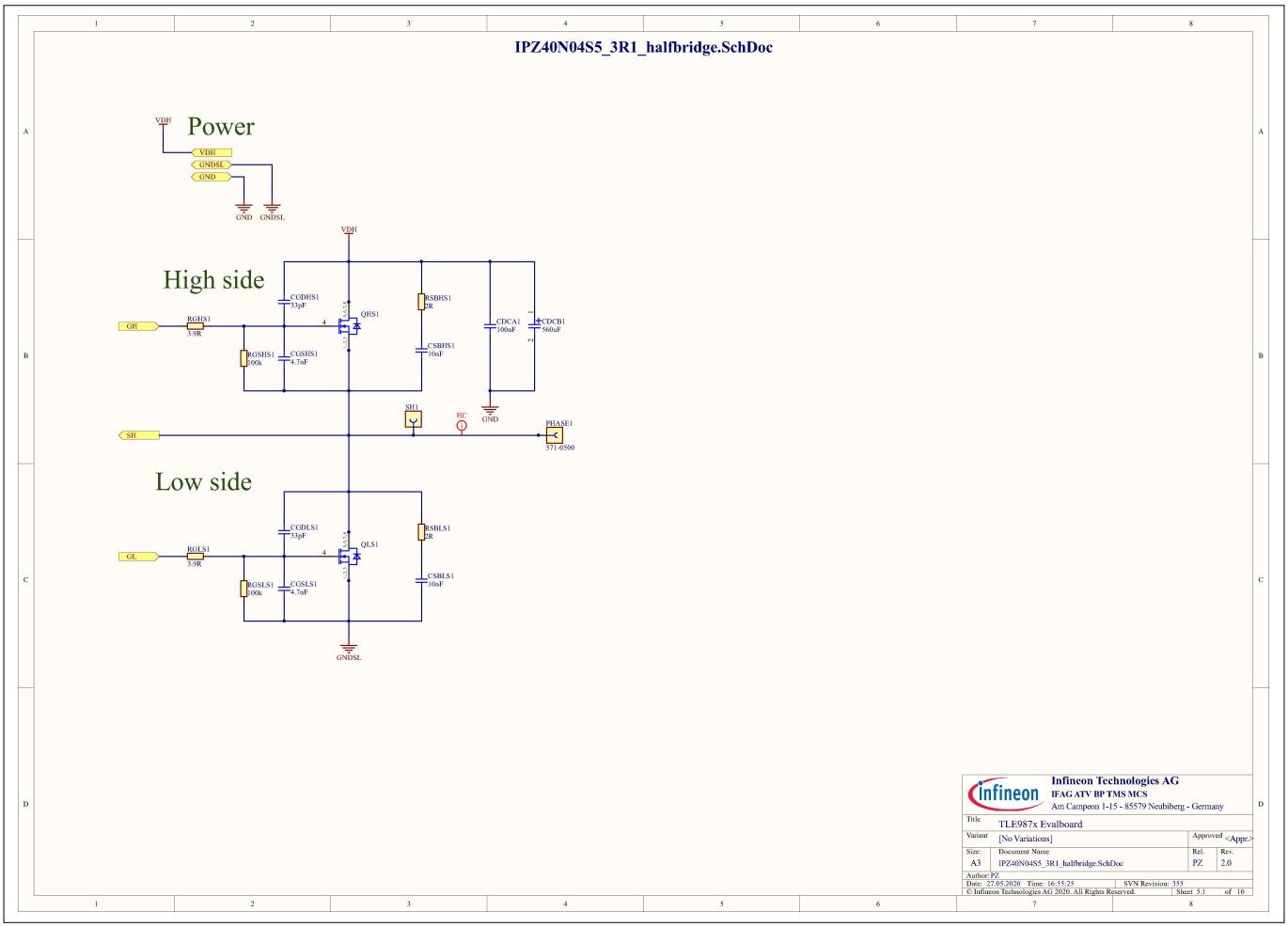

Figure 18 Schematics Sheet 5

9 Schematics and layout baseboard

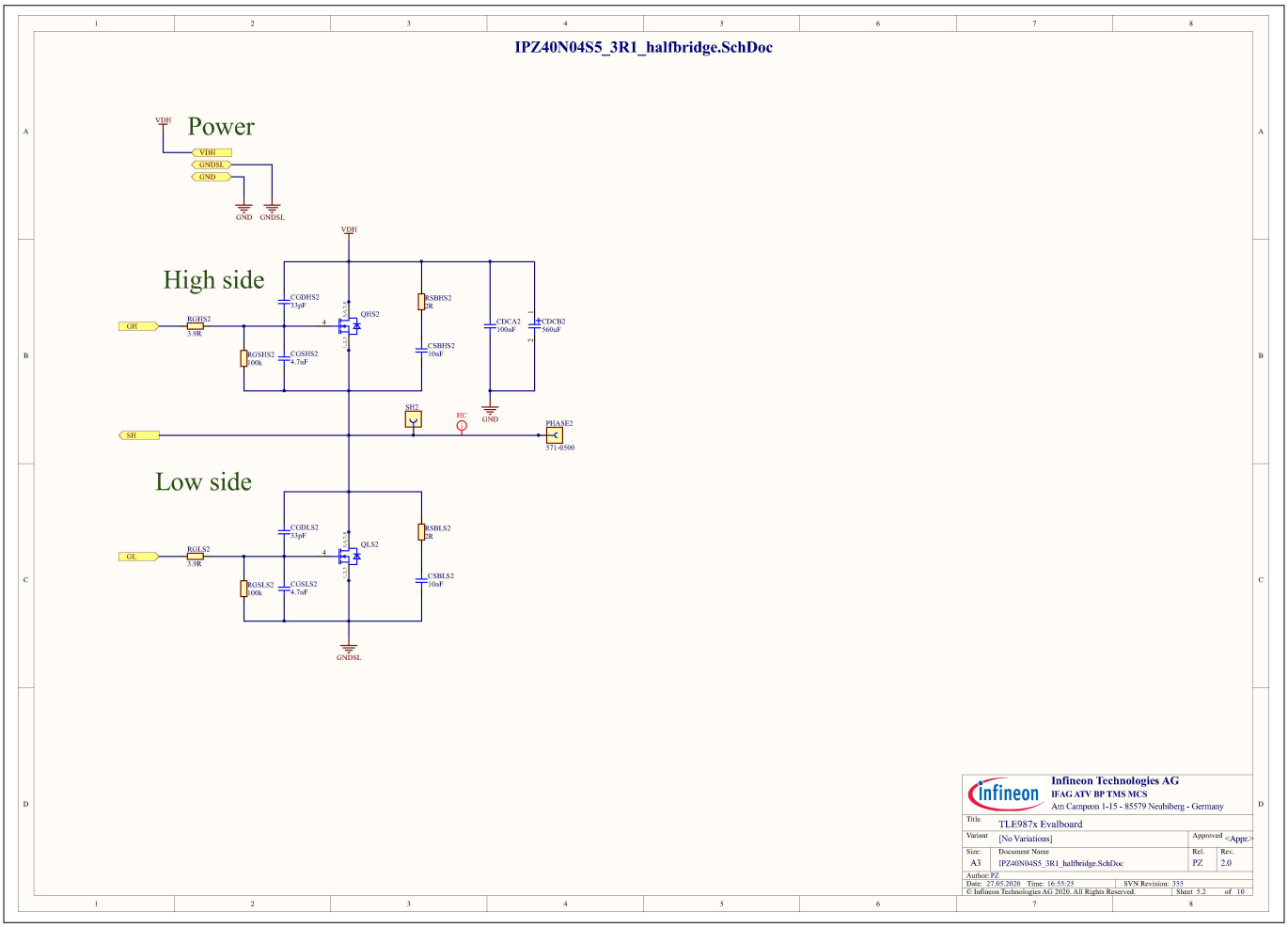

Figure 19 Schematics Sheet 6

9 Schematics and layout baseboard

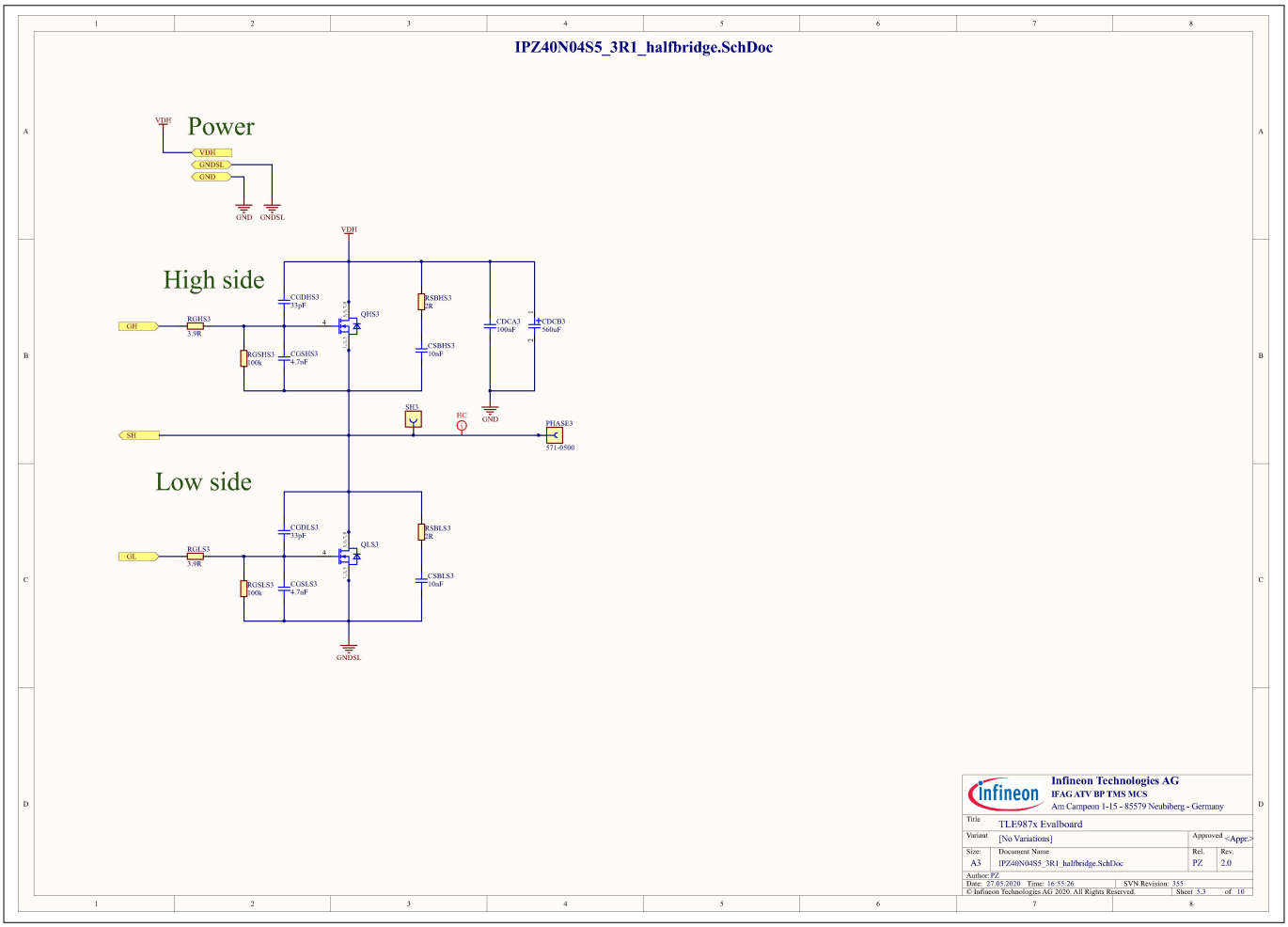

Figure 20 Schematics Sheet 7

9 Schematics and layout baseboard

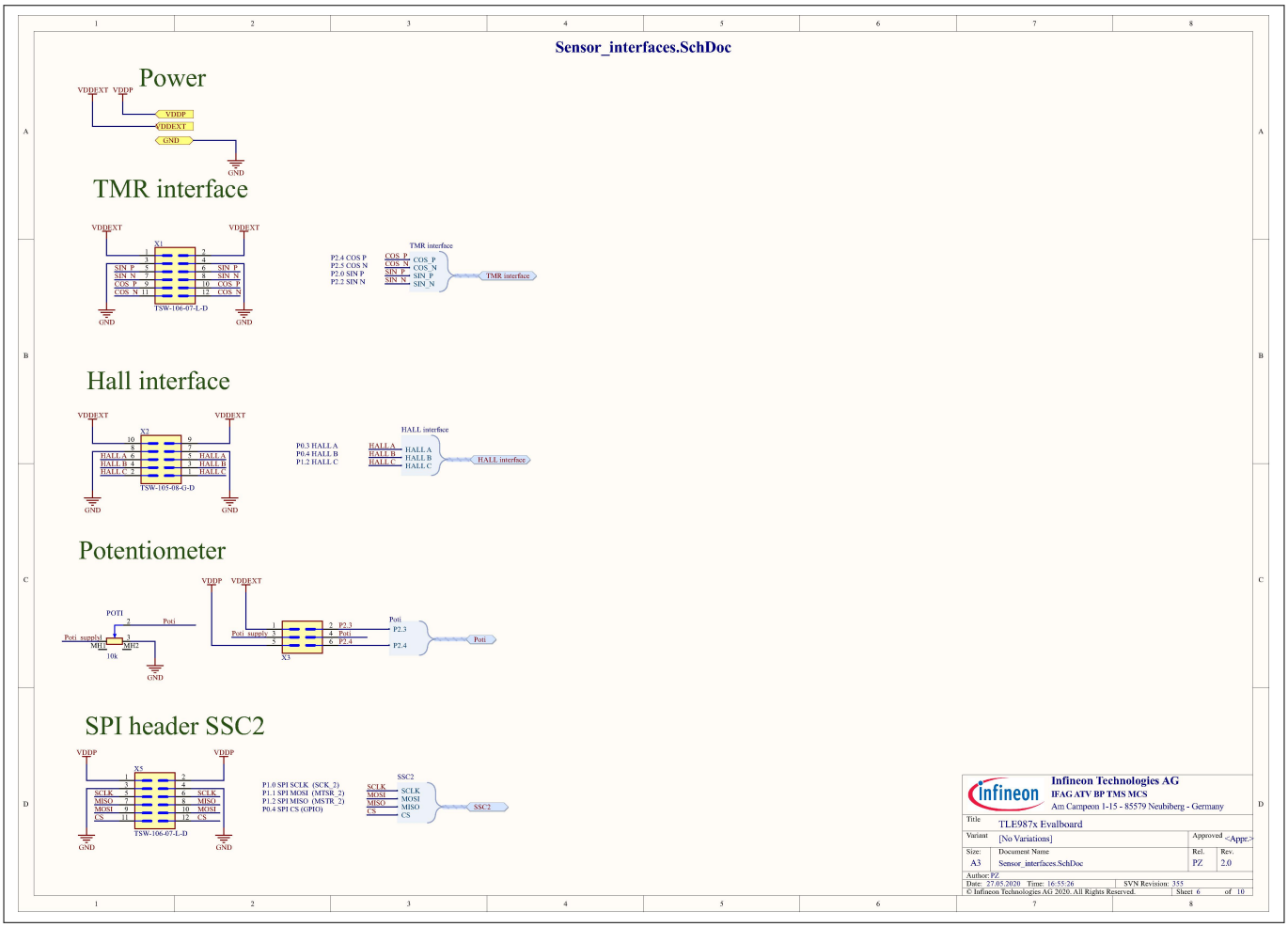

Figure 21 Schematics Sheet 8

9 Schematics and layout baseboard

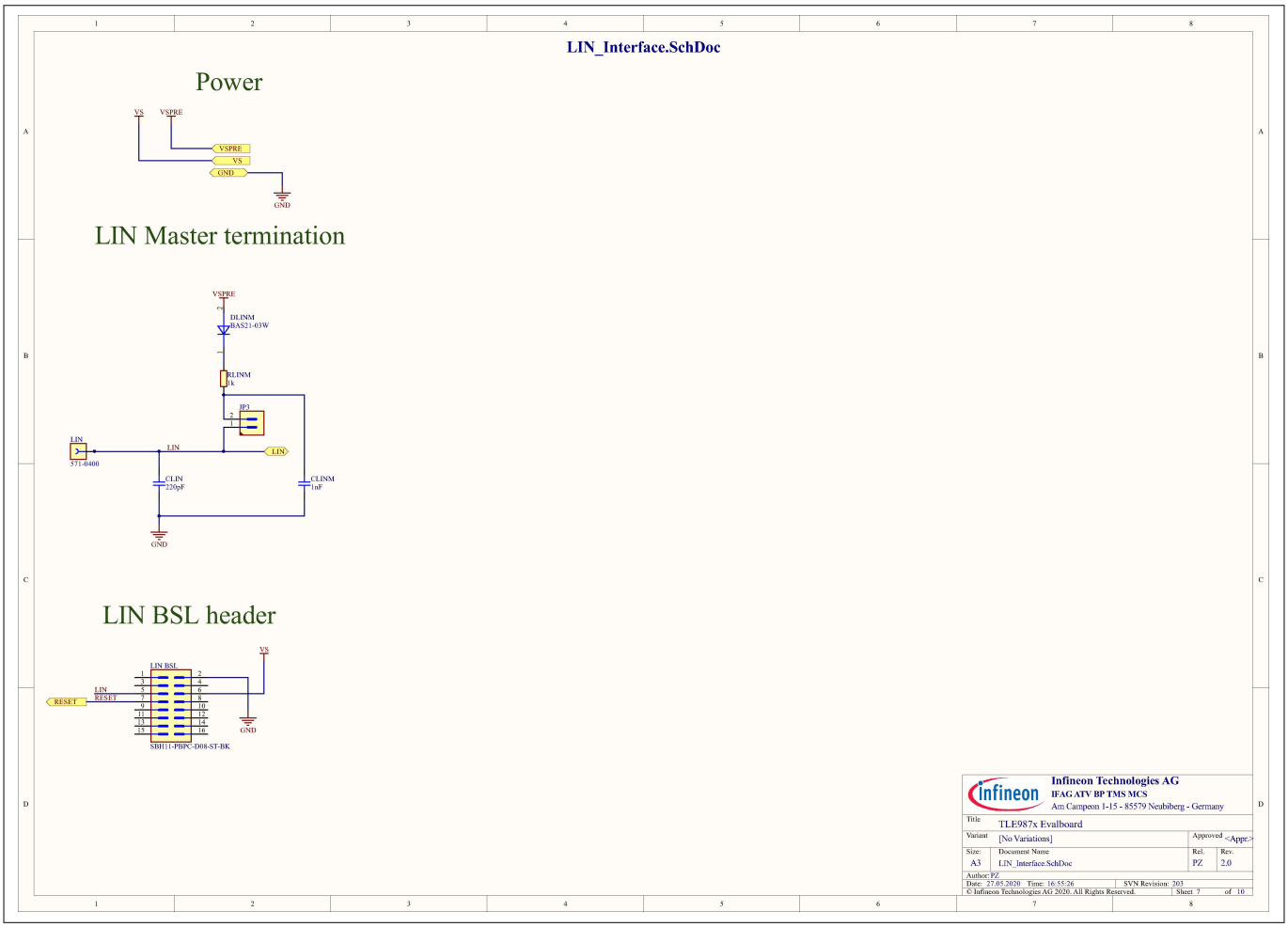

Figure 22 Schematics Sheet 9

9 Schematics and layout baseboard

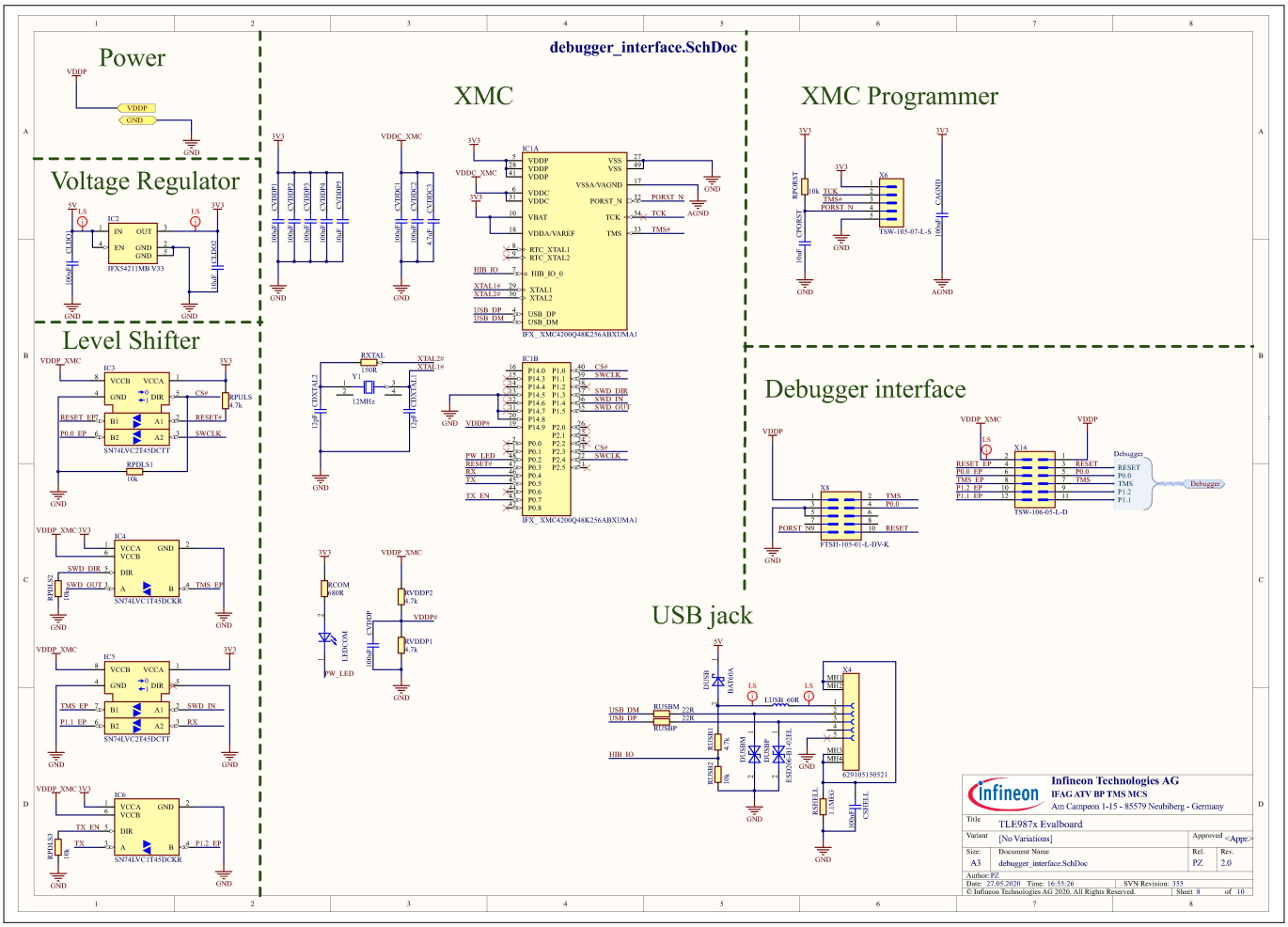

Figure 23 Schematics Sheet 10

9.2 Layout baseboard

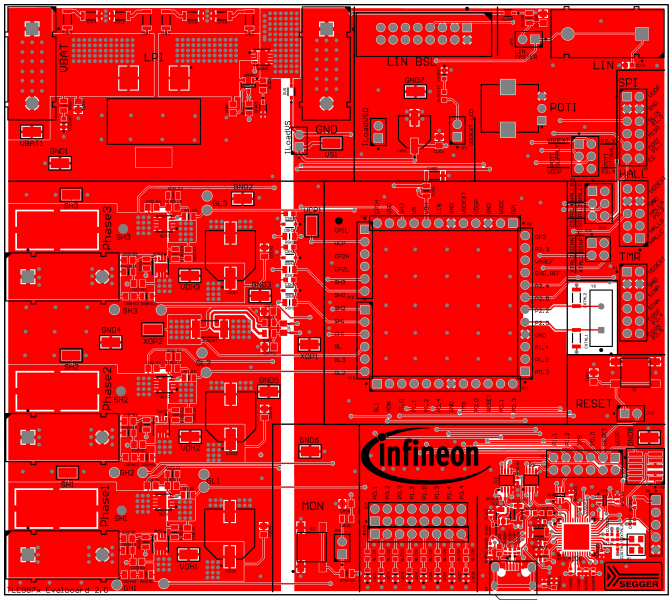

Figure 24 Top layer

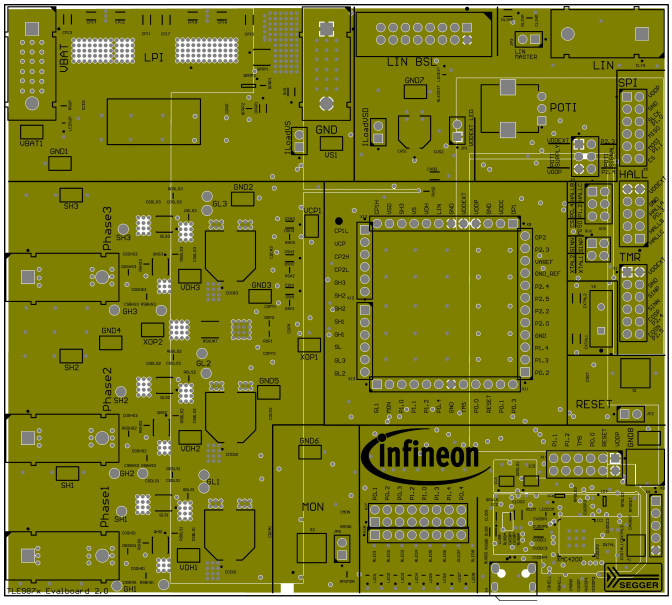

Figure 25 Power layer

9 Schematics and layout baseboard

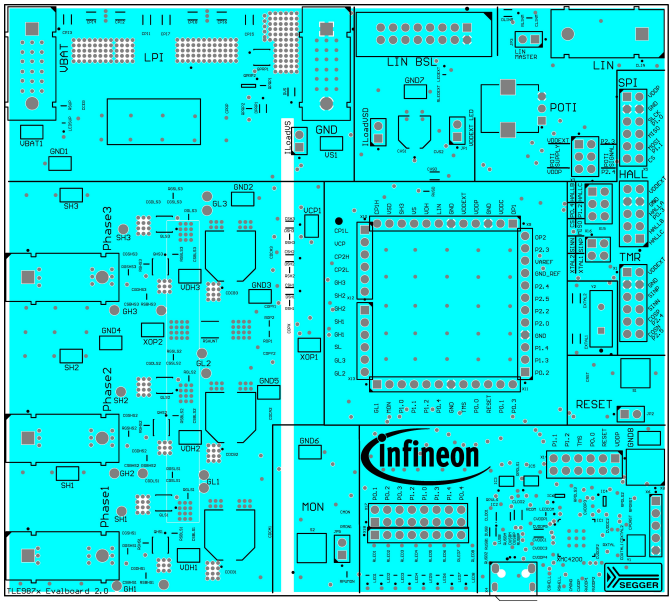

Figure 26 Ground layer

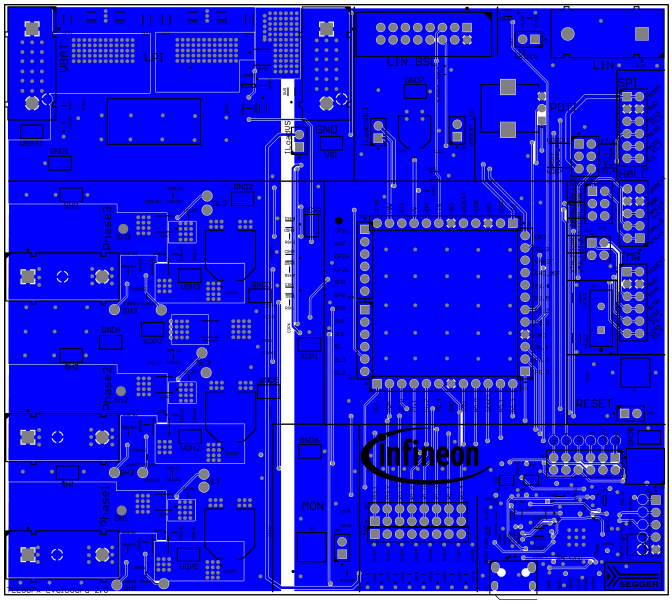

Figure 27 Bottom layer

10 Schematics and layout VQFN socket

10.1 Schematics VQFN socket

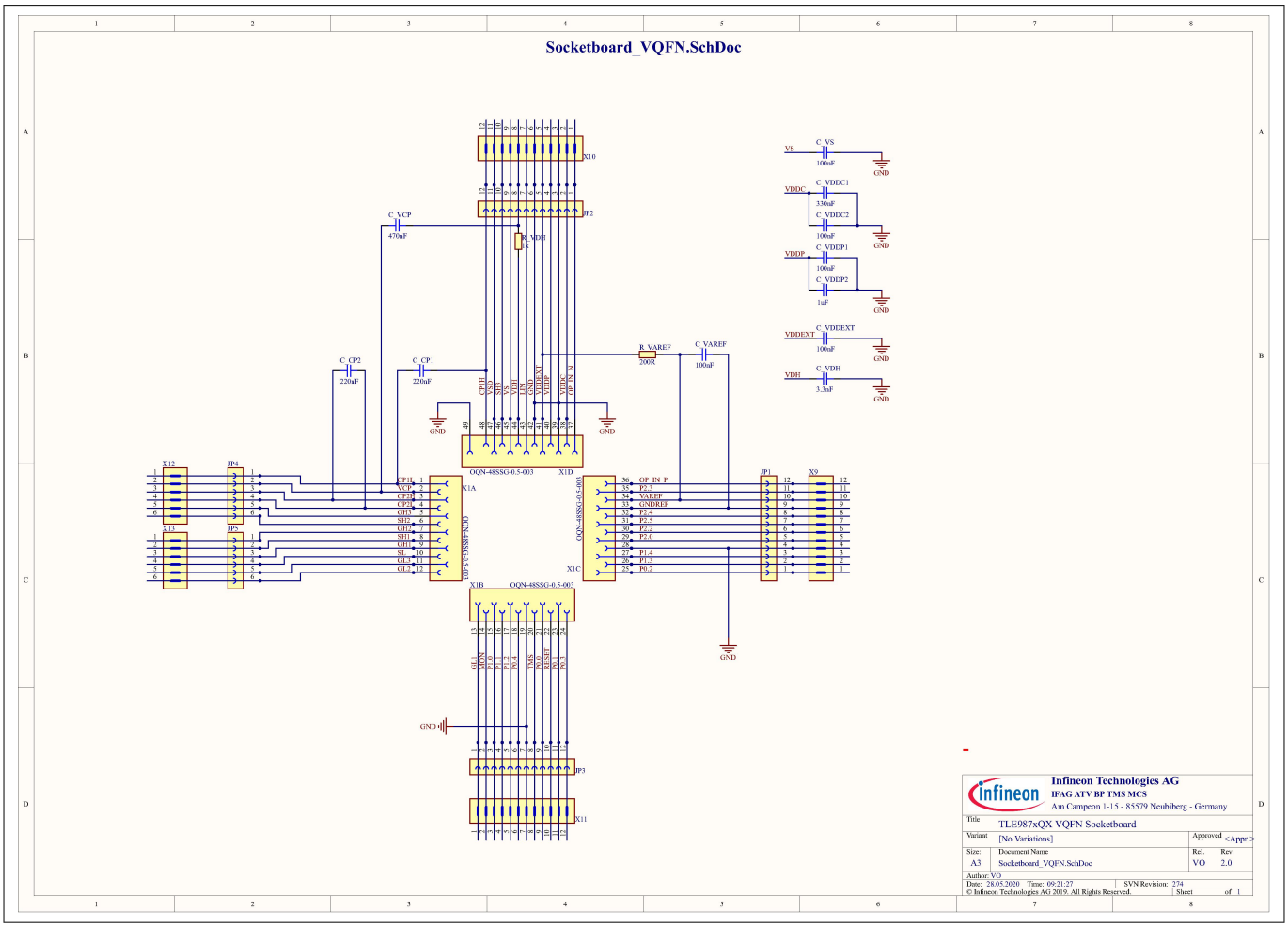

Figure 28 Schematics VQFN socket

10.2 Layout VQFN socket

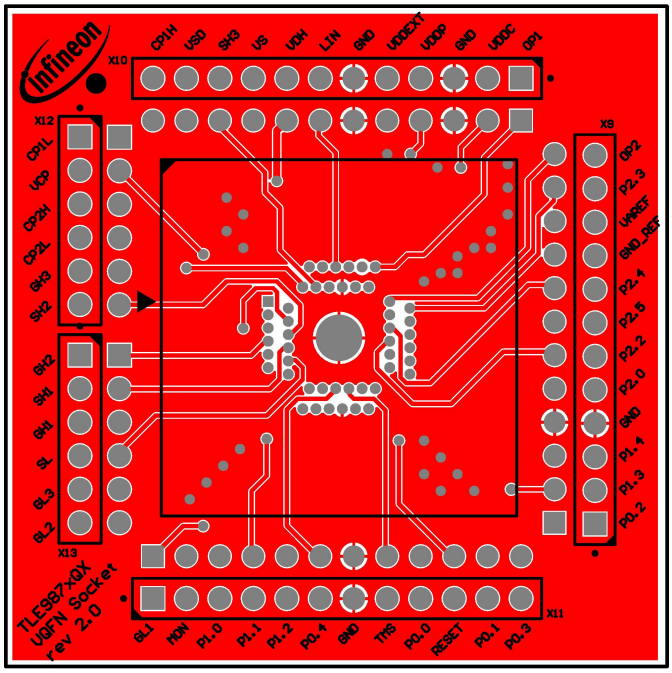

Figure 29 Top layer VQFN socket

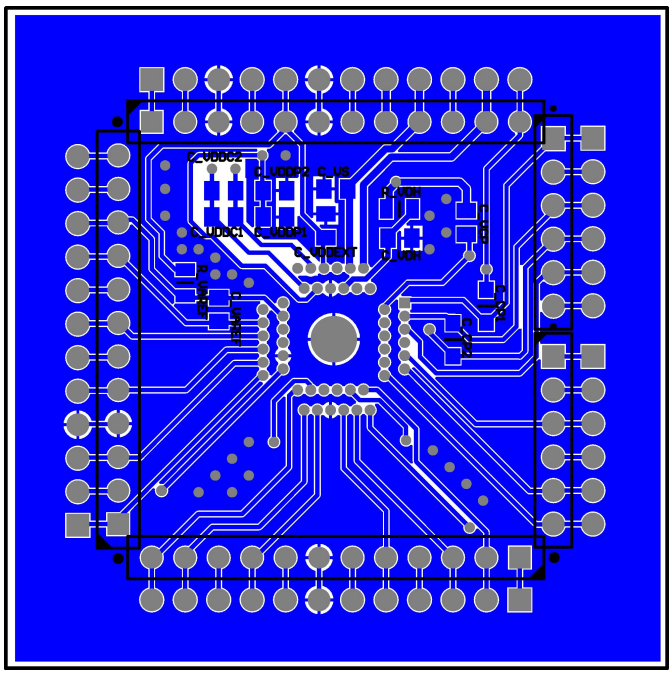

Figure 30 Bottom layer VQFN socket (mirrored)

11 Schematics and layout TQFP socket

11.1 Schematics TQFP socket

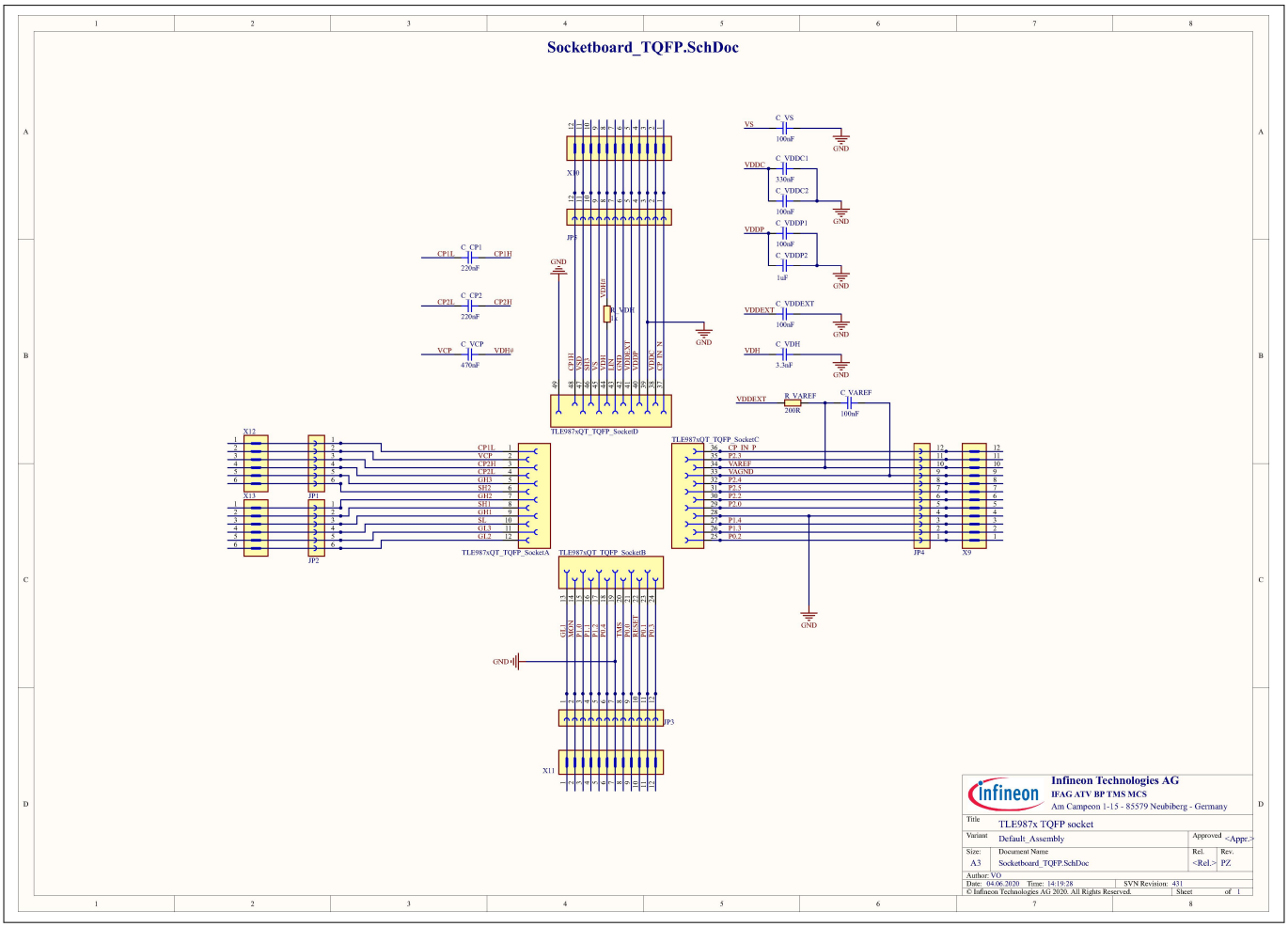

Figure 31 Schematics TQFP socket

11.2 Layout TQFP socket

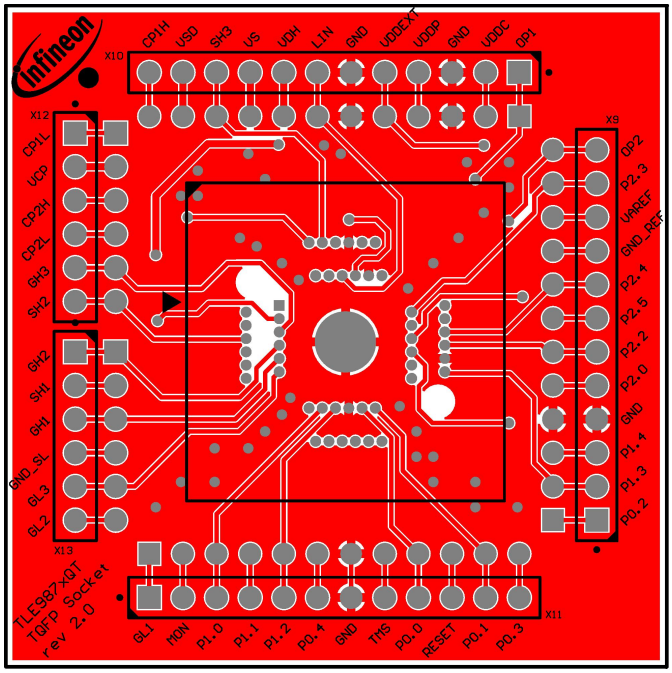

Figure 32 Top layer TQFP socket

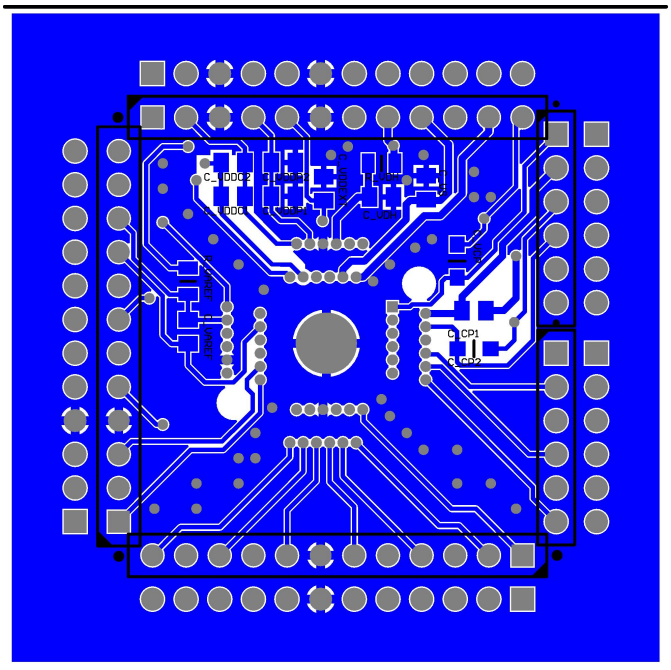

Figure 33 Bottom layer TQFP socket (mirrored)

12 Revision history

Revision	Date	Changes
v1.0	2020-07-30	Initial creation.