Pin	Default function	Pad Function Mux				GPIO Setting						
		Register=2	Register=1	Register=0	Register	Input (R)	IE	OEN	Output	Polarity	DS	Act as GPIO
PWM0_N/ UART_RTS/ TX_CYC2PA/ lc_comp_ain<3>/ sar_aio<3>/ PB<3>	GPIO	TX_CYC2PA	UART_RTS	PWM0_N	0x5aa[7:6]	0x588[3]	afe_0xbd [3]	0x58a[3]	0x58b[3]	0x58c[3]	afe_0xbf [3]	0x58e[3]
PWM4/ lc_comp_ain<4>/ sar_aio<4>/ PB<4>	GPIO	/	PWM4	/	0x5ab[1:0]	0x588[4]	afe_0xbd [4]	0x58a[4]	0x58b[4]	0x58c[4]	afe_0xbf [4]	0x58e[4]
PWM5/ lc_comp_ain<5>/ sar_aio<5>/ PB<5>	GPIO	/	PWM5	/	0x5ab[3:2]	0x588[5]	afe_0xbd [5]	0x58a[5]	0x58b[5]	0x58c[5]	afe_0xbf [5]	0x58e[5]
SPI_DI/ UART_RTS/ lc_comp_ain<6>/ sar_aio<6>/ PB<6>	SPI_DI	UART_RTS	SPI_DI	/	0x5ab[5:4]	0x588[6]	afe_0xbd [6]	0x58a[6]	0x58b[6]	0x58c[6]	afe_0xbf [6]	0x58e[6]
SPI_DO/ UART_RX/ lc_comp_ain<7>/ sar_aio<7>/ PB<7>	SPI_DO	UART_RX	SPI_DO	/	0x5ab[7:6]	0x588[7]	afe_0xbd [7]	0x58a[7]	0x58b[7]	0x58c[7]	afe_0xbf [7]	0x58e[7]
I2C_SDA/ PWM4_N/ UART_RTS/ PGA_P0/ PC<0>	GPIO	UART_RTS	PWM4_N	I2C_SDA	0x5ac[1:0]	0x590[0]	afe_0xc0 [0]	0x592[0]	0x593[0]	0x594[0]	afe_0xc2 [0]	0x596[0]
I2C_SCK/ PWM1_N/ PWM0/ PGA_N0/ PC<1>	GPIO	PWM0	PWM1_N	I2C_SCK	0x5ac[3:2]	0x590[1]	afe_0xc0 [1]	0x592[1]	0x593[1]	0x594[1]	afe_0xc2 [1]	0x596[1]
PWM0/ UART_TX/ I2C_SDA/ XC32K_O/ PGA_P1/ PC<2>	GPIO	I2C_SDA	UART_TX	PWM0	0x5ac[5:4]	0x590[2]	afe_0xc0 [2]	0x592[2]	0x593[2]	0x594[2]	afe_0xc2 [2]	0x596[2]
PWM1/ UART_RX/ I2C_SCK/ XC32K_I/ PGA_N1/ PC<3>	GPIO	I2C_SCK	UART_RX	PWM1	0x5ac[7:6]	0x590[3]	afe_0xc0 [3]	0x592[3]	0x593[3]	0x594[3]	afe_0xc2 [3]	0x596[3]