

650V SuperGaN® GaN FET in PQFN (source tab)

Description

The TP65H480G4JSG 650V, 480mΩ Gallium Nitride (GaN) FET is a normally-off device using Transphorm's Gen IV platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

Related Literature

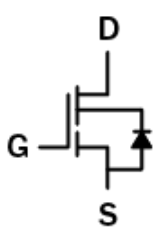
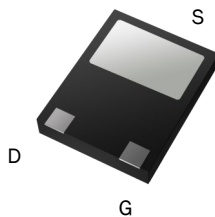
- [AN0003](#): Printed Circuit Board Layout and Probing
- [AN0007](#): Recommendations for Vapor Phase Reflow
- [AN0009](#): Recommended External Circuitry for GaN FETs
- [AN0012](#): PQFN Tape and Reel Information

Product Series and Ordering Information

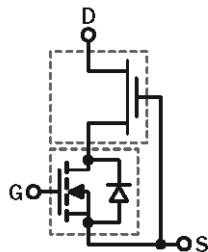
Part Number	Package	Package Configuration
TP65H480G4JSG-TR*	5x6 PQFN	Source

* "-TR" suffix refers to tape and reel. Refer to AN0012 for details.

**TP65H480G4JSG
PQFN
(top view)**



Cascode Schematic Symbol



Cascode Device Structure

Features

- Gen IV technology
- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
 - Wide gate safety margin
 - Transient over-voltage capability
- Very low Q_{RR}
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

Benefits

- Achieves increased efficiency in both hard- and soft-switched circuits
 - Increased power density
 - Reduced system size and weight
 - Overall lower system cost
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

Applications

- Consumer
- Power adapters
- Low power SMPS
- Lighting



Key Specifications

V_{DS} (V)	650
$V_{DSS(TR)}$ (V)	800
$R_{DS(on)}$ (mΩ) max*	560
Q_{RR} (nC) typ	14
Q_G (nC) typ	9

* Dynamic $R_{DS(on)}$; see Figures 18 and 19

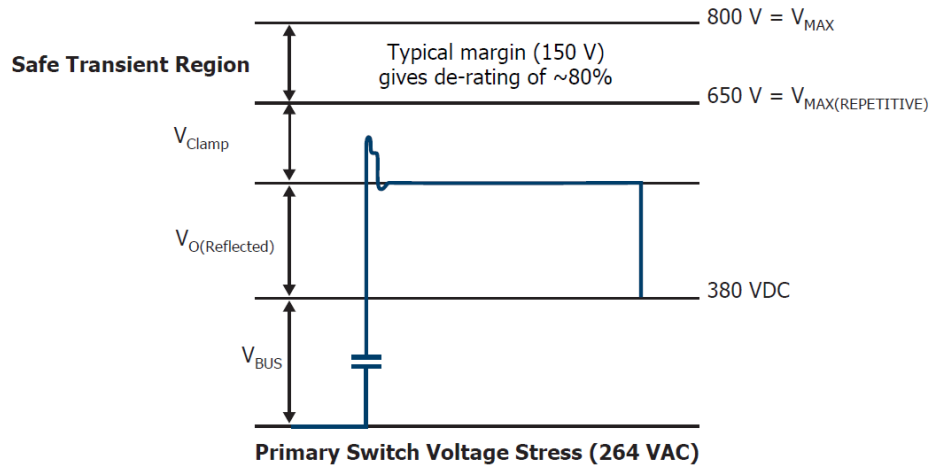
TP65H480G4JSG

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise stated.)

Symbol	Parameter	Limit Value	Unit	
V_{DSS}	Drain to source voltage ($T_J = -55^\circ\text{C}$ to 150°C)	650	V	
$V_{DSS(TR)}$	Transient drain to source voltage ^a	800		
V_{GSS}	Gate to source voltage	± 18		
P_D	Maximum power dissipation @ $T_C=25^\circ\text{C}$	13.2	W	
I_D	Continuous drain current @ $T_C=25^\circ\text{C}$ ^b	3.6	A	
	Continuous drain current @ $T_C=100^\circ\text{C}$ ^b	2.3	A	
I_{DM}	Pulsed drain current (pulse width: 10 μs)	17	A	
T_C	Operating temperature	Case	-55 to +150	$^\circ\text{C}$
T_J		Junction	-55 to +150	$^\circ\text{C}$
T_S	Storage temperature	-55 to +150	$^\circ\text{C}$	
T_{SOLD}	Reflow soldering temperature ^c	260	$^\circ\text{C}$	

Notes:

- In off-state, spike duty cycle $D < 0.01$, spike duration $< 30\mu\text{s}$.
- For increased stability at high current operation, see Circuit Implementation on page 3
- Reflow MSL3



Thermal Resistance

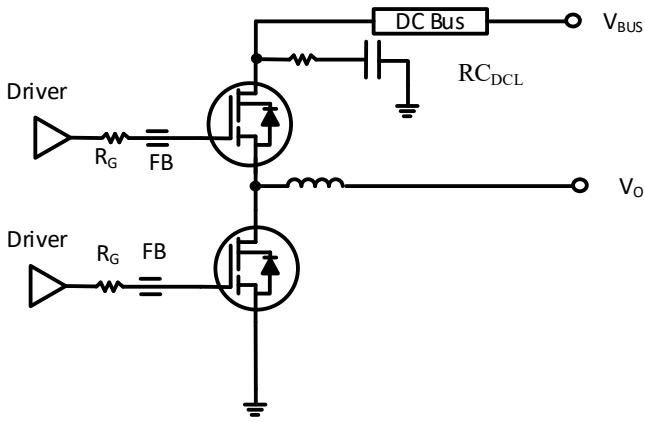
Symbol	Parameter	Maximum	Unit
$R_{\theta JC}$	Junction-to-case	9.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient ^d	50	$^\circ\text{C}/\text{W}$

Notes:

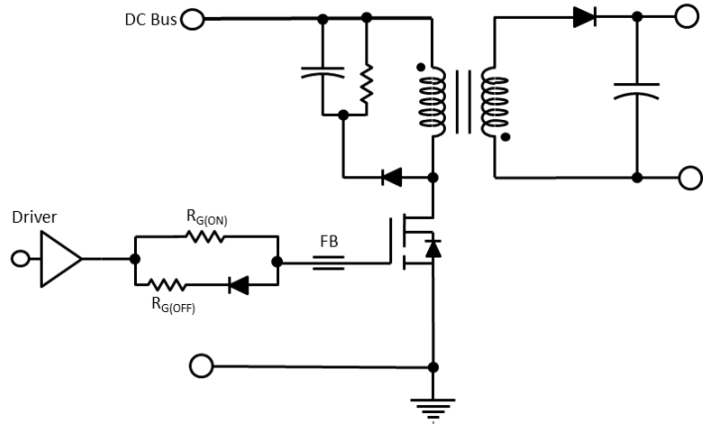
- Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm² copper area and 70 μm thickness)

TP65H480G4JSG

Circuit Implementation



Simplified Half-bridge Schematic



Simplified Single Ended Schematic

Recommended gate drive: (0V, 8V) with $R_{G(tot)} = 30 \Omega^a$

Recommended gate drive: (0V, 12V) with $R_{G(ON)} = 100$ to 300Ω
 $R_{G(OFF)} = 0$ to 15Ω

Gate Ferrite Bead (FB1)	Required DC Link RC Snubber (RC_{DCL}) ^b
240 Ω @ 100MHz	4.7-10nF + 5 Ω

Notes:

- For bridge topologies only. R_G could be much smaller in single ended topologies.
- RC_{DCL} should be placed as close as possible to the drain pin.

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Electrical Parameters (T_J=25 °C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
V _{DSS(BL)}	Maximum drain-source voltage	650	—	—	V	V _{GS} =0V
V _{GS(th)}	Gate threshold voltage	1.6	2.2	2.8	V	V _{DS} =V _{GS} , I _D =0.5mA
ΔV _{GS(th)} /T _J	Gate threshold voltage temperature coefficient	—	-5.8	—	mV/°C	
R _{DS(on)eff}	Drain-source on-resistance ^a	—	480	560	mΩ	V _{GS} =8V, I _D =3.4A
		—	1000	—		V _{GS} =8V, I _D =3.4A, T _J =150 °C
I _{DSS}	Drain-to-source leakage current	—	1	10	μA	V _{DS} =650V, V _{GS} =0V
		—	5	—		V _{DS} =650V, V _{GS} =0V, T _J =150 °C
I _{GSS}	Gate-to-source forward leakage current	—	—	100	nA	V _{GS} =18V
	Gate-to-source reverse leakage current	—	—	-100		V _{GS} =-18V
C _{ISS}	Input capacitance	—	760	—	pF	V _{GS} =0V, V _{DS} =400V, f=1MHz
C _{OSS}	Output capacitance	—	9	—		
C _{RSS}	Reverse transfer capacitance	—	1.5	—		
C _{O(er)}	Output capacitance, energy related ^b	—	13	—	pF	V _{GS} =0V, V _{DS} =0V to 400V
C _{O(tr)}	Output capacitance, time related ^c	—	29	—		
Q _G	Total gate charge	—	9	—	nC	V _{DS} =400V, V _{GS} =0V to 8V, I _D =3.4A
Q _{GS}	Gate-source charge	—	2.1	—		
Q _{GD}	Gate-drain charge	—	2.1	—		
Q _{OSS}	Output charge	—	13.5	—	nC	V _{GS} =0V, V _{DS} =0V to 400V
t _{D(on)}	Turn-on delay	—	16.6	—	ns	V _{DS} =400V, V _{GS} =0V to 8V, I _D =3.4A, R _G =30Ω, Z _F B=240Ω at 100MHz (See Figure 14)
t _R	Rise time	—	3.5	—		
t _{D(off)}	Turn-off delay	—	53.2	—		
t _F	Fall time	—	7.6	—		

Notes:

- Dynamic R_{DS(on)} value; see Figures 18 and 19 for conditions
- Equivalent capacitance to give same stored energy from 0V to 400V
- Equivalent capacitance to give same charging time from 0V to 400V

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Electrical Parameters ($T_J=25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
I_S	Reverse current	—	—	2.3	A	$V_{GS}=0V$, $T_C=100^\circ\text{C}$, $\leq 25\%$ duty cycle
V_{SD}	Reverse voltage ^a	—	1.3	—	V	$V_{GS}=0V$, $I_S=1.15A$
		—	1.8	—		$V_{GS}=0V$, $I_S=2.3A$
t_{RR}	Reverse recovery time	—	14.5	—	ns	$I_S=3.4A$, $V_{DD}=400V$, $di/dt=1000A/\mu s$
Q_{RR}	Reverse recovery charge	—	14	—	nC	

Notes:

a. Includes dynamic $R_{DS(on)}$ effect

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Typical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise stated)

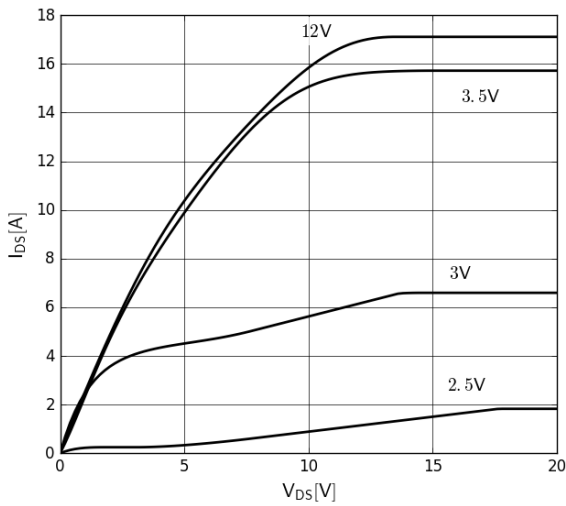


Figure 1. Typical Output Characteristics $T_J=25^\circ\text{C}$

Parameter: V_{GS}

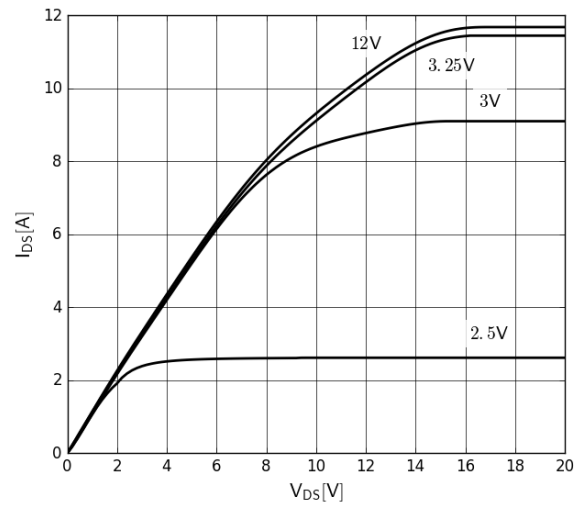


Figure 2. Typical Output Characteristics $T_J=150^\circ\text{C}$

Parameter: V_{GS}

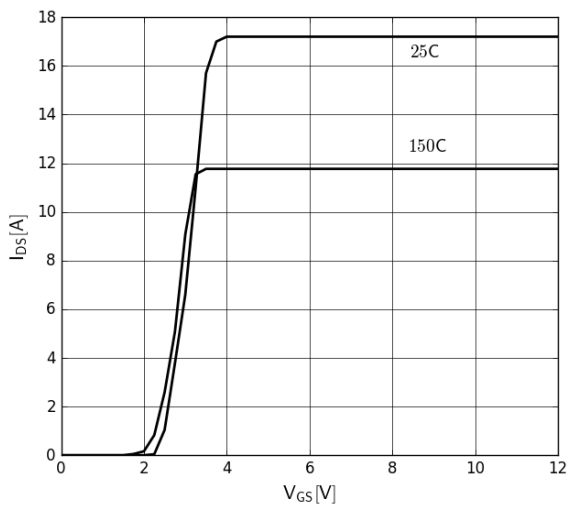


Figure 3. Typical Transfer Characteristics

$V_{DS}=20\text{V}$, parameter: T_J

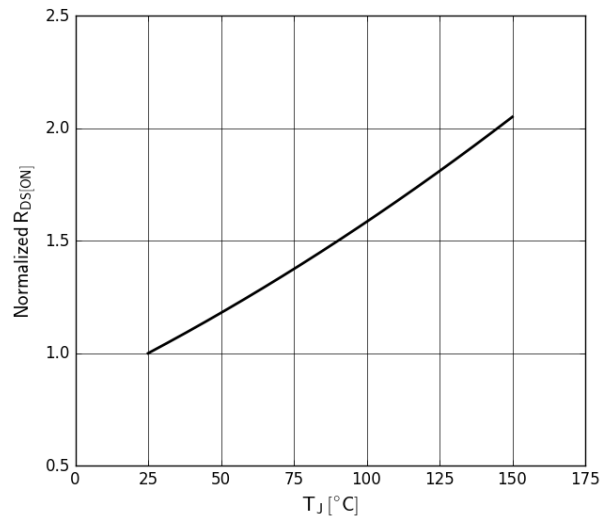


Figure 4. Normalized On-resistance

$I_D=16\text{A}$, $V_{GS}=10\text{V}$

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Typical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise stated)

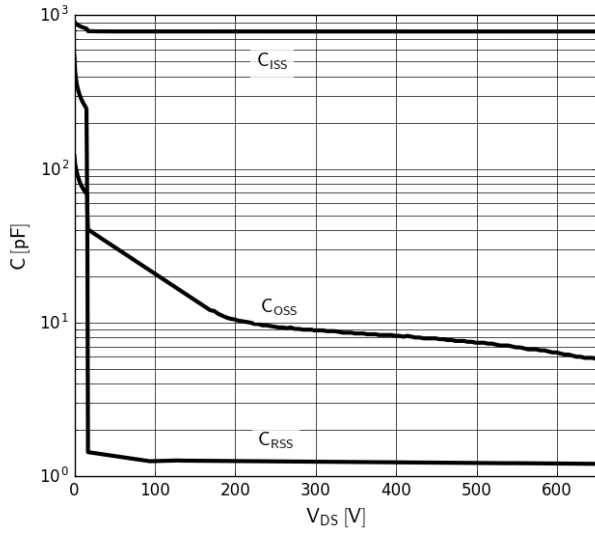


Figure 5. Typical Capacitance

$V_{GS}=0V, f=1MHz$

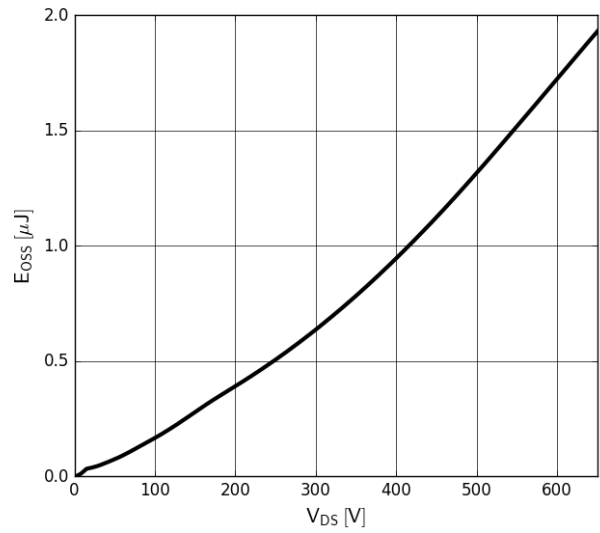


Figure 6. Typical C_{OSS} Stored Energy

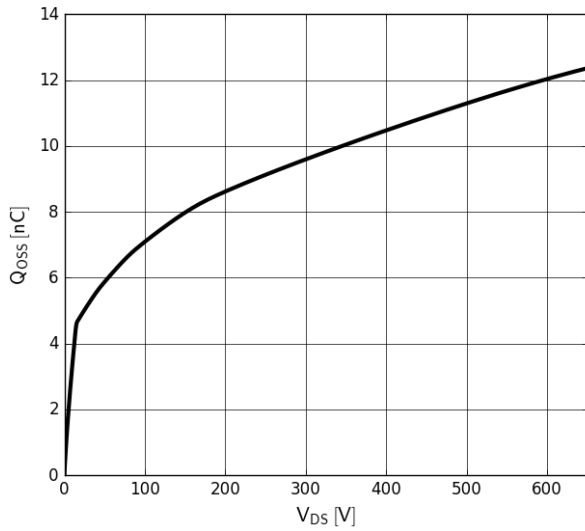


Figure 7. Typical Q_{OSS}

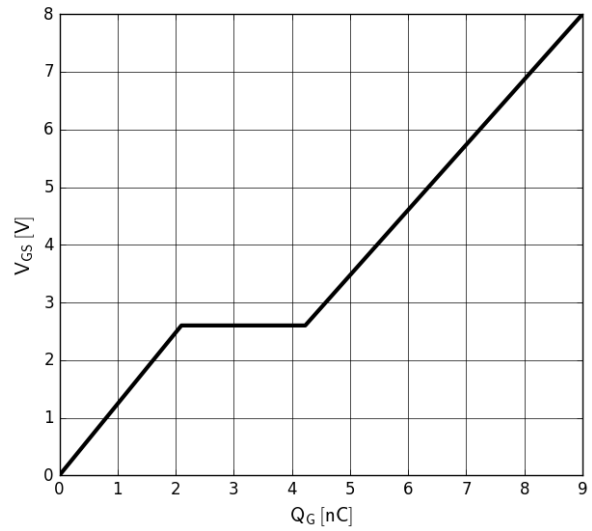


Figure 8. Typical Gate Charge

$I_{DS}=3.4A, V_{DS}=400V$

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Typical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise stated)

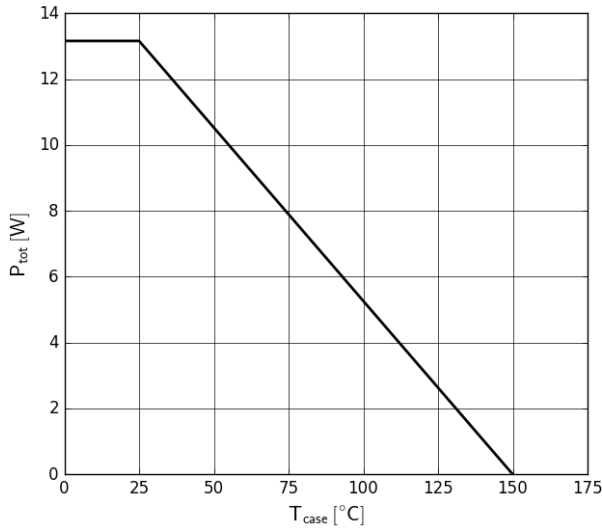


Figure 9. Power Dissipation

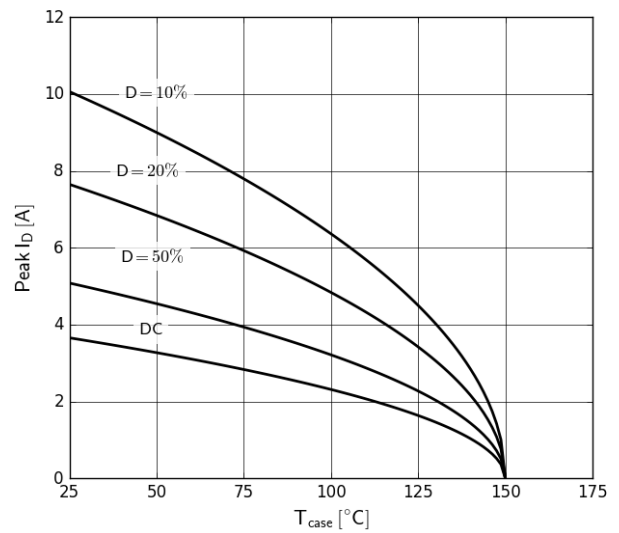


Figure 10. Current Derating
Pulse width $\leq 10\mu\text{s}$, $V_{GS} \geq 10\text{V}$

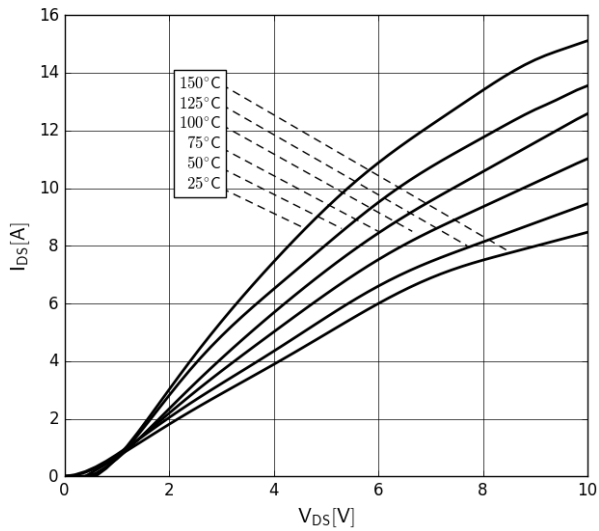


Figure 11. Forward Characteristics of Rev. Diode
 $I_S=f(V_{SD})$, parameter: T_J

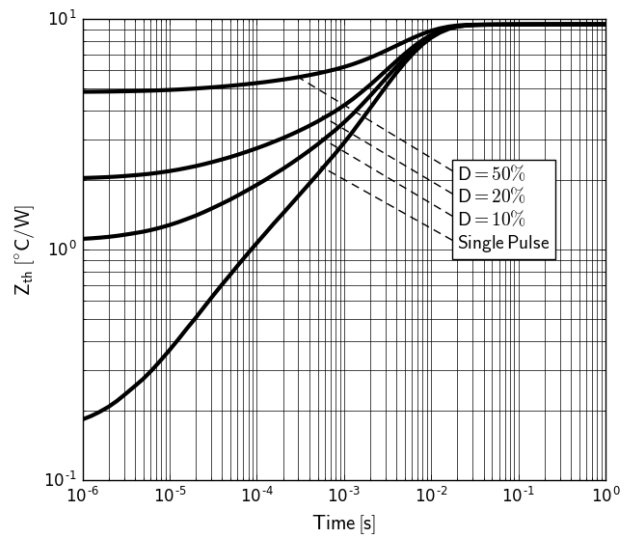


Figure 12. Transient Thermal Resistance

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Typical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise stated)

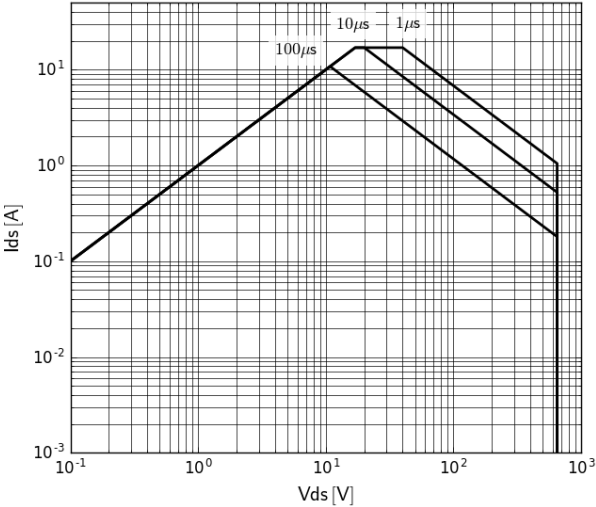


Figure 13. Safe Operating Area $T_c=25^\circ\text{C}$

Test Circuits and Waveforms

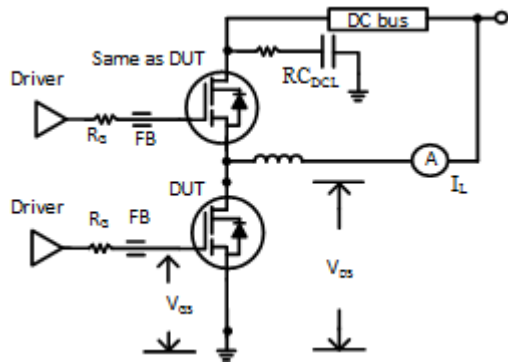


Figure 14. Switching Time Test Circuit
(see circuit implementation on page 3 for methods to ensure clean switching)

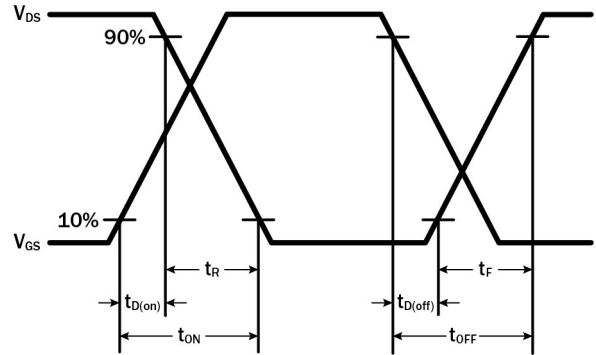


Figure 15. Switching Time Waveform

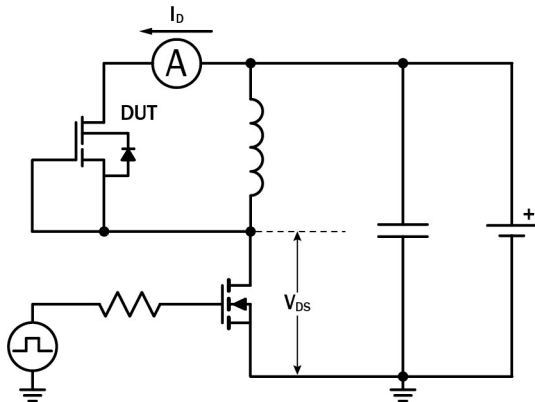


Figure 16. Diode Characteristics Test Circuit

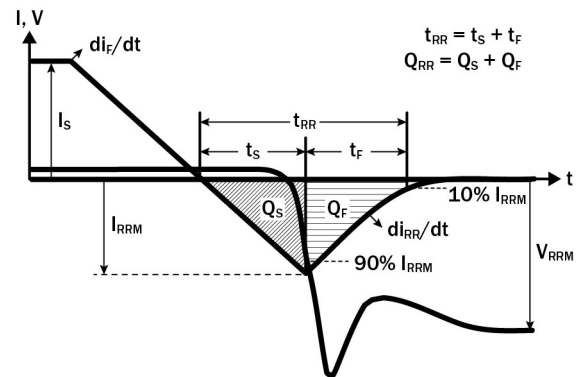


Figure 17. Diode Recovery Waveform

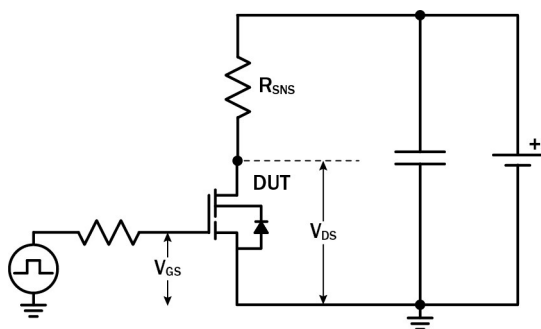


Figure 18. Dynamic $R_{DS(on)eff}$ Test Circuit

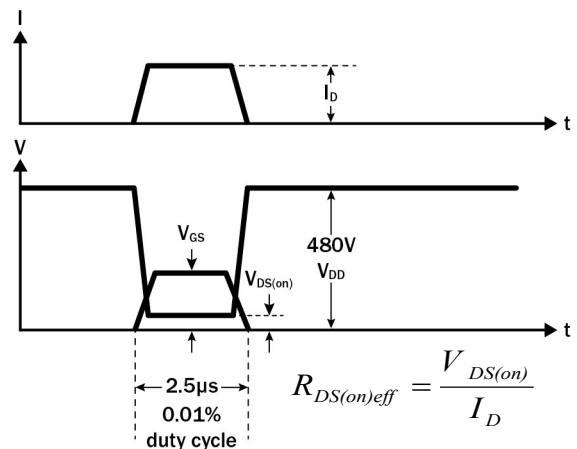


Figure 19. Dynamic $R_{DS(on)eff}$ Waveform

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Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note [Printed Circuit Board Layout and Probing for GaN Power Switches](#). The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See AN0003 : Printed Circuit Board Layout and Probing	

GaN Design Resources

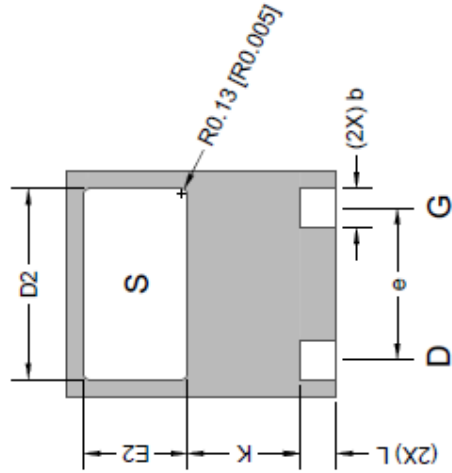
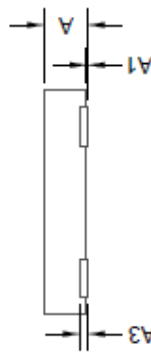
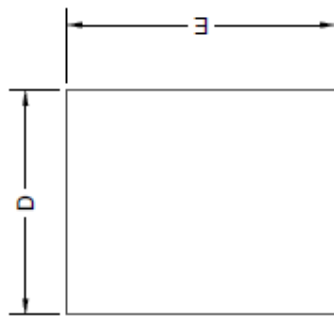
The complete technical library of GaN design tools can be found at transphormusa.com/design:

- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

TP65H480G4JSG

Mechanical

5x6 PQFN Package



G: Gate
 S: Source
 D: Drain
 Lead finish: Sn plating

DIM	mm			inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 REF.			0.007 BSC		
b	0.82	0.87	0.92	0.032	0.034	0.036
D	4.90	5.00	5.10	0.193	0.197	0.201
D2	4.09	4.24	4.39	0.161	0.167	0.173
E	5.90	6.00	6.10	0.232	0.236	0.240
e	3.37 BSC			0.133 BSC		
E2	2.15	2.30	2.45	0.085	0.091	0.096
K	2.50	-	-	0.098	-	-
L	0.71	0.81	0.91	0.028	0.032	0.036

PQFN 5mm x 6mm POD (TP65HxxxG4JSG)

transphorm

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