TQL9042

Ultra Low Noise Bypass LNA

Applications

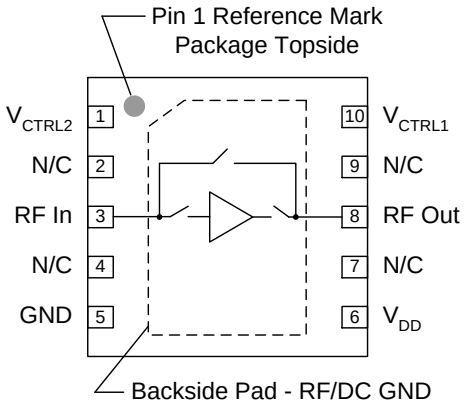
- Base Station Receivers
- Tower Mount Amplifiers
- Repeaters
- FDD-LTE, TDD-LTE, WCDMA
- General Purpose Wireless

10-pin 3 x 3 mm DFN Package

Product Features

- 500 – 2000 GHz Operational Bandwidth
- LNA with Integrated Bypass Mode
- Ability To Turn LNA and Bypass Mode OFF
- Ultra Low Noise, 0.42 dB at 900 MHz
- 19 dB Gain
- +36 dBm Output IP3
- +43 dBm Input IP3 in Bypass Mode
- Internally Matched
- Positive Supply Only, +3.3 to +5 V
- 3 x 3 mm 10-pin DFN Plastic Package

Functional Block Diagram



General Description

The TQL9042 is a high-linearity, ultra-low noise gain block amplifier with a bypass mode functionality integrated in the product. At 900 MHz, the amplifier typically provides 19 dB gain, +36 dBm OIP3, and 0.42 dB noise figure while drawing 70 mA current from a +5 V supply. The component also provides high linearity in the bypass mode with +43 dBm IIP3.

The TQL9042 is internally matched using a high performance E-pHEMT process and only requires four external components for operation from a single positive supply: an external RF choke and blocking/bypass capacitors. This low noise amplifier contains an internal active bias to maintain high performance over temperature.

The TQL9042 covers the 500 – 2000 MHz frequency band and is targeted for wireless infrastructure. The TQL9042 is packaged in a 3 x 3 mm and is pin compatible with the 1.5 – 2.7 GHz TQL9043 and 1.5 – 4.0 GHz TQL9044.

Pin Configuration

Pin No.	Label
1	V_{CTRL2}
2, 4, 7, 9	N/C
3	RFin
5	GND
6	V_{DD}
8	RFout
10	V_{CTRL1}
Backside Paddle	RF/DC GND

Ordering Information

Part No.	Description
TQL9042	500 – 2000 MHz Bypass LNA
TQL9042-PCB	Evaluation Board

Standard T/R size = 2500 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to 150 °C
Drain Voltage (V_{DD})	+7 V
Input Power (CW)	+22 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (V_{DD})	+3.3	+5.0	+5.25	V
Operating Temp. Range	−40		+105	°C
T_{ch} (for>10^6 hrs MTTF)			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} = +5 V, Temp.=+25 °C.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		500		2000	MHz
Test Frequency			900		MHz
Gain	Bypass OFF	17.5	19	20.5	dB
Input Return Loss	Bypass OFF		11		dB
Output Return Loss	Bypass OFF		20		dB
Noise Figure	Bypass OFF		0.42	0.8	dB
Output P1dB	Bypass OFF		+23		dBm
Output IP3	Bypass OFF, Pout=+5 dBm/tone, Δf=1 MHz	+30	+36		dBm
Insertion Loss	Bypass ON		1	1.9	dB
Return Loss	Bypass ON		13		dB
Input IP3	Bypass ON Pin=+6 dBm/tone, Δf=1 MHz		+43		dBm
Isolation	LNA OFF, Bypass OFF		-8.5		dB
Control Voltage, V_1, V_2(1)	V_{IH}	2.4		V_{DD}	V
	V_{IL}	0		0.4	V
Current, I_d	Bypass OFF	40	70	110	mA
	Bypass ON		3	4.5	mA
Switching Speed(2)	Bypass to LNA Mode		483	900	ns
	LNA to Bypass Mode		400	800	ns
Thermal Resistance, θ_{jc}	Channel to case		100		°C/W

Notes:
1. The limits shown are true when using the external resistive divider values as shown on the Qorvo app board.
2. To achieve these fast switching speeds it is required to place a shunt 30K resistor at the RFout pin 8. Refer to pg. 6.

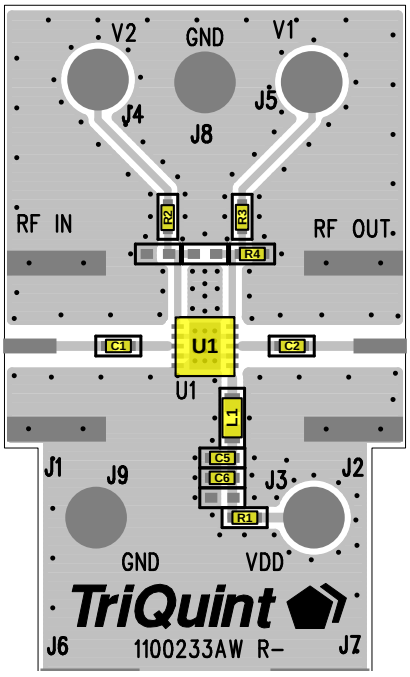
Control Truth Table

V_{CTRL2}	V_{CTRL1}	State
0	1	LNA OFF, Bypass OFF
1	1	LNA OFF, Bypass ON
0	0	LNA ON, Bypass OFF
1	0	Reserved (Do not use)

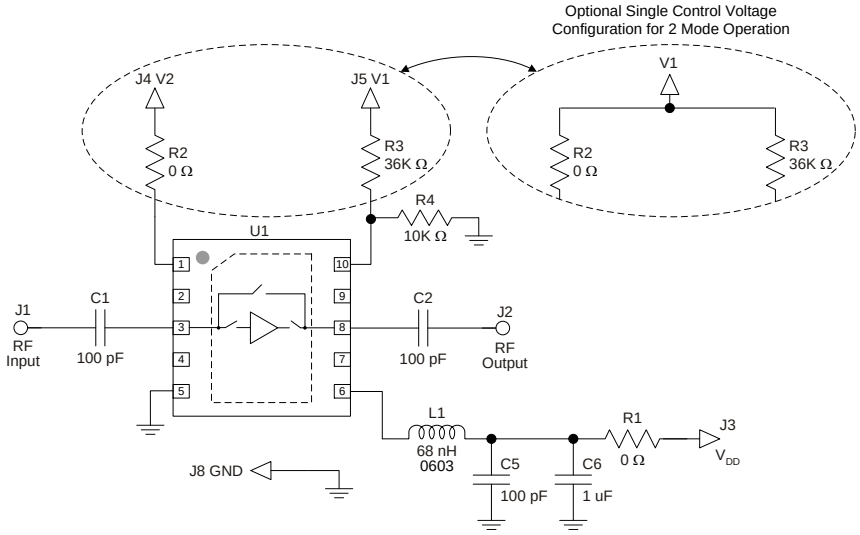
Control Voltage Limits (at device pins)

	State	Bias Condition
V_{CTRL1}	Low	≤ 0.1 V
	High	≥ 0.52 V
V_{CTRL2}	Low	≤ 0.4 V
	High	≥ 1.3 V

TQL9042-PCB Evaluation Board



See Evaluation Board PCB Information section for PCB material and stack-up.



Note:

If a TQL9042 application requires only two operational modes, LNA and bypass, the modes may be set using a single control voltage with the control lines tied together as shown above right. The corresponding truth table is shown below.

Control Truth Table – 2 Mode Operation

V_1	State
1	LNA OFF, Bypass ON
0	LNA ON, Bypass OFF

Bill of Material – TQL9042-PCB

Reference Des.	Value	Description	Manuf.	Part Number
U1	n/a	Bypass LNA	Qorvo	TQL9042
C1, C2, C3, C4, C5	100 pF	CAP, 0402, +/-5%, 50V	Panasonic	ECJ-0EC1H101J
C6	1.0 uF	CAP, 0402, 10%, 10V, X5R	various	
R1, R2	0 Ω	RES, 0402, +/-5%, 1/10W	Various	
R3	36K	RES, 0402, +/-5%, 1/10W	Various	
R4	10K	RES, 0402, +/-5%, 1/10W	Various	
L1	68 nH	IND, 0603, +/-5%, 600mA	Coilcraft	0603CS-68NXJL

Power-up and Power-down Sequencing

		V_{DD}	V_{CTRL1} & V_{CTRL2}
LNA ON, Bypass OFF	Power-up	1st	2nd
	Power-down	1st	2nd
LNA OFF, Bypass ON	Power-up	1st	2nd
	Power-down	1st	2nd

Typical Performance (LNA Mode)

Test conditions unless otherwise noted: V_{DD} = +5 V, I_D =70 mA, Temp.=+25 °C.

Parameter	Typical Value				Units
Frequency	700	800	900	1000	MHz
Gain	20.8	19.9	19.0	18.2	dB
Noise Figure	0.37	0.37	0.42	0.46	dB
Input Return Loss	9.6	10.2	10.8	11.4	dB
Output Return Loss	21.0	20.4	19.8	19.1	dB
Output P1dB	+23.1	+23.1	+23.1	+23.2	dBm
OIP3 (Pout/tone=+5 dBm, Δf = 1 MHz)	+35.3	+35.5	+36.0	+36.0	dBm

Typical Performance (Bypass Mode)

Test conditions unless otherwise noted: V_{DD} = +5 V, I_D = 3 mA, Temp.=+25 °C.

Parameter	Typical Value				Units
Frequency	700	800	900	1000	MHz
Insertion Loss	0.95	0.96	0.98	1.00	dB
Input Return Loss	12.5	12.6	12.7	12.6	dB
Output Return Loss	13.1	13.4	13.6	13.7	dB
Input IP3 (Pin/tone=+6 dBm, Δf = 1 MHz)	+41.2	+40.8	+43.0	+40.2	dBm

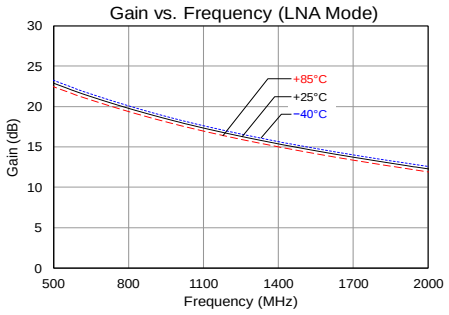
Typical Performance (LNA OFF, Bypass OFF Mode)

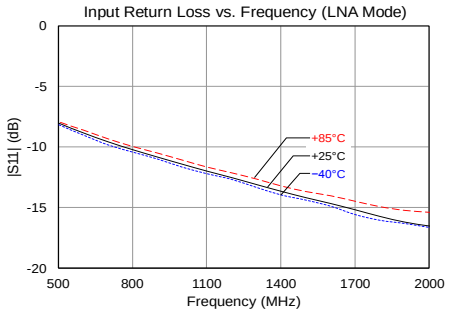
Test conditions unless otherwise noted: V_{DD} = +5 V, Temp. = +25 °C.

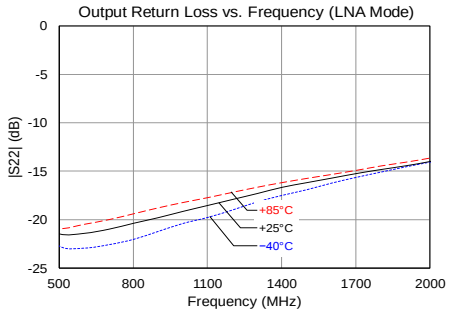
Parameter	Typical Value				Units
Frequency	700	800	900	1000	MHz
Isolation	6.6	7.4	8.2	8.8	dB

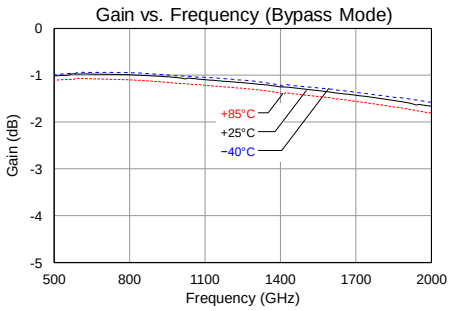
Performance Plots

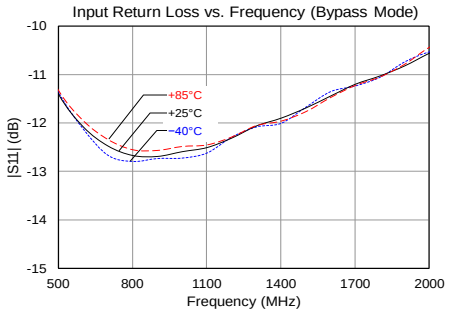
Test conditions unless otherwise noted: V_{DD} = +5 V, I_D =70 mA, Temp.=+25 °C

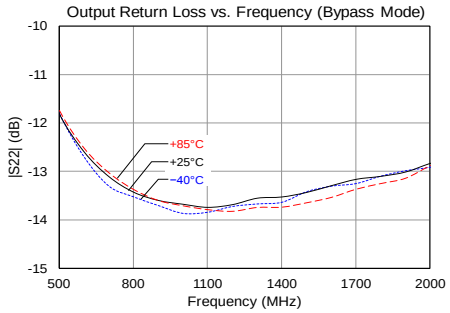


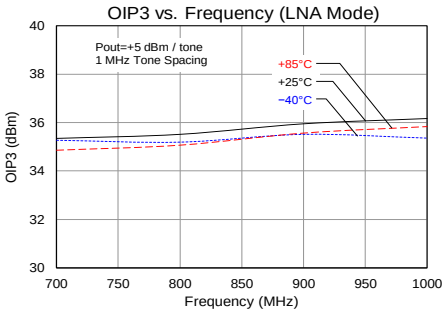


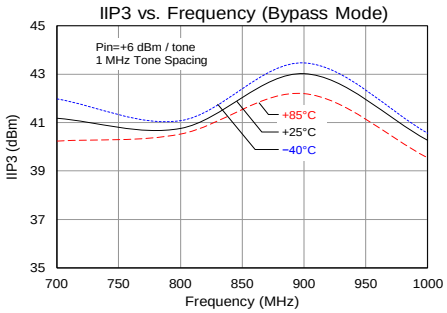


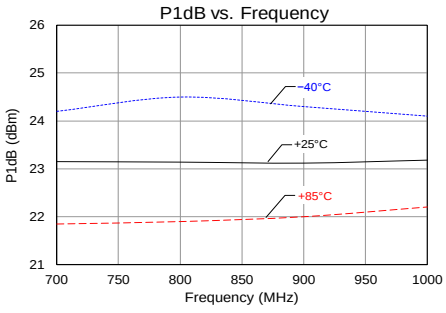


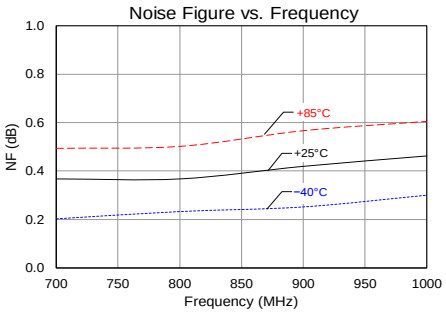


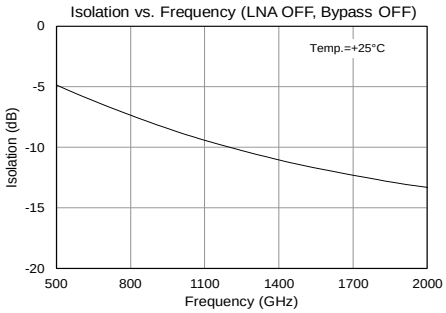




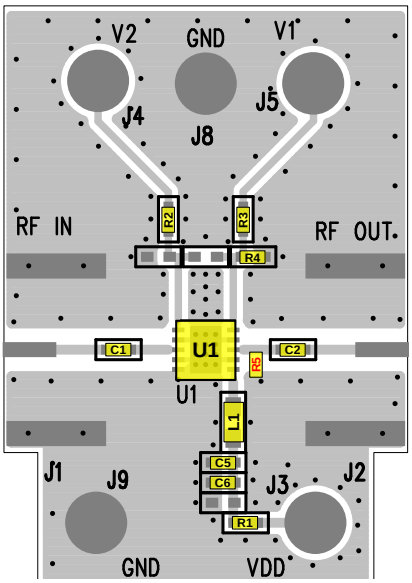


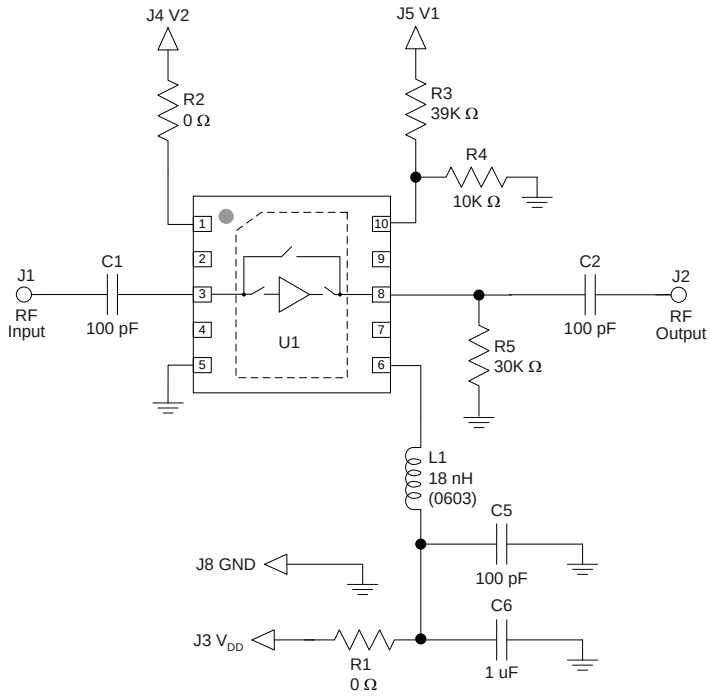






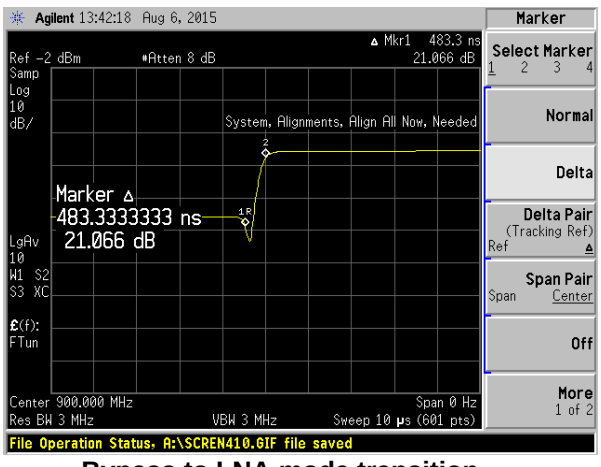
Switching Speed Application Note



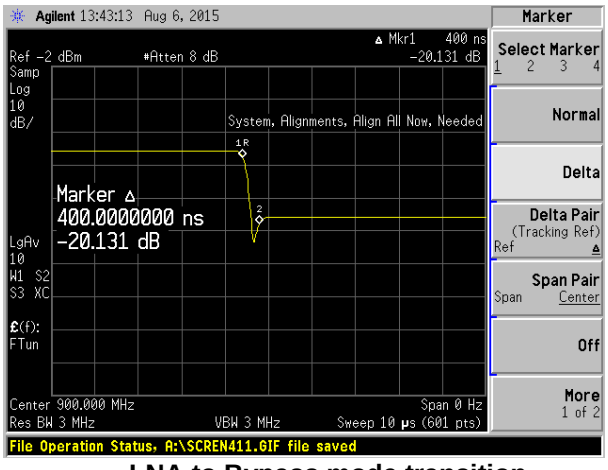


Transition	Value	Units
Bypass to LNA mode	483	ns
LNA to Bypass mode	400	ns

R5, valued 30K, is required to achieve the switching speeds listed above. The placement of R5 is shown on the Qorvo Evaluation Board above.

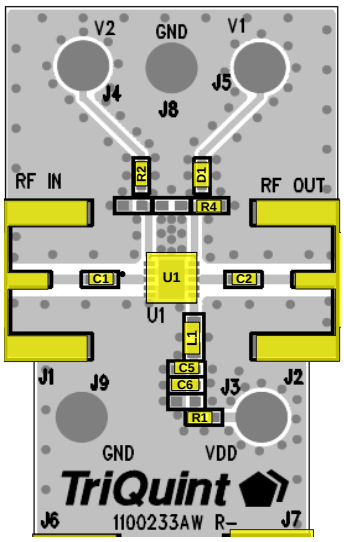


Bypass to LNA mode transition

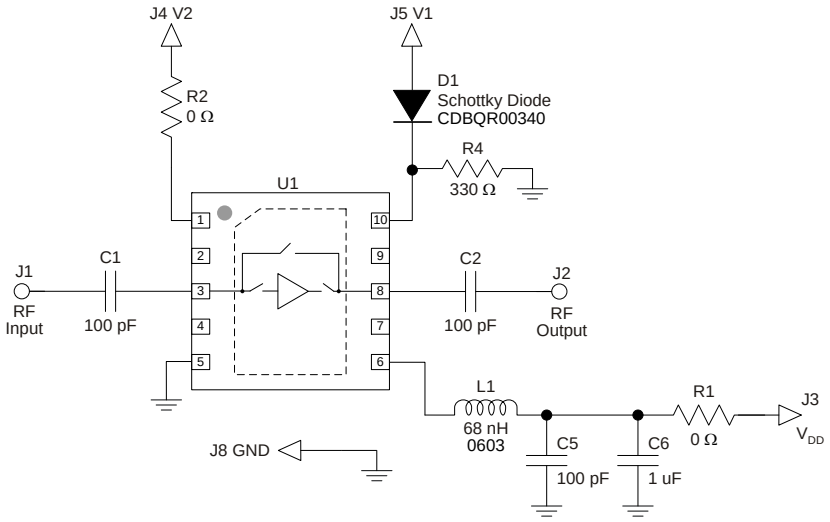


LNA to Bypass mode transition

TQL9042-PCB for 1.8V TTL Compatibility



See Evaluation Board PCB Information section for PCB material and stack-up.



Note:

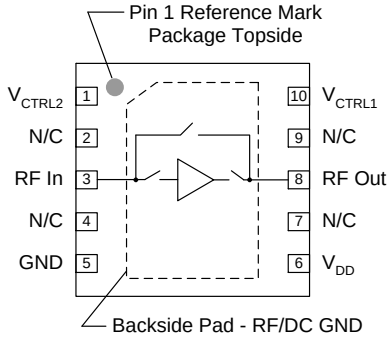
The control voltage limit for Vctrl1 shown in the table in the bottom right corner of pg. 2 cannot be met with a simple resistive divider network at pin 10 when using a 1.8V TTL logic level. A solution is to use a diode drop as shown above. This guarantees a voltage a pin 10 which is ≥0.52V.

Parameter	Conditions	Min		Max	Units
Control Voltage, V_1, V_2	V_{IH}	1.4		1.8	V
	V_{IL}	0		0.4	V

Bill of Material – TQL9042-PCB

Reference Des.	Value	Description	Manuf.	Part Number
U1	n/a	Bypass LNA	Qorvo	TQL9042
C1, C2, C3, C4, C5	100 pF	CAP, 0402, +/-5%, 50V	Panasonic	ECJ-0EC1H101J
C6	1.0 uF	CAP, 0402, 10%, 10V, X5R	Various	
R1, R2	0 Ω	RES, 0402, +/-5%, 1/10W	Various	
D1	n/a	Schottky Barrier Diode,	Comchip	CDBQR00340
R4	330 Ω	RES, 0402, +/-5%, 1/10W	Various	
L1	68 nH	IND, 0603, +/-5%, 600mA	Coilcraft	0603CS-68NXJL

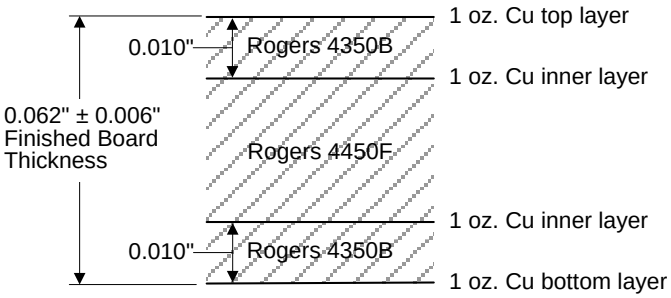
Pin Configuration and Description



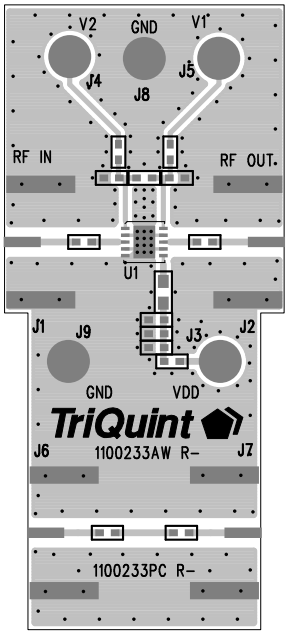
Pin No.	Label	Description
1	V_{CTRL2}	Control pin for bypass mode and LNA mode. Internal resistor divider. Refer to truth table.
2, 4, 7, 9	N/C	No internal connection. Provide grounded PCB land pads for mounting integrity.
3	RFin	RF input pin. DC block required.
5	GND	RF/DC Ground pin.
6	V_{DD}	Supply voltage pin.
8	RFout	RF output pin. DC block required.
10	V_{CTRL1}	Control pin for bypass mode and LNA mode. Requires external resistor divider. Refer to truth table.
Backside Paddle	RF/DC GND	RF/DC Ground. Follow recommended via pattern and ensure good solder attach for best thermal and electrical performance.

Evaluation Board PCB Information

Qorvo PCB 1100233 Material and Stack-up



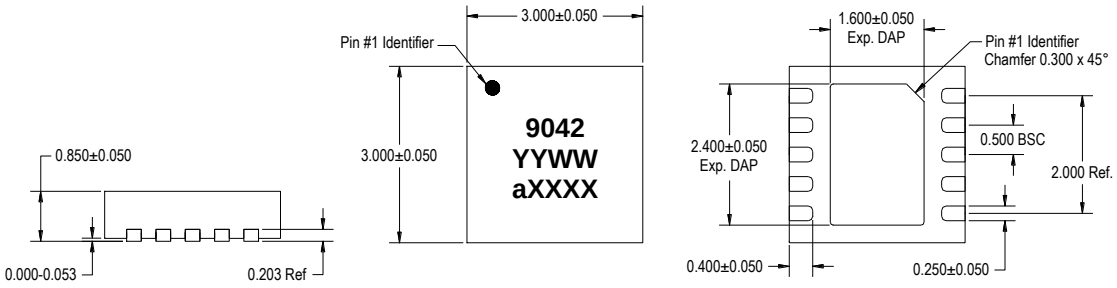
50 ohm line dimensions: width = .020”, spacing = .032”



Mechanical Information

Package Marking and Dimensions

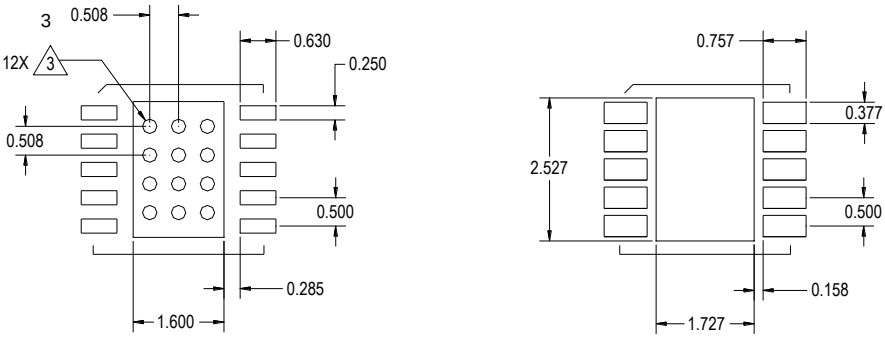
Marking: Part number – 9042
Year/Week – YYWW
Lot Code – aXXXX



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-229.
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.