TQL9062

High Linearity Gain Block with Shutdown

8 pin 2x2 mm DFN Package

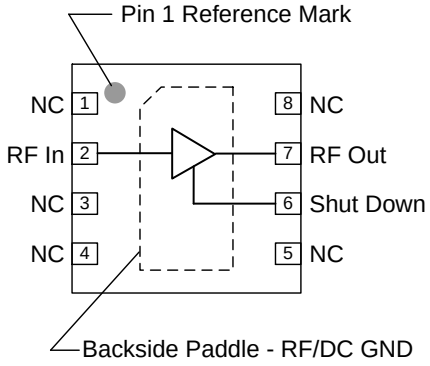
General Description

The TQL9062 is a cascadable high-linearity gain block amplifier in a small 2 x 2 mm surface-mount package. At 3.5 GHz, the amplifier typically provides 16.3 dB gain, +43.6 dBm OIP3 at a 120 mA bias setting, and 1.4 dB noise figure. The LNA can be biased from a single positive supply ranging from 3.3 to 5 volts.

The TQL9062 has good noise figure and high linearity performance allowing the device to be used in both receiver and transmitter chains for high performance systems. The gain block is internally matched using a high performance E-pHEMT process and only requires four external components for operation from a single positive supply: an external RF choke and blocking/bypass capacitors. This low noise amplifier contains an internal active bias circuit to maintain high performance over temperature and integrates a shut-down capability to allow for operation in TDD applications.

The TQL9062 covers the 500-6000 MHz frequency band and is targeted for wireless infrastructure or other applications requiring high linearity and/or low noise figure.

Functional Block Diagram



Applications

- Repeaters / DAS
- Mobile Infrastructure
- LTE / WCDMA / CDMA / GSM
- General Purpose Wireless
- TDD or FDD systems

Product Features

- 0.5-6.0 GHz Operational Bandwidth
- 16.3 dB Gain at 3.5 GHz
- 43.6 dBm OIP3 at 3.5 GHz
- 1.8V TTL logic compatible for shut-down control
- Unconditionally stable
- Integrated on-chip matching, 50 ohm in/out
- Integrated active bias

Ordering Information

Part No.	Description
TQL9062	High Linearity Gain Block
TQL9062-PCB	0.5-6.0 GHz Evaluation Board

Standard T/R size = 2500 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to 150°C
Supply Voltage (V_{DD})	+7 V
RF Input Power, CW, 50Ω, T=25°C	+33 dBm
RF Input Power, WCDMA, 10dB PAR	+27 dBm
RF Input Power, CW, OFF State	+33 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD})	3.3	5.0	5.25	V
T_{CASE}	−40		+105	°C
Tj for >10^6 hours MTTF			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} =+5V, Temp=+25°C, 50 Ω system.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		500		6000	MHz
Test Frequency			3500		MHz
Gain		15	16.5	18	dB
Input Return Loss			13		dB
Output Return Loss			18		dB
Noise Figure(1)			1.4		dB
Output P1dB			+21.3		dBm
Output IP3	Pout=+7 dBm/tone, Δf=1 MHz	+35	+41		dBm
Power Shutdown Control (pin 6)	On state	0		0.63	V
	Off state (Power down)	1.17		V_{DD}	V
Current, I_{DD}	On state	80	122	150	mA
	Off state (Power down)		3		mA
Shutdown pin current, I_{SD}	V_{PD} ≥ 1.17 V		200		µA
Switching Speed	LNA ON to OFF		520		ns
	LNA OFF to ON		450		ns
Thermal Resistance, θ_{jc}	channel to case		48		°C/W

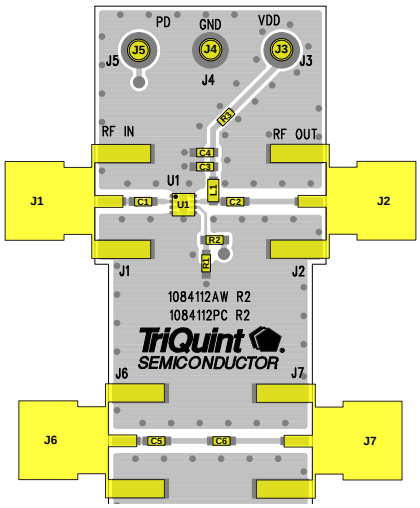
Note: 1) Noise figure data has input trace loss de-embedded.

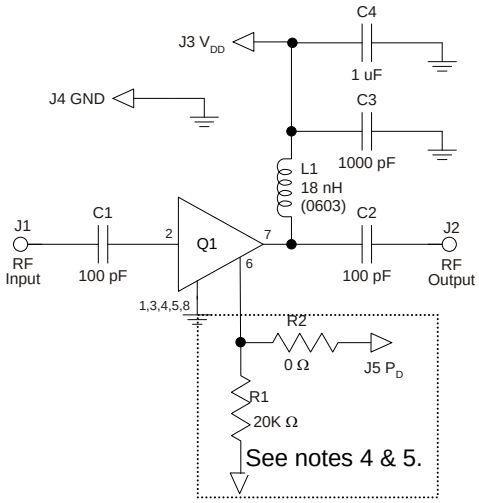
S-Parameters

Test Conditions: V_{DD}=+5 V, I_{DD}=120 mA (typ.), T=+25°C, unmatched 50 ohm system, calibrated to device leads

Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
0.05	-5.58	-25.44	31.12	154.79	-39.32	18.69	-21.45	-78.20
0.1	-6.63	-40.28	29.60	140.90	-38.23	24.37	-21.43	-108.89
0.2	-8.40	-67.49	27.44	121.82	-36.03	32.11	-20.54	-130.56
0.4	-12.21	-117.58	24.34	91.42	-32.46	33.32	-18.10	-142.99
0.6	-15.86	-168.14	21.82	67.54	-30.15	26.01	-15.82	-154.18
0.7	-17.04	165.25	20.76	57.25	-29.34	21.57	-14.95	-160.06
0.8	-17.59	139.89	19.82	47.73	-28.71	16.72	-14.21	-165.79
0.9	-17.69	117.33	18.99	38.80	-28.22	11.88	-13.60	-171.24
1	-17.63	97.93	18.26	30.34	-27.81	7.02	-13.07	-176.47
1.2	-17.67	64.69	17.06	14.40	-27.26	-2.90	-12.20	173.78
1.4	-17.96	32.57	16.16	-0.65	-26.97	-12.93	-11.50	164.97
1.6	-17.84	-0.92	15.49	-15.14	-26.88	-23.05	-10.91	156.98
1.8	-17.07	-33.07	15.02	-29.21	-26.96	-33.20	-10.43	149.90
1.9	-16.52	-48.19	14.85	-36.12	-27.06	-38.34	-10.22	146.83
2	-15.91	-62.83	14.72	-42.97	-27.18	-43.50	-10.03	144.17
2.1	-15.22	-77.12	14.63	-49.78	-27.34	-48.72	-9.84	141.80
2.3	-13.57	-104.04	14.53	-63.46	-27.75	-59.44	-9.50	137.78
2.4	-12.64	-116.18	14.51	-70.30	-28.01	-65.03	-9.31	136.07
2.5	-11.69	-127.19	14.51	-77.18	-28.28	-70.67	-9.13	134.34
2.6	-10.78	-137.01	14.52	-84.07	-28.59	-76.46	-8.95	132.52
2.7	-9.96	-145.92	14.56	-90.99	-28.93	-82.44	-8.78	130.54
2.8	-9.24	-154.12	14.61	-97.95	-29.27	-88.50	-8.65	128.38
3	-8.33	-170.14	14.83	-112.10	-29.90	-101.46	-8.61	123.39
3.2	-7.52	176.37	15.05	-126.52	-30.56	-115.52	-8.52	117.49
3.3	-7.30	169.24	15.20	-133.99	-30.84	-123.29	-8.57	114.62
3.4	-7.19	161.43	15.36	-141.68	-31.08	-131.38	-8.67	112.03
3.5	-7.16	152.84	15.51	-149.61	-31.25	-140.04	-8.82	109.91
3.6	-7.20	143.52	15.66	-157.73	-31.41	-149.11	-9.02	108.36
3.7	-7.29	133.64	15.79	-166.07	-31.47	-158.57	-9.22	107.47
3.8	-7.45	123.39	15.89	-174.50	-31.47	-168.48	-9.43	107.11
3.9	-7.70	113.05	15.97	176.95	-31.41	-178.40	-9.60	107.32
4	-8.08	102.75	16.00	168.34	-31.27	171.57	-9.74	107.82
4.1	-8.63	92.35	16.00	159.65	-31.07	161.46	-9.83	108.60
4.2	-9.42	81.60	15.96	150.83	-30.78	151.14	-9.82	109.35
4.4	-11.83	56.82	15.72	132.91	-30.13	131.39	-9.53	109.52
4.6	-15.03	20.39	15.23	114.98	-29.42	112.31	-9.00	106.37
4.8	-16.25	-29.12	14.52	97.76	-28.77	94.63	-8.57	99.43
5	-15.18	-67.89	13.67	81.87	-27.91	78.35	-8.43	90.91
5.2	-13.99	-95.10	12.78	66.68	-27.18	62.35	-8.72	81.53
5.4	-13.12	-120.17	11.78	52.42	-26.36	46.79	-9.43	73.90
5.6	-11.85	-143.52	10.58	39.61	-25.60	30.29	-10.53	70.22
5.8	-10.34	-163.20	9.35	29.87	-25.11	13.36	-11.30	75.03
6	-8.93	-177.96	8.35	22.35	-24.78	-4.86	-10.53	82.56

TQL9062-PCB Evaluation Board





Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. R3 (0 Ω jumper) is not shown on the schematic and may be replaced with copper trace in the target application layout.
3. All components are of 0402 size unless stated on the schematic.
4. For TDD Applications: R1 = 20K & R2 = 0Ω
5. For FDD Applications: R1 = 20K 'OR' Pin 6 tied to ground. R2 = DNP/Omitted
6. A through line is included on the evaluation board to de-embed the board losses.
7. R4 sets the current draw. Can be changed for the desired bias point. See table below.

Bill of Material – TQL9062-PCB

Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board	Qorvo	
U1	n/a	Ultra Low Noise, Flat Gain LNA	Qorvo	TQL9062
R1	20K	Resistor, chip, 0402, 5%, 1/16W	various	
R2, 3	0 Ω	Resistor, Chip, 0402, 5%, 1/16W	various	
L1	18 nH	Inductor, 0603, coil	various	
C3	1000 pF	Cap, chip, 0402	various	
C4	1.0 uF	Cap., Chip, 0402	various	
C1, C2, C5, C6	100 pF	Cap., Chip, 0402	various	

Typical Performance – TQL9062-PCB

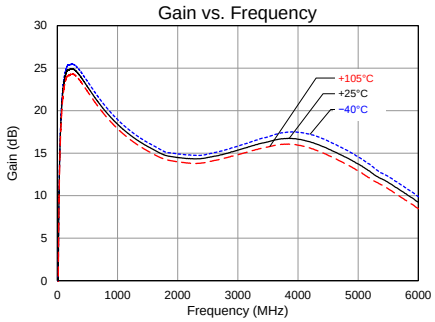
Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=122 mA (typ.), Temp=+25°C

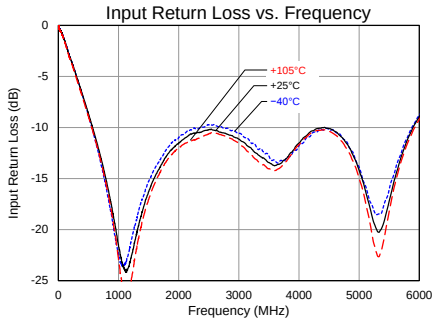
Parameter	Conditions	Typical Values					Units
Frequency		1900	2600	3300	3500	3800	MHz
Gain		14.6	14.8	15.3	16.3	16.7	dB
Input Return Loss		12	10.5	12.5	13.5	13	dB
Output Return Loss		12.5	15	17	18	17	dB
Output P1dB		+23.5	+22.6	+21.3	+21.3	+20.8	dBm
OIP3	Pout=+5 dBm/tone, Δf=1 MHz	+40	+41	+42.2	+43.6	+44.6	dBm
Noise figure (1)		1.0	1.25	1.3	1.4	1.5	dB

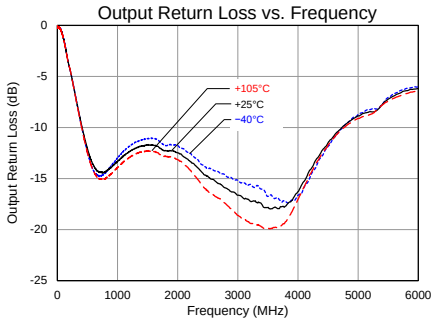
Note: 1) Noise figure data has input trace loss de-embedded.

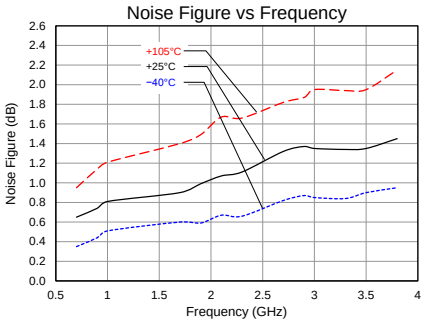
Performance Plots – TQL9062-PCB

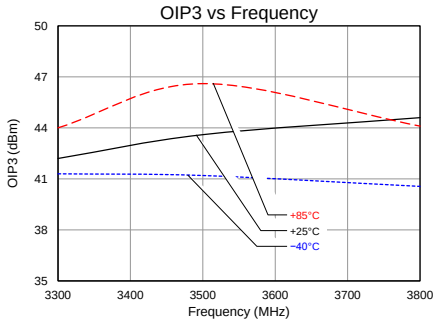
Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD} = 122mA. Noise figure data has input trace loss de-embedded.

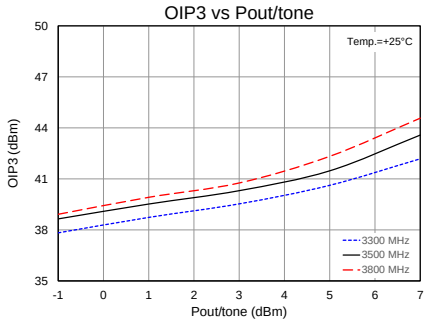


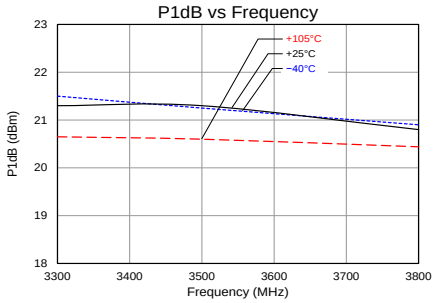


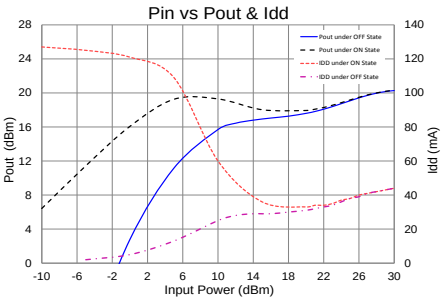






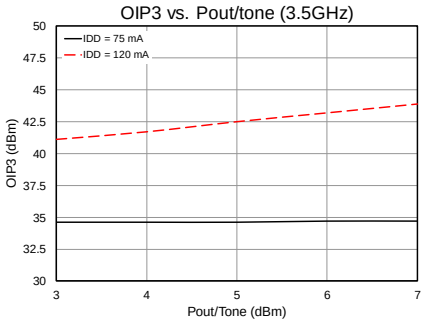


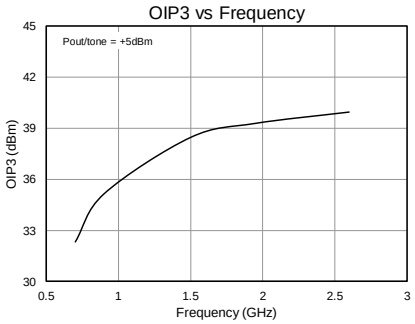


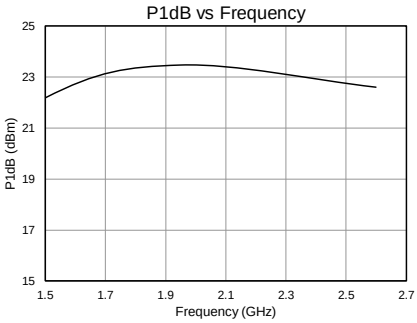


Performance Plots Contd. – TQL9062-PCB

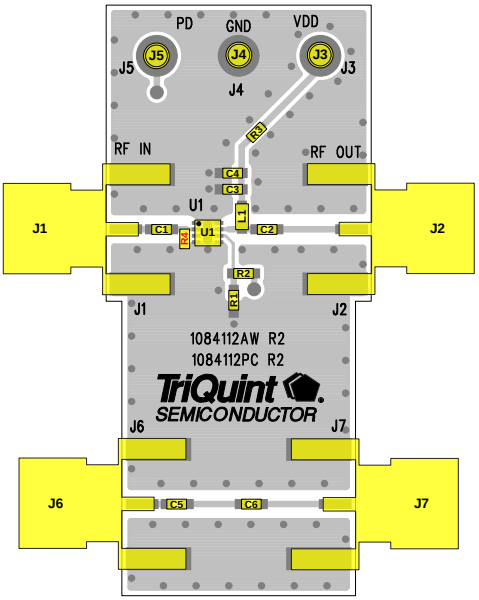
Test conditions unless otherwise noted: V_{DD}=+5 V, Temp=+25°C.

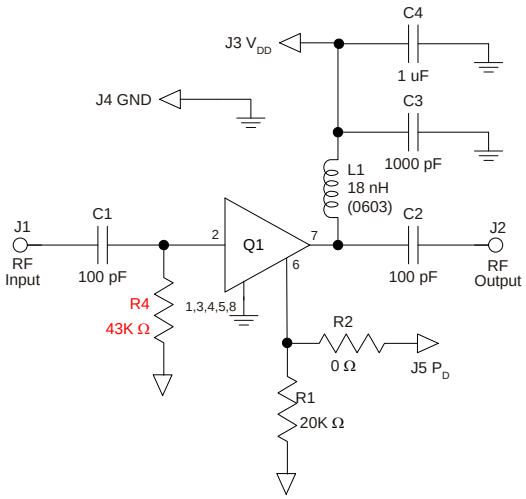






TQL9062-PCB (Reduced Current)

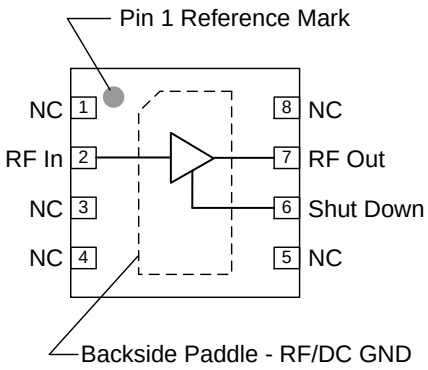




Notes

1. Placing a 43K Ohm shunt resistor at the input of the amplifier reduces the current draw from 120mA to 70mA.
2. Negligible change in s-parameter performance under reduced current conditions. OIP3 performance shown in above plot.

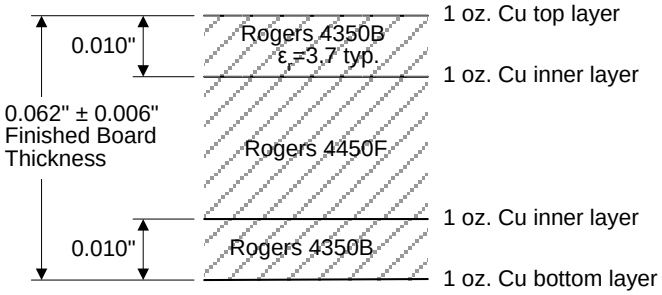
Pin Configuration and Description



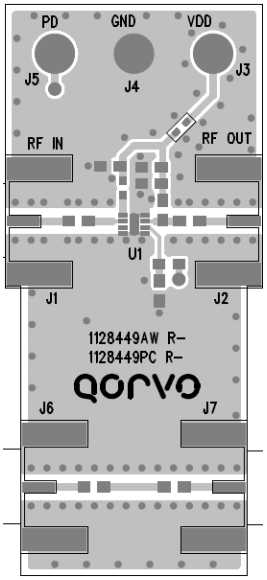
Pin No.	Label	Description
1, 3, 4, 5, 8	NC	No electrical connection. Provide grounded land pads for PCB mounting integrity.
2	RF In	RF Input pin. A DC Block is required.
6	Shut Down	A high voltage(>1.17V) turns off the device. If the pin is pulled to ground or driven with a voltage less than 0.63V, then the device will operate under LNA ON state.
7	RF Out / DCBias	RF Output pin. DC bias will also need to be injected through an RF bias choke/inductor for operation.
Backside Paddle	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

Qorvo PCB 1128449 Material and Stack-up



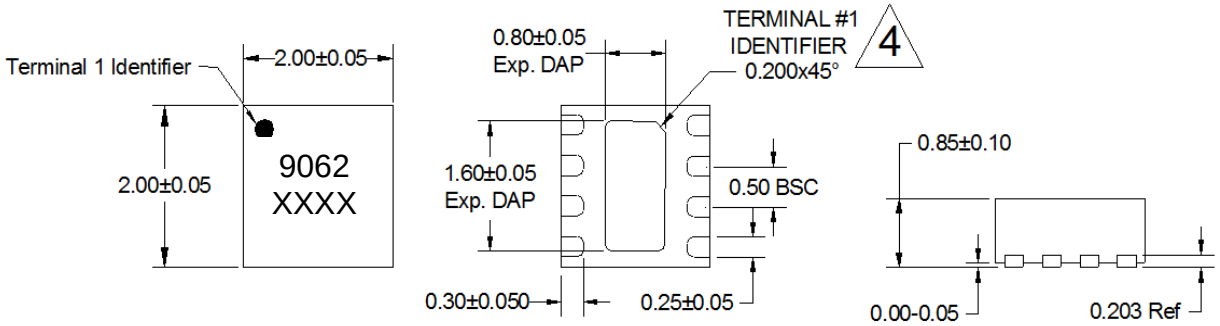
50 ohm line dimensions: width = 0.020”, spacing = 0.032”



Mechanical Information

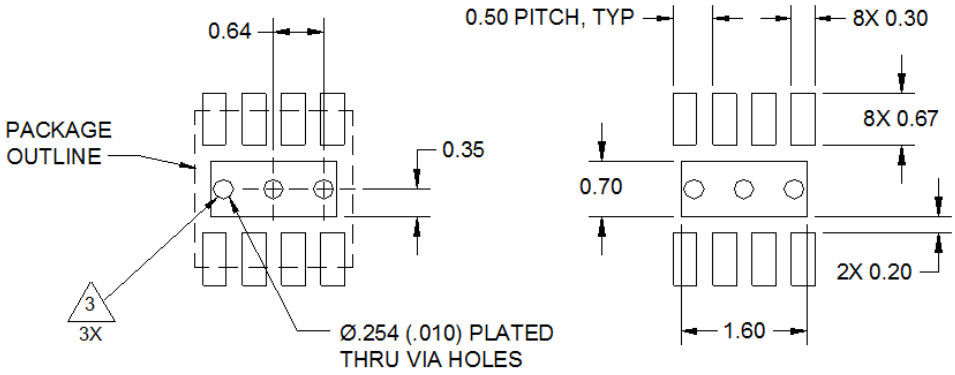
Package Marking and Dimensions

Marking: Part number – 9062
Lot code – XXXX



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.