TQL9063

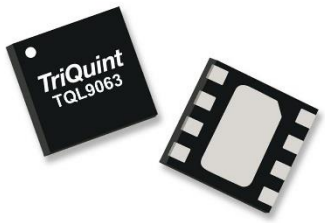
Ultra Low-Noise, Bypass LNA

Product Overview

The TQL9063 is a high-linearity, ultra-low noise gain block amplifier with a bypass mode functionality integrated in the product. At 1.95 GHz, the amplifier typically provides 19 dB gain, +36.3 dBm OIP3, and 0.7 dB noise figure while drawing 77 mA current from a +5 V supply. The component also provides high linearity in the bypass mode with +39 dBm IIP3.

The TQL9063 is internally matched using a high-performance E-pHEMT process and only requires four external components for operation from a single positive supply: an external RF choke and blocking/bypass capacitors. This low noise amplifier contains an internal active bias to maintain high performance over temperature.

The TQL9063 covers the 0.5 – 4.0 GHz frequency band and is targeted for wireless infrastructure. The TQL9063 is packaged in a 2 x 2 mm DFN.

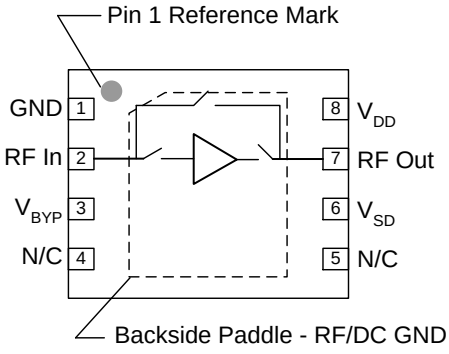


8-pin 2x2 mm DFN Package

Key Features

- 0.5 – 4.0 GHz Operational bandwidth
- LNA with integrated bypass mode
- Ability to turn LNA and bypass mode OFF
- Ultra-low noise, 0.7 dB at 1.95 GHz
- 19 dB Gain at 1.95 GHz
- +36.3 dBm Output IP3 in LNA Mode
- +39 dBm Input IP3 in Bypass Mode
- Internally matched
- Positive supply only, +3.3 to +5 V
- 2x2 mm 8-pin DFN plastic package

Functional Block Diagram



Top View

Applications

- Base Station Receivers
- Tower Mount Amplifiers
- Repeaters
- FDD-LTE, TDD-LTE, WCDMA
- General Purpose Wireless

Ordering Information

Part No.	Description
TQL9063	500−4000 MHz Bypass LNA
TQL9063-PCB	500−4000 MHz Evaluation Board

Standard T/R size = 2500 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to 150 °C
RF Input Power, CW, 50 Ω, T=+25 °C	+22 dBm
Device Voltage (V_{DD})	+7 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V_{DD})	+3.3	+5.0	+5.25	V
T_{CASE}	−40		+105	°C
T_j for >10^6 hours MTTF			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} = +5 V, Temp.=+25°C.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		500		4000	MHz
Test Frequency			1950		MHz
Gain	LNA ON, Bypass OFF	17.5	19	20.5	dB
Input Return Loss	LNA ON, Bypass OFF		12		dB
Output Return Loss	LNA ON, Bypass OFF		9.5		dB
Noise Figure	LNA ON, Bypass OFF		0.7	0.9	dB
Output P1dB	LNA ON, Bypass OFF		+21.2		dBm
Output IP3	LNA ON, Bypass OFF, Pout=+0 dBm/tone, Δf=1 MHz	+31	+36.3		dBm
Insertion Loss	LNA OFF, Bypass ON		1.4		dB
Return Loss	LNA OFF, Bypass ON		18		dB
Input IP3	LNA OFF, Bypass ON Pin=+3 dBm/tone, Δf=1 MHz		+39		dBm
Isolation	LNA OFF, Bypass OFF		17		dB
Control Voltage, V_1, V_2 (1)	V_{IH}	1.6		V_{DD}	V
	V_{IL}	0		0.5	V
Current, I_D	Bypass OFF	60	77	100	mA
	Bypass ON		3		mA
Switching Time (2)	Bypass to LNA Mode		983		ns
	LNA to Bypass Mode		1.9		µs
	LNA to OFF		200		ns
Thermal Resistance, θ_{jc}	Channel to case		44		°C/W

Notes:
1. These voltages are referenced at the turrets labelled V1 and V2 on the circuit schematic on page 4.
2. To achieve fast-switching it is required to place a 91K shunt resistor at the RF Out pin 7. Refer to page 7.

Control Truth Table

V_{BYP}	V_{SD}	State
0	0	LNA ON, Bypass OFF
0	1	LNA OFF, Bypass OFF
1	x	LNA OFF, Bypass ON

De-embedded S-Parameters (LNA Mode)

Test Conditions: V_{DD}=+5 V, I_{DD}=75 mA (typ.), T=+25°C, 50 ohm system impedance, reference on device leads

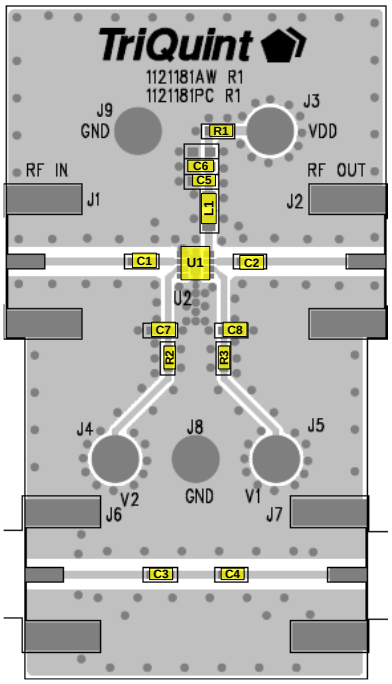
Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
0.1	-0.34	-18.46	10.47	-40.24	-49.61	153.06	-0.20	-49.20
0.3	-2.46	-56.16	25.14	-126.62	-33.50	92.83	-4.56	-154.92
0.4	-4.03	-65.89	26.03	-156.47	-31.84	74.30	-8.52	162.29
0.6	-5.84	-77.87	25.55	166.99	-30.62	57.06	-14.43	89.93
0.7	-6.38	-83.02	25.03	154.63	-30.24	52.96	-15.50	58.24
0.8	-6.80	-87.84	24.47	144.39	-29.91	50.25	-15.55	32.10
1	-7.45	-96.37	23.34	127.97	-29.31	47.05	-14.41	-4.20
1.2	-7.92	-103.39	22.23	114.95	-28.74	45.37	-13.04	-27.33
1.3	-8.11	-106.38	21.70	109.30	-28.47	44.80	-12.41	-36.16
1.4	-8.27	-109.05	21.18	104.07	-28.20	44.35	-11.83	-43.80
1.5	-8.41	-111.43	20.67	99.21	-27.93	43.96	-11.30	-50.53
1.6	-8.52	-113.55	20.18	94.65	-27.67	43.62	-10.81	-56.56
1.7	-8.62	-115.44	19.69	90.36	-27.42	43.31	-10.36	-62.02
1.8	-8.71	-117.11	19.23	86.30	-27.17	43.01	-9.95	-67.01
1.9	-8.78	-118.58	18.77	82.44	-26.92	42.72	-9.57	-71.62
2	-8.83	-119.88	18.33	78.75	-26.68	42.42	-9.22	-75.91
2.1	-8.88	-121.03	17.90	75.22	-26.45	42.13	-8.90	-79.92
2.2	-8.91	-122.03	17.48	71.83	-26.22	41.83	-8.60	-83.70
2.3	-8.93	-122.92	17.07	68.57	-26.00	41.51	-8.33	-87.26
2.4	-8.94	-123.69	16.66	65.42	-25.78	41.19	-8.08	-90.64
2.5	-8.94	-124.36	16.27	62.37	-25.56	40.86	-7.85	-93.86
2.6	-8.92	-124.95	15.89	59.42	-25.35	40.52	-7.64	-96.93
2.7	-8.91	-125.47	15.52	56.55	-25.15	40.17	-7.45	-99.87
2.8	-8.88	-125.92	15.15	53.76	-24.95	39.81	-7.27	-102.69
3	-8.80	-126.67	14.45	48.39	-24.56	39.06	-6.97	-108.03
3.2	-8.69	-127.26	13.77	43.26	-24.18	38.26	-6.73	-113.00
3.4	-8.56	-127.74	13.12	38.32	-23.82	37.41	-6.53	-117.68
3.6	-8.41	-128.16	12.50	33.56	-23.46	36.52	-6.39	-122.10
3.8	-8.24	-128.54	11.90	28.94	-23.12	35.57	-6.30	-126.30
4	-8.05	-128.93	11.32	24.43	-22.78	34.56	-6.26	-130.29

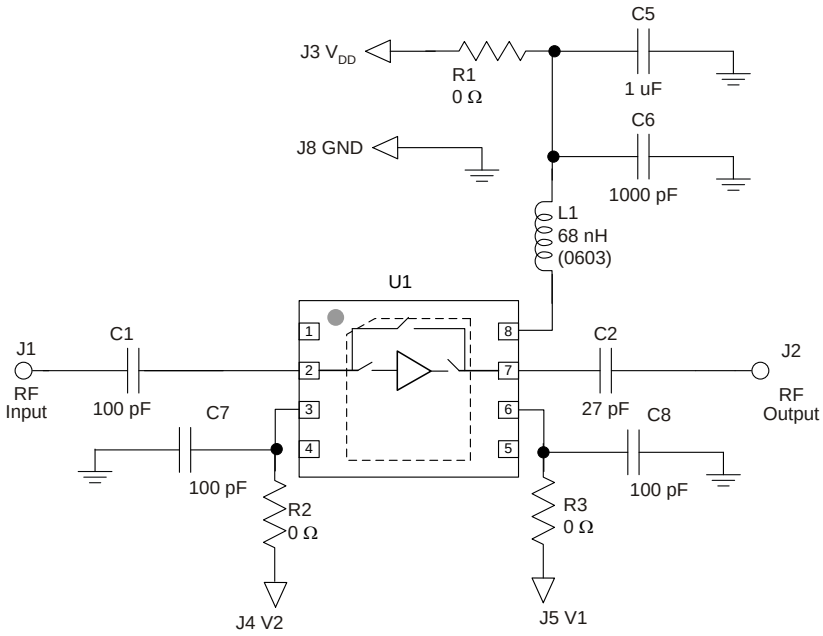
Noise Parameters (LNA Mode)

Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=75 mA (typ.), Temp=+25°C, 50 Ohm system impedance

Freq (GHz)	NF_{min} (dB)	GammaOpt (mag)	GammaOpt (deg)	Rn (Ω)
1.5	0.46	0.27	73.07	3.17
1.6	0.47	0.27	76.39	3.15
1.7	0.47	0.28	79.57	3.14
1.8	0.48	0.28	82.63	3.12
1.9	0.49	0.29	85.57	3.11
2	0.50	0.29	88.39	3.10
2.1	0.50	0.30	91.10	3.08
2.2	0.51	0.31	93.70	3.07
2.3	0.52	0.31	96.20	3.06
2.4	0.53	0.32	98.60	3.04
2.5	0.54	0.33	100.91	3.03
2.6	0.55	0.33	103.13	3.02
2.7	0.56	0.34	105.27	3.00

TQL9063-PCB Evaluation Board





See Evaluation Board PCB Information section for PCB material and stack-up.

Bill of Material – TQL9063-PCB

Reference Des.	Value	Description	Manuf.	Part Number
U1	-	LNA, with bypass mode	Qorvo	TQL9063
C2	27 pF	CAP, 5%, 50V, NPO/C0G, 0402	Various	
C1, C3, C4, C7, C8	100 pF	CAP, 5%, 50V, 0402	Panasonic	ECJ-0EC1H101J
C6	1000 pF	CAP, 10%, 50V, 0402	various	
C5	1.0 µF	CAP, 10%, 10V, X7S, 0402	various	
R1, R2, R3	0 Ω	RES, 1/10W, 0402	various	
L1	68 nH	IND, 5%, CER CORE, 0603	Coilcraft	0603CS-68NXJL

Typical Performance (LNA Mode)

Test conditions unless otherwise noted: V_{DD} = +5 V, V_1 = 0.5V, V_2 = 0.5V, I_D = 77 mA, Temp.=+25 °C.

Parameter	Typical Value				Units
Frequency	700	1950	2600	3500	MHz
Gain	+24.3	19.2	17.3	14	dB
Noise Figure	0.64	0.7	0.8	1.1	dB
Input Return Loss	7.8	12	15.3	13.7	dB
Output Return Loss	9.4	9.3	9.5	6	dB
OIP3 (Pout/tone=+0 dBm, Δf = 1 MHz)	+35.5	+36.3	+36.1	+36.4	dBm
P1dB	+21.7	+21.2	+21.6	+19.8	dBm

Typical Performance (Bypass Mode)

Test conditions unless otherwise noted: V_{DD} = +5 V, V_1 = 0.5V or 1.6V, V_2 = 1.6V, I_d = 3 mA, Temp.=+25 °C.

Parameter	Typical Value				Units
Frequency	700	1950	2600	3500	MHz
Insertion Loss	1.2	1.4	1.5	1.6	dB
Input Return Loss	13.6	20	25	20	dB
Output Return Loss	13.6	18	18	17	dB
Input IP3 (Pin/tone=+3 dBm, Δf = 1 MHz)	+38.2	+39	+39	+36.6	dBm

Typical Performance (LNA OFF, Bypass OFF Mode)

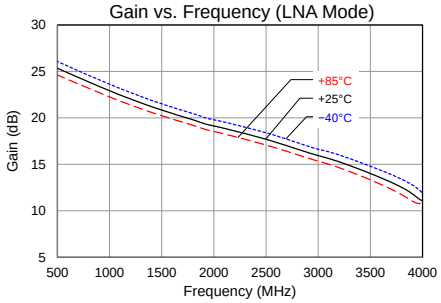
Test conditions unless otherwise noted: V_{DD} = +5 V, V_1 = 1.6V, V_2 = 0.5V, Temp. = +25 °C.

Parameter	Typical Value				Units
Frequency	700	1950	2600	3500	MHz
Isolation	23	17	15	15	dB

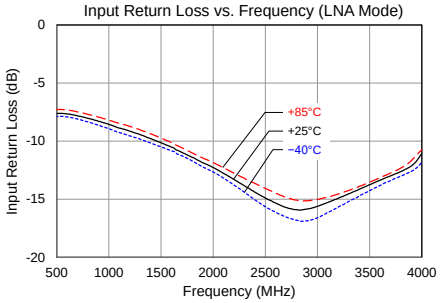
Performance Plots

Test conditions unless otherwise noted: V_{DD} = +5 V

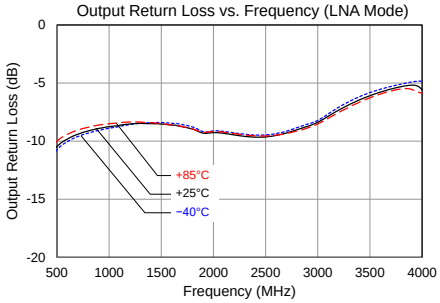
Gain vs. Frequency (LNA Mode)



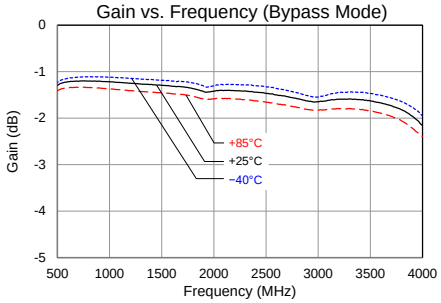
Input Return Loss vs. Frequency (LNA Mode)



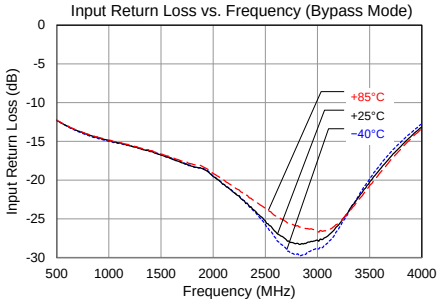
Output Return Loss vs. Frequency (LNA Mode)



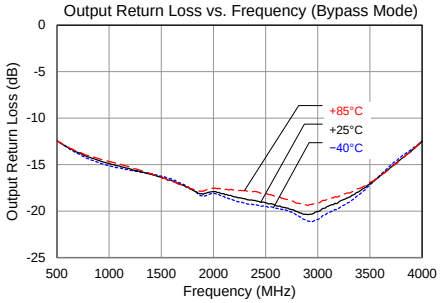
Gain vs. Frequency (Bypass Mode)



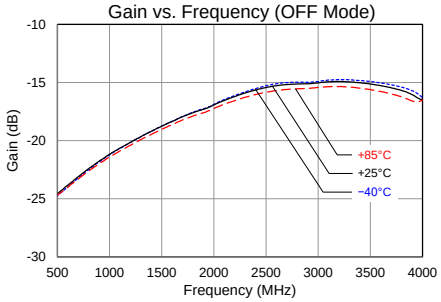
Input Return Loss vs. Frequency (Bypass Mode)



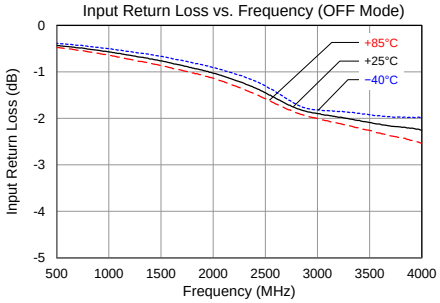
Output Return Loss vs. Frequency (Bypass Mode)



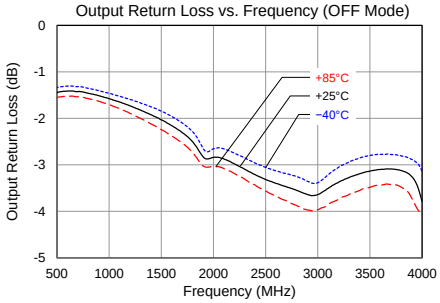
Gain vs. Frequency (OFF Mode)



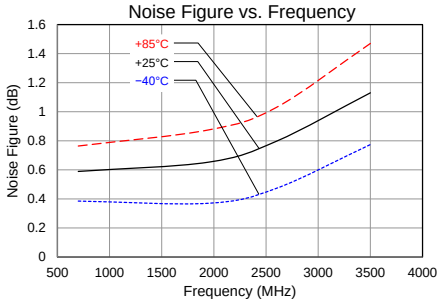
Input Return Loss vs. Frequency (OFF Mode)



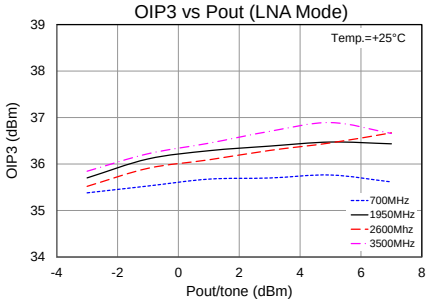
Output Return Loss vs. Frequency (OFF Mode)



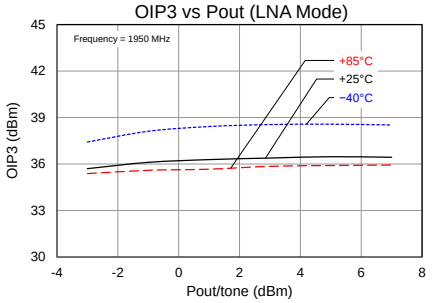
Noise Figure vs. Frequency



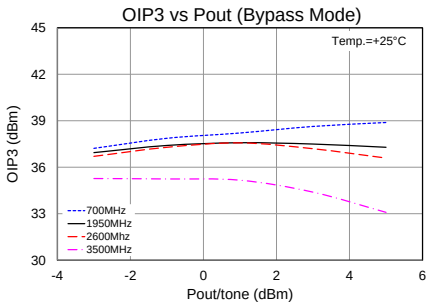
OIP3 vs Pout (LNA Mode)



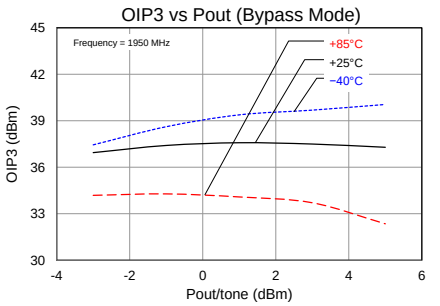
OIP3 vs Pout (LNA Mode)



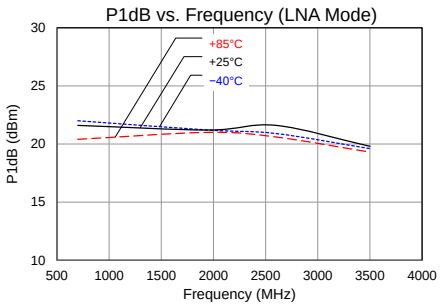
OIP3 vs Pout (Bypass Mode)



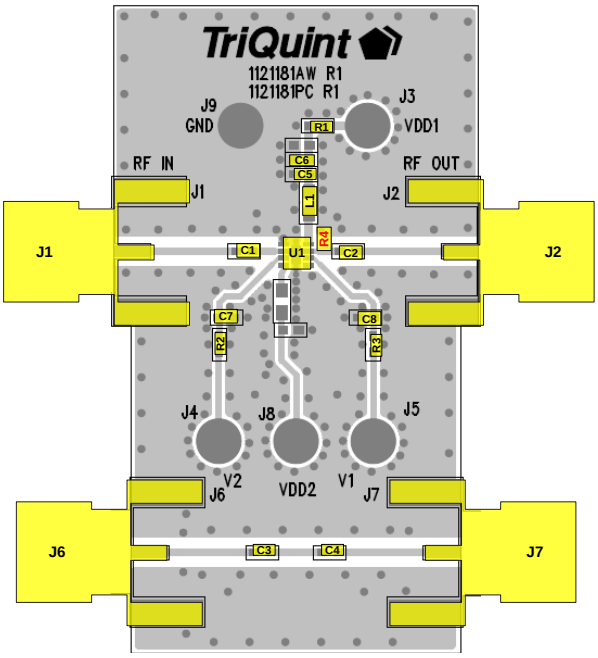
OIP3 vs Pout (Bypass Mode)

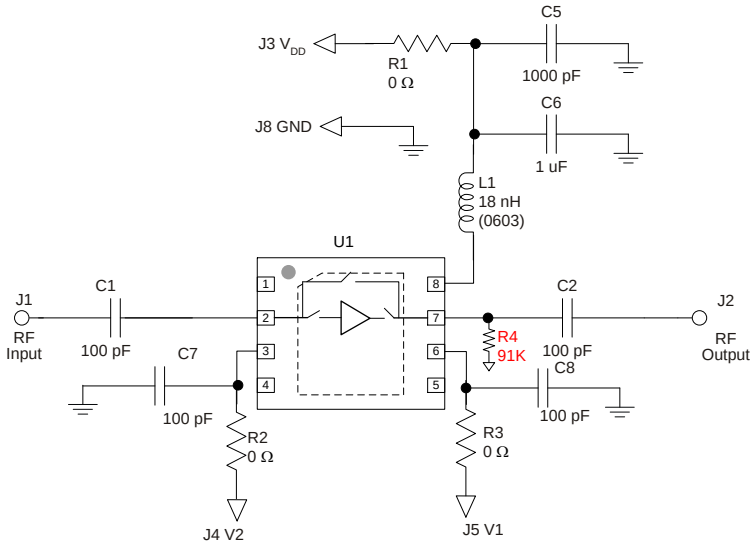


P1dB vs. Frequency (LNA Mode)



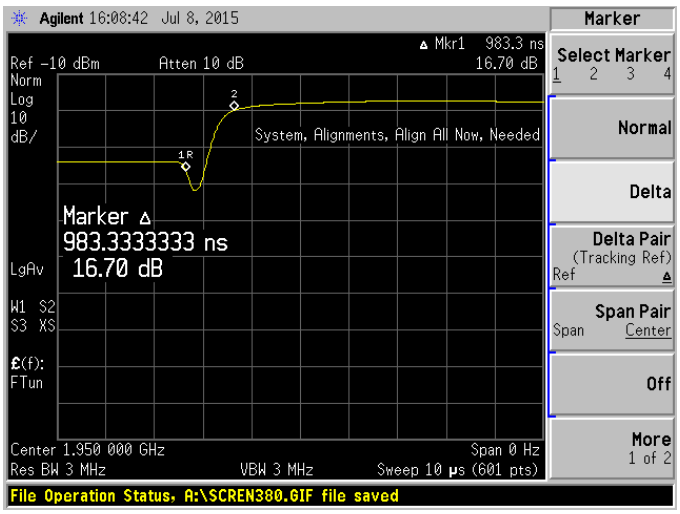
Switching Time



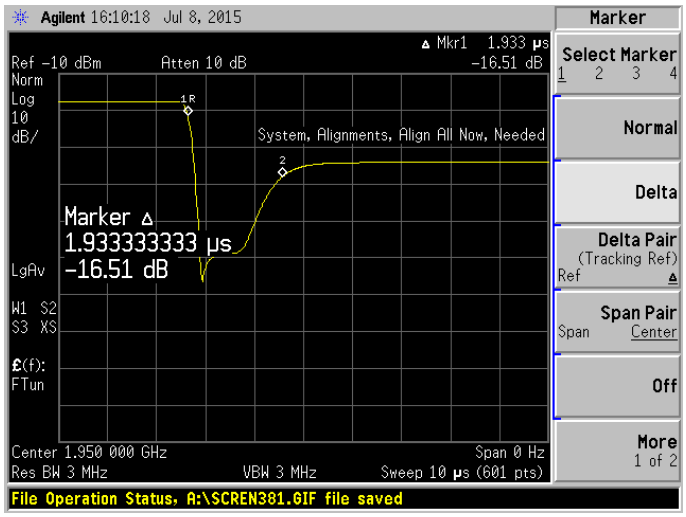


Transition	Value	Units
Bypass to LNA mode	983	ns
LNA to Bypass mode	1.9	µs

R4, valued 91K, is required to achieve the switching times listed above. The placement of R4 is shown on the Qorvo EVB above.

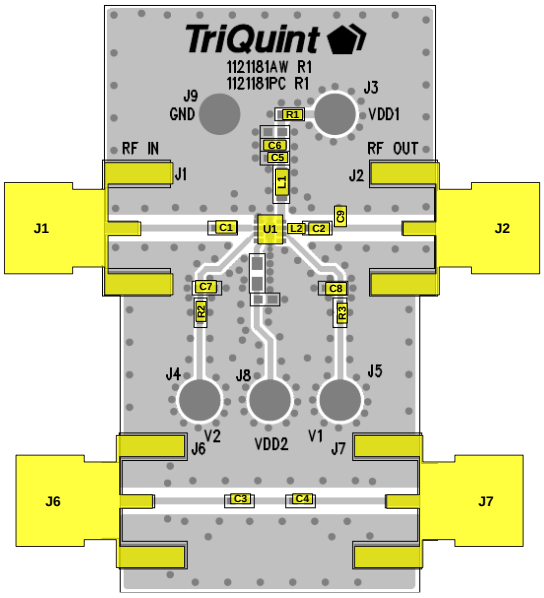


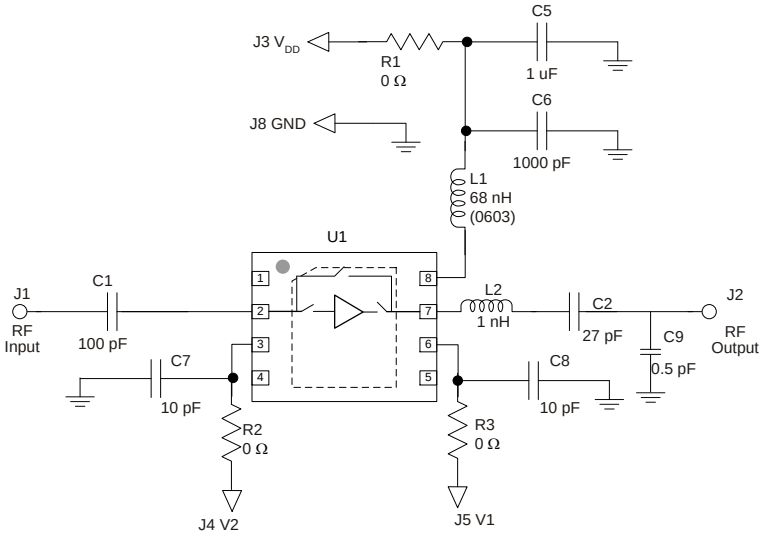
Bypass to LNA mode transition



LNA to Bypass mode transition

TQL9063 – Optimized Return Loss Tune





See Evaluation Board PCB Information section for PCB material and stack-up.

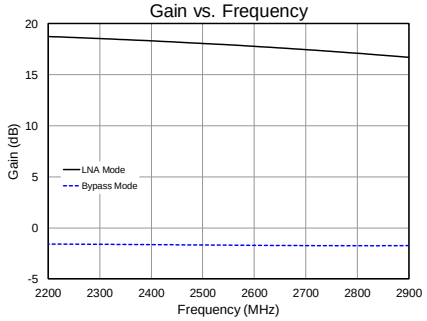
Bill of Material – Optimized Return Loss Tune

Reference Des.	Value	Description	Manuf.	Part Number
U1	-	Bypass LNA	Qorvo	TQL9063
C2	27 pF	CAP, 5%, 50V, NPO/C0G, 0402	Various	
C1, C3, C4	100 pF	CAP, 5%, 50V, 0402	Panasonic	ECJ-0EC1H101J
C6	1000 pF	CAP, 10%, 50V, 0402	various	
C5	1.0 µF	CAP, 10%, 10V, X7S, 0402	various	
C9	0.5 pF	CAP, ±0.1pF, 50V, 0402	Murata	GJM1555C1HR50BB01D
R1, R2, R3	0 Ω	RES, 1/10W, 0402	various	
L1	68 nH	IND, 5%, CER CORE, 0603	Coilcraft	0603CS-68NXJL
L2	1 nH	IND, ±0.1nH, 0402	Murata	LQP15MN1N0B

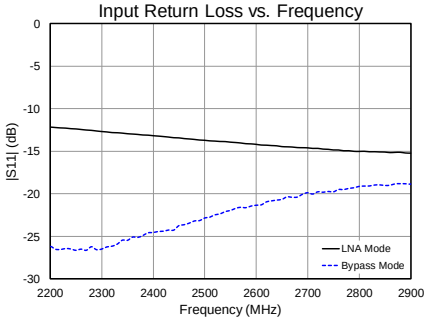
Performance Plots- Optimized Return Loss

Test conditions unless otherwise noted: V_{DD} = +5 V

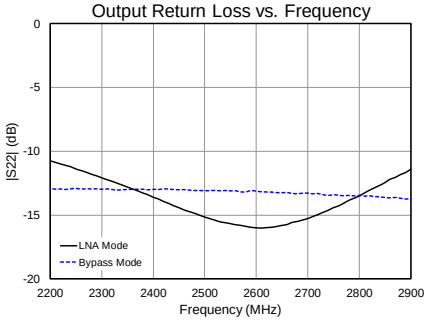
Gain vs. Frequency



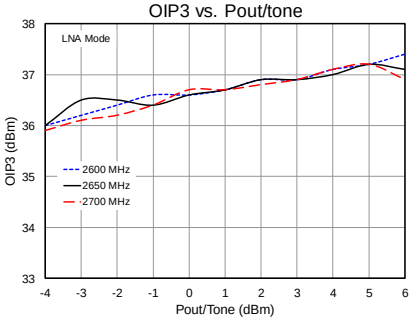
Input Return Loss vs. Frequency



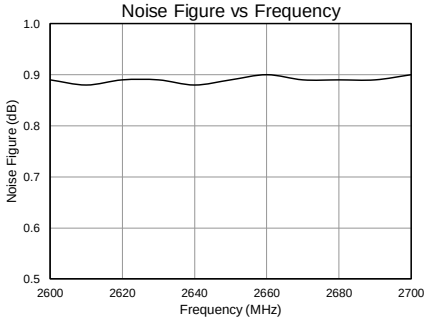
Output Return Loss vs. Frequency



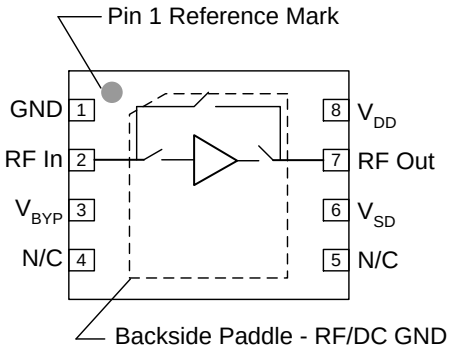
OIP3 vs. Pout/tone



Noise Figure vs Frequency



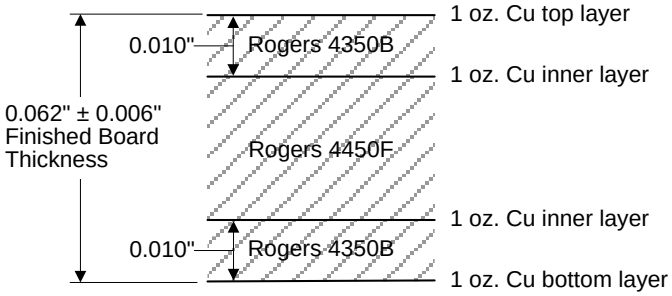
Pin Configuration and Description



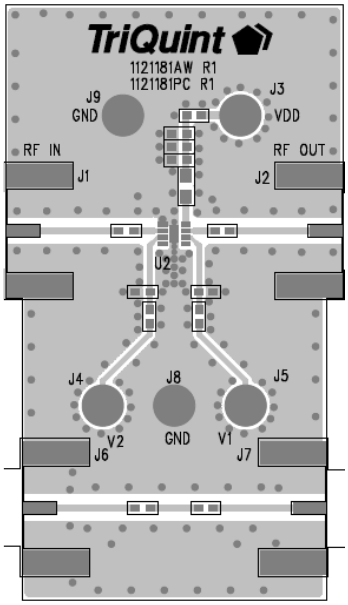
Pin No.	Label	Description
1	GND	RF/DC Ground pin.
2	RF In	RF input pin. DC block required.
3	V_{BYP}	Control pin for bypass mode. The LNA is automatically turned off when the bypass mode is activated. Refer to truth table.
4, 5	N/C	No internal connection. Provide grounded PCB land pads for mounting integrity.
6	V_{SD}	Control pin to disable the LNA. Refer to truth table.
7	RF Out	RF output pin. DC block required.
8	V_{DD}	Supply voltage pin.
Backside Paddle	RF/DC GND	RF/DC Ground. Follow recommended via pattern and ensure good solder attach for best thermal and electrical performance.

Evaluation Board PCB Information

Qorvo PCB 1121181 Material and Stack-up

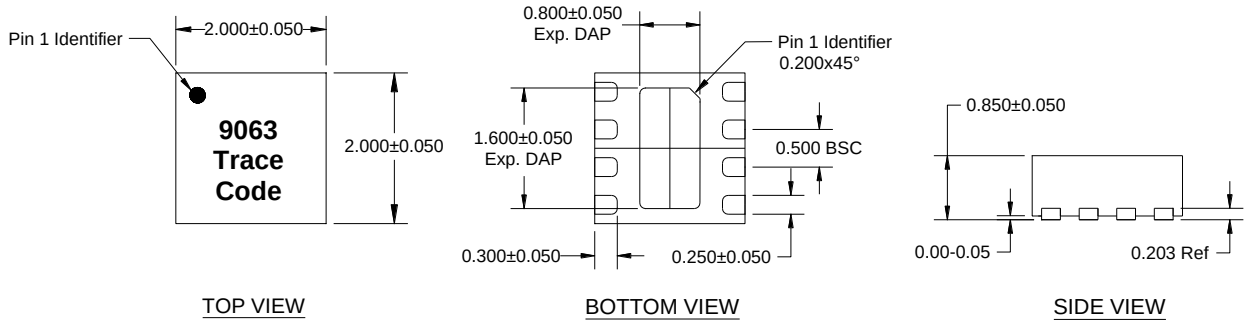


50 ohm line dimensions: width = .020”, spacing = .032”



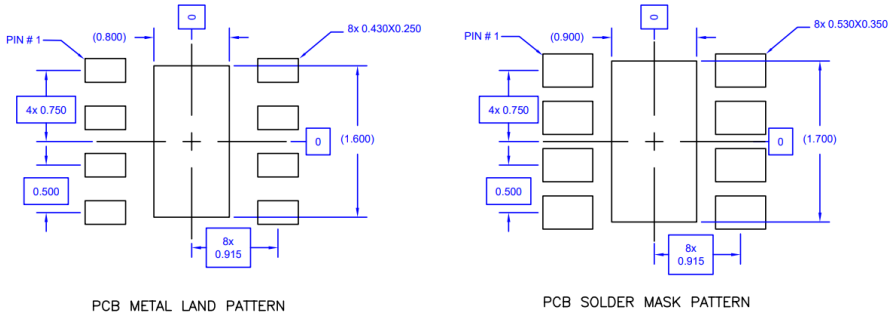
Mechanical Information

Package Marking and Dimensions



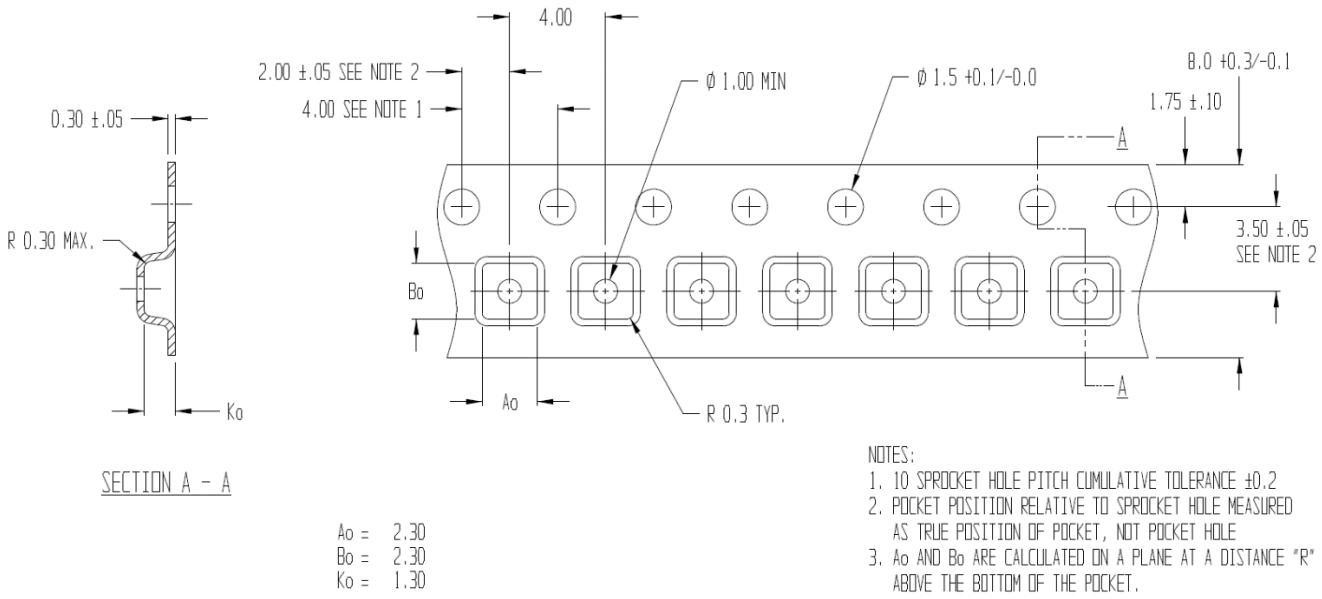
Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-229.
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern

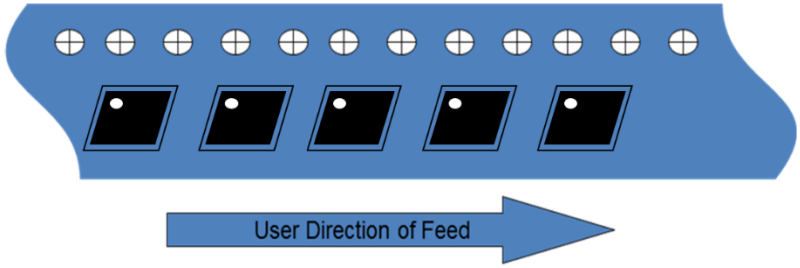


Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated through diameter of 0.25 mm (0.010").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Tape and Reel Information – Carrier and Cover Tape Dimensions

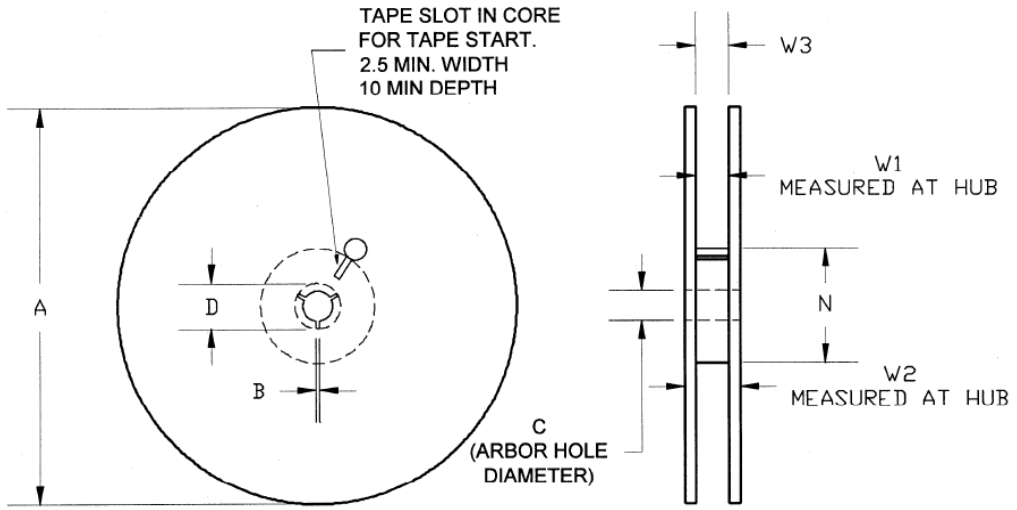


Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.091	2.30
	Width	B0	0.091	2.30
	Depth	K0	0.039	1.30
	Pitch	P1	0.157	4.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.138	3.50
Cover Tape	Width (Reference Only)	C	0.213	5.40
Carrier Tape	Width	W	0.315	8.00



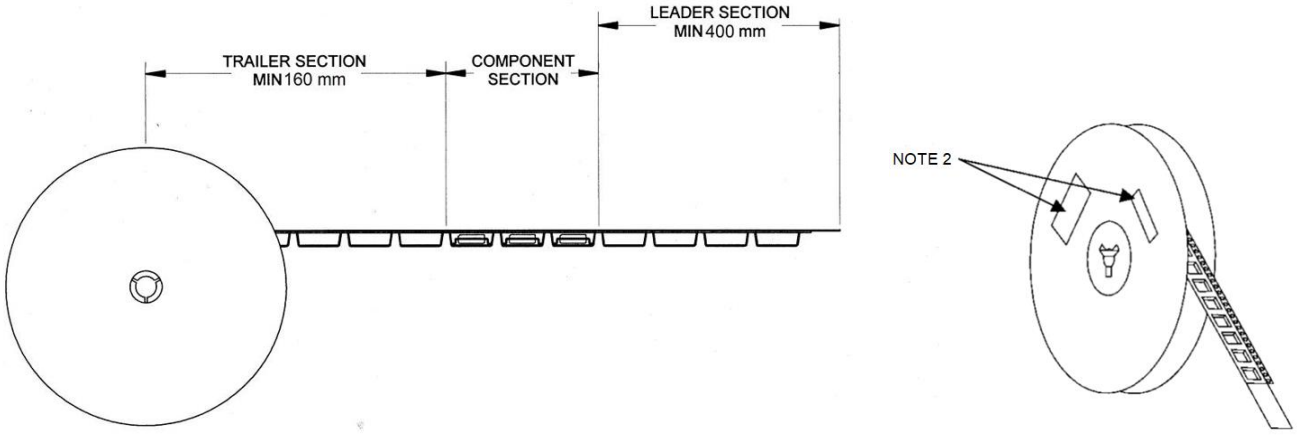
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2500 pieces on a 7” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177.0
	Thickness	W2	0.559	14.2
	Space Between Flange	W1	0.346	8.8
Hub	Outer Diameter	N	2.283	58.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.