TQP3M9037

Ultra Low-Noise, High Linearity LNA

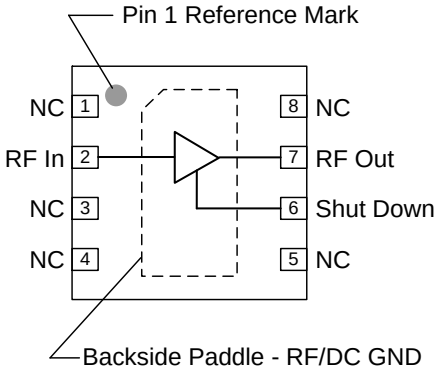
General Description

The TQP3M9037 is a high-linearity, ultra-low noise gain block amplifier in a small 2 x 2 mm surface-mount package. At 1.95 GHz, the amplifier typically provides 20 dB gain, +35 dBm OIP3, and 0.4 dB noise figure while drawing 70 mA current from a +5 V supply. This amplifier does not require a negative supply for operation and can be biased from a single positive supply ranging from +3.3 to +5 volts. The device is housed in a green/RoHS-compliant industry-standard 2 x 2 mm package.

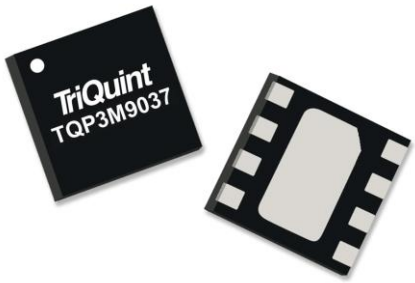
The TQP3M9037 is internally matched using a high performance E-pHEMT process and only requires four external components for operation from a single positive supply: an external RF choke and blocking/bypass capacitors. This low noise amplifier contains an internal active bias to maintain high performance over temperature and integrates a shut-down biasing capability to allow for operation for TDD applications.

The TQP3M9037 covers the 0.7 – 6.0 GHz frequency band and is targeted for wireless infrastructure. It is pin compatible with the low-band, 0.4–2.0 GHz TQP3M9036.

Functional Block Diagram



Top View



8 Pin 2X2 mm DFN Package

Product Features

- 0.7-6.0 GHz Operational Bandwidth
- Ultra Low Noise Figure, 0.4 dB NF at 1.95 GHz
- High Gain, 20 dB Gain at 1.95 GHz
- High Linearity, +35 dBm Output IP3
- High Input Power Ruggedness, +22 dBm CW
- Unconditionally Stable
- Integrated On-chip Matching, 50 Ohm In/Out
- Integrated Active Bias
- Integrated Shutdown Control Pin
- +3V to +5V Supply; Does Not Require −Vgg
- Pin Compatible with Low-Band TQP3M9036

Applications

- Repeaters
- Mobile Infrastructure
- LTE / WCDMA / CDMA / GSM
- General Purpose Wireless
- TDD or FDD Systems

Ordering Information

Part No.	Description
TQP3M9037	Ultra low noise, High IP3 LNA
TQP3M9037-PCB	0.7 – 6.0 GHz Evaluation Board

Standard T/R size = 2500 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to 150°C
Supply Voltage (V_{DD})	+7 V
RF Input Power, CW, 50Ω, T=25°C	+22 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD})	3.0	4.2	5.25	V
T_{CASE}	−40		+105	°C
Tj for >10^6 hours MTTF			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} =+5V, Temp=+25°C, 50 Ω system.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		700		6000	MHz
Test Frequency			1950		MHz
Gain		18.5	20.0	21.5	dB
Input Return Loss			10		dB
Output Return Loss			11		dB
Noise Figure			0.40	0.65	dB
Output P1dB			+20		dBm
Output IP3	Pout=+5 dBm/tone, Δf=1 MHz	+32	+35		dBm
Power Shutdown Control (V_{PD})[1]	On state	0		0.4	V
	Off state (Power down)	2.5	3.3	V_{DD}	V
Current, I_{DD}	On state	40	70	90	mA
	Off state (Power down)		3	4	mA
Shutdown pin current, I_{SD}	V_{PD} ≥ +2.5 V		140		µA
Switching Speed[(2)]	Rise time (10% to 90%)		116		ns
	Fall time (90% to 10%)		340		ns
Thermal Resistance, θ_{jc}	channel to case			53.4	°C/W

Notes:
1. This voltage is referred to the turret labelled PD on the Qorvo EVB as shown on pg. 4.
2. Input DC block capacitor, C1 = 10 pF. Also see bottom of pg. 5.

VPD (pin 6) Voltage Limits

V_{PD}	Min	Max	Units
V_{low}	0	0.1	V
V_{high}	0.55	V_{DD}	V

S-Parameters

Test Conditions: V_{DD}=+5 V, I_{DD}=70 mA (typ.), T=+25°C, unmatched 50 ohm system, calibrated to device leads

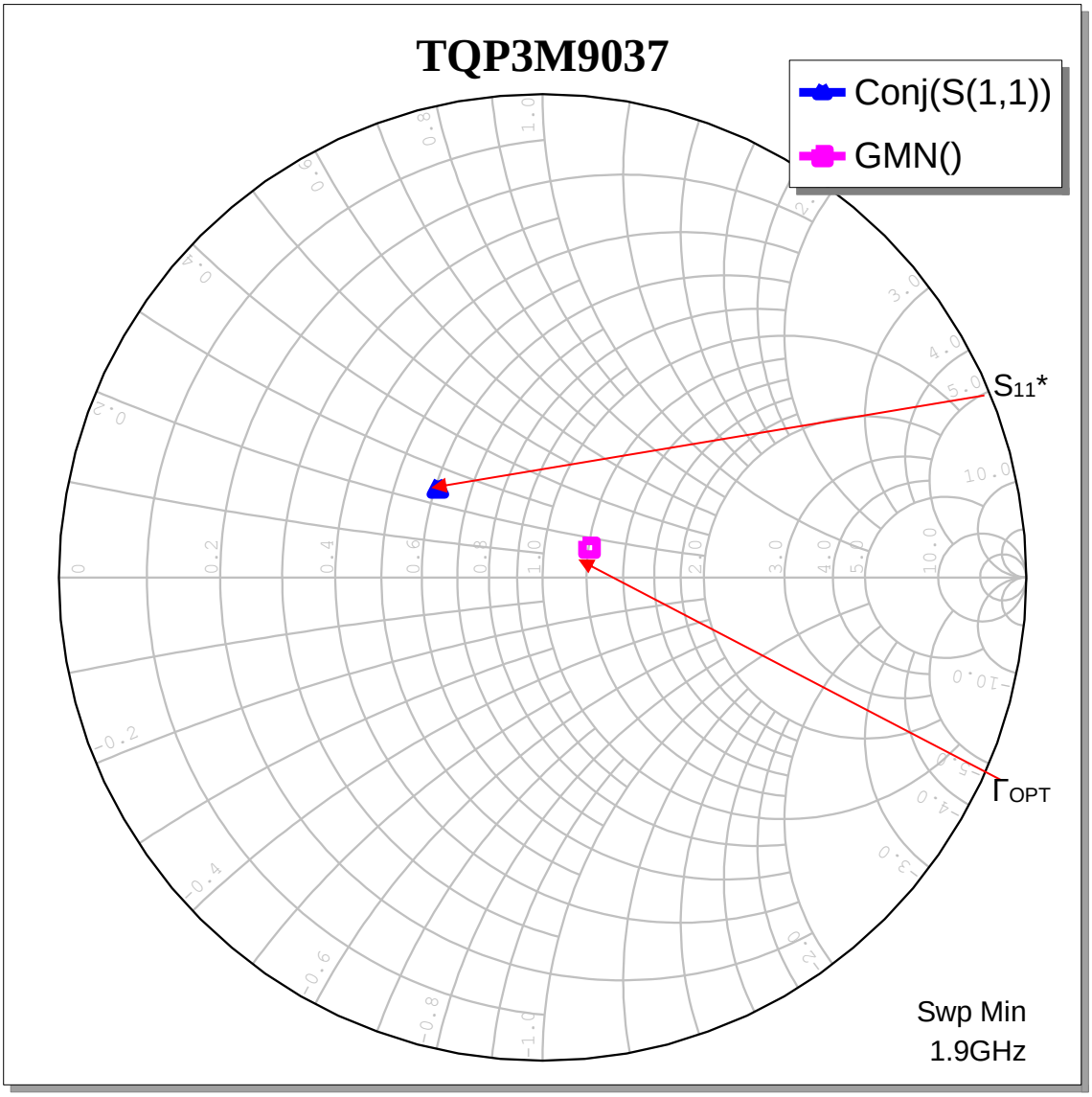
Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
0.05	-7.08	-13.38	28.74	173.92	-32.91	8.58	-15.03	0.20
0.10	-7.30	-16.67	28.70	169.79	-32.76	4.97	-14.12	2.20
0.20	-7.55	-27.25	28.51	160.47	-32.60	5.69	-13.67	-1.25
0.40	-7.89	-48.81	27.68	143.44	-32.47	8.81	-13.09	-6.33
0.60	-8.28	-67.86	26.67	128.94	-32.31	11.76	-12.61	-12.97
0.80	-8.67	-82.83	25.57	116.72	-31.94	14.83	-12.17	-19.29
1.00	-9.10	-96.01	24.54	106.22	-31.49	16.95	-11.87	-25.85
1.20	-9.48	-106.85	23.55	97.05	-30.96	17.84	-11.62	-31.76
1.40	-9.97	-116.61	22.63	88.79	-30.34	19.60	-11.45	-37.19
1.60	-10.36	-126.05	21.78	81.19	-29.81	19.78	-11.41	-42.80
1.80	-10.78	-135.06	20.99	74.13	-29.42	19.53	-11.43	-47.57
2.00	-11.14	-144.52	20.28	67.42	-28.85	19.14	-11.56	-53.18
2.20	-11.43	-153.91	19.61	60.92	-28.45	19.04	-11.79	-58.28
2.40	-11.54	-163.77	19.00	54.49	-27.99	17.71	-12.17	-64.71
2.60	-11.50	-174.25	18.41	48.28	-27.67	16.22	-12.63	-71.10
2.80	-11.30	175.64	17.86	41.94	-27.19	14.85	-13.20	-79.45
3.00	-10.90	166.39	17.33	35.76	-26.85	12.36	-13.86	-89.04
3.20	-10.45	157.46	16.79	29.69	-26.50	10.04	-14.51	-101.79
3.40	-9.89	150.34	16.29	23.57	-26.19	8.06	-14.74	-116.68
3.60	-9.29	144.41	15.76	17.56	-25.95	5.99	-14.57	-133.42
3.80	-8.86	140.00	15.22	11.78	-25.75	3.39	-13.78	-148.27
4.00	-8.32	136.87	14.67	6.13	-25.57	1.64	-12.70	-161.52
4.20	-8.03	133.99	14.10	0.74	-25.50	-1.15	-11.25	-169.83
4.40	-7.68	136.01	13.50	-4.52	-25.43	-2.83	-10.05	-178.99
4.60	-7.40	136.69	12.83	-9.19	-25.38	-4.24	-8.64	175.79
4.80	-7.21	140.78	12.13	-13.41	-25.53	-5.31	-7.25	170.49
5.00	-6.35	149.93	11.26	-16.91	-25.78	-6.38	-6.41	163.10

Noise Parameters

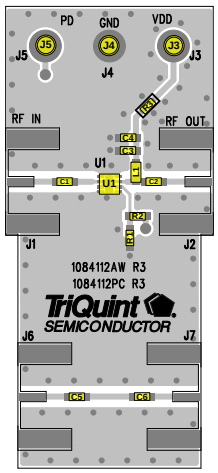
Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=70 mA (typ.), Temp=+25°C, 50 Ohm system

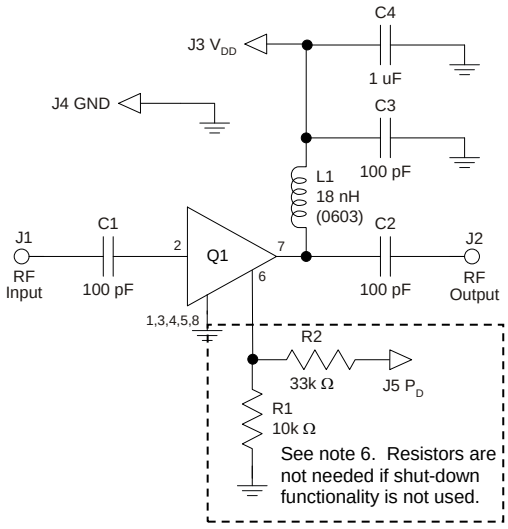
Freq (GHz)	NF_{min} (dB)	MagOpt (mag)	AngOpt (deg)	Rn (Ω)
1.5	0.40	0.15	14.1	0.08
1.7	0.29	0.16	43.7	0.06
1.8	0.3	0.13	55.1	0.06
1.9	0.30	0.11	30.2	0.06
2	0.32	0.11	65.3	0.05
2.1	0.32	0.13	77.6	0.05
2.2	0.35	0.14	89.0	0.05
2.4	0.43	0.06	85.8	0.05
2.5	0.51	0.02	42.1	0.06
2.6	0.46	0.08	157.4	0.04
2.7	0.46	0.07	148.6	0.05

Γopt and S11*



TQP3M9037-PCB Evaluation Board





Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. R3 (0 Ω jumper) is not shown on the schematic and may be replaced with copper trace in the target application layout.
3. All components are of 0402 size unless stated on the schematic.
4. C1, C2, and C3 are non-critical values. The reactive impedance should be as low as possible at the frequency of operation for optimal performance.
5. The L1 value is non-critical and needs to provide high reactive impedance at the frequency of operation.
6. R1 and R2 are optional and do not need to be loaded if the shut-down functionality is not needed; i.e. FDD applications. If R1 and R2 are not loaded, the LNA will operate in its standard "ON" state.
7. A through line is included on the evaluation board to de-embed the board losses.

Bill of Material − TQP3M9037-PCB

Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board	Qorvo	
U1	n/a	Ultra Low Noise, High Linearity LNA	Qorvo	TQP3M9037
R1	10 kΩ	Resistor, Chip, 0402, 5%, 1/16W	various	
R2	33 kΩ	Resistor, Chip, 0402, 5%, 1/16W	various	
R3	0 Ω	Resistor, Chip, 0402, 5%, 1/16W	various	
L1	18 nH	Inductor, 0603, 5%, Ceramic	various	
C4	1.0 uF	Cap., Chip, 0402, 10%, 10V, X5R	various	
C1, C2, C3, C5, C6	100 pF	Cap., Chip, 0402, 5%, 50V, NPO/COG	various	

Resistive Divider Values

V_{PD} Signal Level	+3.3 V TTL	+2.5 V TTL	Units
R1	10 kΩ	11 kΩ	Ω
R2	33 kΩ	33 kΩ	Ω

Switching Speed

V_{PD} toggled with a 1KHz square wave(0-2V), V_{DD}=5V, RF freq = 1.95GHz

Parameter	C1=100pF	C1=10pF	Units
Turn-off Fall time (50% TTL – 10% RF)	1.4	0.34	µs
Turn-on Rise time (50% TTL – 90% RF)	0.39	0.116	µs

Typical Performance – TQP3M9037-PCB V_{DD} = +5 V

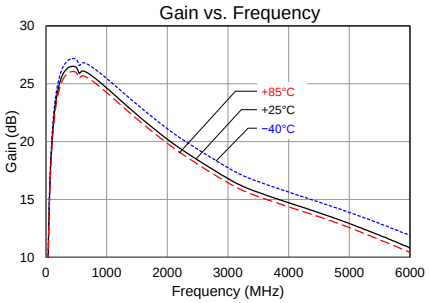
Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=70 mA (typ.), Temp=+25 °C

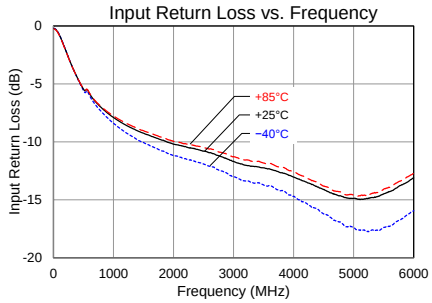
Parameter	Conditions	Typical Values					Units
Frequency		900	1700	1950	2300	2600	MHz
Gain		25.3	21.4	20.4	19.1	18.1	dB
Input Return Loss		7.4	9.6	10.1	10.5	10.9	dB
Output Return Loss		11.7	11.6	11.0	10.2	9.8	dB
Output P1dB		+22	+20.7	+20	+19.8	+19.5	dBm
OIP3	Pout=+5 dBm/tone, Δf=1 MHz	+34.4	+34.9	+35.7	+35.1	+35.0	dBm
Noise figure (1)		0.4	0.36	0.41	0.43	0.53	dB

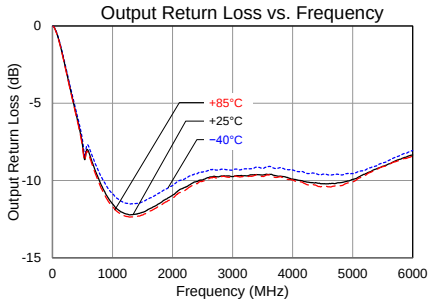
Notes:
1. Noise figure data shown in the table above is de-embedded to the device pin pads.

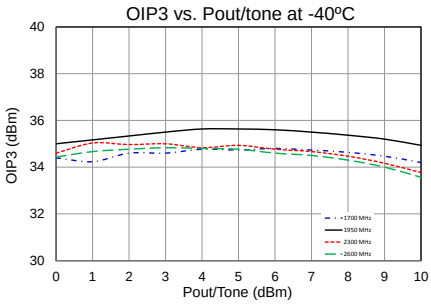
Performance Plots – TQP3M9037-PCB V_{DD} = +5 V

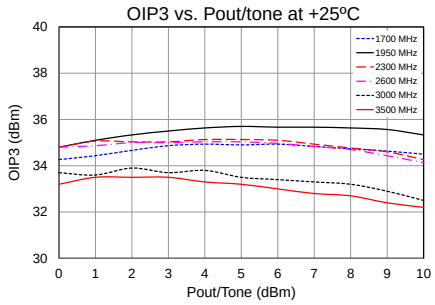
Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=70 mA (typ.), Temp=+25°C

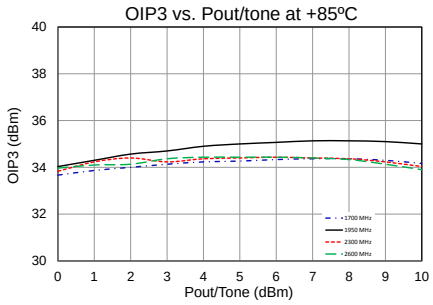


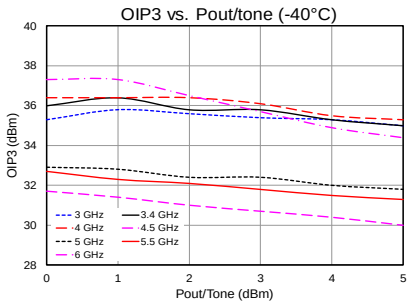


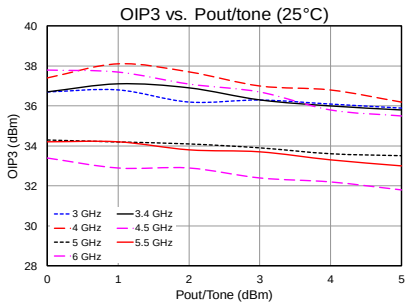


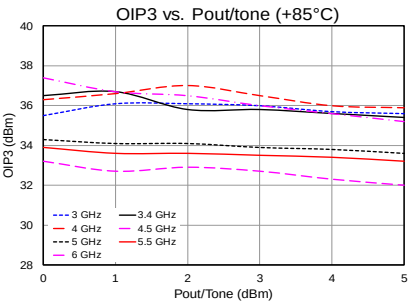






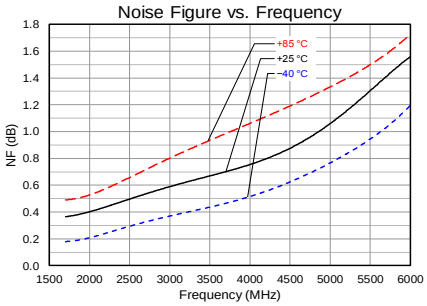


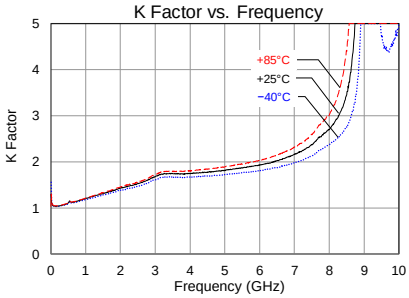


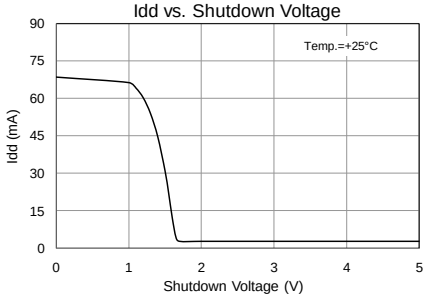


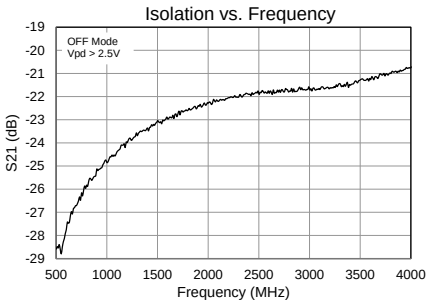
Performance Plots − TQP3M9037-PCB V_{DD} = +5 V

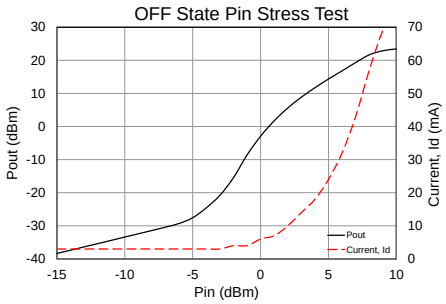
Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=70 mA (typ.), Temp=+25°C











Typical Performance – TQP3M9037-PCB V_{DD} = +3.3 V

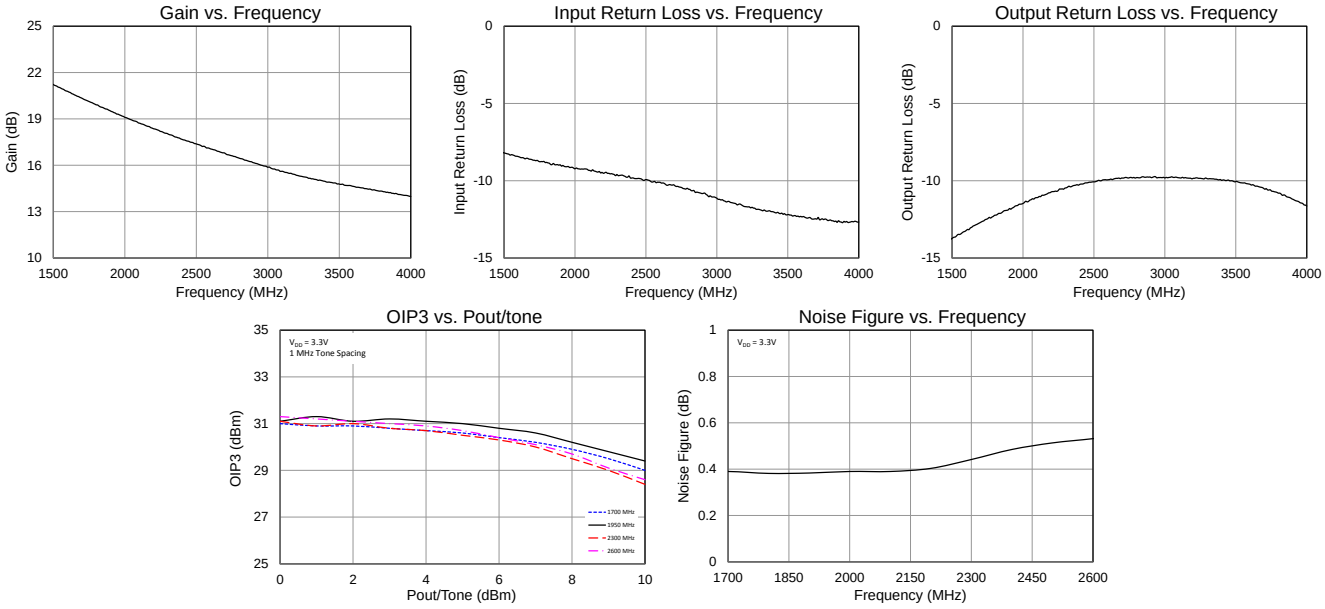
Test conditions unless otherwise noted: V_{DD} = +3.3V, I_{DD} = 44 mA (typ.), Temp= +25°C

Parameter	Conditions	Typical Values				Units
Frequency		1700	1950	2300	2600	MHz
Gain		19.9	19.2	17.7	17.0	dB
Input Return Loss		8.3	9.2	9.5	10.5	dB
Output Return Loss		11.3	11.3	9.5	9.5	dB
Output P1dB		+16.2	+16.1	+15.5	+15.5	dBm
OIP3	Pout = +5 dBm/tone, Δf=1 MHz	+30.6	+31	+30.5	+30.7	dBm
Noise figure (1)		0.4	0.38	0.44	0.53	dB

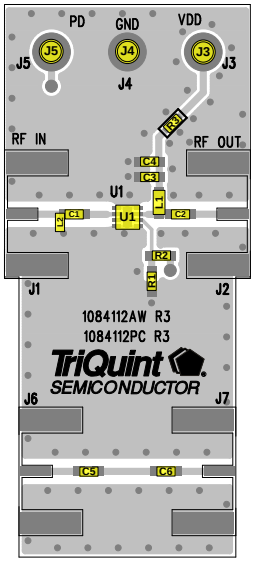
Notes:
1. Noise figure data shown in the table above is de-embedded from the eval board loss.

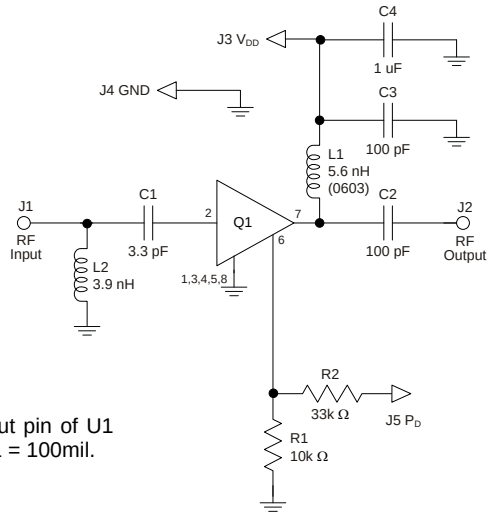
Performance Plots – TQP3M9037-PCB V_{DD} = +3.3 V

Test conditions unless otherwise noted: V_{DD} = +3.3V, I_{DD} = 44 mA (typ.), Temp= +25°C



Reference Design – Optimized Return Loss





Notes:

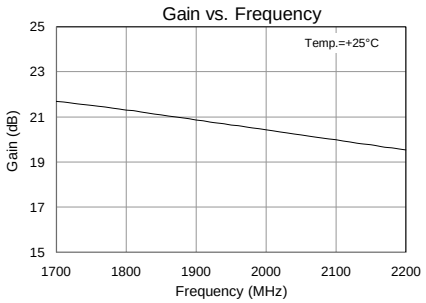
1. Distance from input pin of U1 to right edge of C1 = 100mil.

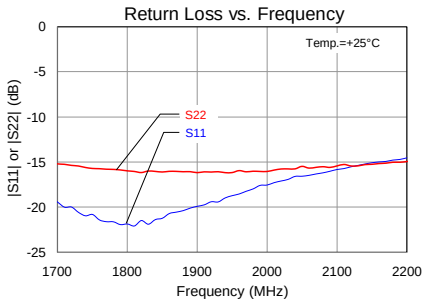
Bill of Material

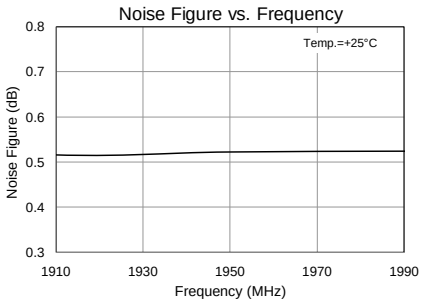
Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	Ultra Low Noise Amplifier	Qorvo	TQP3M9037
R1	10 kΩ	Resistor, Chip, 0402, 5%, 1/16W	various	
R2	33 kΩ	Resistor, Chip, 0402, 5%, 1/16W	various	
R3	0 Ω	Resistor, Chip, 0402, 5%, 1/16W	various	
L1	5.6 nH	Inductor, 0603, 5%, Ceramic	various	
L2	3.9 nH	Inductor, 0402, 5%, Ceramic	various	
C1	3.3 pF	Cap, Chip, 0402, ±0.25 pF, 50V, NPO/COG	various	
C4	1.0 uF	Cap, Chip, 0402, 10%, 10V, X5R	various	
C2, C3, C5, C6	100 pF	Cap, Chip, 0402, 5%, 50V, NPO/COG	various	

Performance Plots

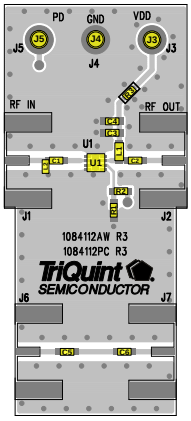
Test conditions unless otherwise noted: V_{DD} = +5V, I_{DD} = 70 mA (typ.), Temp= +25°C

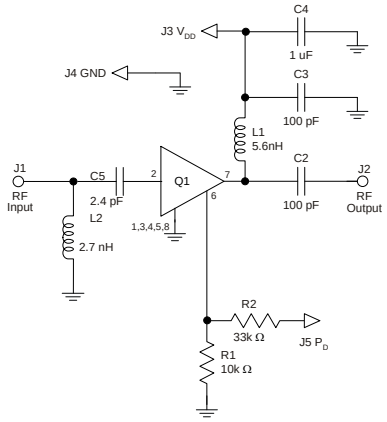




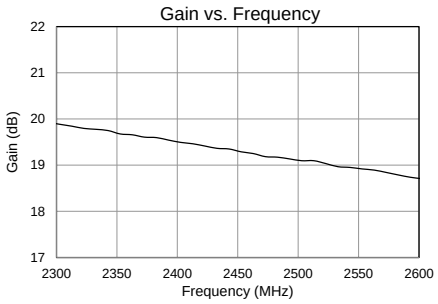


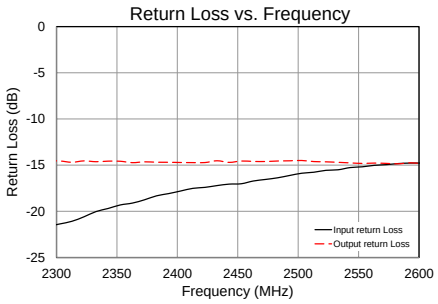
Evaluation Board: 2300 – 2600 MHz Reference Design

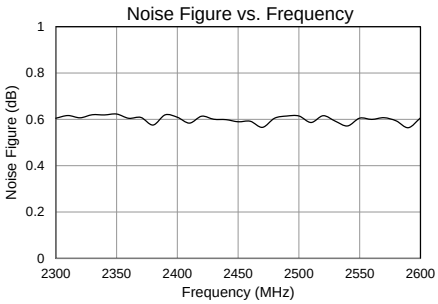




Performance Plots: 2300 – 2600 MHz Reference Design



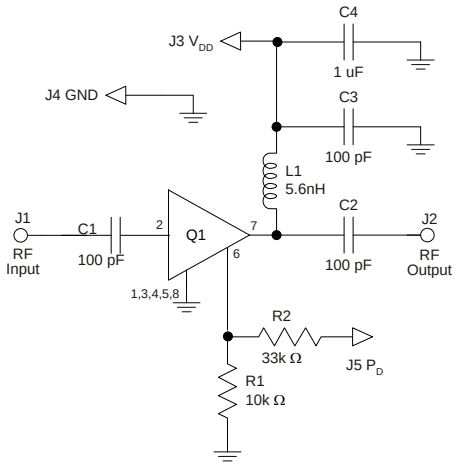


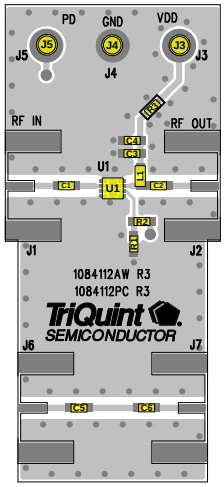


Bill of Material: 2300 – 2600 MHz Reference Design

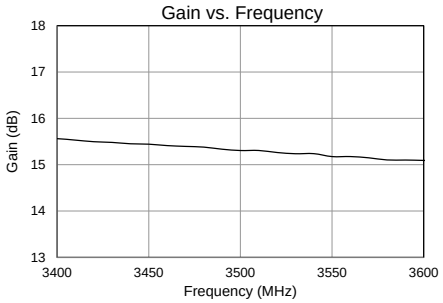
Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	Ultra Low Noise Amplifier	Qorvo	TQP3M9037
R1	10 kΩ	Resistor, Chip, 0402, 5%, 1/16W	various	
R2	33 kΩ	Resistor, Chip, 0402, 5%, 1/16W	various	
R3	0 Ω	Resistor, Chip, 0402, 5%, 1/16W	various	
L1	5.6 nH	Inductor, 0603, 5%, Ceramic	Coilcraft	0603CS-5N6XJL
L2	2.7 nH	Inductor, 0402, 5%, Ceramic	TOKO	LL1005-FHL2N7S
C1	2.4 pF	Cap, Chip, 0402, ±0.25 pF, 50V, NPO/COG	AVX	04023J2R4BBSTR
C4	1.0 uF	Cap, Chip, 0402, 10%, 10V, X5R	various	
C2, C3, C5, C6	100 pF	Cap, Chip, 0402, 5%, 50V, NPO/COG	various	

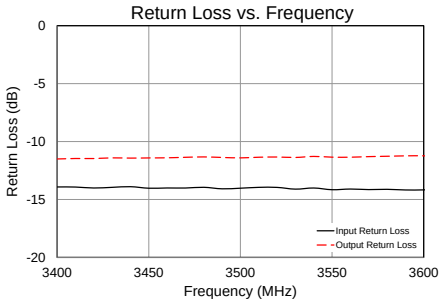
Evaluation Board: 3400 -3600 MHz Reference Design

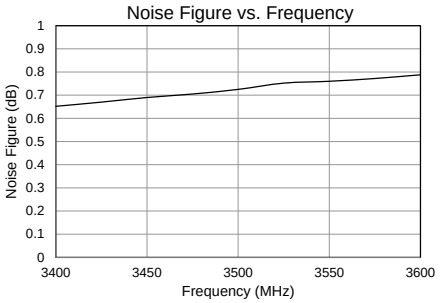




Performance Plots: 3400 -3600 MHz Reference Design







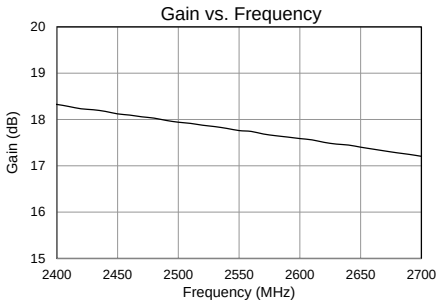
Bill of Material: 3400 -3600 MHz Reference Design

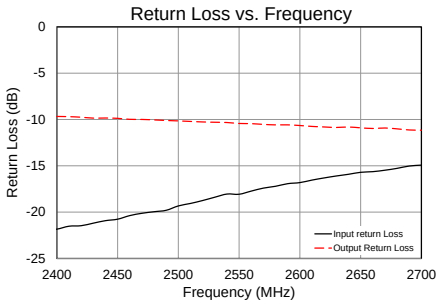
Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	Ultra Low Noise Amplifier	Qorvo	TQP3M9037
R1	10K Ω	Resistor, Chip, 0402, 5%, 1/16W	various	
R2	33K Ω	Resistor, Chip, 0402, 5%, 1/16W	various	
R3	0 Ω	Resistor, Chip, 0402, 5%, 1/16W	various	
L1	5.6 nH	Inductor, 0603, 5%, Ceramic	Coilcraft	0603CS-5N6XJL
C4	1.0 uF	Cap, Chip, 0402, 10%, 10V, X5R	various	
C1, C2, C3, C5, C6	100 pF	Cap, Chip, 0402, 5%, 50V, NPO/COG	various	

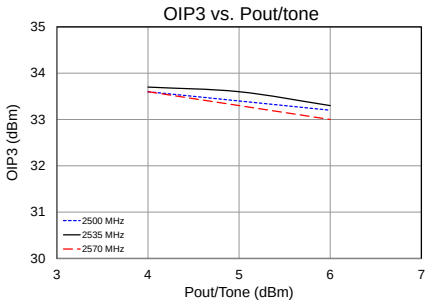
+3.3 V V_{DD} Performance Improvement with External Input Bias

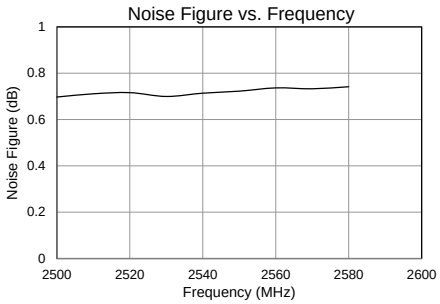
This page shows performance data of TQP3M9037 tuned for better input return loss for B7 UL. The device is biased at 3.3V Vdd. At this bias voltage the device draws about 45mA Idd but the OIP3 drops by almost 5dB. To improve the linearity performance an external bias is introduced to the input port by a resistive divider tied to the 3.3V. This results in increased current draw of about 60mA and the OIP3 is up by 5dB.

Performance Plots

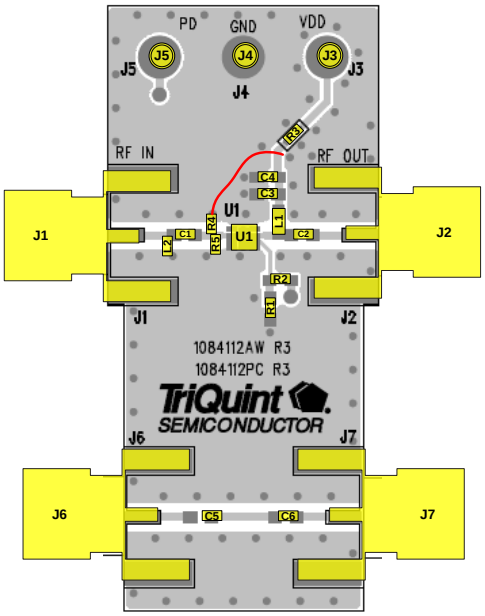


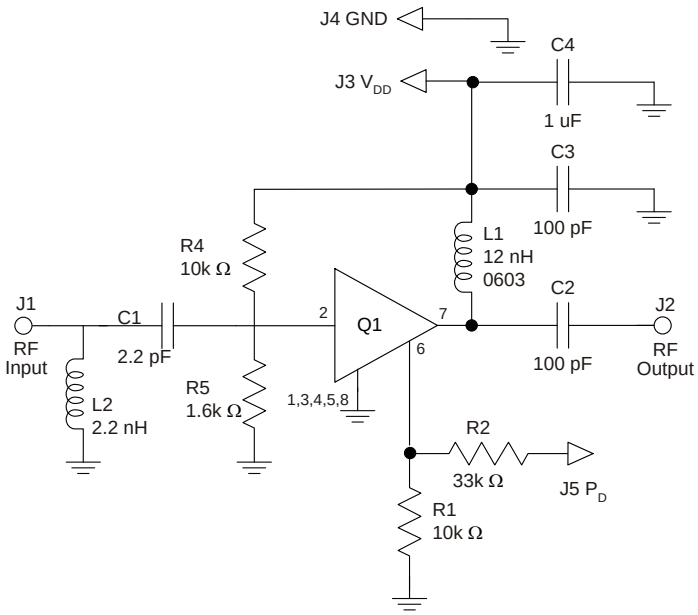






Evaluation Board

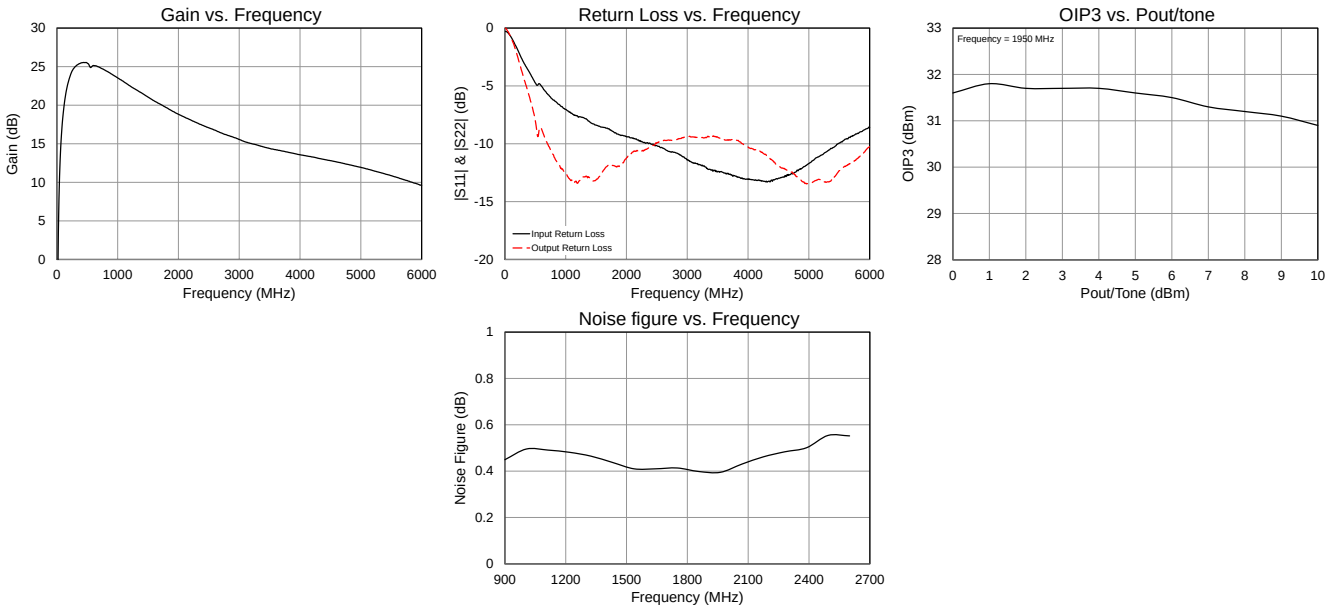




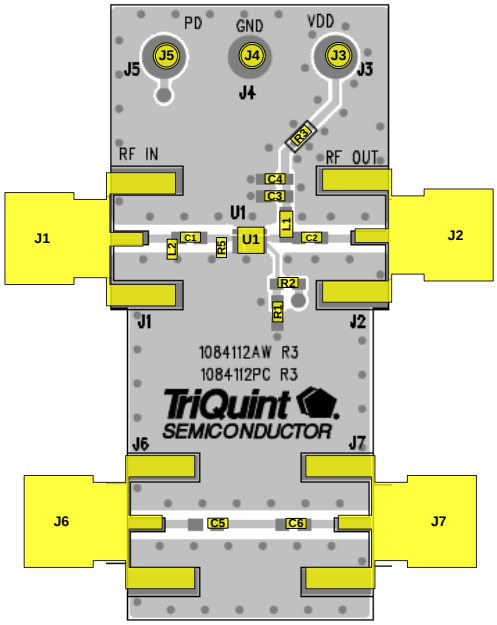
+5 V V_{DD} Reduced Current Reference Design

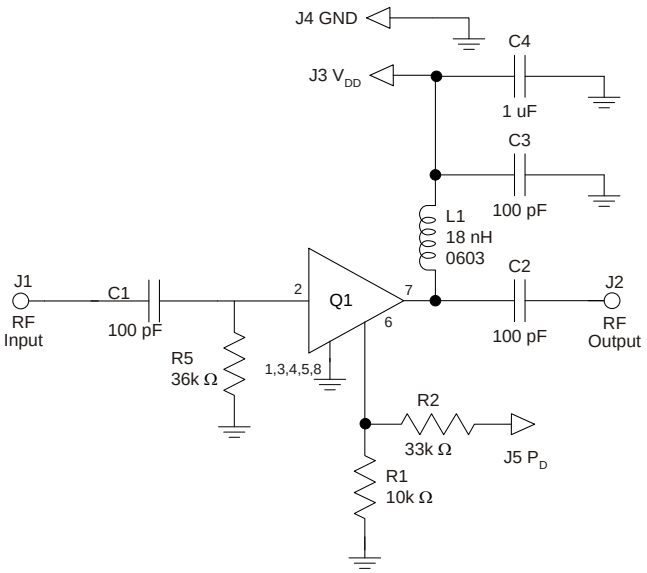
This page shows performance data of TQP3M9037 with reduced current consumption of around 40mA. The Vdd is kept at +5V and to reduce the current a shunt resistor of 36K ohms is added at the input pin. This drops the gate voltage of the input transistor and hence bringing the bias point of the LNA down.

Performance Plots

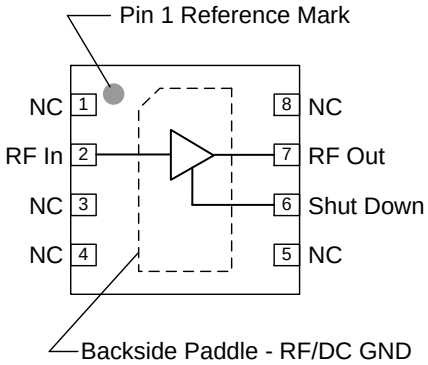


Evaluation Board





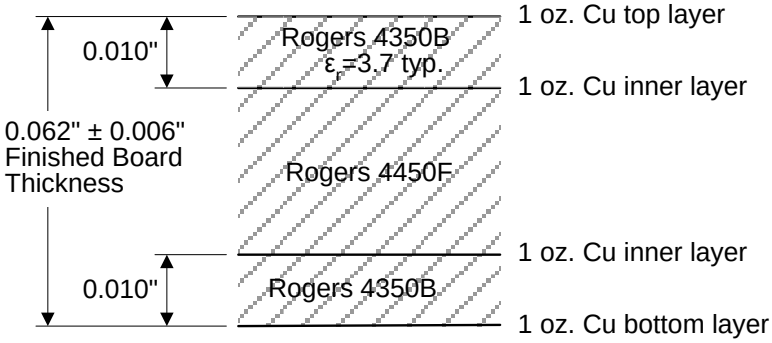
Pin Configuration and Description



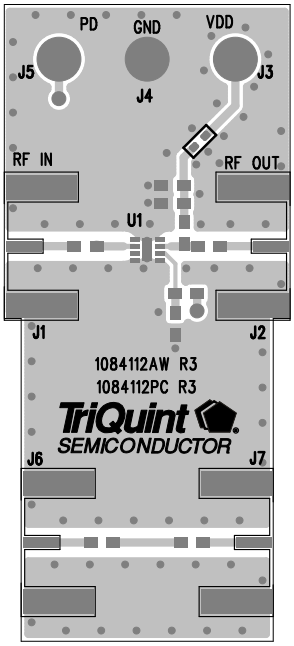
Pin No.	Label	Description
2	RF In	RF Input pin. A DC Block is required.
6	Shut Down	A high voltage turns off the device. If the pin is not connected or is less than 1V, then the device will operate under its normal operating condition.
7	RF Out / DCBias	RF Output pin. DC bias will also need to be injected through a RF bias choke/inductor for operation.
1, 3, 4, 5, 8	NC	No electrical connection. Provide grounded land pads for PCB mounting integrity.
Backside Paddle	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

Qorvo PCB 1084112 Material and Stack-up



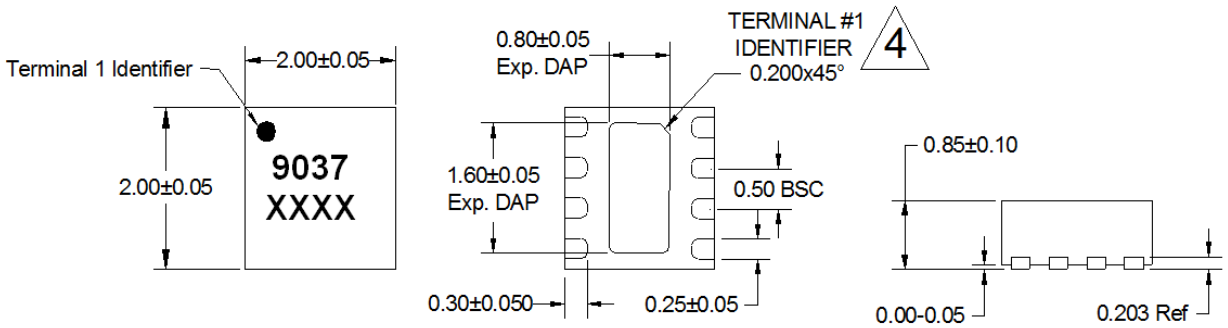
50 ohm line dimensions: width = 0.020”, spacing = 0.032”



Mechanical Information

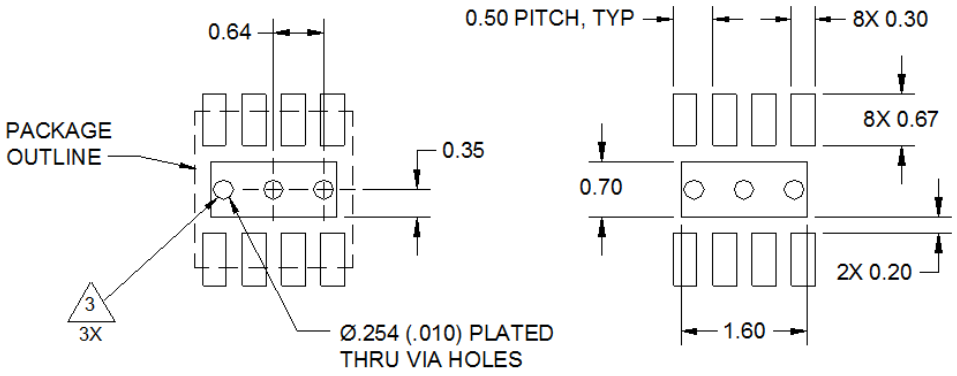
Package Marking and Dimensions

Marking: Part number – 9037
Lot code – XXXX



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.