TQP3M9041

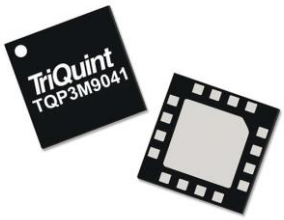
2300 – 6000 MHz Dual LNA

Product Description

The TQP3M9041 is a high linearity, ultra low noise figure dual device amplifier in a 4x4 mm package. At 2600 MHz in a balanced configuration, this LNA provides 18.4dB gain, 20.2 dBm IIP3 and 0.8 dB noise figure. The part does not require a negative supply for operation and is bias adjustable for both drain current and voltage. The device is housed in a green/RoHS-compliant industry standard QFN package.

The TQP3M9041 consists of a single monolithic GaAs E-pHEMT die and integrates bias circuitry as well as shut-down capability allowing the LNA to be useful for both FDD and TDD applications.

The TQP3M9041 is optimized for the 2500−2700 MHz band, but can be used outside of the band. Qorvo offers pin-compatible dual LNAs for 500−1500 MHz (TQP3M9039) and 1500−2300 MHz (TQP3M9040). The balanced amplifier is optimized for high performance receivers in wireless infrastructure and can be used for base-station transceivers or tower-mounted amplifiers.

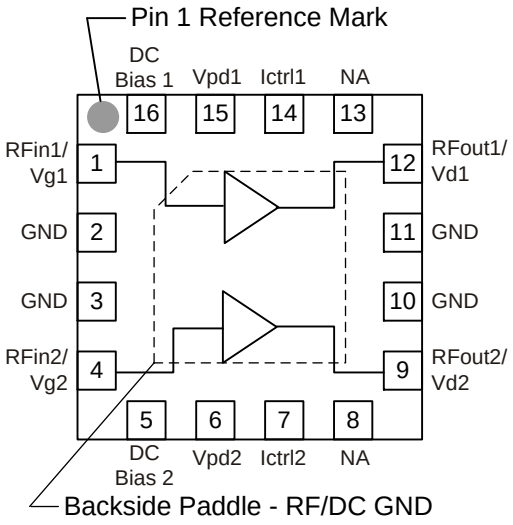


16-pin 4 mm x 4 mm QFN Package

Key Features

- 0.33 dB NFmin (Single Channel) at 2600 MHz
- 2300−6000 MHz operational bandwidth
- Gain = 18.4 dB at 2600 MHz
- +20.2 dBm Input IP3
- Integrated shut-down biasing feature
- Bias adjustable
- Does not require negative voltage supply
- 4x4 mm 16-pin QFN plastic package

Functional Block Diagram



Top View

Applications

- Base Station Receivers
- Tower Mount Amplifiers
- Balanced Amplifiers
- FDD-LTE, TDD-LTE, WCDMA, CDMA, GSM
- General Purpose Wireless

Ordering Information

Part No.	Description
TQP3M9041	2300−6000 MHz Dual LNA
TQP3M9041-PCB	2500−2700 MHz Evaluation Board

Standard T/R size = 2500 pieces on a 13” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to 150°C
Drain Voltage (V_d)	+7 V
I_{dd} (V_d = 5V), single channel	300 mA
Input Power (CW)	+22 dBm
Input Power (DC off condition)	+22 dBm
Input Power (DC off condition & 10% Duty Cycle)	+30 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{pd}	0		+5	V
V_g	0	+0.5	+1	V
V_d	+2		+5	V
I_d, single channel		57	80	mA
Operating Temp. Range	−40		+105	°C
T_{ch} (for>10^6 hrs MTTF)			190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions (1)	Min	Typ	Max	Units
Operational Frequency Range		2300		6000	MHz
Test Frequency			2600		MHz
Gain		17.2	18.4	19.6	dB
Output P1dB			+22.5		dBm
Input IP3	Pin=−13 dBm/tone, Δf=1 MHz	+17	+20.2		dBm
Output IP3	Pout=+5 dBm/tone, Δf=1 MHz		+38.2		dBm
Noise Figure (2)	Balanced Configuration		0.8	1.15	dB
Drain Voltage, V_d			+4.35		V
Drain Current, I_d	Single Channel	35	57	80	mA
Power Down Control Voltage, V_{pd}	On-State	0		+0.3	V
	Off-State	+2.1		V_d	V
Thermal Resistance, θ_{jc}	Junction to case - per channel		53		°C/W

Notes:
1. Test conditions unless otherwise noted: V_d = +4.35V, Temp.=+25°C, tuned balanced configuration.
2. The Noise Figure is de-embedded to the input pin of the input hybrid coupler.

De-embedded S-parameters Data

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
10	-0.08	-1.55	31.76	-178.90	-65.61	72.04	-3.83	5.41
100	-0.50	-10.68	32.14	166.28	-52.51	55.96	-1.53	2.04
200	-1.05	-19.42	31.64	151.59	-49.17	66.30	-1.46	-2.87
500	-3.22	-37.41	28.96	121.07	-42.32	70.95	-1.73	-10.88
750	-4.87	-45.81	26.85	104.52	-39.50	69.80	-1.93	-16.10
1000	-6.16	-52.39	25.05	91.86	-37.11	71.15	-2.08	-21.29
1200	-7.06	-57.60	23.85	83.20	-35.62	68.87	-2.22	-25.66
1400	-7.76	-62.48	22.80	75.39	-34.21	67.84	-2.33	-30.17
1600	-8.45	-68.59	21.91	67.93	-32.82	65.63	-2.46	-35.08
1800	-9.08	-74.44	21.10	60.75	-31.80	63.08	-2.59	-40.23
2000	-9.57	-82.20	20.38	53.44	-30.84	60.61	-2.76	-46.28
2200	-9.79	-86.21	19.63	44.72	-30.49	54.60	-3.25	-52.79
2300	-9.82	-84.43	18.95	43.91	-30.09	62.95	-3.09	-51.68
2400	-9.84	-91.72	18.86	41.02	-29.15	59.62	-2.92	-56.18
2500	-9.86	-95.33	18.62	37.63	-28.66	57.75	-2.94	-59.74
2600	-9.98	-99.27	18.33	34.26	-28.31	56.06	-3.06	-62.94
2700	-9.94	-103.51	18.07	31.03	-27.82	54.48	-3.03	-66.14
2800	-9.88	-105.66	17.80	27.96	-27.46	52.93	-3.01	-69.18
3000	-10.07	-111.89	17.30	21.52	-26.72	49.72	-3.10	-75.44
3200	-10.20	-114.68	16.77	15.32	-26.10	46.67	-3.14	-81.16
3400	-9.85	-121.75	16.42	10.10	-25.13	44.73	-3.09	-86.87
3600	-10.15	-126.13	16.07	3.95	-24.62	40.82	-3.18	-92.92
3800	-10.35	-131.51	15.70	-2.03	-23.94	38.08	-3.26	-98.91
4000	-11.47	-137.19	15.37	-6.61	-23.29	36.19	-3.23	-99.29
4250	-11.77	-148.96	15.01	-14.80	-22.49	31.20	-3.43	-107.68
4500	-12.31	-165.19	14.67	-23.65	-21.74	24.83	-3.83	-116.92
4750	-14.33	173.97	14.14	-33.60	-21.58	15.26	-4.72	-126.02
5000	-13.32	-164.72	13.63	-35.01	-21.34	29.91	-3.76	-126.65
5250	-11.33	158.91	13.84	-46.81	-19.30	17.10	-4.12	-145.25
5500	-10.50	136.31	13.58	-57.49	-18.52	8.06	-4.70	-160.18
5750	-9.39	120.64	13.11	-67.85	-17.91	0.21	-5.11	-175.27
6000	-7.88	105.14	12.50	-78.40	-17.38	-8.68	-5.53	168.20

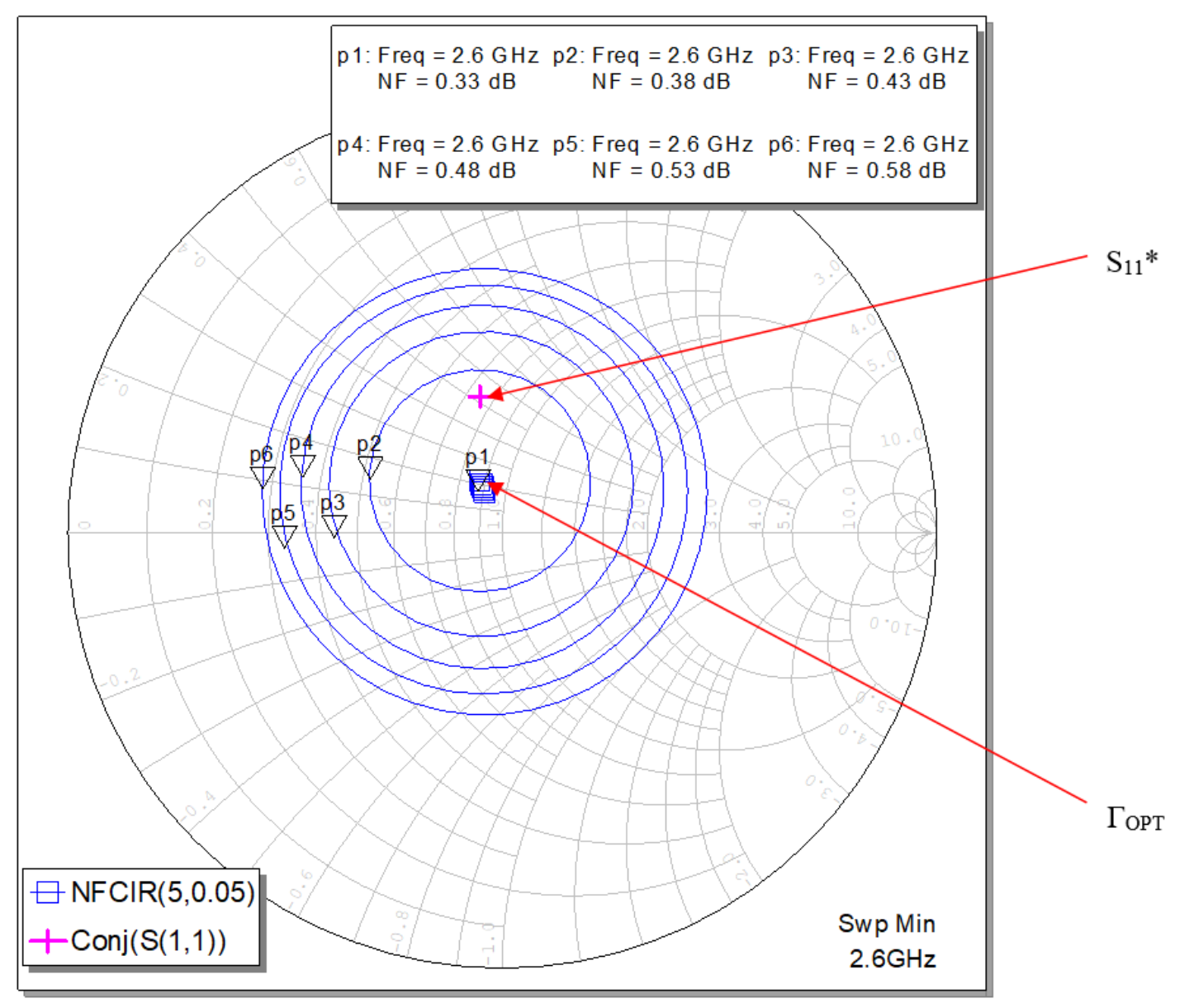
Notes:
1. Test conditions unless otherwise noted: V_{DD}=+4.35 V, I_{DD}=57 mA, Temp=+25°C, 50 Ohm system.

Noise Parameters

Freq (GHz)	NF_{min} (dB)	ΓOpt (mag)	ΓOpt (deg)	Rn (Ω)
2	0.16	0.16	57.92	0.05
2.1	0.21	0.17	71.64	0.05
2.2	0.30	0.20	53.88	0.07
2.3	0.24	0.15	84.16	0.05
2.35	0.27	0.13	97.19	0.05
2.4	0.29	0.13	101.49	0.05
2.5	0.32	0.13	117.86	0.05
2.6	0.33	0.14	113.34	0.04
2.7	0.34	0.12	112.27	0.05
2.8	0.38	0.10	141.65	0.05
2.9	0.38	0.11	153.72	0.05
3	0.53	0.13	-152.67	0.06
3.2	0.64	0.03	89.21	0.06
3.4	0.56	0.09	176.76	0.06
3.6	0.54	0.16	-105.65	0.07
3.8	0.64	0.17	-130.46	0.08
4	0.62	0.16	-127.44	0.06

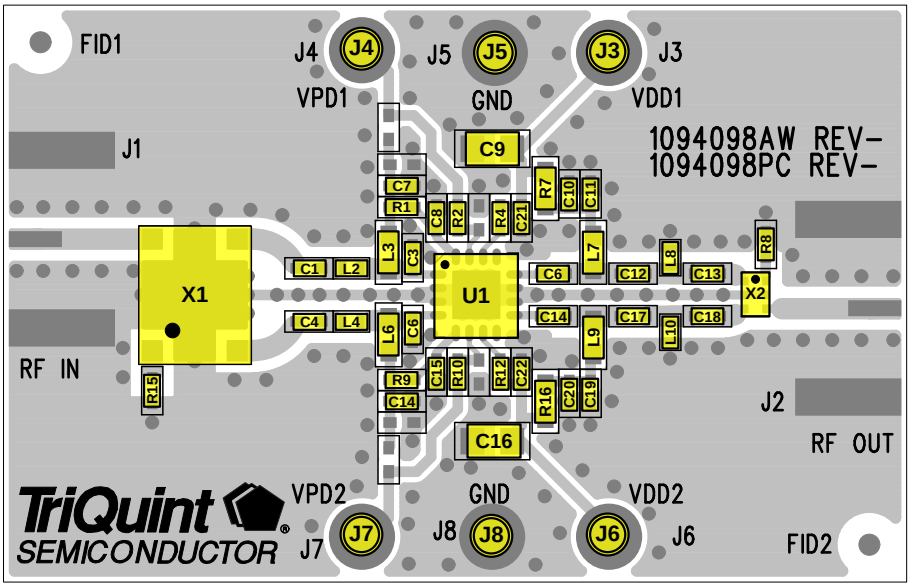
Notes:
1. Test conditions unless otherwise noted: V_{DD}=+4.35 V, I_{DD}=57 mA, Temp=+25°C, 50 Ohm system.

De-embedded S-parameters Data



Notes:
1. Noise parameter measurements taken at the package pin reference plane. The gate and drain are biased externally through bias-tees. The achievable NFmin will worsen with on board non-ideal bias circuit.

TQP3M9041-PCB Evaluation Board (2500-2700 MHz)



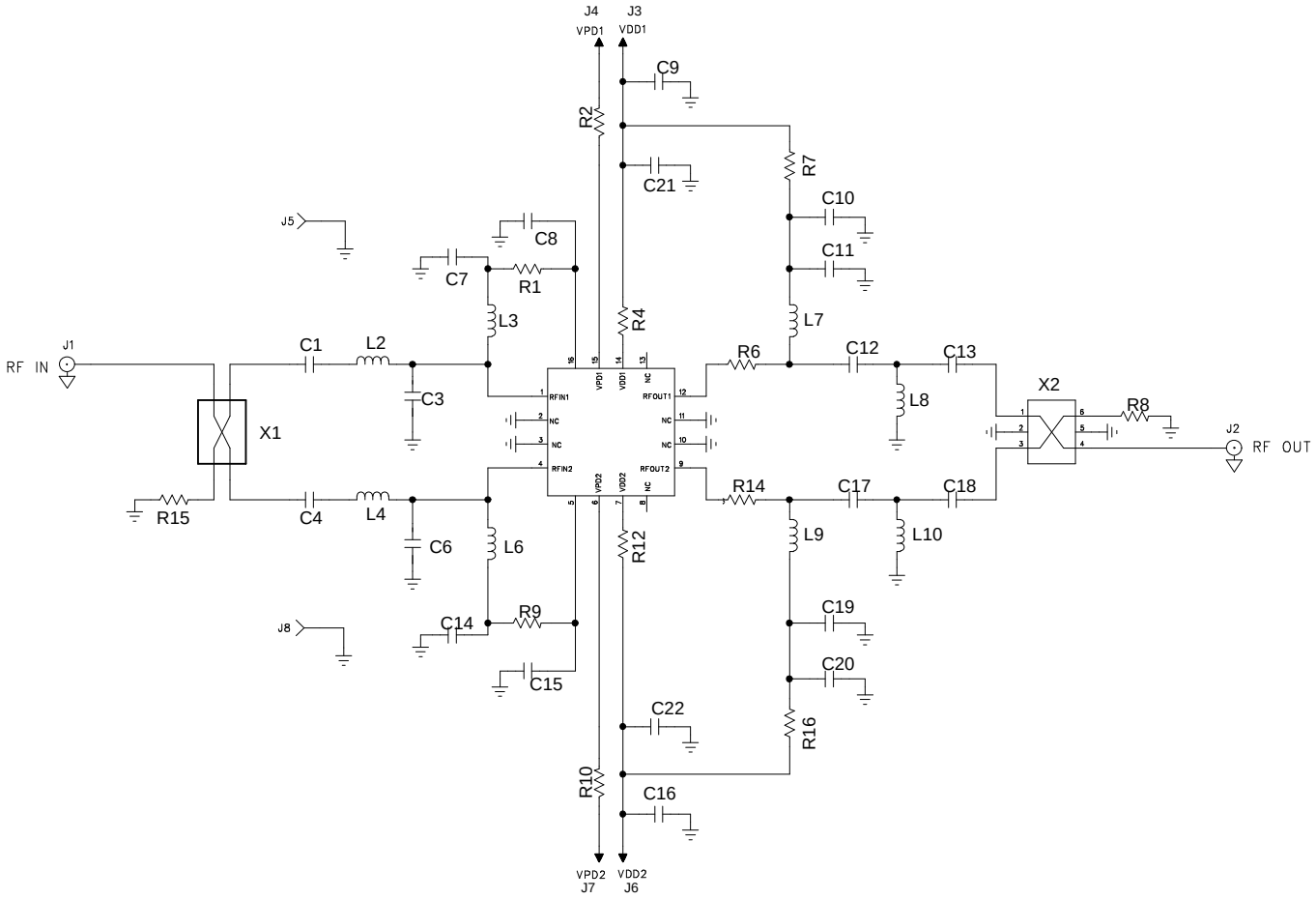
See Evaluation Board PCB Information section for PCB material and stack-up.

Bill of Material – TQP3M9041-PCB

Reference Des.	Value	Description	Manufacturer	Part Number
U1	n/a	Dual LNA	TriQuint	TQP3M9041
X1	n/a	Hybrid Coupler	Anaren	X3C26P1-03S
X2	n/a	Hybrid Coupler	Anaren	C2327J5003AHF
R1, R9	330 Ω	RES, 0402, +/-5%, 1/10W	Various	
R8, R15	51 Ω	RES, 0402, +/-5%, 1/10W	Various	
R4, R12	2.7K Ω	RES, 0402, +/-5%, 1/10W	Various	
R7, R16	6.8 Ω	RES, 0603, +/-5%, 1/8W	Various	
R2, R6, R10, R14, L2, L4	0 Ω	RES, 0402, +/-5%, 1/10W	Various	
C1, C4, C7, C14	22 pF	CAP, 0402, +/-5%, 50V	Panasonic	ECJ-0EC1H220J
C11, C19, C21, C22	100 pF	CAP, 0402, +/-5%, 50V	Panasonic	ECJ-0EC1H101J
C9, C16	0.01 uF	CAP, 0805, +/-5%, 50V, X7R	Various	
C10, C20	1000 pF	CAP, 0402, +/-10%, 50V	Various	
C12, C13, C17, C18	1 pF	CAP, 0402, +/-0.05pF, 25V	AVX	04023J1R0ABSTR
L3, L6, L7, L9	47 nH	IND, 0603, +/-5%, 600mA	Coilcraft	0603CS-47NXJL
L8, L10	2.2 nH	IND, 0402, +/-5%	Coilcraft	0402CS-2N2XJL
C3, C6, C8, C15	DNP			

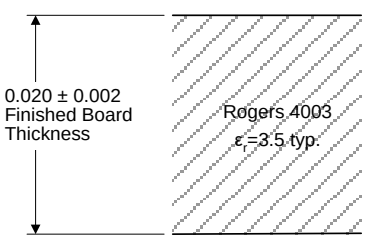
Notes:
1. R2, R6, R10 and R14 may be replaced with metal trace in target applications.
2. L2 and L4, or an equivalent transmission line length, are required for impedance matching

Application Circuit – TQP3M9041-PCB (2500-2700 MHz)

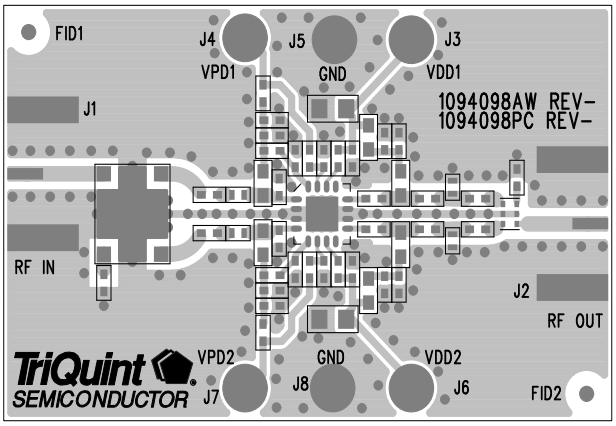


Evaluation Board PCB Information

TriQuint PCB 1094098 Material and Stack-up



50 ohm line dimensions: width = .040”, spacing = .020”

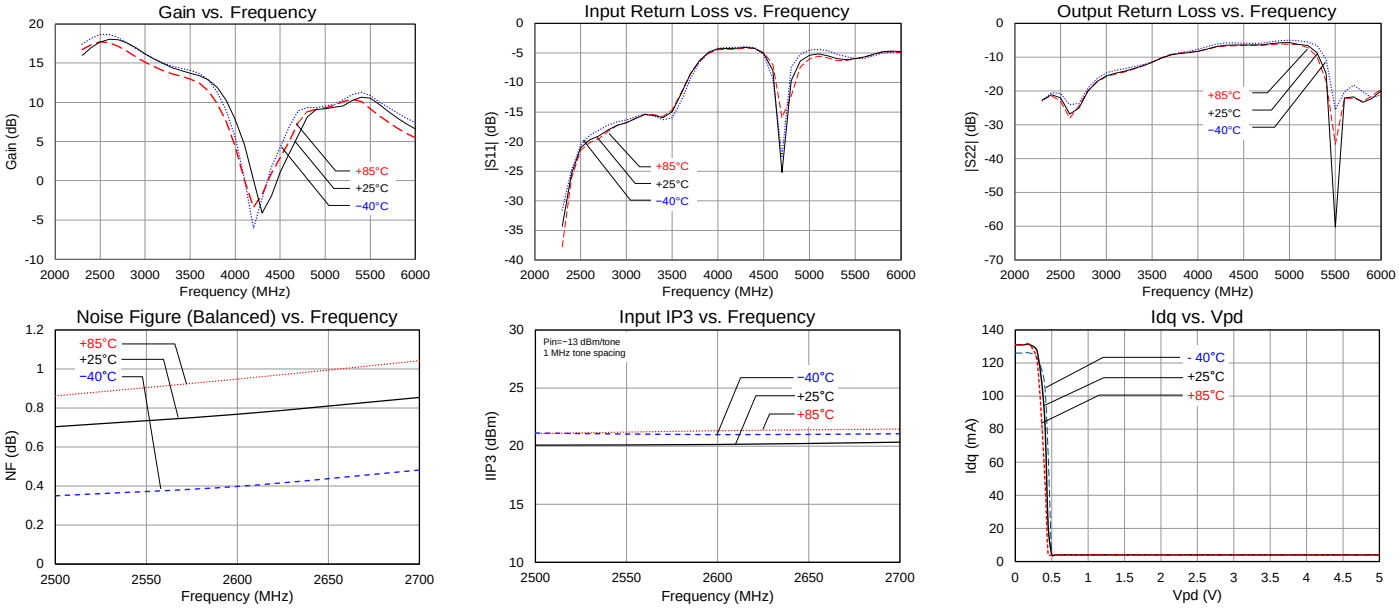


Typical Performance (Balanced Configuration)

Parameter	Typical Value (1)			Units
Frequency	2500	2600	2700	MHz
Gain	18.1	18.1	17.7	dB
Noise Figure	0.7	0.77	0.85	dB
Input Return Loss	22	19	18	dB
Output Return Loss	22	29	26	dB
Output P1dB	+22.6	+22.5	+22.5	dBm
IIP3 (Pin/tone=−13 dBm, Δf = 1 MHz)	+20.1	+20.2	+20.3	dBm

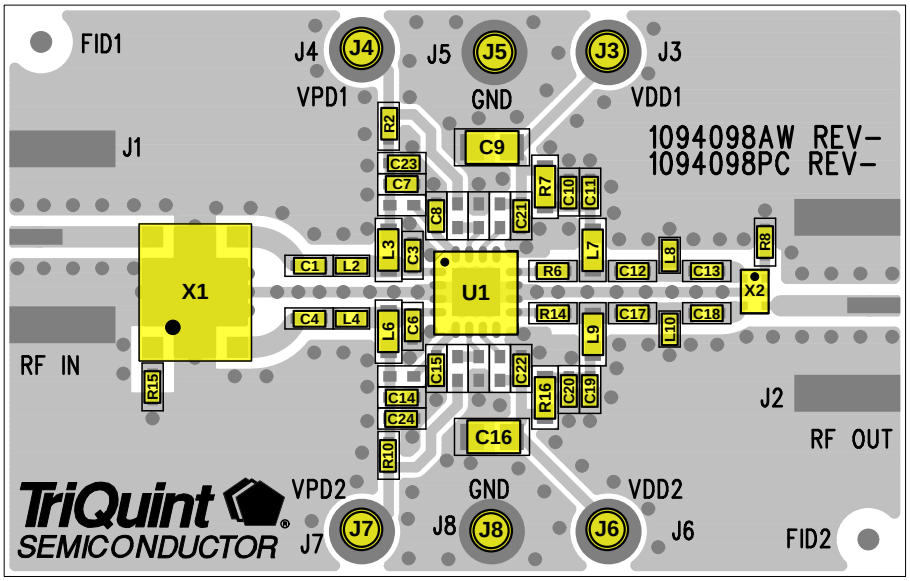
Notes:
1. Test conditions unless otherwise noted: V_{DD}=+4.35 V, I_{DD}=57 mA, Temp=+25°C, 50 Ohm system.
2. NF is de-embedded to the input of the input hybrid coupler.

Performance Plots (Balanced Configuration)



Notes:
1. Test conditions unless otherwise noted: V_{DD}=+4.35 V, I_{DD}=57 mA, Temp=+25°C, 50 Ohm system.
2. NF is de-embedded to the input of the input hybrid coupler.

TQP3M9041-PCB Evaluation Board (3400-3600 MHz)



See Evaluation Board PCB Information section for PCB material and stack-up.

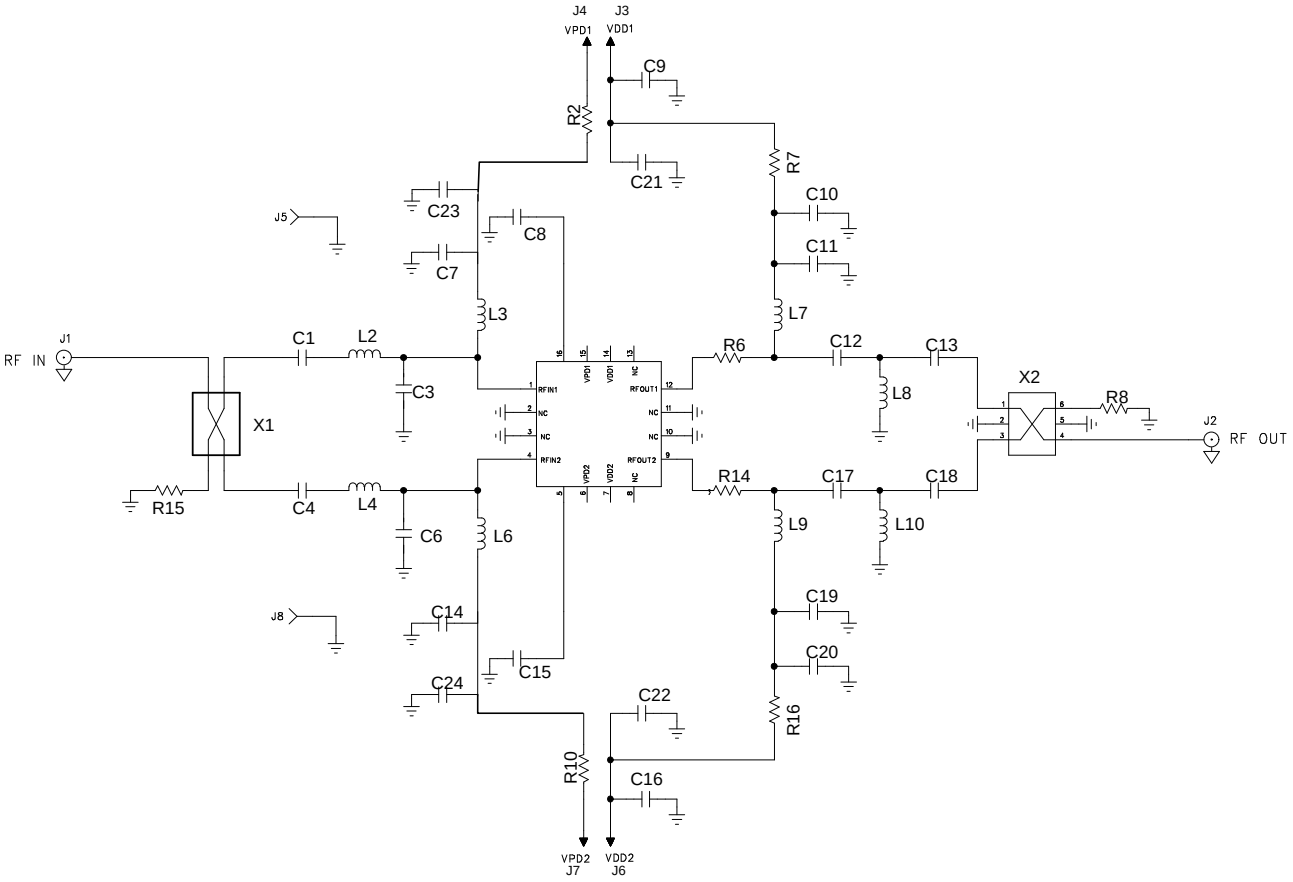
Bill of Material – TQP3M9041-PCB

Reference Des.	Value	Description	Manufacturer	Part Number
U1	n/a	Dual LNA	TriQuint	TQP3M9041
X1	n/a	Hybrid Coupler	Anaren	XC3500P-03S
X2	n/a	Hybrid Coupler	Anaren	C3337J5003AHF
R8, R15	51 Ω	RES, 0402, +/-5%, 1/10W	Various	
R7, R16	6.8 Ω	RES, 0603, +/-5%, 1/8W	Various	
R2, R6, R10, R14, L2, L4	0 Ω	RES, 0402, +/-5%, 1/10W	Various	
C1, C4	22 pF	CAP, 0402, +/-5%, 50V	Panasonic	ECJ-0EC1H220J
C7, C11, C14, C19, C21, C22	100 pF	CAP, 0402, +/-5%, 50V	Panasonic	ECJ-0EC1H101J
C9, C16, C23, C24	0.01 uF	CAP, 0805, +/-5%, 50V, X7R	Various	
C10, C20	1000 pF	CAP, 0402, +/-10%, 50V	Various	
C12, C13, C17, C18	0.7 pF	CAP, 0402, +/-0.05pF, 25V	AVX	04023J0R7BBS
C3, C6	0.1 pF	CAP, 0402, +/-0.05pF, 25V	AVX	04023J0R1BBS
L3, L6, L7, L9	27 nH	IND, 0603, +/-5%, 600mA	Coilcraft	0603CS-27NXJL
L8, L10	1 nH	IND, 0402, +/-5%	Coilcraft	0402HP-1N0XJLU
C8, C15	DNP			

Notes:

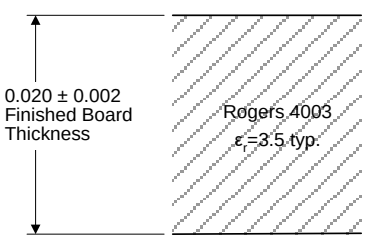
1. R2, R6, R10, and R14 may be replaced with metal trace in target applications.
2. L2 and L4, or an equivalent transmission line length, are required for impedance matching.

Application Circuit – TQP3M9041-PCB (3400-3600 MHz)

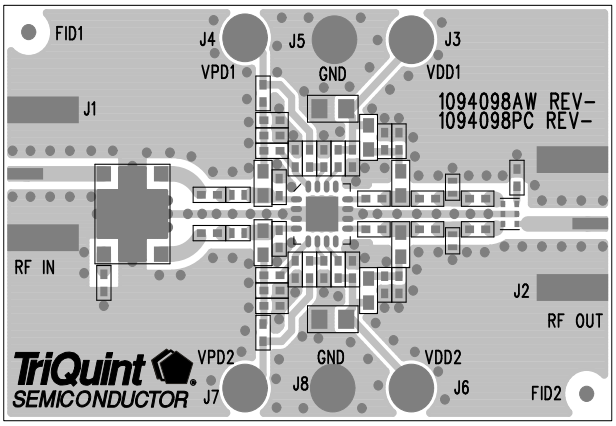


Evaluation Board PCB Information

TriQuint PCB 1094098 Material and Stack-up



50 ohm line dimensions: width = .040”, spacing = .020”

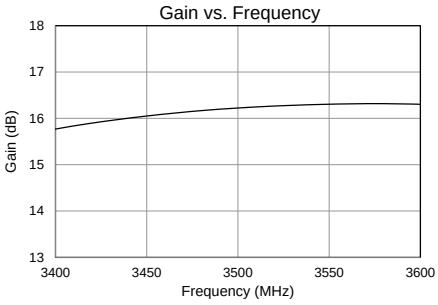


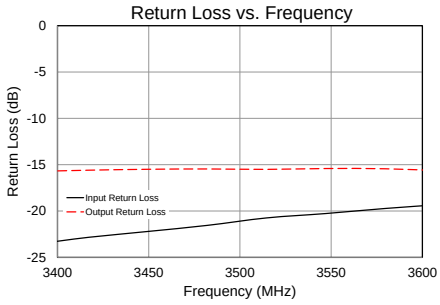
Typical Performance (Balanced Configuration)

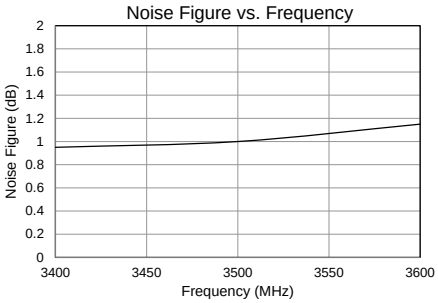
Parameter	Typical Value (1)			Units
Frequency	3400	3500	3600	MHz
Gain	15.8	16.2	16.3	dB
Noise Figure	0.95	1.0	1.15	dB
Input Return Loss	23.0	21.0	19.2	dB
Output Return Loss	15.6	15.5	15.6	dB
Output P1dB	+21.9	+21.8	+21.8	dBm
IIP3 (Pin/tone=−15 dBm, Δf = 1 MHz)	+22.3	+21.7	+21.7	dBm

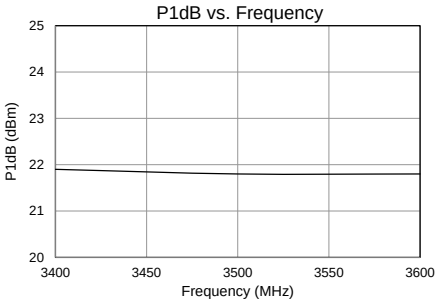
Notes:
1. Test conditions unless otherwise noted: V_{DD}=+4.35 V, V_{GG} = Vpd = 0.43V, I_{DD}=55 mA, Temp=+25°C, 50 Ohm system.
2. NF is de-embedded to the input of the input hybrid coupler.

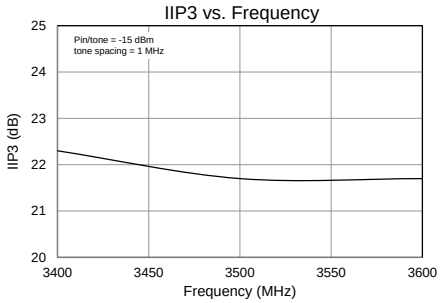
Performance Plots (Balanced Configuration)





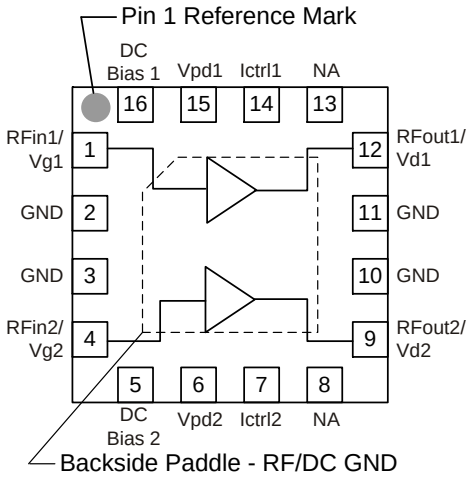






Notes:
1. Test conditions unless otherwise noted: V_{DD}=+4.35 V, V_{GG} = Vpd = 0.43V, I_{DD}=55 mA, Temp=+25°C, 50 Ohm system.

Pad Configuration and Description

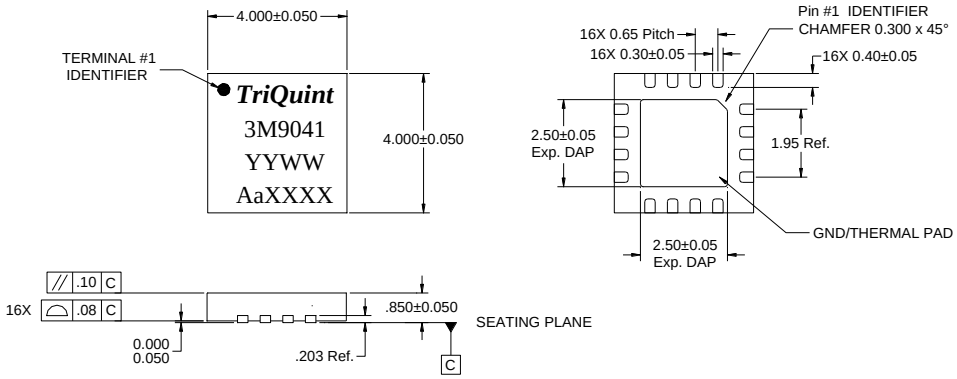


Top View

Pad No.	Label	Description
1	RFin1/Vg1	RF input pin for channel 1. Gate voltage bias pin for channel 1.
2, 3, 10, 11	GND	No internal connection but should be grounded to provide PCB mounting integrity and isolation between the two RF paths.
4	RFin2/Vg2	RF input pin for channel 2. Gate voltage bias pin for channel 2.
5	DC Bias 2	DC out bias for channel 2
6	Vpd2	Power down control voltage for channel 1
7	Ictrl2	Channel 2 drain current control
8, 13	NA	No internal connection. These pins can be grounded to provide PCB mounting integrity.
9	RFout2/Vd2	RF output pin for channel 2. Gate voltage bias pin for channel 2.
12	RFout1/Vd1	RF output pin for channel 1. Drain voltage bias pin for channel 1.
14	Ictrl1	Channel 1 drain current control
15	Vpd1	Power down control voltage for channel 1
16	DC Bias 1	DC out bias for channel 1
Backside Paddle	RF/DC GND	RF/DC Ground. Follow recommended via pattern and ensure good solder attach for best thermal and electrical performance.

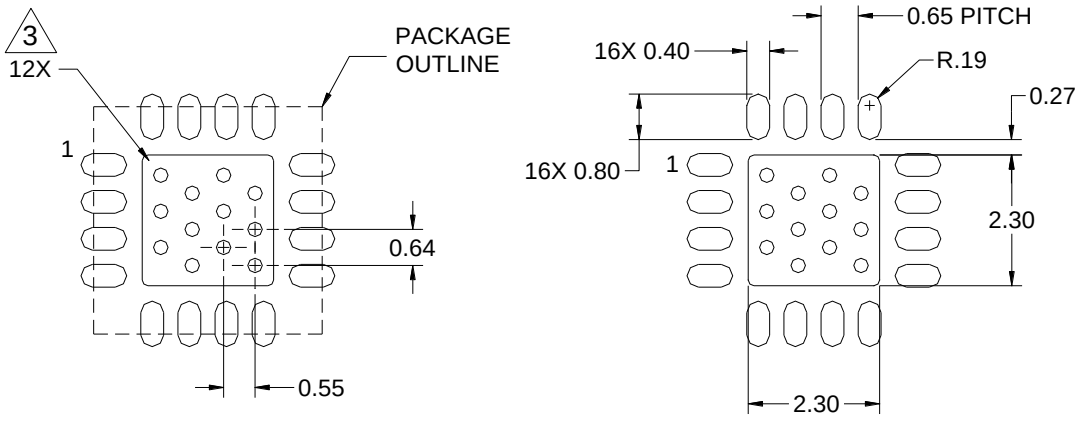
Package Marking and Dimensions

Marking: Part number – 3M9041
Year, week - YYWW
Assembly code - AaXXXX



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012

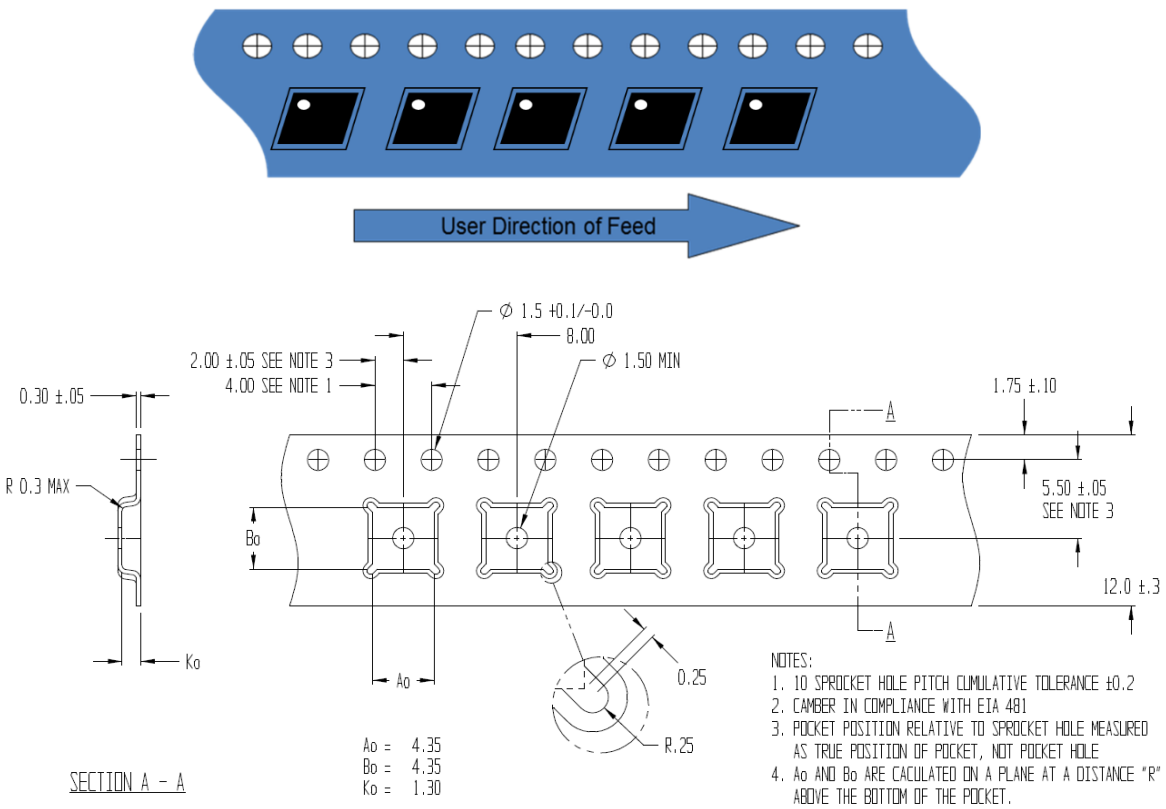
Recommended PCB Layout Pattern



COMPONENT SIDE

Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

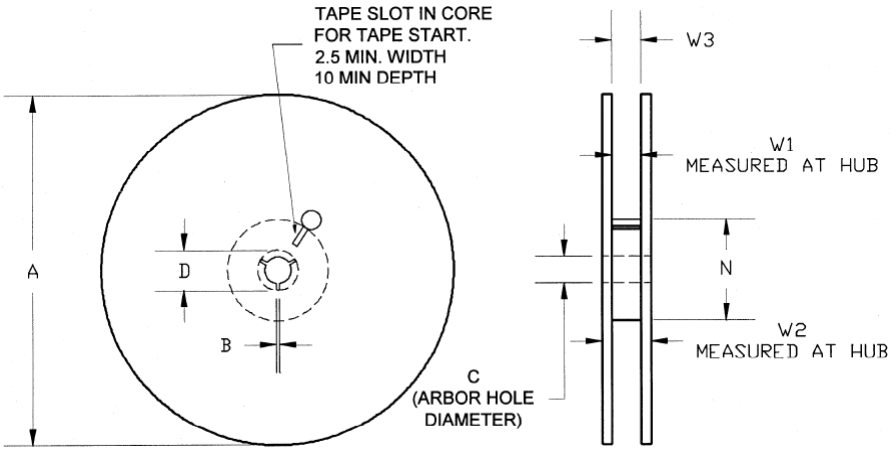
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.171	4.35
	Width	B0	0.171	4.35
	Depth	K0	0.051	1.30
	Pitch	P1	0.315	8.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.0

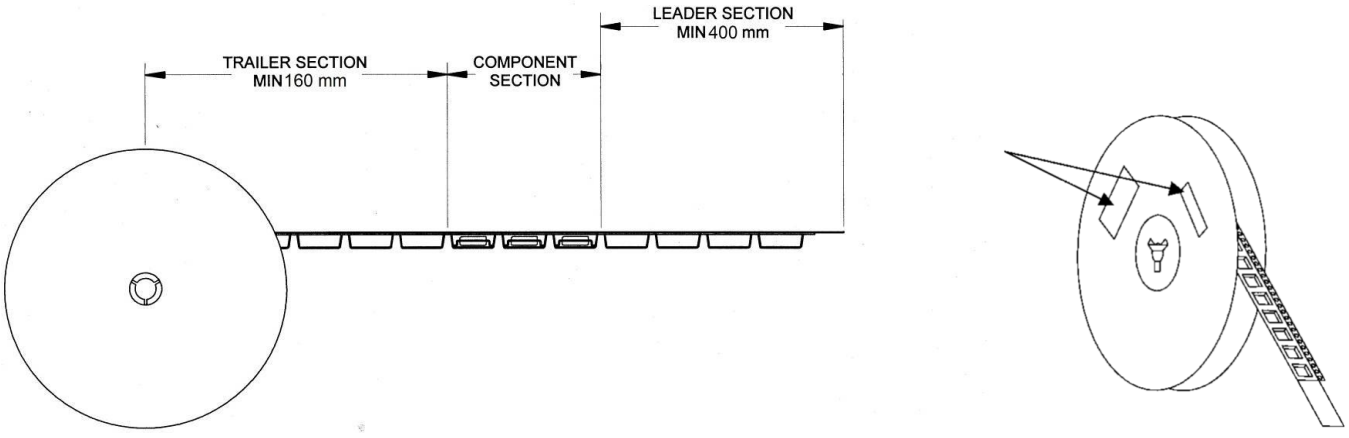
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 13” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.795	20.2

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.