TQP4M9072

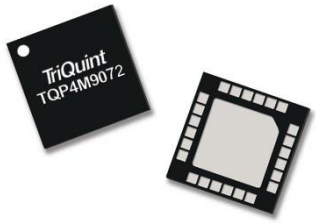
High Linearity 6-Bit, 31.5 dB Digital Step Attenuator

Product Overview

The TQP4M9072 is a high linearity, low insertion loss, 6 bit, 31.5 dB Digital Step Attenuator (DSA) operating over the DC – GHz frequency range. The digital step attenuator uses a single +5 V DC supply and has a serial periphery interface (SPI™) for changing attenuation states. This product maintains high attenuation accuracy over frequency and temperature. No external matching components are needed for the DSA. The product has an added feature of not requiring external AC grounding capacitors for operation above 700 MHz.

The TQP4M9072 is in a standard lead-free green /RoHS compliant 24-pin 4 x 4 mm QFN package.

There is also a device available from Qorvo. Which is TQP4M9071, a footprint and pin compatible DSA with a parallel control interface.

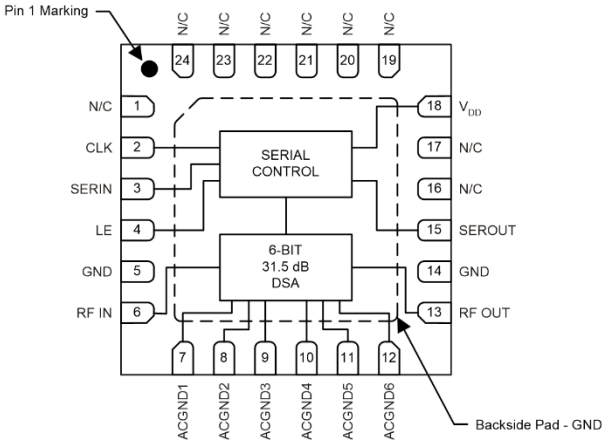


16 Pad 3 x 3 mm QFN Package

Key Features

- DC – 4000 MHz
- 50 Ω Impedance
- 0.5 dB LSB Steps to 31.5 dB
- +57 dBm Output IP3
- 1.7 dB Insertion Loss at 2200 MHz
- No external bypass capacitors required for operation above 700 MHz
- Serial Control Interface
- 3.3V TTL logic compatible
- +5 V Single Supply

Functional Block Diagram



Top View

Applications

- Mobile Infrastructure
- LTE / WCDMA / CDMA / EDGE
- Test Equipment and Sensors
- IF and RF Applications
- General Purpose Wireless

Ordering Information

Part No.	Description
TQP4M9072	2,500 pieces on a 13” reel (standard)
TQP4M9072-PCB_IF	40 –500 MHz Evaluation Board
TQP4M9072-PCB_RF	0.7 –4.0 GHz Evaluation Board

EVB kit includes an USB control interface board, EVH

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−55 to +150 °C
Junction Temperature	+150 °C
RF Input Power, 50 Ω, T = 85 °C	+28 dBm
Device Voltage (V_{DD})	+6.0 V
Digital Input Voltage	V_{DD} + 0.5 V

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V_{DD})	+3.3	+5	+5.25	V
T_{CASE}	−40		+105	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD}=+5 V, Temp= +25 °C, 50 Ω system, Mode 1

Parameter	Conditions (1)	Min	Typ	Max	Units
Operational Frequency Range		DC		4000	MHz
Insertion Loss	1.0 GHz		1.3		dB
	2.0 GHz		1.6		dB
	2.2 GHz		1.7	2.2	dB
	3.5 GHz		2.1		dB
Return Loss	All states		17		dB
Attenuation Accuracy	0.04 – 2.7 GHz, All States, Mode 2	± (0.3 + 3% of Atten. Setting) Max			dB
	0.7 – 2.7 GHz, All States, Mode 1 or 2	± (0.3 + 3% of Atten. Setting) Max			dB
	2.7 – 3.5 GHz, All States, Mode 1 or 2	± (0.4 + 4% of Atten. Setting) Max			dB
Step Attenuation	Monotonic over all states 0 to 63	0	0.5		dB
Input IP3	Input Power +15 dBm / tone, All States		+57		dBm
Input P0.1dB	DC – 4.0 GHz, All States		+30		dBm
Rise / Fall Time	10% to or from 90% RF		90		ns
Attenuation Settling Time	50% LE rise edge to 10% or 90% RF		100		ns
DC Supply Voltage, V_{DD}			+5		V
DC supply Current, I_{DD}			2.0		mA

Notes:
1. Mode 1 – No external bypass capacitors used on pin 7-12 and operating frequency in 0.7 – 4.0 GHz.
2. Mode 2 – External bypass capacitors used on pin 7-12, and operating frequency extended to 0.04 – 4.0 GHz

Serial Control Interface

The TQP4M9072 has a CMOS SPI™ compatible controller. This controller converts the serial data input stream to a parallel output word. The 3-wire (CLK, LE and SID) input is SPI™ compatible. At power up, the controller resets the DSA to the minimum gain state. The 6-bit SID (Serial Input Data) word is loaded into the register on rising edge of the CLK, MSB first. When LE is high, CLK is internally disabled.

Serial Control Timing Characteristics (Test conditions: V_{DD} = +5 V, Temp.=25°C)

Parameter	Condition	Min	Max	Units
Clock Frequency	50% Duty Cycle		10	MHz
LE Setup Time, t_{LESUP}	after last CLK rising edge	10		ns
LE Pulse Width, t_{LEPW}		30		ns
SERIN set-up time, t_{SDSUP}	before CLK rising edge	10		ns
SERIN hold-time, t_{SDHLD}	after CLK rising edge	10		ns
LE Pulse Spacing, t_{LE}	LE to LE pulse spacing	630		ns

Serial Control DC Logic Characteristics, V_{DD} +5 V (Test conditions: Temp.=25°C)

Parameter	Condition	Min	Max	Units
Input Low State Voltage, V_{IL}		0	0.8	V
Input High State Voltage, V_{IH}		2.4	V_{DD}	V
Output High State Voltage, V_{OH}	On SOD pin	2.0	V_{DD}	V
Output Low State Voltage, V_{OL}	On SOD pin	0	0.8	V
Input Current, I_{IH} / I_{IL}	On SID, LE and CLK pins	−10	+10	µA

Serial Control DC Logic Characteristics, VDD +3.3 V (Test conditions: Temp.=25°C)

Parameter	Condition	Min	Max	Units
Input Low State Voltage, V_{IL}		0	0.8	V
Input High State Voltage, V_{IH}		2.8	V_{DD}	V
Input Current, I_{IH} / I_{IL}	On SID, LE and CLK pins	−10	+10	µA

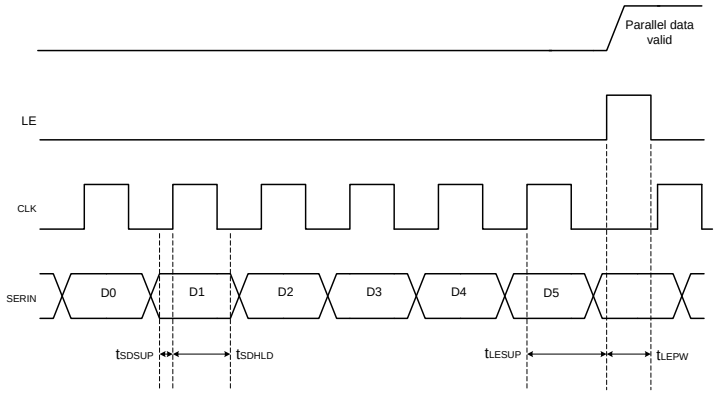
SERIN Control Logic Truth Table

6-Bit Control Word						Attenuation State
MSB					LSB	
D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	Reference : IL
1	1	1	1	1	0	0.5 dB
1	1	1	1	0	1	1 dB
1	1	1	0	1	1	2 dB
1	1	0	1	1	1	4 dB
1	0	1	1	1	1	8 dB
0	1	1	1	1	1	16 dB
0	0	0	0	0	0	31.5 dB

Any combination of the possible 64 states will provide an attenuation of approximately the sum of bits selected

Timing Diagram

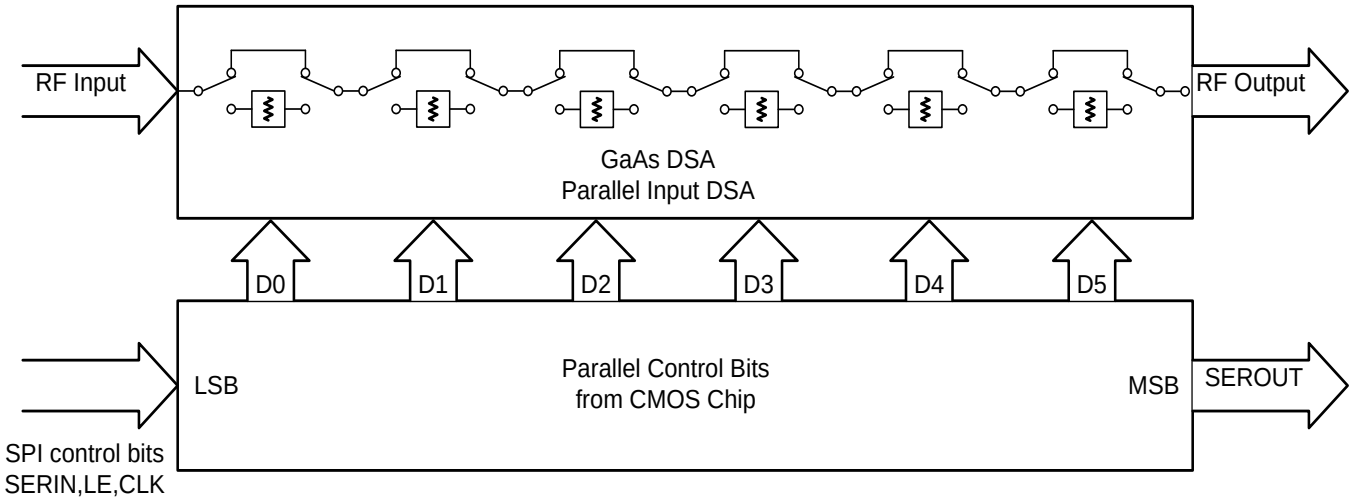
CLK is internally disabled when LE is high



Detailed Device Description

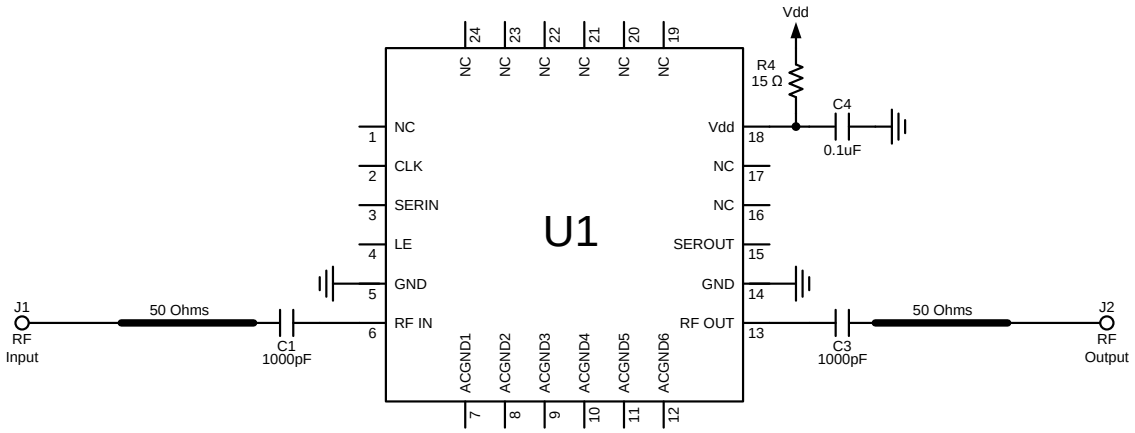
The TQP4M9072 is a high linearity, low insertion loss, wideband, 6-bit, 31.5 dB digital step attenuator. The digital step attenuator uses a single 5 V supply and has a CMOS SPI™ controller. This product maintains high attenuation accuracy over frequency and temperature. The product does not require any external bypass capacitors on AC ground pins for operation above 700 MHz. The DSA performance remains unchanged for frequency range 0.7 – 4 GHz in either Mode 1 or Mode 2. The low end of operating frequency can be extended to the range of 40 MHz – 700 MHz with external bypass capacitors on AC ground pins (ACGND1-ACGND6).

Functional Block Diagram



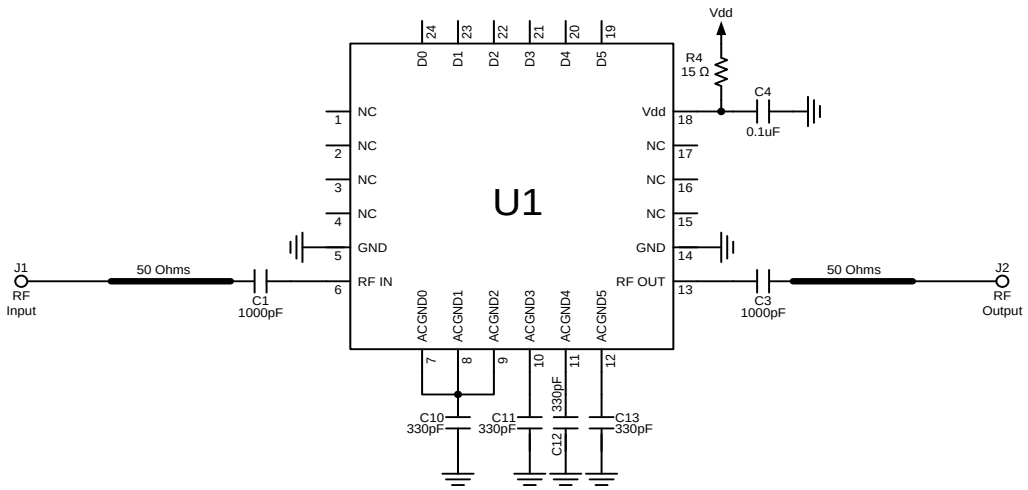
Mode 1: 0.7 – 4.0 GHz Operation (EVB TQP4M9072-PCB_RF)

No external bypass capacitors required on ACGND1 to ACGND6

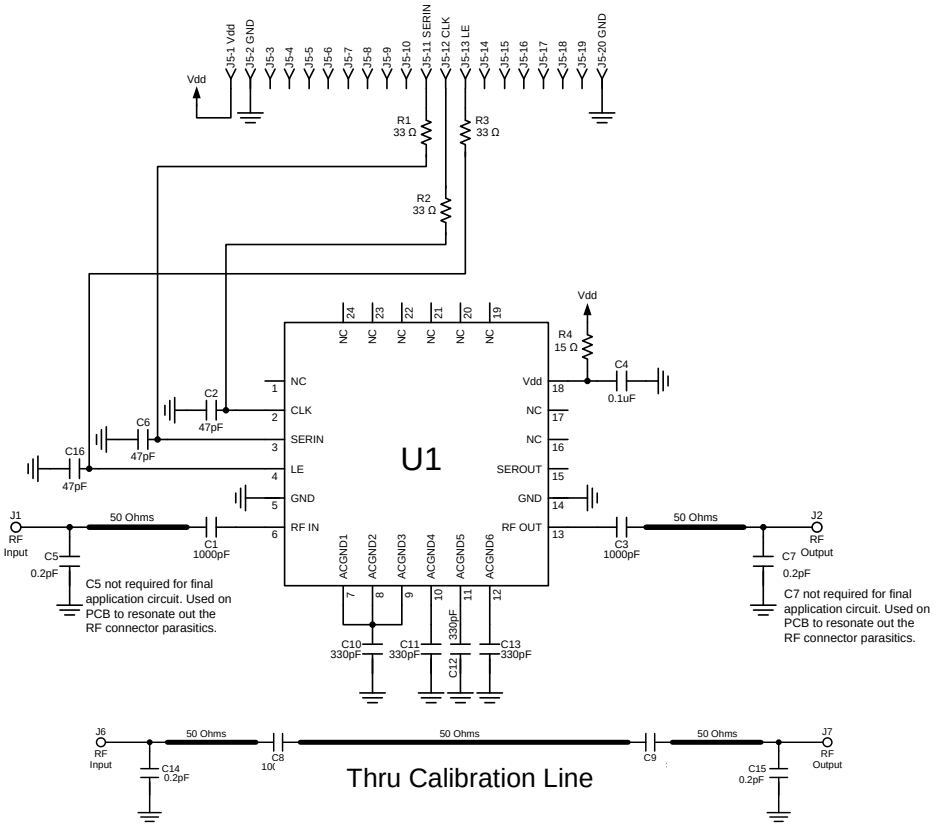


Mode 2: 0.04 – 4.0 GHz Operation (EVB TQP4M9072-PCB_IF)

External bypass capacitors required on ACGND0 – ACGND5 pins. For improved operation below 0.1 GHz, blocking and bypass capacitors values can be increased to 10 nF. This circuit configuration can also be used for operation up to 4 GHz. The DSA performance remains unchanged for frequency range 0.7 – 4 GHz in either Mode 1 or Mode 2.



Evaluation Board Schematic – TQP4M9072-PCB_RF/IF



Bill of Material: TQP4M9071-PCB_RF

Reference Designation	Value	Description	Manufacturer	Part Number
U1	-	High Linearity 6-Bit, 31.5dB, DSA	Qorvo	TQP4M9072
C2, C6, C16	47 pF	Cap, Chip, 0402, 50V, NPO, 5%	various	
C1,C3	1000 pF	Cap, Chip, 0402, 50V, X7R, 10%	various	
C4	0.1 µF	Cap, Chip, 0402, 50V, X7R, 10%	various	
R1, R2, R3	33 Ω	Res, Chip, 0402, 1/16W, 1%	various	
R4	15 Ω	Res, Chip, 0402, 1/16W, 5%	various	
C10, C11, C12, C13	DNP	Do Not Place	various	

Bill of Material: TQP4M9071-PCB_IF

Reference Designation	Value	Description	Manufacturer	Part Number
U1	-	High Linearity 6-Bit, 31.5dB, DSA	Qorvo	TQP4M9072
C2, C6, C16	47 pF	Cap, Chip, 0402, 50V, NPO, 5%	various	
C1,C3	1000 pF	Cap, Chip, 0402, 50V, X7R, 10%	various	
C4	0.1 µF	Cap, Chip, 0402, 50V, X7R, 10%	various	
R1, R2, R3	33 Ω	Res, Chip, 0402, 1/16W, 1%	various	
R4	15 Ω	Res, Chip, 0402, 1/16W, 5%	various	
C10, C11, C12, C13	330 pF	Cap, Chip, 0402, 50V, X7R, 10%	various	

Evaluation Board Layout Information

PC Board Layout

The PCB made with .020" Rogers 4003, ϵ_r = 3.45, 4 layers with total thickness of 0.062" for mechanical rigidity. Metal layers are 1-oz copper. Microstrip line width is .040" with spacing of .020".

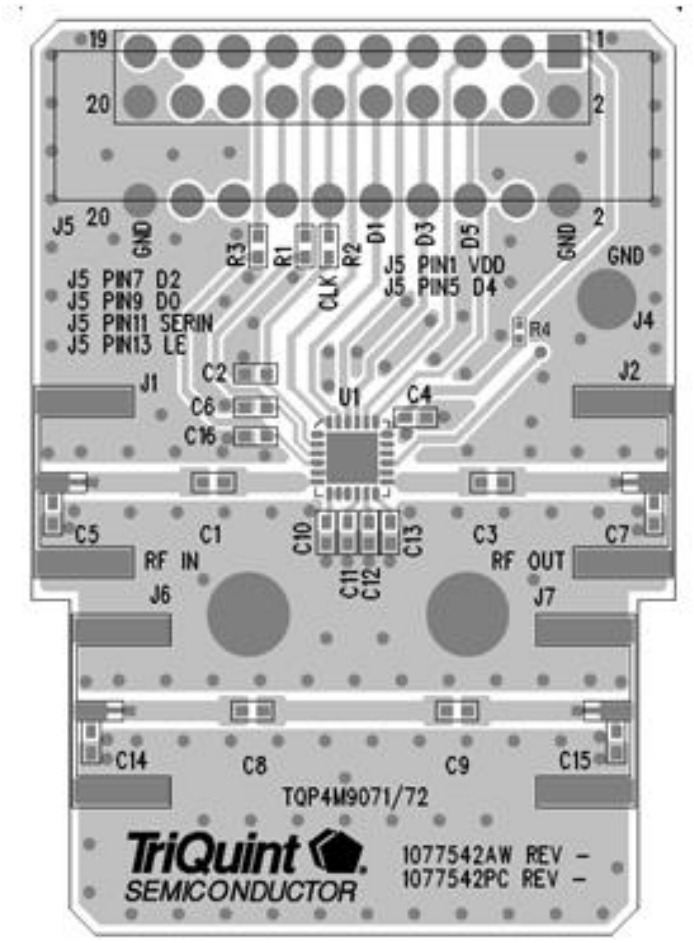
External DC blocking capacitors are required on RF IN and RF OUT pins of the device. The supply voltage for the DSA is supplied externally through pin V_{DD}. Frequency bypassing for this pin is the surface mount capacitor 0.1 µF (C4). This capacitor is placed close to the device pin on the board. To ensure application circuit is well working with standard power supplies, 15 Ω (R4) dropping resistor is highly recommended on V_{DD} supply line.

R1, R2 and R3 are used as damper or termination for digital noise or any reflection on Serial Input Data, CLK and LE pins.

RF layout is critical for getting the best performance. RF trace impedance needs to be 50 Ω. In order to deduct the input and output trace losses on the EVB, an equivalent length of through line is also included on the EVB. A through calibration with the microstrip line from J6 to J7 can remove the PCB trace and DC blocking capacitor losses to get the data right on the device. All data shown on the datasheet are referenced up on the device input and output pins.

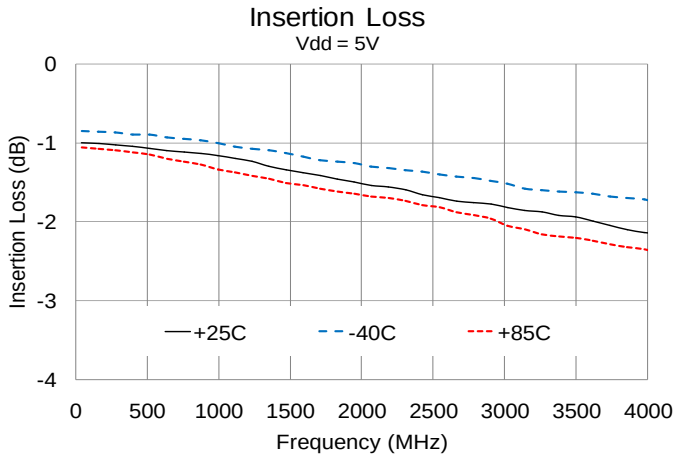
The PC board is designed to directly mating with Qorvo USB to SPI convertor called Evaluation Board Host (EVH). Each TQP4M9072 evaluation kit is supplied with the EVH module, and USB cable. The EVH graphical user interface (EVH GUI) sets the device attenuation state. The Manual and the GUI software of the EVH are also available. Refer to Qorvo website for more information

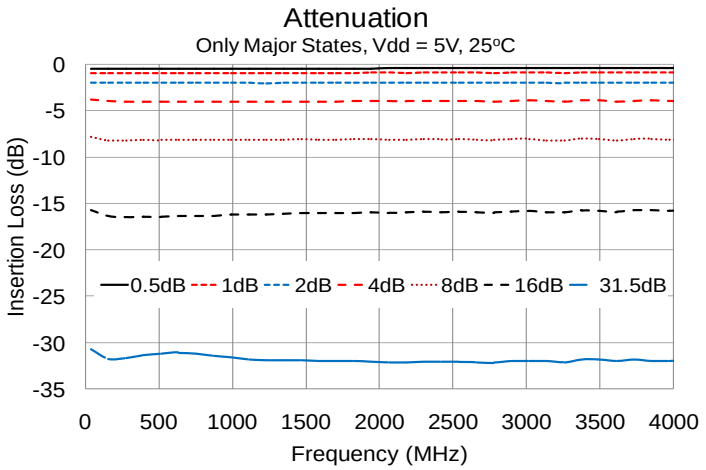
The device PCB land pattern shown has been developed and tested for optimum assembly results at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes may vary, careful development is recommended.

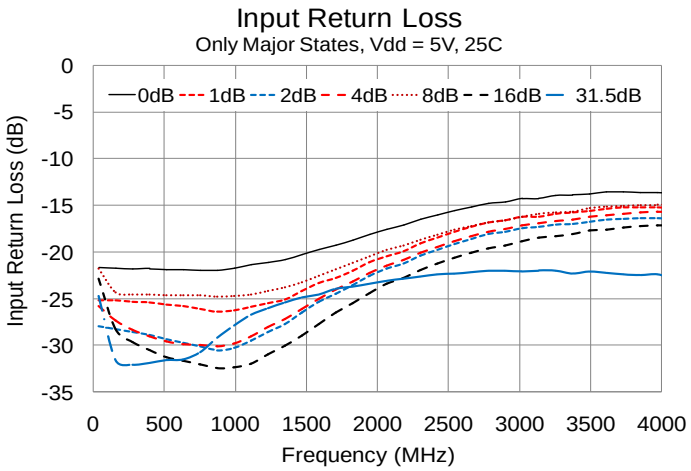


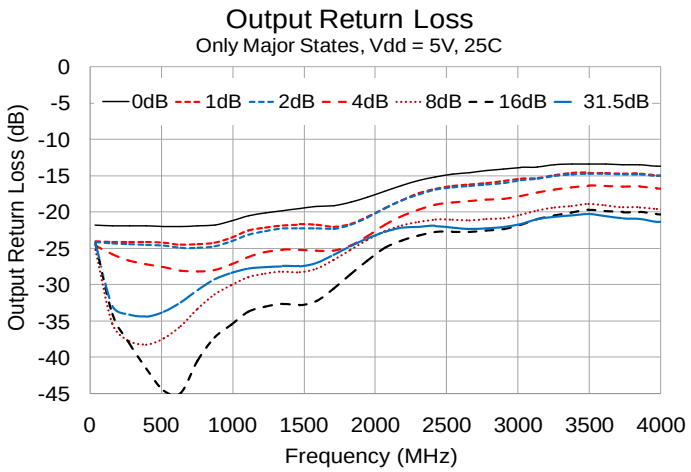
Typical Performance Plots

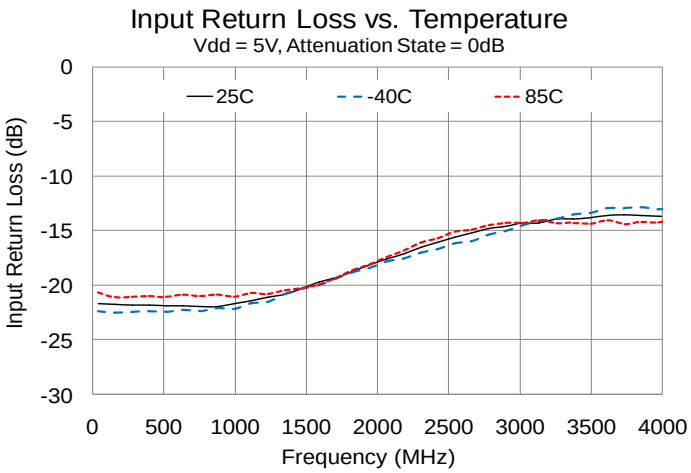
Performance plots data is measured using Bias Tee on RF ports in Mode 2 configuration. Mode 2 operation is required to obtain performance at frequencies lower than 0.7 GHz. For frequency range 0.7 – 4.0 GHz, data is identical in Mode 1 and Mode 2.

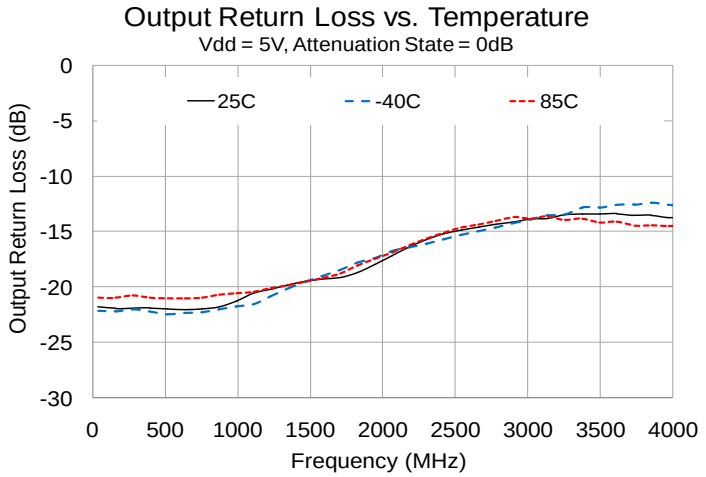




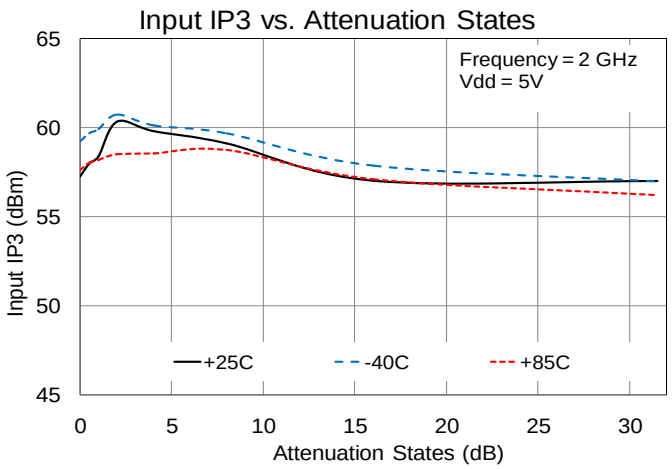


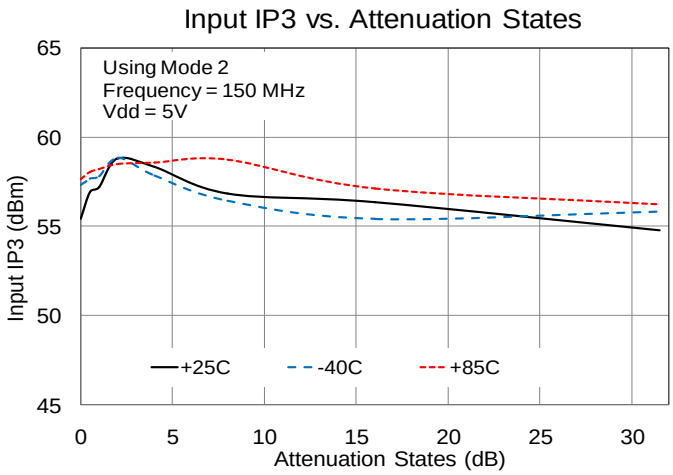


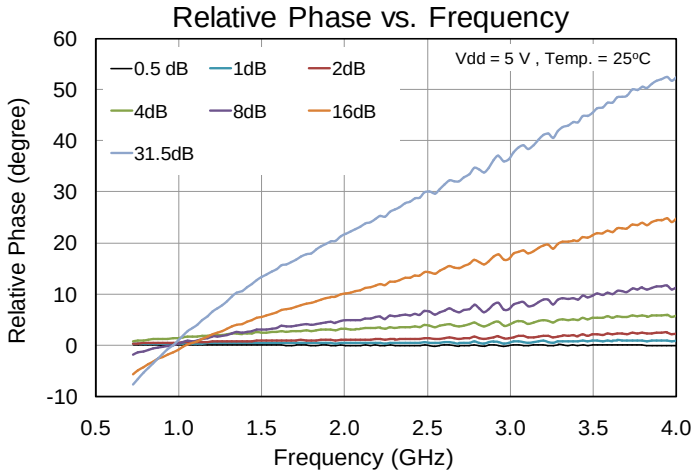


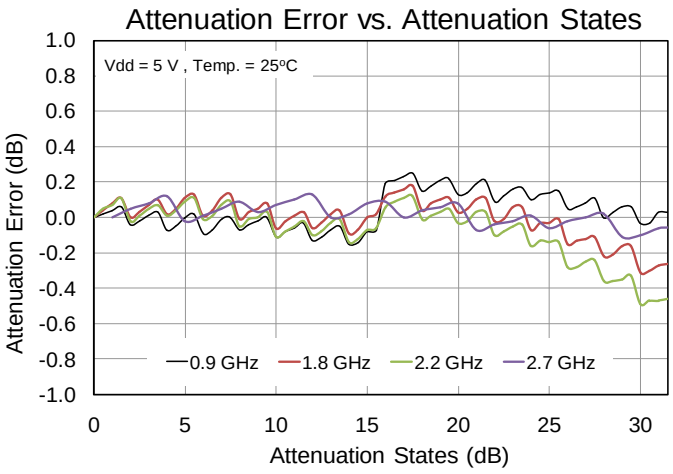


Typical Performance Plots (Continue)

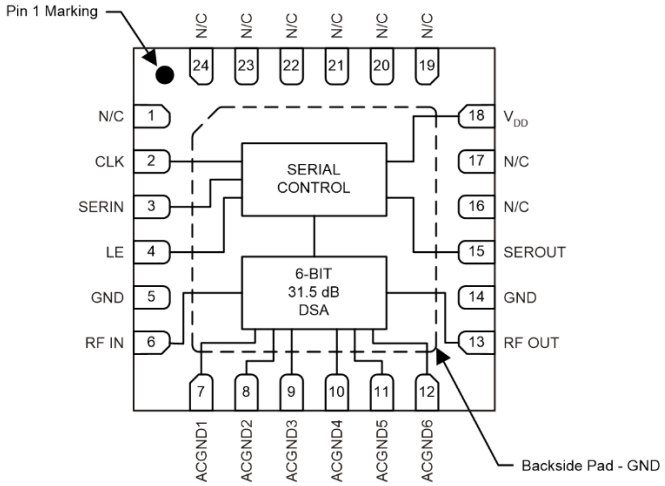








Pad Configuration and Description

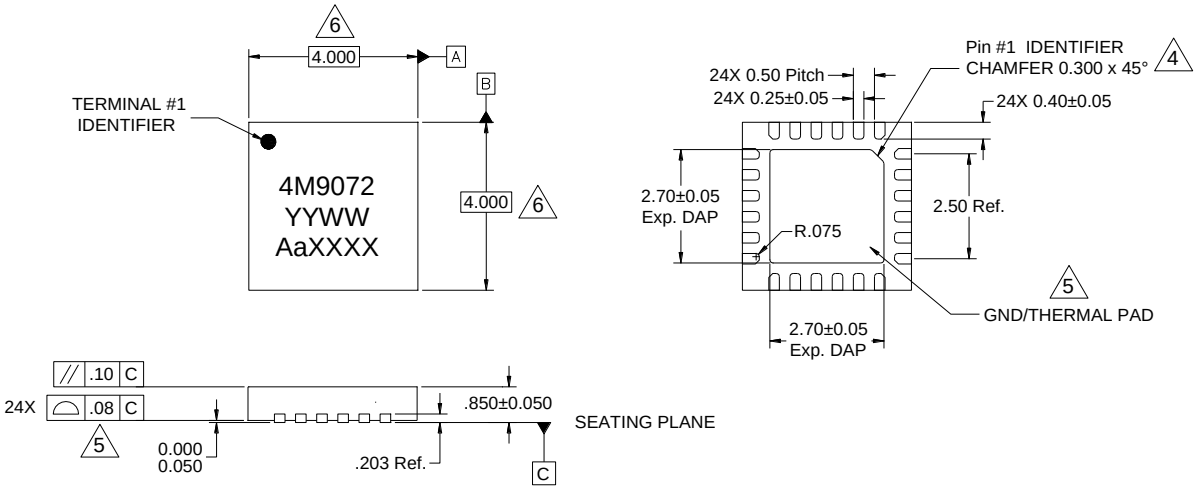


Top View

Pad No.	Label	Description
1, 16, 17, 19-24	NC	No electrical connection. Land pads should be provided for PCB mounting integrity.
2	CLK	Clock input. This serial clock is used to clock in the serial data to the registers. The data is latched on the CLK rising edge. This is a high impedance CMOS input.
3	SERIN	SID, Serial Data Input. The 6-bit serial data is loaded MSB first. This is a high impedance CMOS input.
4	LE	Latch Enable input, When LE goes high, 6-bit data in the serial input register is transferred to the attenuator. When LE is high, CLK is disabled
5, 14	GND	Ground connection, must be connected to RF/DC ground
6	RF IN	RF Input, DC voltage present, blocking capacitor required. Can be used for Input or Output.
7	ACGND1	AC ground connection for extended low frequency operation
8	ACGND2	
9	ACGND3	
10	ACGND4	
11	ACGND5	
12	ACGND6	
13	RF OUT	RF Output, DC voltage present, blocking capacitor required. Can be used for Input or Output.
15	SEROUT	SOD, Serial Data output. No application recommended.
18	V_{DD}	DC Supply Voltage input. Bypass capacitor required close to the pin. Dropping resistor highly recommended ensuring compatibility with different power supplies.
Backside Paddle	GND	RF/DC ground. Use recommended via hole pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

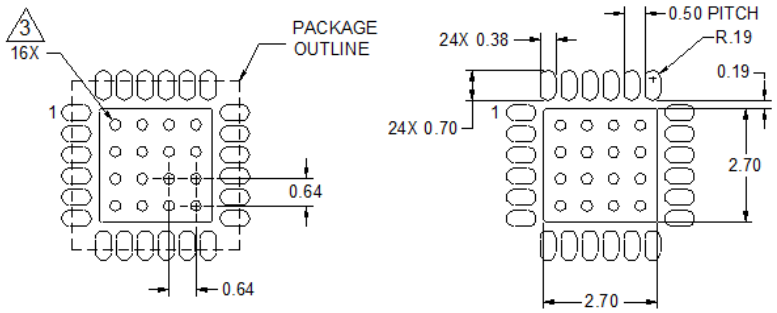
Package Marking and Dimensions

Marking: Part Number – 4M9072
Date Code – YYWW
Assembly Code – AaXXXX



Notes:
1. All dimensions are in millimeters. Angles are in degrees. Dimension and tolerance format conform to ASME Y14.4M-1994.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Co-planarity applies to the exposed ground/thermal pad as well as the contact pins
4. Package body length/width does not include plastic flash protrusion across mold parting line.

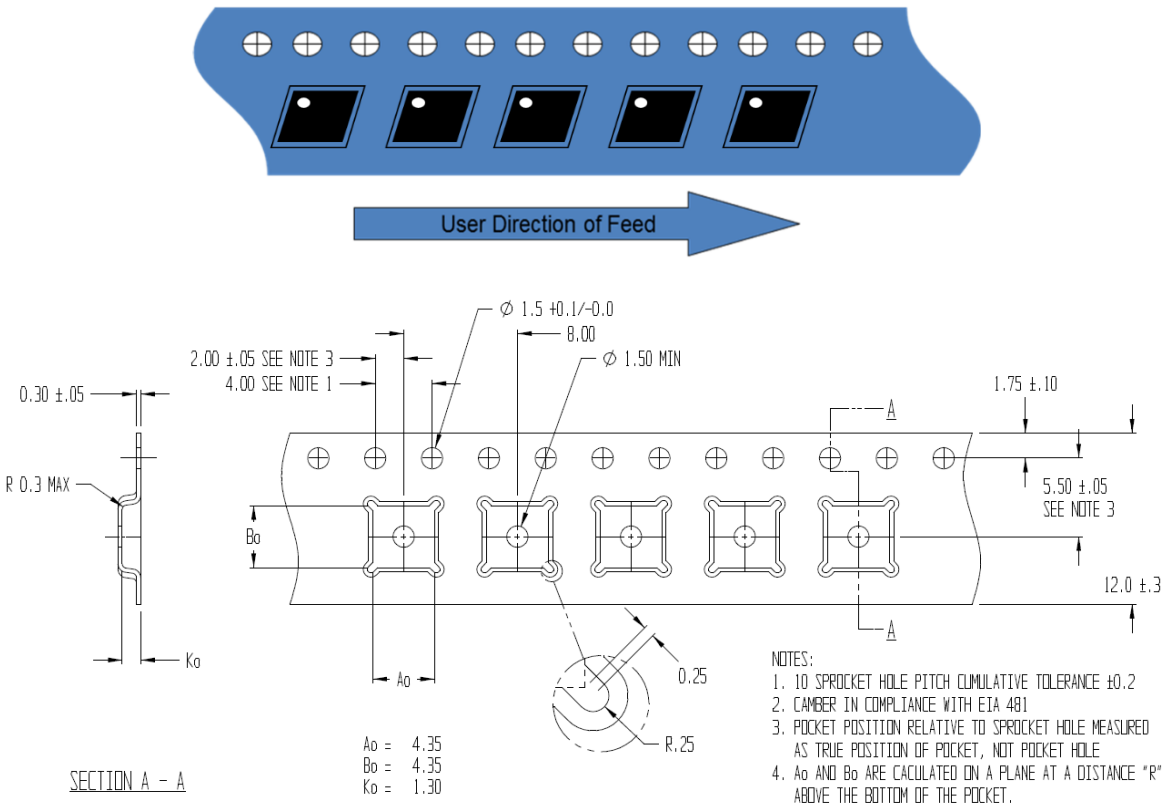
PCB Mounting Pattern



COMPONENT SIDE

Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.010").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

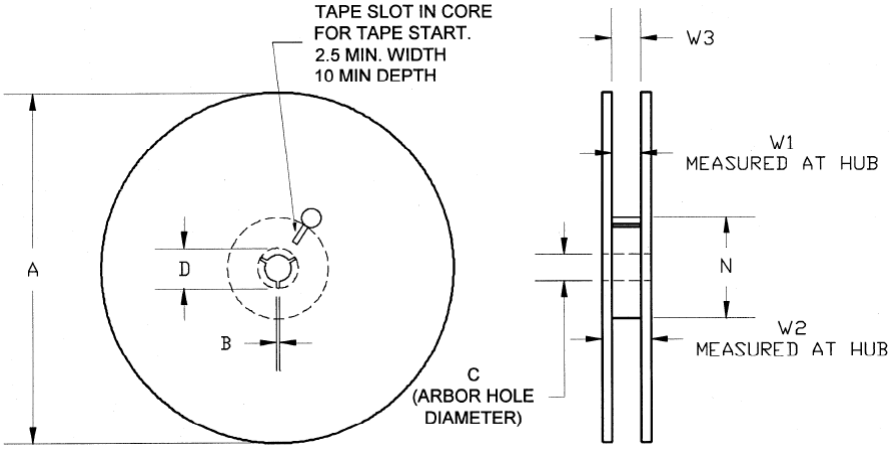
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.171	4.35
	Width	B0	0.171	4.35
	Depth	K0	0.051	1.30
	Pitch	P1	0.315	8.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.0

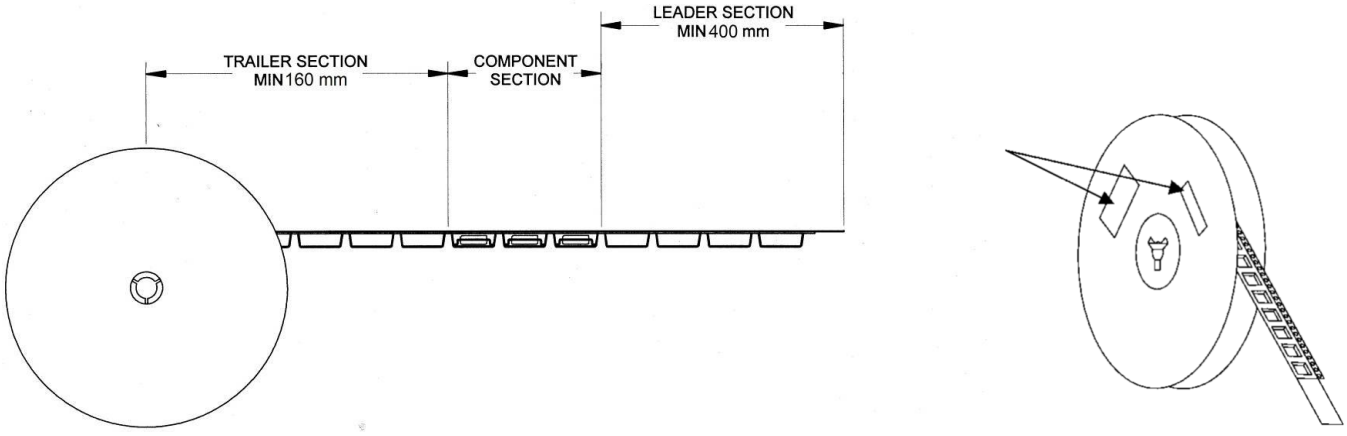
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 13” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.