

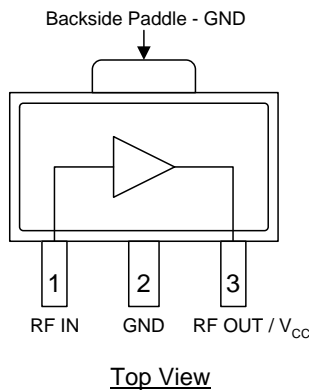
General Description

The TQP7M9101 is a high-linearity driver amplifier in a standard SOT-89 surface mount package. This InGaP GaAs HBT delivers high performance across a broad range of frequencies with +40 dBm OIP3 and with +25 dBm P1dB while only consuming 87 mA quiescent current. All devices are 100% RF and DC tested.

The TQP7M9101 incorporates on-chip features that differentiate it from other products in the market. The RF output is internally matched in to 50 ohms. Only input matching is required for optimal performance in specific frequency bands making the component easy for design engineers to implement in their systems. The amplifier integrates an on-chip DC over-voltage and RF over-drive protection. This protects the amplifier from electrical DC voltage surges and high input RF input power levels that may occur in a system. On-chip ESD protection allows the amplifier to have a very robust Class 2 HBM ESD rating.

The TQP7M9101 is targeted for use as a driver amplifier in wireless infrastructure where high linearity, medium power, and high efficiency are required. The device an excellent candidate for transceiver line cards in current and next generation multi-carrier 3G / 4G base stations.

Functional Block Diagram



3 Pin SOT-89 Package

Product Features

- 400 – 5000 MHz
- +25 dBm P1dB
- +39.5 dBm Output IP3
- 17.5 dB Gain at 2140 MHz
- +5 V Single Supply, 87 mA Current
- Internal RF Overdrive Protection
- Internal DC Overvoltage Protection
- On-Chip ESD Protection
- SOT-89 Package

Applications

- Repeaters
- Mobile Infrastructure
- CDMA / WCDMA / LTE
- General Purpose Wireless

Ordering Information

| Part No. | Description |
|-------------------|----------------------------------|
| TQP7M9101 | 1/4 W High Linearity Amplifier |
| TQP7M9101-PCB900 | 869 – 960 MHz Evaluation Board |
| TQP7M9101-PCB2140 | 2.11 – 2.17 GHz Evaluation Board |
| TQP7M9101-PCB2600 | 2.5 – 2.7 GHz Evaluation Board |

Standard T/R size = 1000 pieces on a 7" reel

Absolute Maximum Ratings

| Parameter | Rating |
|------------------------------------|----------------|
| Storage Temperature | -65 to +150 °C |
| RF Input Power, CW, 50Ω, T = +25°C | +23 dBm |
| Device Voltage, V _{CC} | +8 V |

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

| Parameter | Min | Typ | Max | Units |
|--|-----|-----|-------|-------|
| Device Voltage, V _{CC} | +3 | +5 | +5.25 | V |
| T _{CASE} | -40 | | +105 | °C |
| T _j for >10 ⁶ hours MTTF | | | +170 | °C |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

| Parameter | Conditions ⁽¹⁾ | Min | Typ | Max | Units |
|-------------------------------------|--|-------|-------|------|-------|
| Operational Frequency Range | | 400 | | 5000 | MHz |
| Test Frequency | | | 2140 | | MHz |
| Gain | | 15.6 | 17.5 | 18.6 | dB |
| Input Return Loss | | | 15 | | dB |
| Output Return Loss | | | 13.5 | | dB |
| Output P1dB | | +23.5 | +25 | | dBm |
| Output IP3 | P _{out} = +8 dBm/tone, Δf = 1 MHz | +36.5 | +39.5 | | dBm |
| WCDMA Channel Power | -50 dBc ACLR ⁽²⁾ | | +14.5 | | dBm |
| Noise Figure | | | 3.9 | | dB |
| Quiescent Current, I _{CCQ} | | 70 | 87 | 105 | mA |
| Thermal Resistance, θ _{JC} | Junction to backside paddle | | 71 | | °C/W |

Notes:

1. Test conditions unless otherwise noted: V_{CC} = +5 V, Temp. = +25 °C, matched 2140 MHz reference circuit
2. ACLR test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Probability

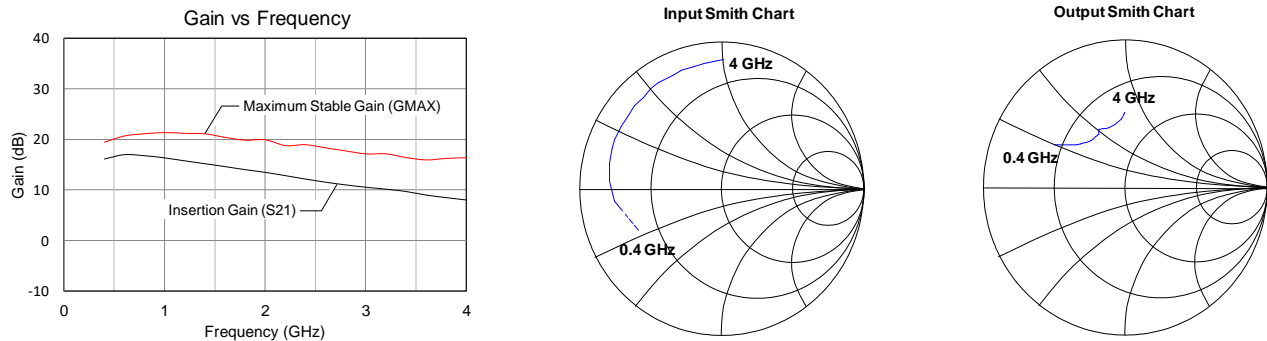
Performance Summary Table

| Frequency | 635 | 700 | 800 | 960 | 1500 | 1805 | 1900 | 2100 | 2140 | 2600 | 3500 | MHz |
|--------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-----|
| Gain | 20 | 18.5 | 18.7 | 20.1 | 19.4 | 18.0 | 16.6 | 15.9 | 17.5 | 16.5 | 15.0 | dB |
| Input Return Loss | 12 | 11.8 | 17.7 | 14 | 19 | 10.7 | 12 | 12 | 15 | 10 | 17 | dB |
| Output Return Loss | 33 | 12.8 | 19.1 | 17 | 13 | 15.8 | 11 | 9.5 | 13.5 | 14 | 11 | dB |
| Output P1dB | +25.0 | +24.1 | +24.2 | +24.4 | +23.8 | +25.0 | +24.0 | +24.2 | +24.8 | +24.9 | +23.4 | dBm |
| Output IP3 | +40.0 | +39.6 | +40.4 | +38.2 | +42.8 | +39.7 | +47.8 | +43.8 | +39.5 | +40.6 | +39.4 | dBm |

Notes:

1. Test conditions unless otherwise noted: V_{CC} = +5 V, Temp. = +25 °C, matched reference circuit
2. Reference designs for the various frequencies are either included on this datasheet

Device Characterization Data



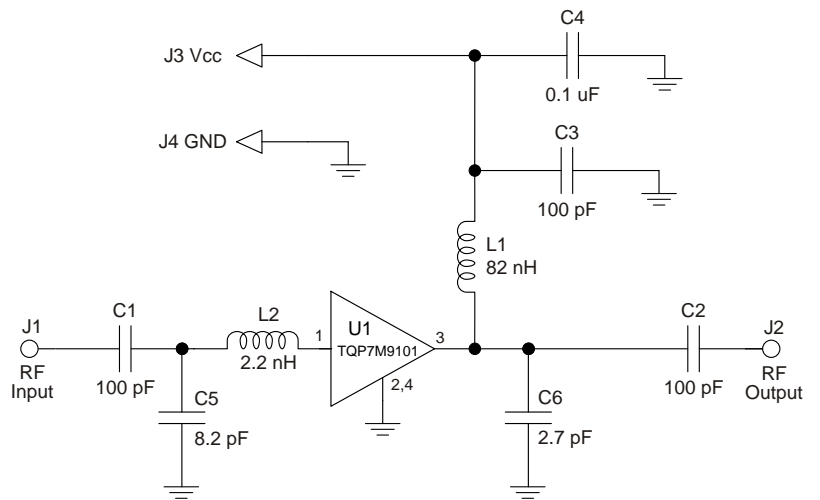
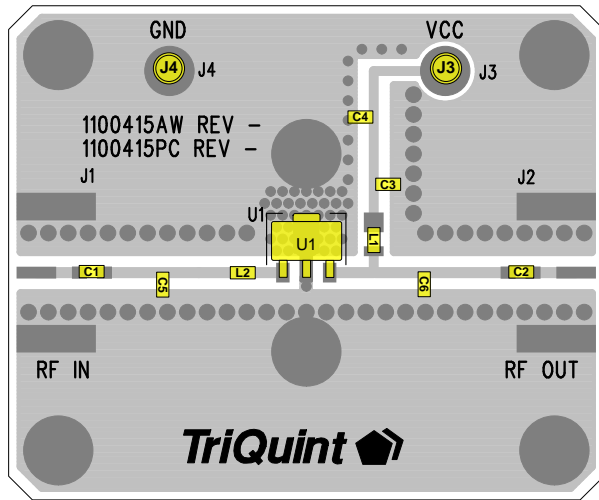
Note: The gain for the unmatched device in a 50 Ω system is shown as the black trace labeled "Gain (S21)". In a circuit tuned for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown as the red trace [Gmax]. The reflection coefficient plots on Smith Chart are shown from 0.4 GHz to 4 GHz.

S-Parameters

| Freq (MHz) | S11 (dB) | S11 (ang) | S21 (dB) | S21 (ang) | S12 (dB) | S12 (ang) | S22 (dB) | S22 (ang) |
|------------|----------|-----------|----------|-----------|----------|-----------|----------|-----------|
| 400 | -3.74 | -154.94 | 16.08 | 172.65 | -30.84 | 32.65 | -4.47 | 155.03 |
| 600 | -2.43 | -174.00 | 16.93 | 152.42 | -28.85 | 13.25 | -6.02 | 149.89 |
| 800 | -2.00 | 175.84 | 16.72 | 137.72 | -28.64 | 3.42 | -6.63 | 147.55 |
| 1000 | -1.81 | 167.43 | 16.29 | 123.90 | -28.38 | -4.74 | -7.05 | 144.48 |
| 1200 | -1.71 | 160.50 | 15.71 | 112.48 | -28.45 | -10.23 | -7.29 | 142.81 |
| 1400 | -1.68 | 155.82 | 15.15 | 102.29 | -28.29 | -15.72 | -7.67 | 139.67 |
| 1600 | -1.66 | 149.16 | 14.58 | 91.96 | -28.34 | -19.66 | -7.92 | 136.04 |
| 1800 | -1.65 | 143.36 | 13.98 | 82.32 | -28.40 | -25.64 | -8.05 | 132.86 |
| 2000 | -1.56 | 137.28 | 13.45 | 72.43 | -28.25 | -30.76 | -8.05 | 129.68 |
| 2200 | -1.60 | 131.41 | 12.80 | 64.37 | -28.52 | -35.06 | -7.96 | 125.67 |
| 2400 | -1.43 | 126.29 | 12.14 | 56.45 | -28.43 | -39.47 | -7.47 | 122.90 |
| 2600 | -1.41 | 122.01 | 11.52 | 48.81 | -28.73 | -42.87 | -7.49 | 122.21 |
| 2800 | -1.43 | 117.57 | 10.99 | 41.39 | -28.68 | -47.17 | -7.71 | 119.34 |
| 3000 | -1.45 | 114.12 | 10.53 | 34.73 | -28.78 | -49.96 | -7.92 | 116.57 |
| 3200 | -1.36 | 109.38 | 10.15 | 27.42 | -28.85 | -52.90 | -7.87 | 114.37 |
| 3400 | -1.40 | 103.72 | 9.69 | 19.90 | -29.00 | -59.40 | -7.85 | 106.77 |
| 3600 | -1.32 | 98.51 | 8.99 | 12.40 | -29.04 | -63.10 | -7.32 | 100.14 |
| 3800 | -1.19 | 93.06 | 8.49 | 5.24 | -29.04 | -68.03 | -6.75 | 96.77 |
| 4000 | -1.11 | 89.37 | 8.02 | -0.57 | -29.02 | -70.86 | -6.53 | 95.94 |

Test Conditions: $V_{CC} = +5\text{ V}$, $I_{CC} = 87\text{ mA}$, Temp. = $+25\text{ }^\circ\text{C}$, unmatched 50 Ohm system, reference plane at device leads

617 – 652 MHz Reference Design



Notes:

1. See Evaluation Board PCB Information section for PCB material and stack-up
2. All components are 0603 size unless otherwise specified.
3. Critical component placement locations:
 Distance from U1 Pin 1 (left edge) to L2 (right edge): 90 mils
 Distance from U1 Pin 1 (left edge) to C5 (right edge): 310 mils
 Distance from U1 Pin 3 (right edge) to C6 (left edge): 245 mils

Bill of Material 617 – 652 MHz Reference Design

| Reference Des. | Value | Description | Manuf. | Part Number |
|----------------|-------------|---|-----------|----------------|
| n/a | n/a | Printed Circuit Board | Qorvo | 1100415 |
| U1 | n/a | Amplifier, SOT-89 pkg. | Qorvo | TQP7M9101 |
| L1 | 82 nH | Inductor, 0805, 5%, Coilcraft CS Series | Coilcraft | 0805CS-820XJLB |
| L2 | 2.2 nH | Inductor, Chip, 0603 | various | |
| C1, C2, C3 | 100 pF | Cap., Chip, 5%, 50 V, NPO/C0G | various | |
| C4 | 0.1 μ F | Cap., Chip, 10%, 50 V, X7R | various | |
| C5 | 8.2 pF | Cap., Chip, +/-0.1 pF. 50 V NPO/C0G | various | |
| C6 | 2.7 pF | Cap., Chip, +/-0.1 pF. 50 V NPO/C0G | various | |
| J3, J4 | n/a | Solder Turret | various | |

Typical Performance 617 – 652 MHz Reference Design

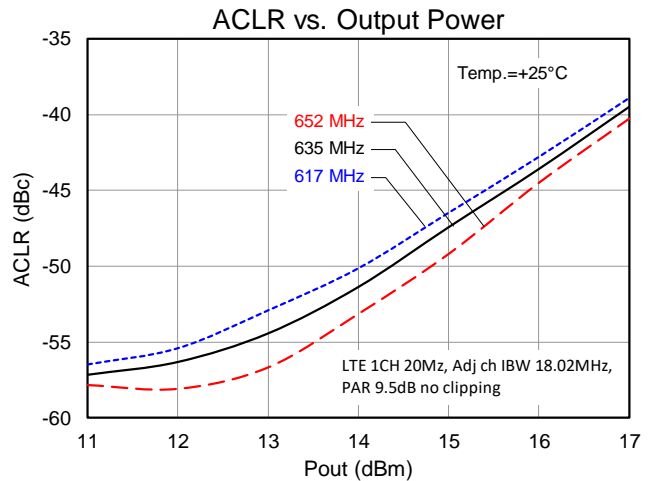
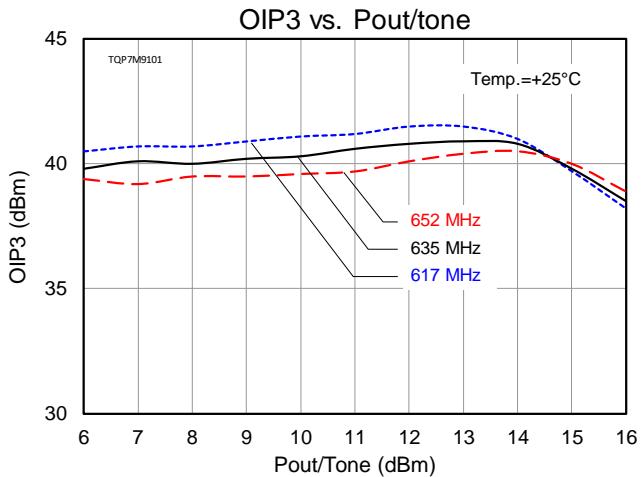
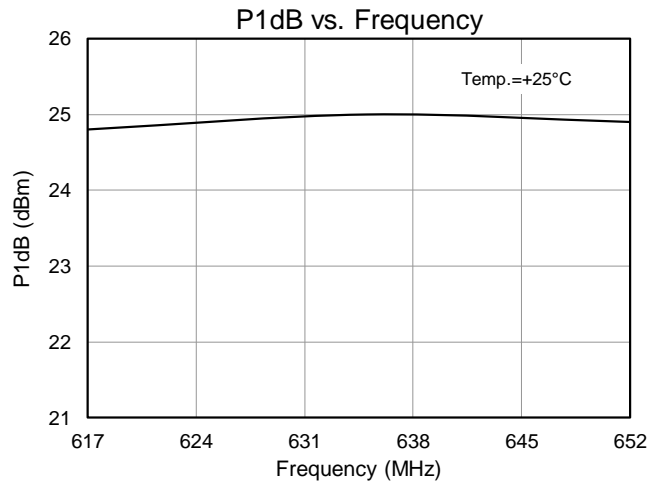
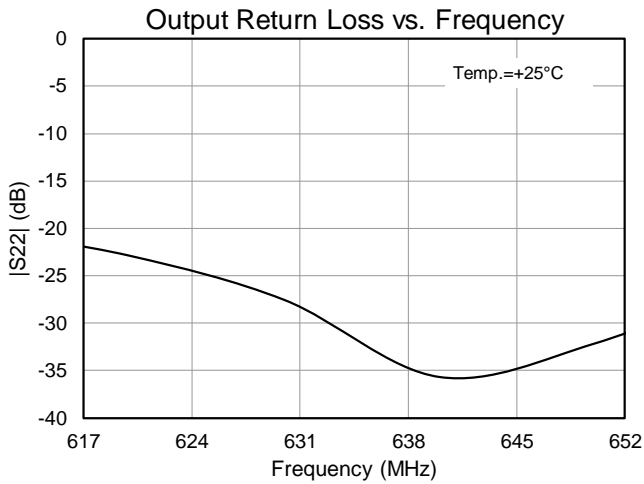
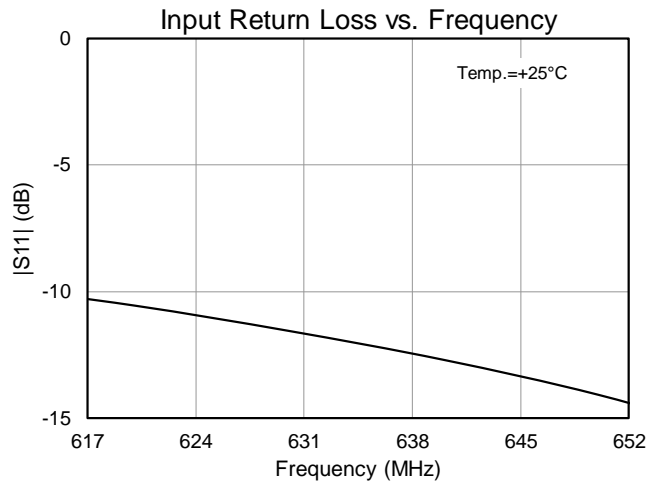
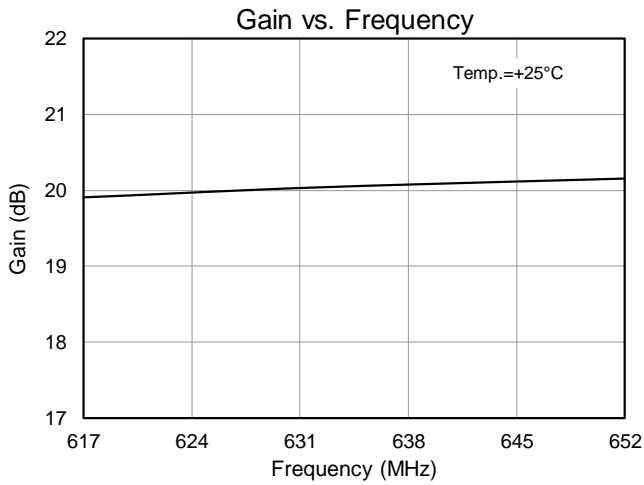
| Parameter | Typical Value | | | | |
|----------------------------------|--------------------------------------|-------|-------|-----|--|
| | 617 | 635 | 652 | MHz | |
| Frequency | | | | | |
| Gain | 20 | 20 | 20 | dB | |
| Input Return Loss | 10 | 12 | 14 | dB | |
| Output Return Loss | 22 | 33 | 31 | dB | |
| Output P1dB | +24.8 | +25.0 | +24.9 | dBm | |
| Output IP3 | Pout=+8 dBm/tone, $\Delta f = 1$ MHz | | | | |
| LTE Channel Power ⁽²⁾ | +14.0 | +14.4 | +14.8 | dBm | |

Notes:

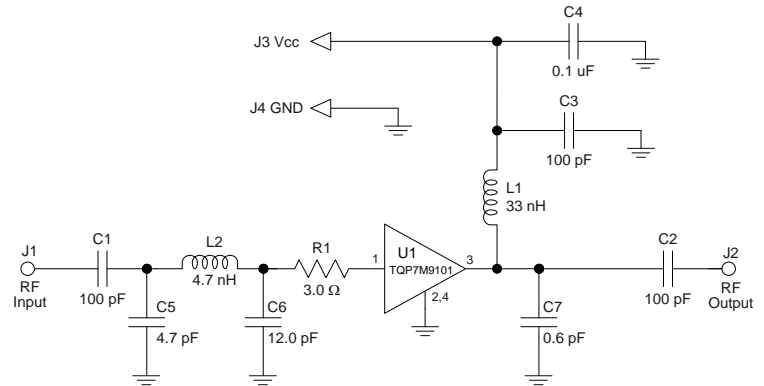
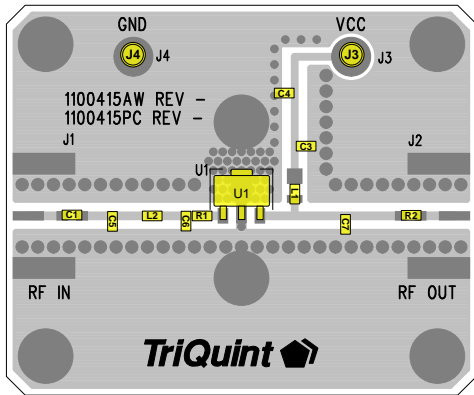
1. Test conditions unless otherwise noted: $V_{CC} = +5$ V, $I_{CO} = 87$ mA (typ.), Temp. = +25 °C
2. ACLR test set-up: 1 CH, 20 MHz BW, LTE E-TM1.1, 9.5 dB PAR at 0.01% Probability

Performance Plots 617 – 652 MHz Reference Design

Test conditions unless otherwise noted: $V_{CC} = +5\text{ V}$, $I_{CQ} = 87\text{ mA}$ (typ.), $Temp. = +25^\circ\text{C}$



700 – 1000 MHz Reference Design



Notes:

1. See Evaluation Board PCB Information section for PCB material and stack-up
2. All components are 0603 size unless otherwise specified.
3. Critical component placement locations:
 - Distance from U1 Pin 1 Pad (left edge) to R1 (right edge): 10 mils (0.5° at 900 MHz)
 - Distance from R1 (left edge) to C6 (right edge): 5 mils (0.2° at 900 MHz)
 - Distance from C6 (left edge) to L2 (right edge): 60 mils (2.8° at 900 MHz)
 - Distance from L2 (left edge) to C5 (right edge): 60 mils (2.8° at 900 MHz)
 - Distance from U1 Pin 3 Pad (right edge) to C7 (left edge): 250 mils (11.7° at 900 MHz)

Bill of Material 700 – 1000 MHz Reference Design

| Reference Des. | Value | Description | Manuf. | Part Number |
|----------------|--------|---|-----------|----------------|
| n/a | n/a | Printed Circuit Board | Qorvo | 1100415 |
| U1 | n/a | Amplifier, SOT-89 pkg. | Qorvo | TQP7M9101 |
| L1 | 33 nH | Inductor, 0805, 5%, Coilcraft CS Series | Coilcraft | 0805CS-330XJLB |
| L2 | 4.7 nH | Inductor, Chip, 0603 | various | |
| C1, C2, C3 | 100 pF | Cap., Chip, 5%, 50 V, NPO/C0G | various | |
| C4 | 0.1 uF | Cap., Chip, 10%, 50 V, X7R | various | |
| C5 | 4.7 pF | Cap., Chip, +/-0.1 pF. 50 V NPO/C0G | various | |
| C6 | 12 pF | Cap., Chip, 2% 50 V NPO/C0G | various | |
| C7 | 0.6 pF | Cap., Chip, +/-0.05 pF. 50 V NPO/C0G | various | |
| J3, J4 | n/a | Solder Turret | various | |

Typical Performance 700 – 1000 MHz Reference Design

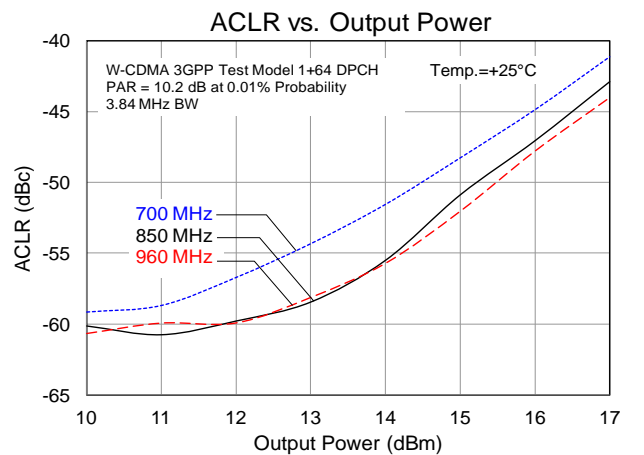
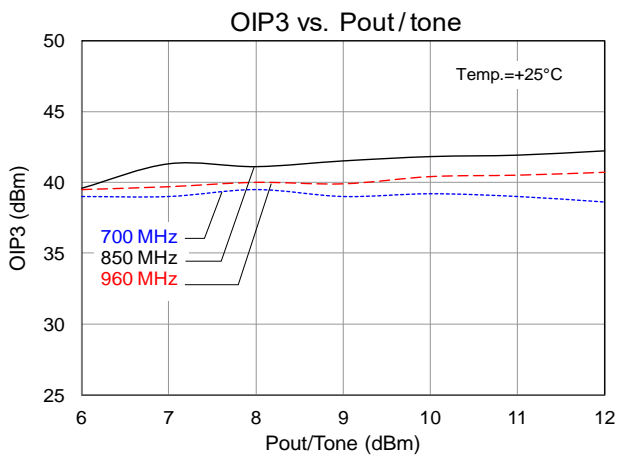
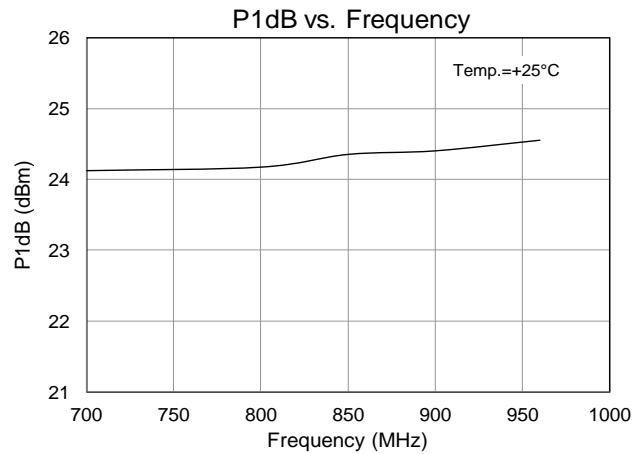
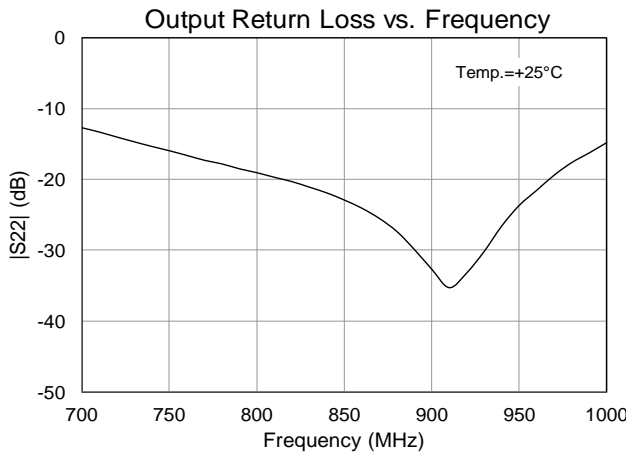
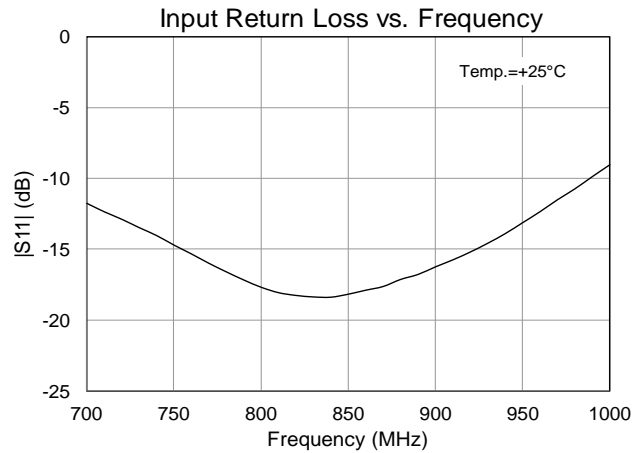
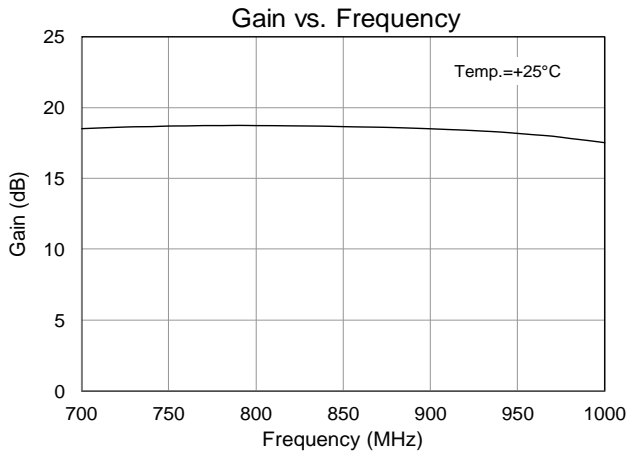
| Parameter | Typical Value | | | | | | | |
|-----------------------|------------------------------|-------|-------|-------|-------|-------|-------|-----|
| | 700 | 800 | 850 | 900 | 960 | MHz | | |
| Frequency | | | | | | | | |
| Gain | 18.5 | 18.7 | 18.6 | 18.5 | 18.2 | dB | | |
| Input Return Loss | 11.8 | 17.7 | 18.2 | 16.2 | 13.1 | dB | | |
| Output Return Loss | 12.8 | 19.1 | 22.9 | 32.7 | 23.7 | dB | | |
| Output P1dB | +24.1 | +24.2 | +24.4 | +24.4 | +24.6 | dBm | | |
| Output IP3 | Pout=+8 dBm/tone, Δf = 1 MHz | | +39.6 | +40.4 | +41.2 | +39.7 | +39.8 | dBm |
| WCDMA Chan. Power (2) | -55 dBc ACLR | | +12.8 | +13.2 | +13.5 | +14.0 | +14.0 | dBm |
| Noise Figure | 5.0 | 5.0 | 5.1 | 5.2 | 5.9 | dB | | |

Notes:

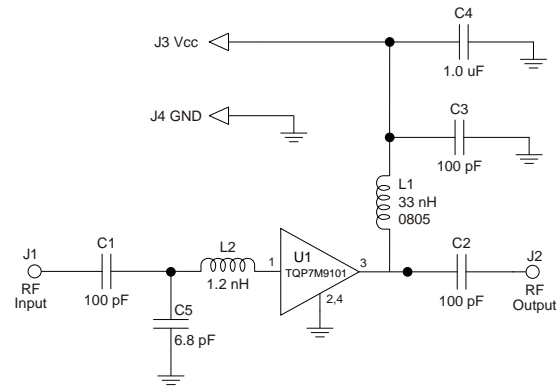
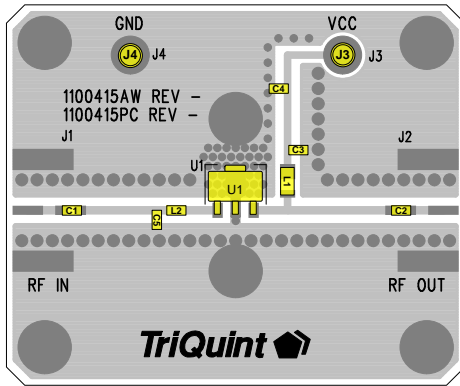
1. Test conditions unless otherwise noted: $V_{CC} = +5V$, $I_{CO} = 87\text{ mA}$ (typ.), Temp. = +25 °C
2. ACLR test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Probability

Performance Plots 700 – 1000 MHz Reference Design

Test conditions unless otherwise noted: $V_{CC} = +5\text{ V}$, $I_{CQ} = 87\text{ mA}$ (typ.), $Temp. = +25\text{ }^{\circ}\text{C}$



869 – 960 MHz Evaluation Board (TQP7M9101– PCB900)



Notes:

1. See Evaluation Board PCB Information section for PCB material and stack-up
2. Components (C1 and C2) are blocking capacitors and their locations are not critical to the matching network.
3. All components are of 0603 size unless otherwise specified.
4. Critical component placement locations:
 Distance from U1 Pin 1 Pad (left edge) to L2 (right edge): 90 mils (4.8° at 920 MHz)
 Distance from L2 (left edge) to C5 (right edge): 40 mils (2.1° at 920 MHz)

Bill of Material TQP7M9101– PCB900

| Reference Des. | Value | Description | Manuf. | Part Number |
|----------------|--------|---|-----------|----------------|
| n/a | n/a | Printed Circuit Board | Qorvo | 1100415 |
| U1 | n/a | Amplifier, SOT-89 pkg. | Qorvo | TQP7M9101 |
| L1 | 33 nH | Inductor, 0805, 5%, Coilcraft CS Series | Coilcraft | 0805CS-330XJLB |
| L2 | 1.2 nH | Inductor, Chip, 0603 | various | |
| C1, C2, C3 | 100 pF | Cap., Chip, 5%, 50V, NPO/C0G | various | |
| C4 | 1.0 μF | Cap., Chip, 10%, 10V, X5R | various | |
| C5 | 6.8 pF | Cap., Chip, +/-0.1pF. 50V NPO/C0G | various | |
| J1, J2 | n/a | RF SMA Connector | Johnson | 142-0701-851 |
| J3, J4 | n/a | Solder Turret | various | |

Typical Performance TQP7M9101– PCB900

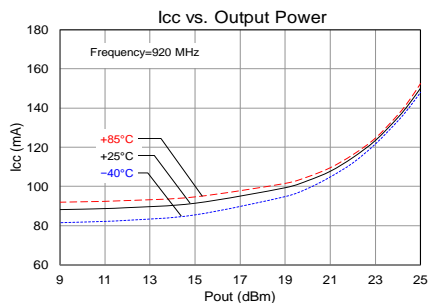
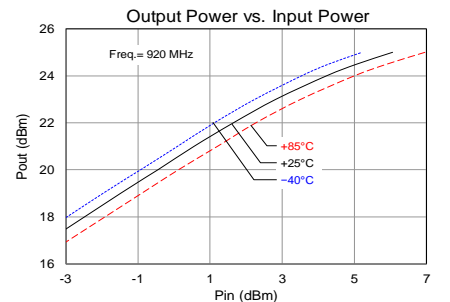
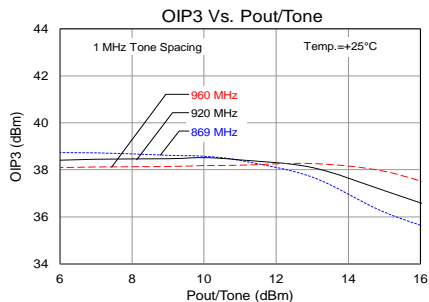
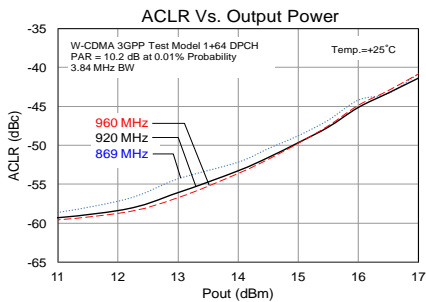
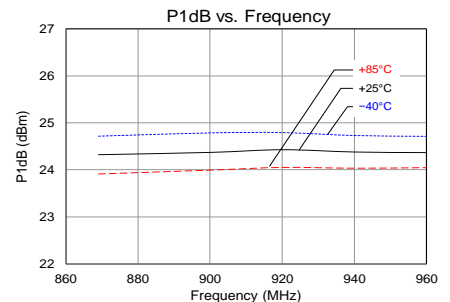
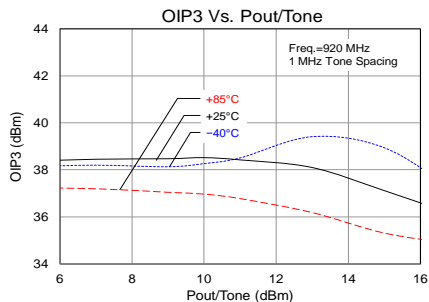
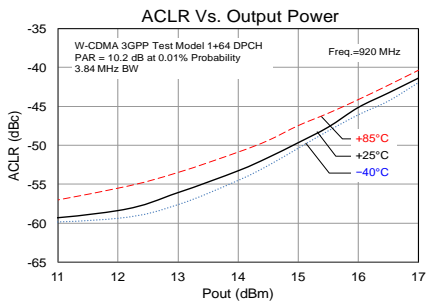
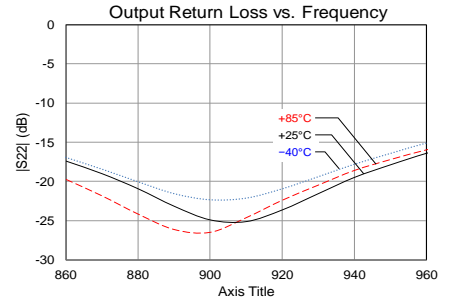
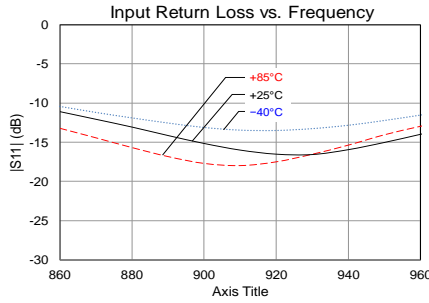
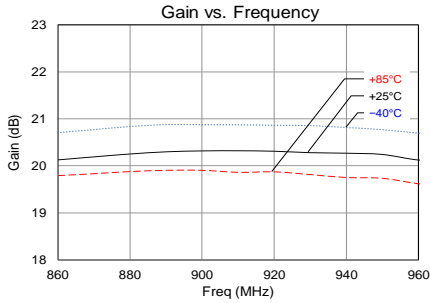
| Parameter | Conditions | Typical Value | | | Units |
|------------------------------------|-----------------------------|---------------|-------|-------|-------|
| Frequency | | 869 | 920 | 960 | MHz |
| Gain | | 20.2 | 20.4 | 20.1 | dB |
| Input Return Loss | | 12 | 17 | 14 | dB |
| Output Return Loss | | 18 | 23 | 17 | dB |
| Output P1dB | | +24.3 | +24.4 | +24.4 | dBm |
| OIP3 | Pout= +8 dBm/tone, Δf=1 MHz | +39.2 | +38.6 | +38.2 | dBm |
| WCDMA Channel Power ⁽²⁾ | -55 dBc ACLR | +12.7 | +13.4 | +13.5 | dBm |
| Noise Figure | | 4.0 | 4.0 | 3.9 | dB |

Notes:

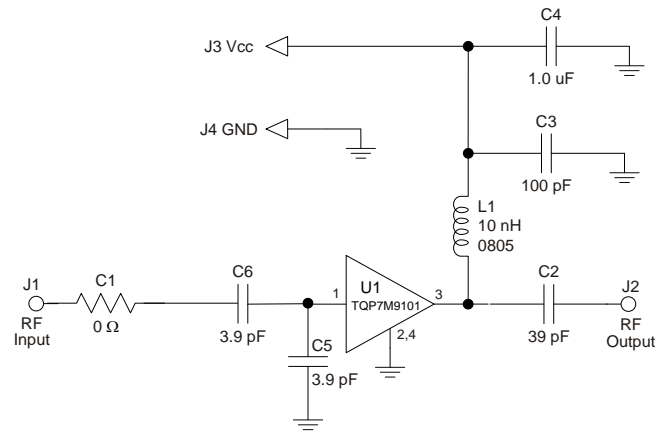
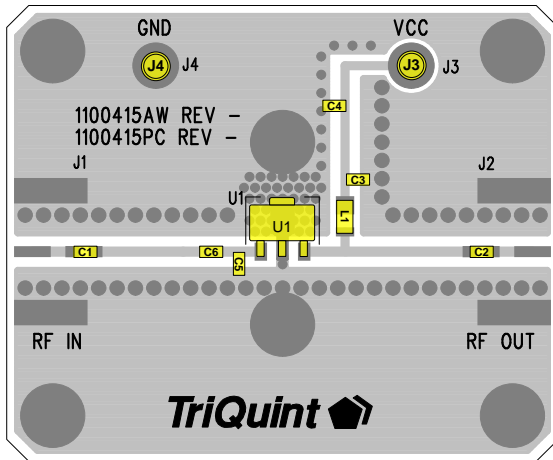
1. Test conditions unless otherwise noted: V_{CC} = +5 V, I_{CO} = 87 mA (typ.), Temp. = +25 °C
2. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Probability

Performance Plots TQP7M9101-PCB900

Test conditions unless otherwise noted: $V_{CC} = +5\text{ V}$, $I_{CQ} = 87\text{ mA}$ (typ.), Temp. = $+25\text{ }^{\circ}\text{C}$



1460 – 1540 MHz Reference Design



Notes:

1. See Evaluation Board PCB Information for material and stack up.
2. 0 Ω resistor (C1) may be replaced with copper trace in the target application layout.
3. All components are of 0603 size unless stated on the schematic.
4. Critical component placement locations:
 Distance between U1 Pin 1 Pad (left edge) to C5 (right edge): 60 mils
 Distance between U1 Pin 1 Pad (left edge) to C6 (right edge): 90 mils

Bill of Material 1460 – 1540 MHz Reference Design

| Reference Des. | Value | Description | Manuf. | Part Number |
|----------------|-------------|---|-----------|----------------|
| n/a | n/a | Printed Circuit Board | Qorvo | 1100415 |
| U1 | n/a | 0.25 W High Linearity Amplifier | Qorvo | TQP7M9101 |
| C5 , C6 | 3.9 pF | CAP, 0603, +/-0.1pF. 200V. NPO/C0G | various | |
| C1 | 0 Ω | RES, 0603, +/-5%, 1/16 W | various | |
| C2 | 39 pF | CAP, 0603, +/-5%, 50V NPO/C0G | various | |
| C3 | 100 pF | Cap., Chip, 0603, +/-5%. 50V NPO/C0G | various | |
| C4 | 1.0 μ F | CAP, 0603, 10%, X5R , 10V | various | |
| L1 | 10 nH | Inductor, 0805, 5%, Coilcraft CS Series | Coilcraft | 0805CS-100XJLB |
| J3, J4 | n/a | Solder Turret | various | |

Typical Performance 1460 – 1540 MHz Reference Design

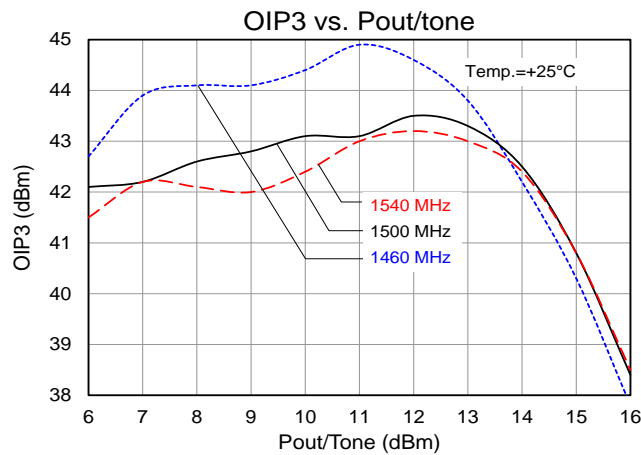
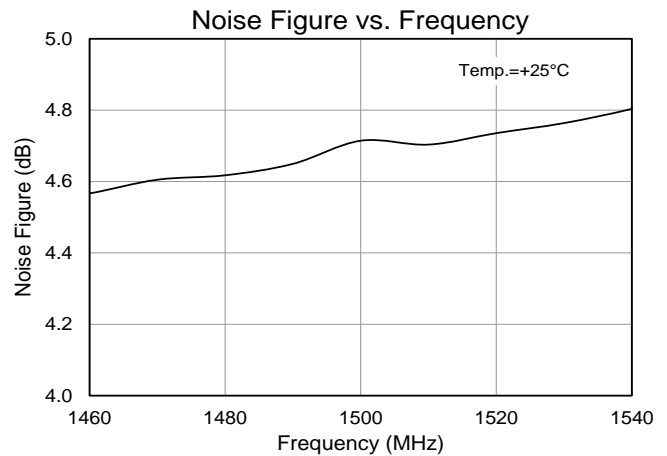
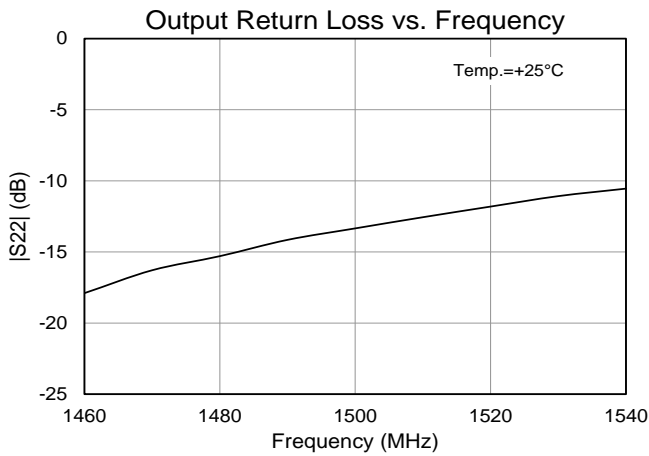
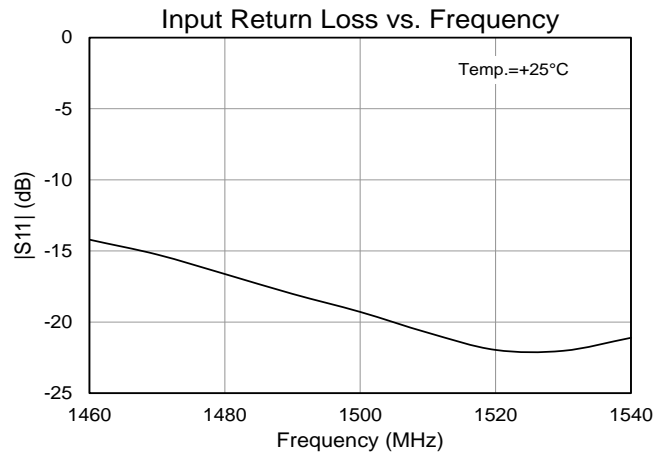
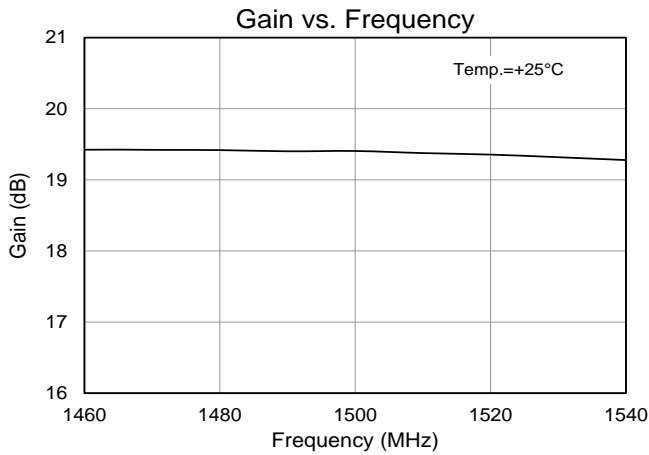
| Parameter | Conditions | Typical Value | | | Units |
|--------------------|-------------------------------------|---------------|-------|-------|-------|
| | | 1460 | 1500 | 1540 | |
| Frequency | | 1460 | 1500 | 1540 | MHz |
| Gain | | 19.4 | 19.4 | 19.3 | dB |
| Input Return Loss | | 14 | 19 | 20 | dB |
| Output Return Loss | | 17 | 13 | 10 | dB |
| Output P1dB | | +24.4 | +23.8 | +23.7 | dBm |
| OIP3 | Pout= +8 dBm/tone, Δ f=1 MHz | +44 | +42.8 | +42 | dBm |
| Noise Figure | | 4.6 | 4.7 | 4.8 | dBm |

Notes:

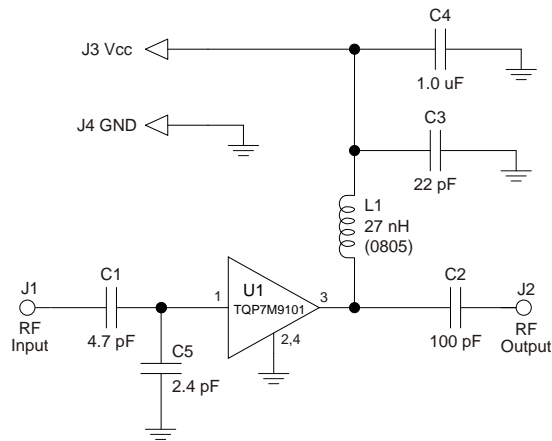
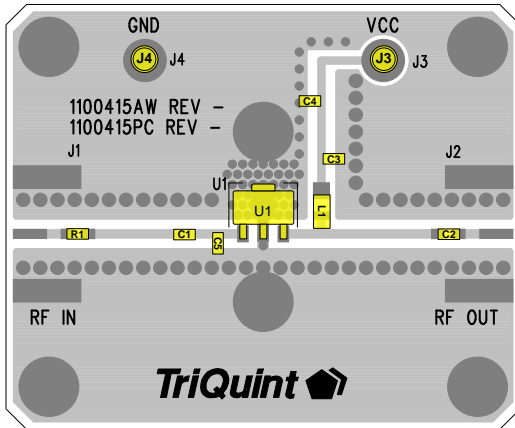
1. Test conditions unless otherwise noted: $V_{CC} = +5V$, $I_{CQ} = 87\text{ mA}$ (typ.), Temp. = +25 $^{\circ}\text{C}$

Performance Plots 1460 – 1540 MHz Reference Design

Test conditions unless otherwise noted: $V_{CC} = +5V$, $I_{CQ} = 87\text{ mA}$ (typ.), Temp. = +25 °C



1805 – 1990 MHz Reference Design



Notes:

1. See Evaluation Board PCB Information section for PCB material and stack-up.
2. Component R1 on the PCB is a (0 Ω) Resistor and may be replaced by a copper trace
3. All components are of 0603 size unless otherwise specified.
4. Critical component placement:
 Distance from U1 Pin 1 Pad (left edge) to C5 (right edge): 30 mils (3.0° at 1900 MHz)
 Distance from C5 (left edge) to C1 (right edge): 55 mils (5.5° at 1900 MHz)

Bill of Material 1805 – 1990 MHz Reference Design

| Reference Des. | Value | Description | Manuf. | Part Number |
|----------------|--------|---|-----------|----------------|
| n/a | n/a | Printed Circuit Board | Qorvo | 1100415 |
| U1 | n/a | 0.25 W High Linearity Amplifier | Qorvo | TQP7M9101 |
| R1 | 0 Ω | RES, 0603, 5PCT. 1/16W. CHIP | various | |
| C1 | 4.7 pF | CAP, Chip, +/-0.1pF. 50V NPO/C0G | various | |
| C5 | 2.4 pF | CAP, Chip, +/-0.1pF. 50V NPO/C0G | various | |
| C2 | 100 pF | CAP, 0603, 5%, 50V, NPO/C0G | various | |
| C3 | 22 pF | CAP, 0603, 5%, 50V, NPO/C0G | various | |
| C4 | 1.0 μF | CAP, 0603, 10%, X5R , 10V | various | |
| L1 | 27 nH | Inductor, 0805, 5%, Coilcraft CS series | Coilcraft | 0805CS-270XJLB |
| J3, J4 | n/a | Solder Turret | various | |

Typical Performance 1805 – 1990 MHz Reference Design

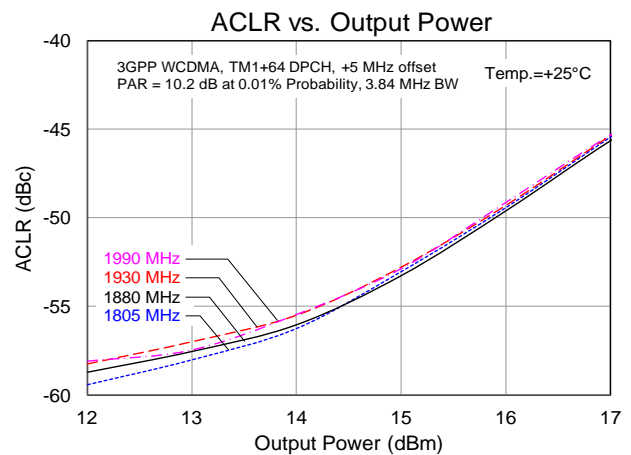
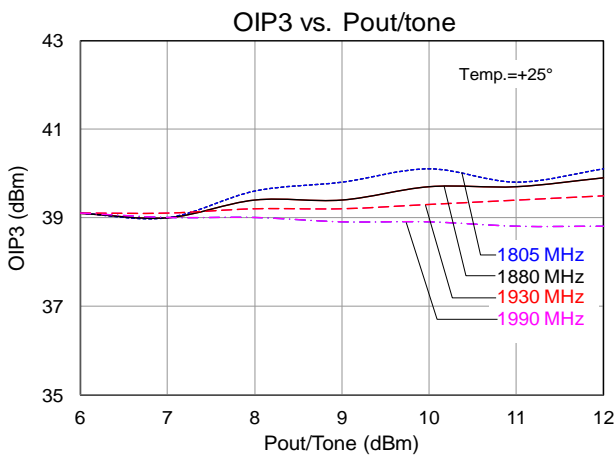
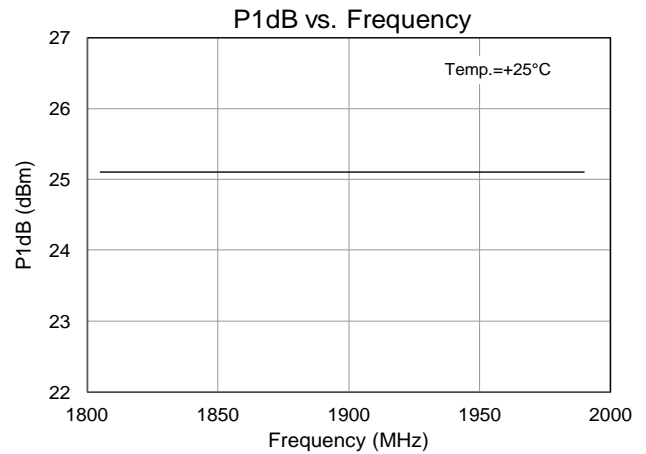
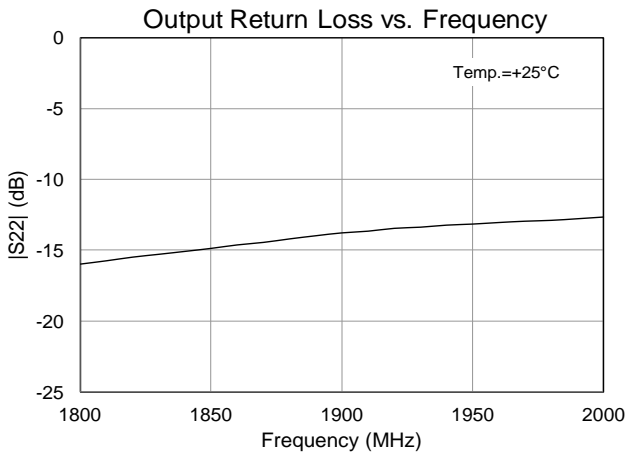
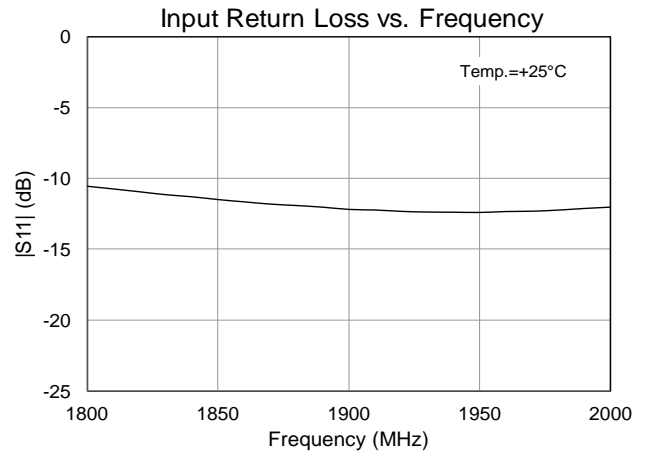
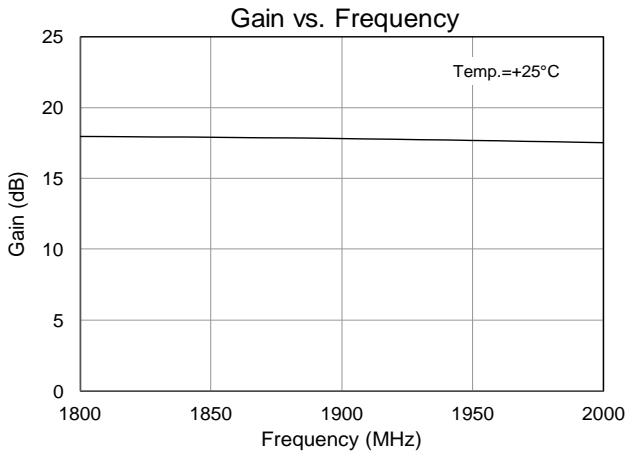
| Parameter | Conditions ⁽¹⁾ | Typical Value | | | | | | Units |
|---------------------|-----------------------------|---------------|-------|-------|-------|-------|-------|-------|
| | | 1805 | 1850 | 1880 | 1930 | 1960 | 1990 | |
| Frequency | | 1805 | 1850 | 1880 | 1930 | 1960 | 1990 | MHz |
| Gain | | 18.0 | 17.9 | 17.9 | 17.7 | 17.7 | 17.6 | dB |
| Input Return Loss | | 10.7 | 11.5 | 11.9 | 12.4 | 12.4 | 12.2 | dB |
| Output Return Loss | | 15.8 | 14.9 | 14.2 | 13.4 | 13.1 | 12.8 | dB |
| Output P1dB | | +25.0 | +25.1 | +25.1 | +25.1 | +25.1 | +25.1 | dBm |
| Output IP3 | +8 dBm/tone, Δf = 1 MHz | +39.7 | +39.6 | +39.5 | +39.2 | +38.7 | +39.1 | dBm |
| WCDMA Channel Power | -55 dBc ACLR ⁽²⁾ | +14.5 | +14.5 | +14.4 | +14.3 | +14.0 | +14.1 | dBm |

Notes:

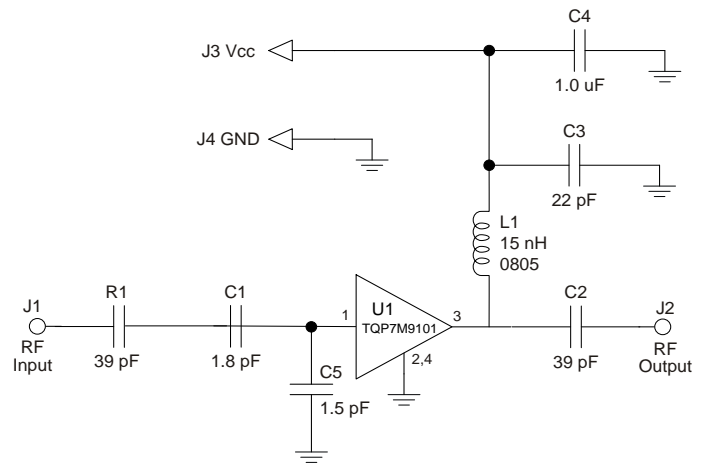
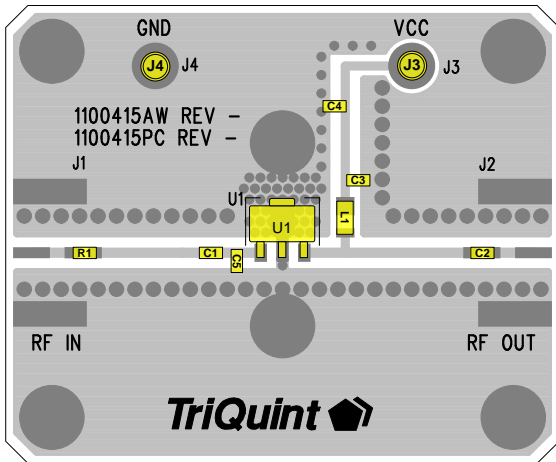
1. Test conditions unless otherwise noted: V_{CC} = +5 V, I_{CO} = 87 mA (typ.), Temp. = +25 °C
2. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Probability

Performance Plots 1805 – 1990 MHz

Test conditions unless otherwise noted: $V_{CC} = +5\text{ V}$, $I_{CQ} = 87\text{ mA}$ (typ.), Temp. = $+25^\circ\text{C}$



2110 – 2170 MHz Evaluation Board (TQP7M9101-PCB2140)



Notes:

1. See Evaluation Board PCB Information section for PCB material and stack-up.
2. Component (R1) is a 39 pF capacitor and may be replaced with copper trace in the target application layout.
3. All components are of 0603 size unless otherwise specified.
4. Critical component placement locations:
 - Distance from U1 Pin 1 Pad (left edge) to C5 (right edge): 40 mils (4.5° at 2140 MHz)
 - Distance from U1 Pin 1 Pad (left edge) to C1 (right edge): 90 mils (10.0° at 2140 MHz)

Bill of Material TQP7M9101-PCB2140

| Reference Des. | Value | Description | Manuf. | Part Number |
|----------------|--------|---|-----------|----------------|
| n/a | n/a | Printed Circuit Board | Qorvo | 1100415 |
| U1 | n/a | Amplifier, SOT-89 pkg. | Qorvo | TQP7M9101 |
| L1 | 15 nH | Inductor, 0805, 5%, Coilcraft CS Series | Coilcraft | 0805CS-150XJLB |
| C1 | 1.8 pF | Cap., Chip, 0603, +/-0.1pF. 200V. NPO/C0G | various | |
| C5 | 1.5 pF | Cap., Chip, 0603, +/-0.1pF. 200V. NPO/C0G | various | |
| R1, C2 | 39 pF | Cap., Chip, 5%, 50V, NPO/C0G | various | |
| C3 | 22 pF | Cap., Chip, 5%, 50V, NPO/C0G | various | |
| C4 | 1.0 μF | Cap., Chip, 10%, 10V, X5R | various | |
| J3, J4 | n/a | Solder Turret | various | |

Typical Performance TQP7M9101-PCB2140

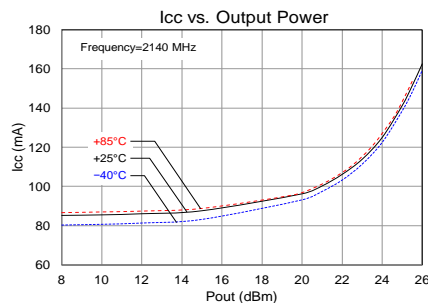
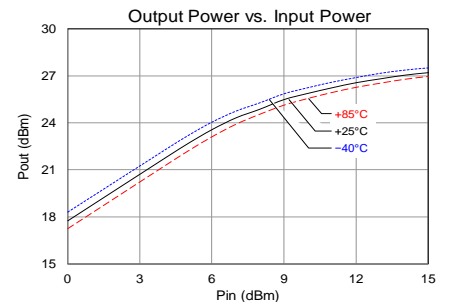
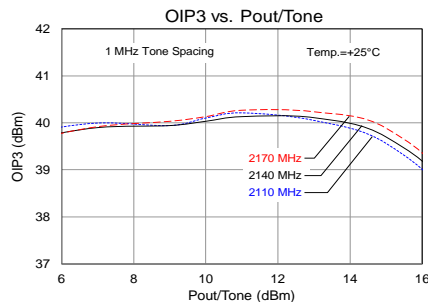
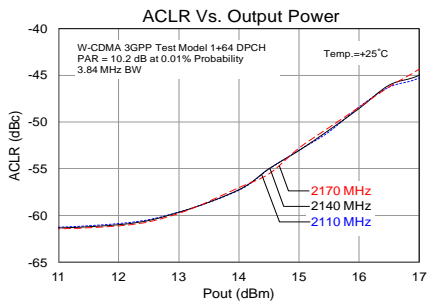
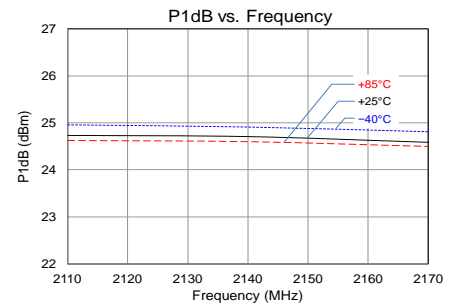
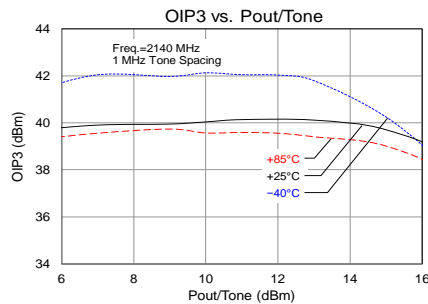
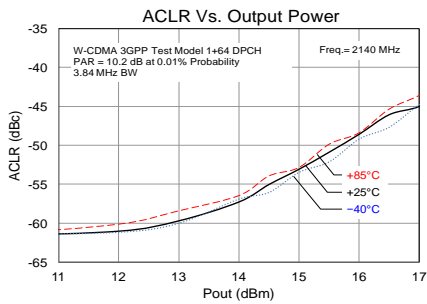
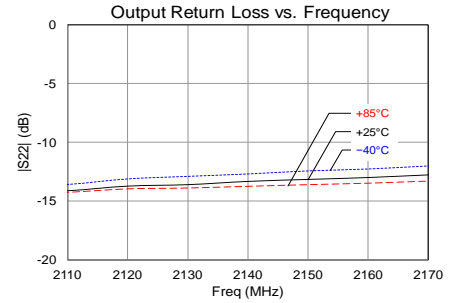
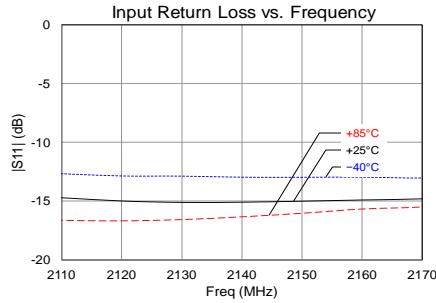
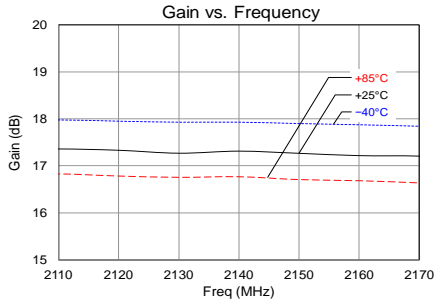
| Parameter | Conditions ⁽¹⁾ | Typical Value | | | Units |
|---------------------|-----------------------------|---------------|-------|-------|-------|
| | | 2110 | 2140 | 2170 | |
| Frequency | | 2110 | 2140 | 2170 | MHz |
| Gain | | 17.6 | 17.5 | 17.4 | dB |
| Input Return Loss | | 15 | 15 | 15 | dB |
| Output Return Loss | | 14 | 13.5 | 13 | dB |
| Output P1dB | | +24.8 | +24.8 | +24.6 | dBm |
| OIP3 | Pout= +8 dBm/tone, Δf=1 MHz | +39.5 | +39.5 | +39.5 | dBm |
| WCDMA Channel Power | -55 dBc ACLR ⁽²⁾ | +14.5 | +14.5 | +14.5 | dBm |
| Noise Figure | | 4.0 | 3.9 | 4.1 | dB |

Notes:

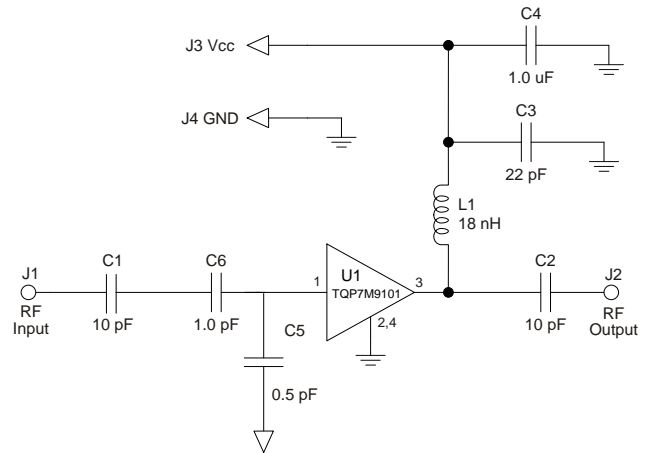
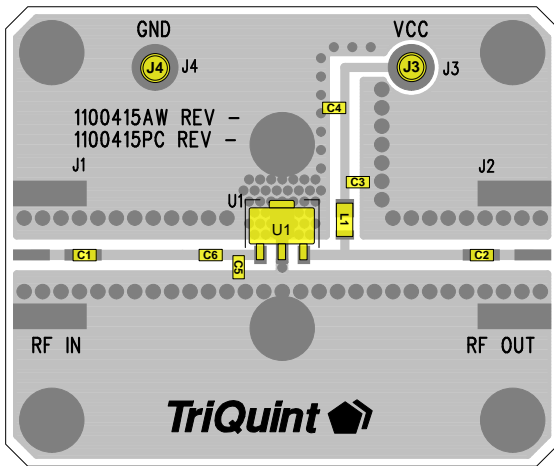
1. Test conditions unless otherwise noted: V_{CC} = +5 V, I_{CO} = 87 mA (typ.), Temp. = +25 °C
2. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Probability

Performance Plots – TQP7M9101-PCB2140

Test conditions unless otherwise noted: $V_{CC} = +5\text{ V}$, $I_{CQ} = 87\text{ mA}$ (typ.), Temp. = $+25\text{ }^{\circ}\text{C}$



2.5 – 2.7 GHz Evaluation Board (TQP7M9101-PCB2600)



Notes:

1. See Evaluation Board PCB Information for material and stack up.
2. The recommended component values are dependent upon the frequency of operation.
3. All components are of 0603 size unless stated on the schematic.
4. Critical component placement locations:
 Distance from U1 Pin 1 (left edge) to C5 (right edge): 20 mils
 Distance from U1 Pin 1 (left edge) to C6 (right edge): 123 mils

Bill of Material TQP7M9101-PCB2600

| Reference Des. | Value | Description | Manuf. | Part Number |
|----------------|--------|---|-----------|----------------|
| n/a | n/a | Printed Circuit Board | Qorvo | 1100415 |
| U1 | n/a | 0.25 W High Linearity Amplifier | Qorvo | TQP7M9101 |
| C6 | 1.0 pF | CAP, 0603, +/-0.1pF. 200V. NPO/C0G | various | |
| C5 | 0.5 pF | CAP, 0603, +/-0.1pF. 200V. NPO/C0G | various | |
| C1 , C2 | 10 pF | Cap., Chip, 0603, +/-5%. 50V NPO/C0G | various | |
| C3 | 22pF | Cap., Chip, 0603, +/-5%. 50V NPO/C0G | various | |
| C4 | 1.0 μF | CAP, 0603, 10%, X5R , 10V | various | |
| L1 | 18 nH | Inductor, 0805, 5%, Coilcraft CS series | Coilcraft | 0805CS-180XJLB |
| J3, J4 | n/a | Solder Turret | various | |

Typical Performance TQP7M9101-PCB2600

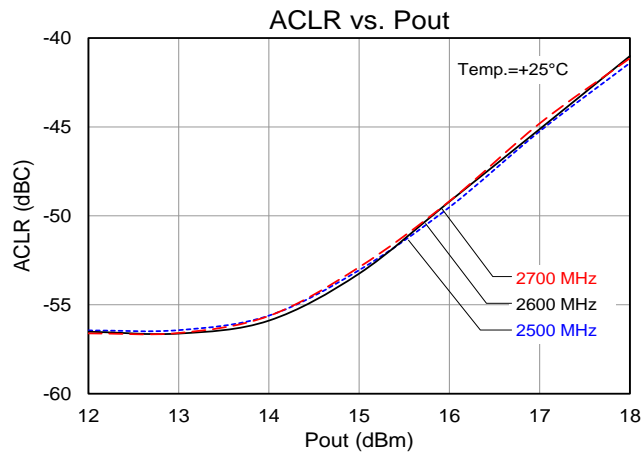
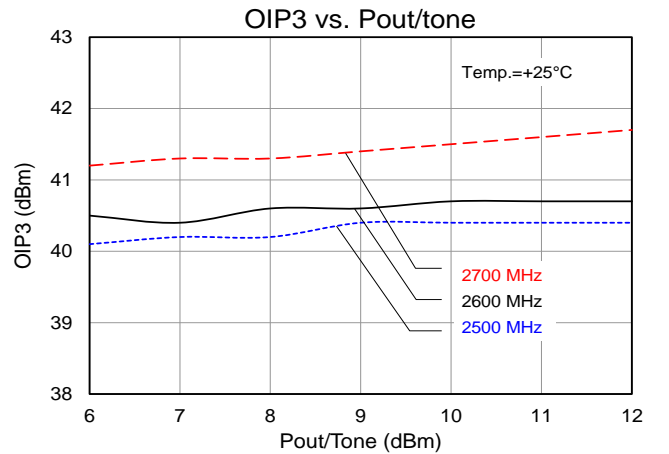
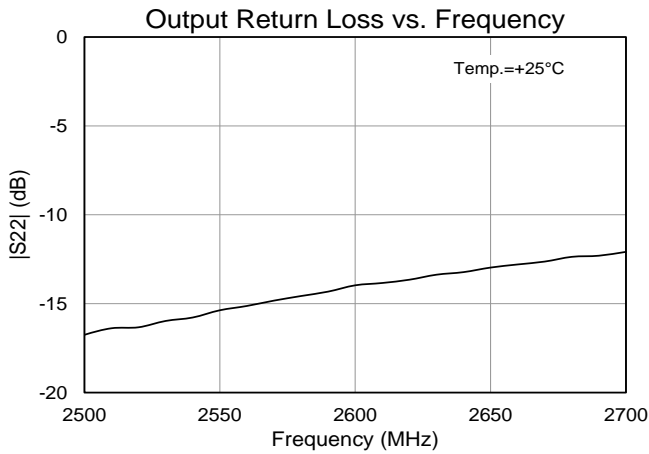
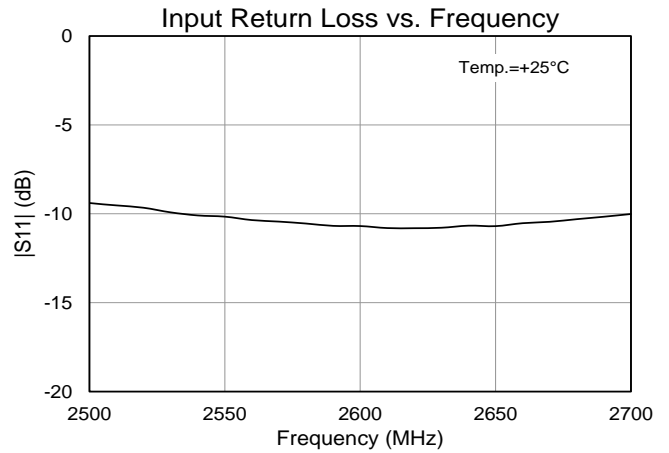
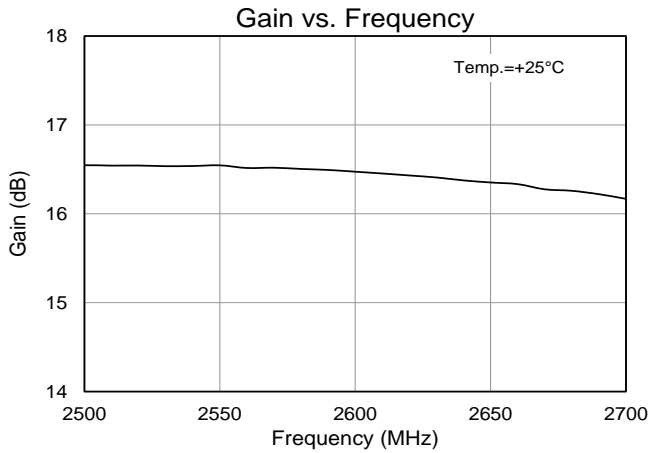
| Parameter | Conditions ⁽¹⁾ | Typical Value | | | Units |
|---------------------|-----------------------------|---------------|-------|-------|-------|
| Frequency | | 2500 | 2600 | 2700 | MHz |
| Gain | | 16.5 | 16.5 | 16.2 | dB |
| Input Return Loss | | 9 | 10 | 10 | dB |
| Output Return Loss | | 17 | 14 | 13 | dB |
| Output P1dB | | +25.1 | +24.9 | +25.0 | dBm |
| OIP3 | Pout= +8 dBm/tone, Δf=1 MHz | +40.2 | +40.6 | +41.3 | dBm |
| WCDMA Channel Power | -50 dBc ACLR ⁽²⁾ | +14.3 | +14.4 | +14.3 | dBm |

Notes:

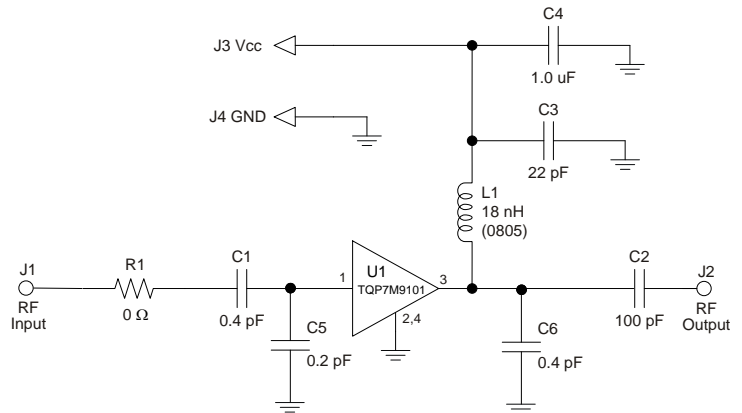
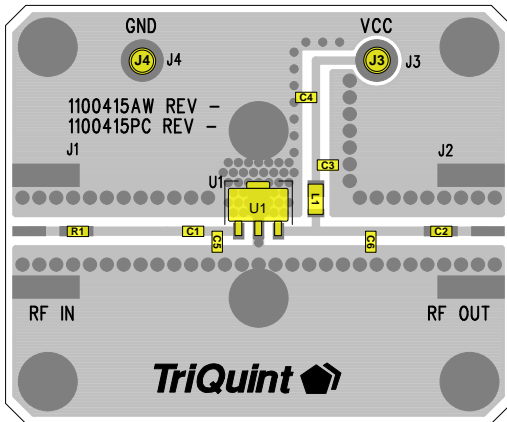
1. Test conditions unless otherwise noted: $V_{CC} = +5V$, $I_{CQ} = 87\text{ mA}$ (typ.), Temp. = +25 °C
2. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Probability

Performance Plots TQP7M9101-PCB2600

Test conditions unless otherwise noted: $V_{CC} = +5\text{ V}$, $I_{CQ} = 87\text{ mA}$ (typ.), Temp. = $+25\text{ }^{\circ}\text{C}$



3400 – 3600 MHz Reference Design



Notes:

1. See Evaluation Board PCB Information for material and stack up.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω resistors (R1) may be replaced with copper trace in the target application layout.
4. The recommended component values are dependent upon the frequency of operation.
5. All components are of 0603 size unless stated on the schematic.
6. Critical component placement locations:
 - Distance from U1 Pin 1 (left edge) to C1 (right edge): 90 mils
 - Distance from U1 Pin 1 (left edge) to C5 (right edge): 30 mils
 - Distance from U1 Pin 3 (right edge) to C6 (left edge): 300 mils

Bill of Material 3400 – 3600 MHz Reference Design

| Reference Des. | Value | Description | Manuf. | Part Number |
|----------------|--------|---|-----------|----------------|
| n/a | n/a | Printed Circuit Board | Qorvo | 1100415 |
| U1 | n/a | 0.25 W High Linearity Amplifier | Qorvo | TQP7M9101 |
| R1 | 0 Ω | RES , 0603, 5PCT. 1/16W. CHIP | various | |
| C1 , C6 | 0.4 pF | CAP, 0603, ± 0.05 pF, 50V, ACCU-P | AVX | 06035J0R4ABSTR |
| C5 | 0.2 pF | CAP, 0603, ± 0.05 pF, 50V, ACCU-P | AVX | 06035J0R2ABSTR |
| C2 | 100 pF | Cap., Chip, 0603, +/-5%. 50V NPO/COG | various | |
| C3 | 22 pF | CAP, 0603, 5%, 50V, NPO/COG | various | |
| C4 | 1.0 μF | CAP, 0603, 10%, X5R , 10V | various | |
| L1 | 18 nH | Inductor, 0805, 5%, Coilcraft CS series | Coilcraft | 0805CS-180XJLB |

Typical Performance 3400 – 3600 MHz Reference Design

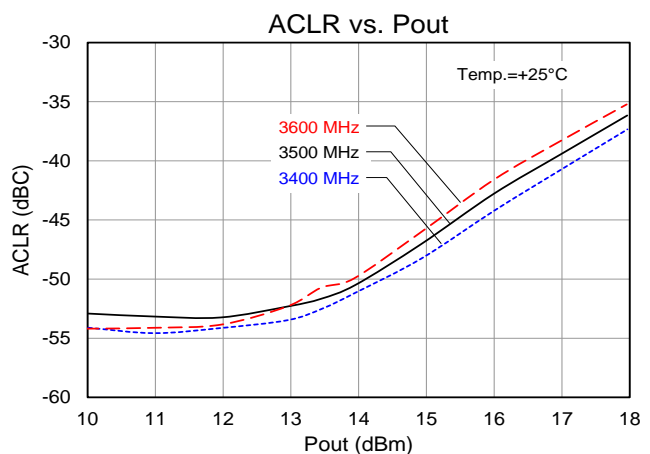
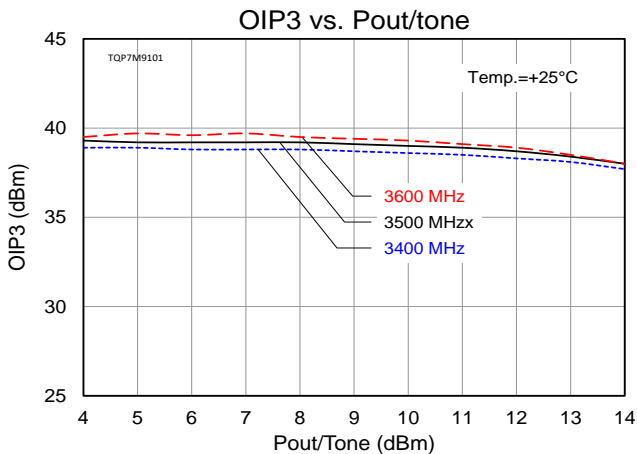
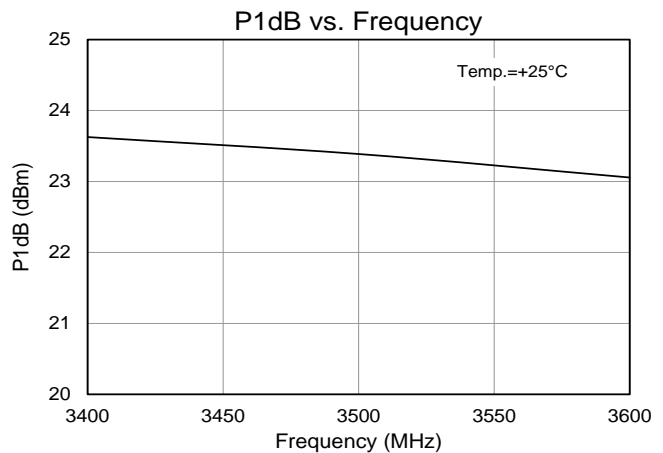
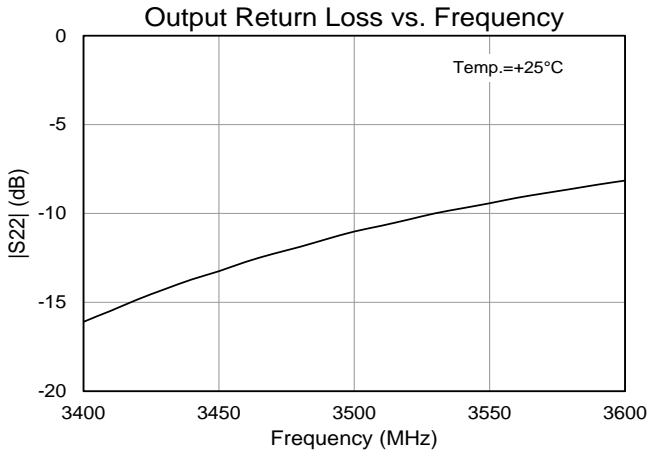
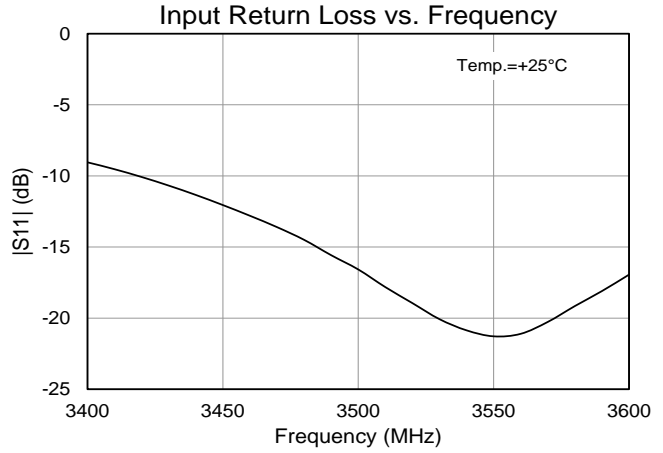
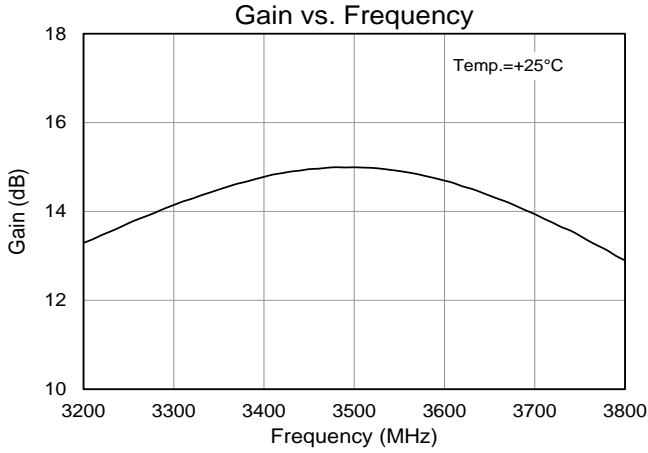
| Parameter | Conditions ⁽¹⁾ | Typical Value | | | Units |
|---------------------|-----------------------------|---------------|-------|-------|-------|
| | | 3400 | 3500 | 3600 | |
| Frequency | | 3400 | 3500 | 3600 | MHz |
| Gain | | 14.8 | 15.0 | 14.7 | dB |
| Input Return Loss | | 9 | 17 | 17 | dB |
| Output Return Loss | | 16 | 11 | 7.5 | dB |
| Output P1dB | | +23.7 | +23.4 | +23.1 | dBm |
| OIP3 | Pout= +8 dBm/tone, Δf=1 MHz | +39.5 | +39.4 | +38.8 | dBm |
| WCDMA Channel Power | -50 dBc ACLR ⁽²⁾ | +14.4 | +14.1 | +13.9 | dBm |

Notes:

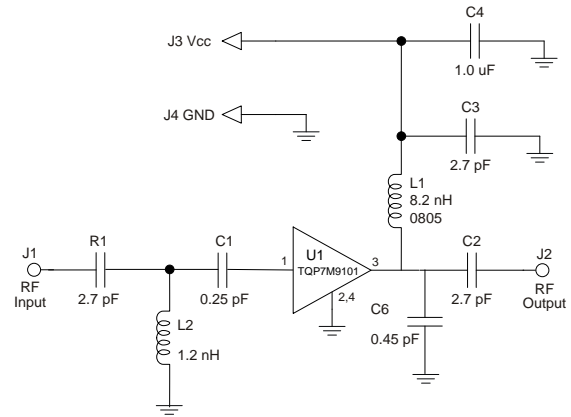
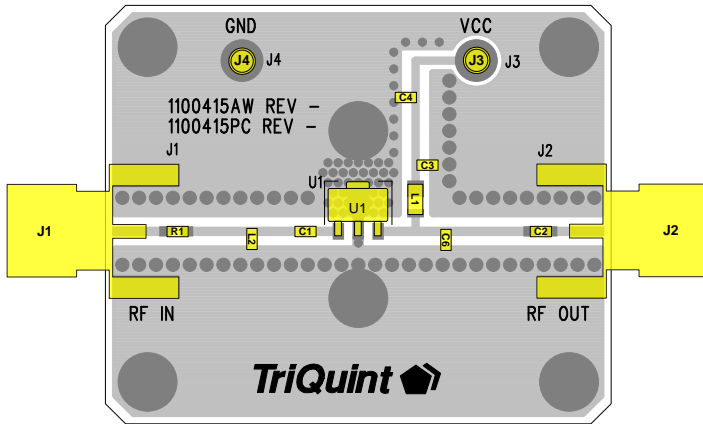
1. Test conditions unless otherwise noted: V_{CC} = +5 V, I_{CC} = 87 mA (typ.), Temp. = +25 °C
2. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Probability

Performance Plots 3400 – 3600 MHz Reference Design

Test conditions unless otherwise noted: $V_{CC} = +5\text{ V}$, $I_{CQ} = 87\text{ mA}$ (typ.), Temp. = $+25\text{ }^{\circ}\text{C}$



4.4 – 5.0 GHz Reference Design



Notes:

1. Components shown on the silkscreen but not on the schematic are not used.
2. 0 Ω resistor can be replaced with copper trace in the target application layout.
3. All components are of 0603 size unless stated on the schematic.
4. The recommended component values are dependent upon the frequency of operation.
5. Critical component placement locations:
 - Distance between U1 Pin 1 Pad (left edge) to C1 (right edge): 10 mils
 - Distance between U1 Pin 1 Pad (left edge) to L2 (right edge): 280 mils
 - Distance between U1 Pin 3 Pad (right edge) to C6 (left edge): 110 mils

Bill of Material 4.4 – 5.0 GHz Reference Design

| Reference Des. | Value | Description | Manuf. | Part Number |
|----------------|---------|---|-----------|----------------|
| n/a | n/a | Printed Circuit Board | Qorvo | |
| U1 | n/a | 0.25 W High Linearity Amplifier | Qorvo | TQP7M9101 |
| C1 | 0.25 pF | CAP, 0402, ± 0.02 pF, 50V, ACCU-P | AVX | 04021JR25PBS |
| C6 | 0.45 pF | CAP, 0603, ± 0.02 pF, 50V, ACCU-P | AVX | 06035JR45PBS |
| L2 | 1.2 nH | Inductor, 0603, chip | various | |
| C2, C3, R1 | 2.7 pF | CAP, 0603, ± 0.1 pF, 50V, NPO/COG | various | |
| C4 | 1.0 μF | CAP, 0603, 10%, X5R , 10V | various | |
| L1 | 8.2 nH | Inductor, 0805, 5%, Coilcraft CS series | Coilcraft | 0805CS-8N2XJLB |

Typical Performance 4.4 – 5.0 GHz Reference Design

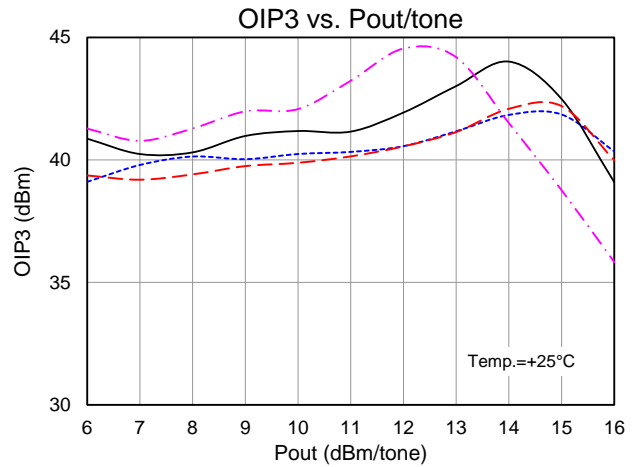
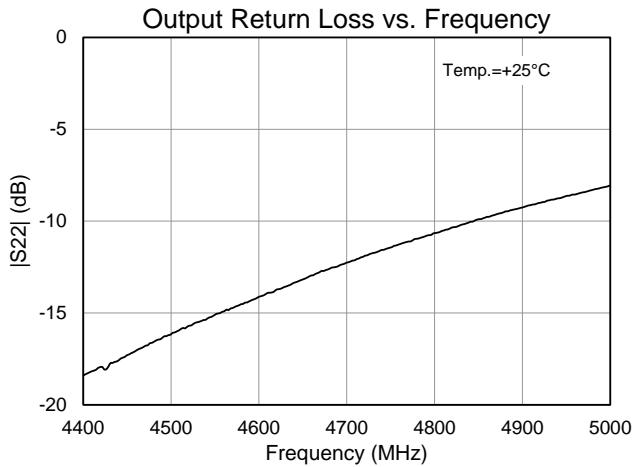
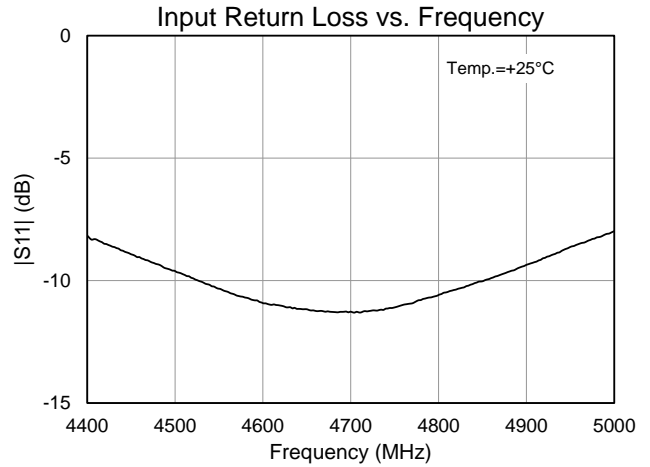
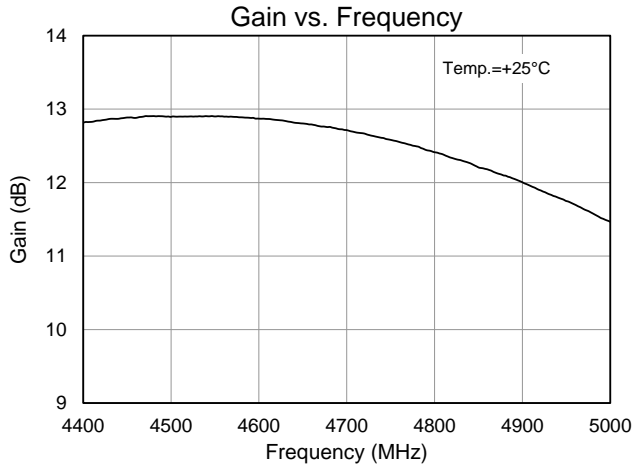
| Parameter | Conditions ⁽¹⁾ | Typical Value | | | | Units |
|--|------------------------------|---------------|-------|-------|-------|-------|
| | | 4400 | 4600 | 4800 | 5000 | |
| Frequency | | 4400 | 4600 | 4800 | 5000 | MHz |
| Gain | | 12.8 | 12.9 | 12.4 | 11.5 | dB |
| Input Return Loss | | 8.3 | 10.9 | 10.6 | 8.0 | dB |
| Output Return Loss | | 18 | 14 | 11 | 8.1 | dB |
| Output P1dB | | +23.9 | +23.5 | +23.9 | +23.1 | dBm |
| Output IP3 | Pout= +8 dBm/tone, Δf= 1 MHz | +40.1 | +40.3 | +39.4 | +41.3 | dBm |
| Quiescent Collector Current, I _{CC} | | 86 | | | | mA |

Notes:

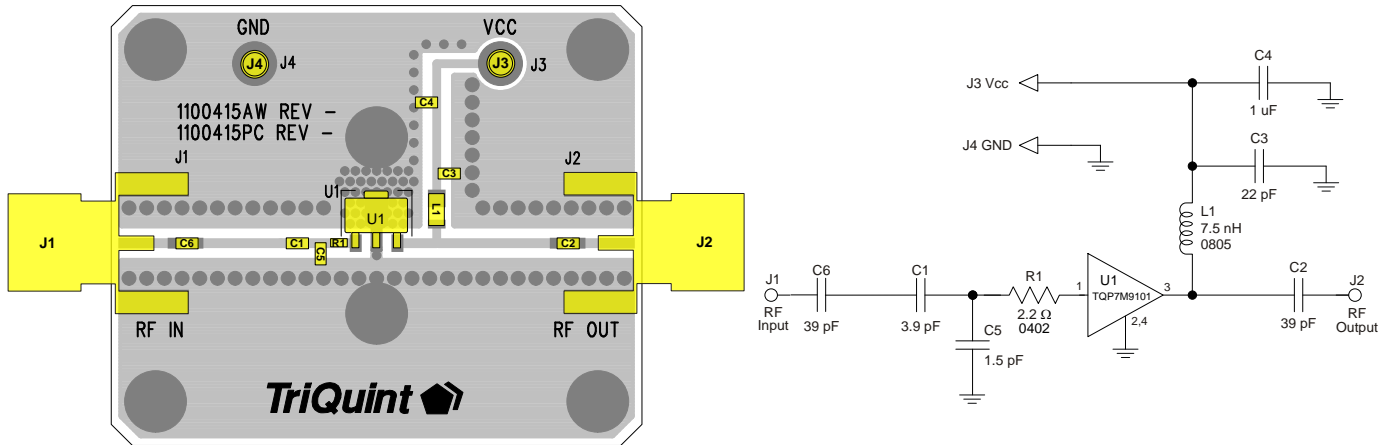
1. Test Conditions: V_{CC}=+5V, Temp.=+25 °C, 50 Ω System

Performance Plots 4.4 – 5.0 GHz Reference Design

Test conditions unless otherwise noted: $V_{CC} = +5\text{ V}$, $I_{CQ} = 87\text{ mA}$ (typ.), Temp. = $+25^\circ\text{C}$



1800 – 2200 MHz Reference Design Optimized for OIP3



Notes:

- 6. All components are of 0603 size unless stated on the schematic.
- 7. The recommended component values are dependent upon the frequency of operation.
- 8. Critical component placement locations:
 - Distance between U1 Pin 1 Pad to R1 (right edge): 10 mil
 - Distance between U1 Pin 1 Pad to C5 (right edge): 45 mil
 - Distance between U1 Pin 3 Pad to C1 (right edge): 90 mil

Bill of Material 1800 – 2200 MHz Reference Design

| Reference Des. | Value | Description | Manuf. | Part Number |
|----------------|--------|---|-----------|----------------|
| n/a | n/a | Printed Circuit Board | Qorvo | |
| U1 | n/a | 0.25 W High Linearity Amplifier | Qorvo | TQP7M9101 |
| C1 | 3.9 pF | CAP, 0603, +/-0.1pF. 200V. NPO/COG | various | |
| C5 | 1.5 pF | CAP, 0603, +/-0.1pF. 200V. NPO/COG | various | |
| C2, C6 | 39 pF | Cap., Chip, 0603, +/-5%. 50V NPO/COG | various | |
| C3 | 22 pF | Cap., Chip, 0603, +/-5%. 50V NPO/COG | various | |
| R1 | 2.2 Ω | Res., Chip, 0603, +/-1%, 1/10W | various | |
| C4 | 1.0 μF | CAP, 0603, 10%, X5R , 10V | various | |
| L1 | 7.5 nH | Inductor, 0805, 5%, Coilcraft CS series | Coilcraft | 0805CS-7N5XJLB |

Typical Performance 1800 – 2200 MHz Reference Design

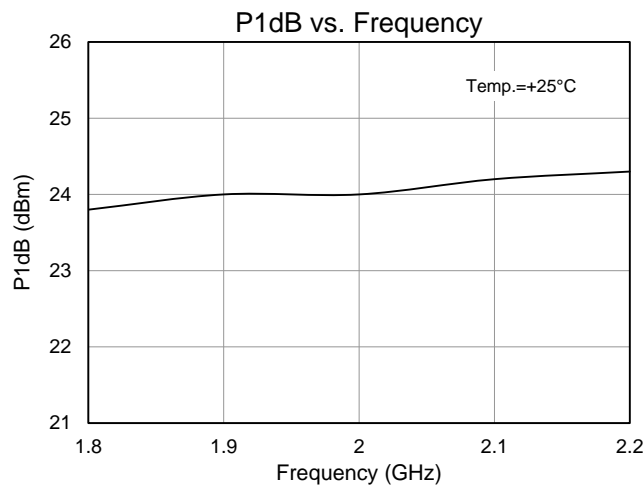
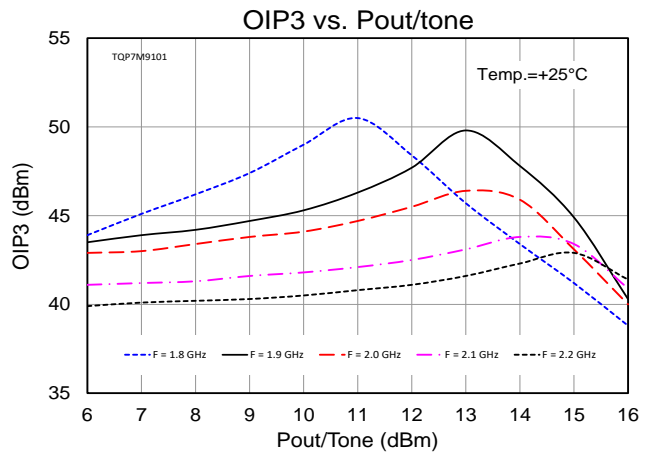
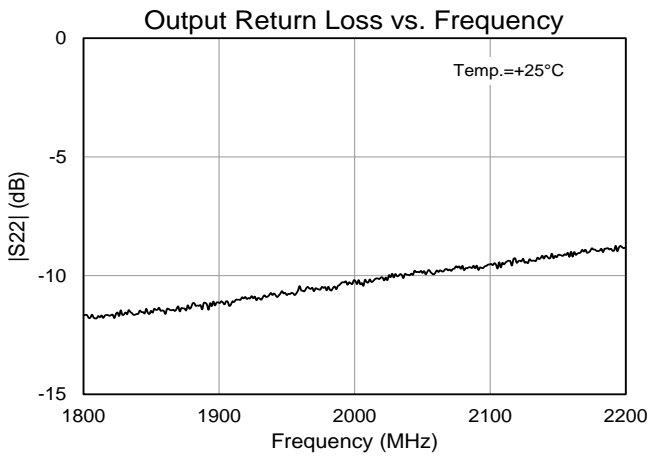
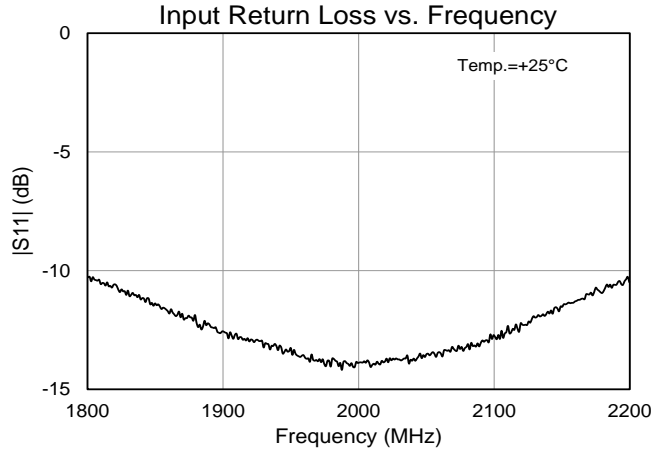
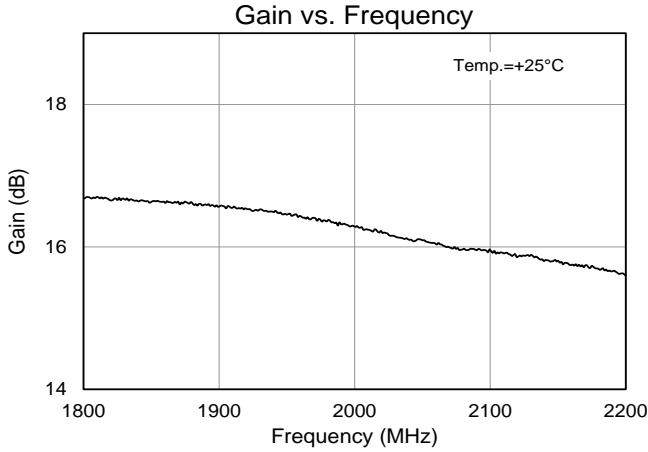
| Parameter | Conditions | Typical Value | | | | | Units |
|--|-------------------------------|---------------|-------|-------|-------|-------|-------|
| | | 1800 | 1900 | 2000 | 2100 | 2200 | |
| Frequency | | 1800 | 1900 | 2000 | 2100 | 2200 | MHz |
| Gain | | 16.7 | 16.6 | 16.3 | 15.9 | 15.6 | dB |
| Input Return Loss | | 10 | 12 | 13 | 12 | 10 | dB |
| Output Return Loss | | 11 | 11 | 10 | 9.5 | 8.5 | dB |
| Output P1dB | | +23.8 | +24.0 | +24.0 | +24.2 | +24.3 | dBm |
| Output IP3 | Pout= +14 dBm/tone, Δf= 1 MHz | +43.4 | +47.8 | +45.9 | +43.8 | +42.3 | dBm |
| Quiescent Collector Current, I _{CQ} | | 87 | | | | | mA |

Notes:

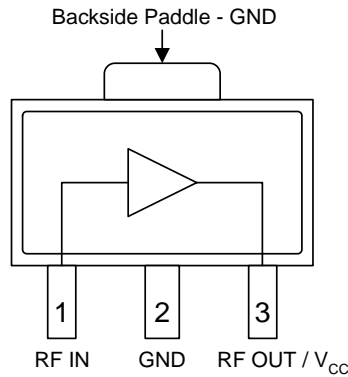
- 1. Test Conditions: V_{CC}=+5 V, Temp.=+25 °C, 50 Ω System

Performance Plots 1800 – 2200 MHz Reference Design

Test conditions unless otherwise noted: $V_{CC} = +5\text{ V}$, $I_{CQ} = 87\text{ mA}$ (typ.), Temp. = $+25\text{ }^{\circ}\text{C}$



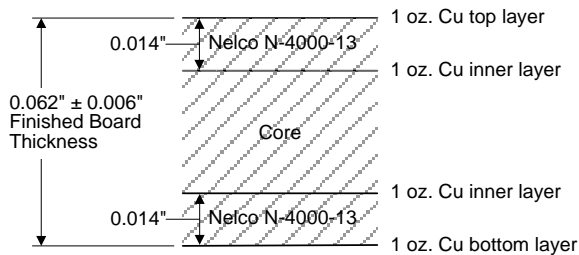
Pin Configuration and Description



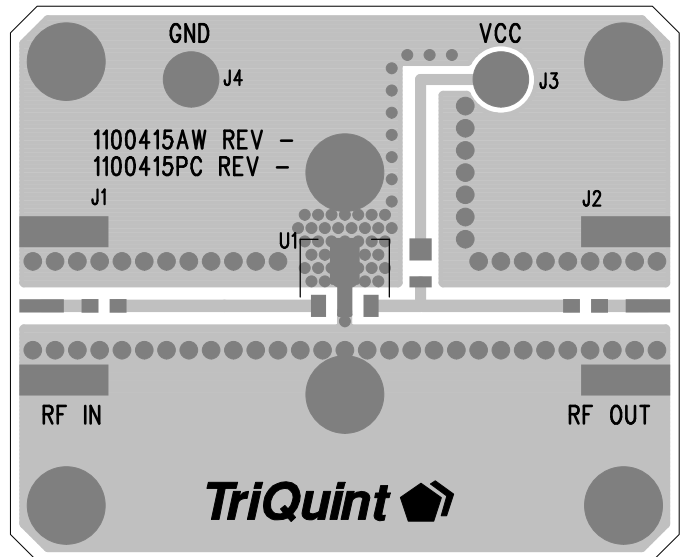
| Pin No. | Label | Description |
|--------------------|--------------------------|---|
| 1 | RF IN | RF Input. External DC Block required. Requires conjugate match for optimal performance. |
| 2, Backside Paddle | GND | RF/DC ground. Use recommended via hole pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint. |
| 3 | RF OUT / V _{CC} | RF Output, matched to 50 Ω. External DC Block, RF choke and bias voltage required. |

Evaluation Board PCB Information

Qorvo PCB 1100415 Material and Stack-up



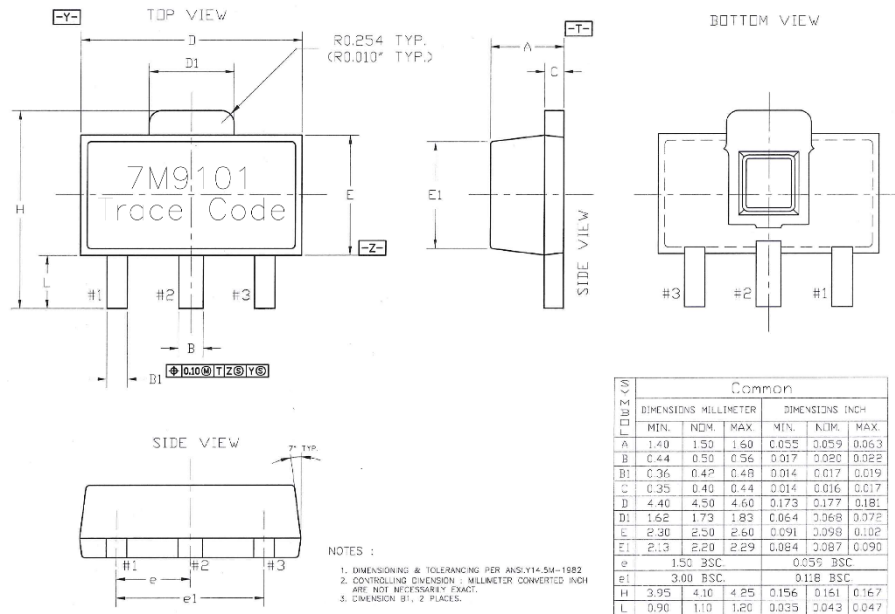
50 ohm line dimensions: width = .031"
spacing = .035".



Package Marking and Dimensions

Package Marking

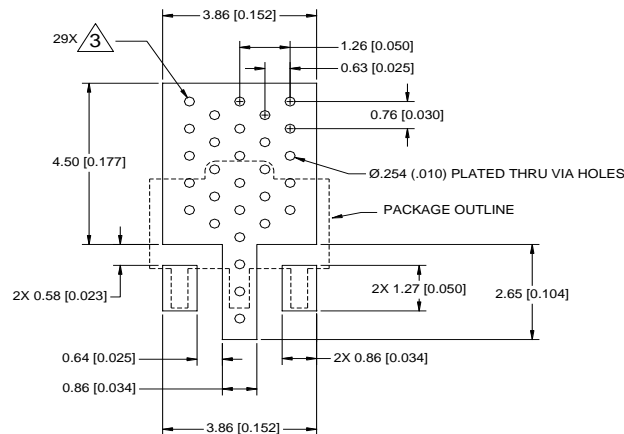
Product ID: 7M9101
 Trace code: XXXX



Notes:

1. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
2. Trace code up to 4 characters to be assigned by sub-contractor.

PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters [inches]. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal conductivity.
4. Do not remove or minimize via hole structure in the PCB. Thermal and RF grounding is critical.
5. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.010").
6. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Tape and Reel Information – Carrier and Cover Tape Dimensions



| Feature | Measure | Symbol | Size (in) | Size (mm) |
|---------------------|--|--------|-----------|-----------|
| Cavity | Length | A0 | 0.181 | 4.60 |
| | Width | B0 | 0.193 | 4.90 |
| | Depth | K0 | 0.075 | 1.90 |
| | Pitch | P1 | 0.315 | 8.00 |
| Centerline Distance | Cavity to Perforation - Length Direction | P2 | 0.079 | 2.00 |
| | Cavity to Perforation - Width Direction | F | 0.217 | 5.50 |
| Cover Tape | Width | C | 0.362 | 9.20 |
| Carrier Tape | Width | W | 0.472 | 12.0 |

Tape and Reel Information – Reel Dimensions (7")

Standard T/R size = 1,000 pieces on a 7" reel.



| Feature | Measure | Symbol | Size (in) | Size (mm) |
|---------|----------------------|--------|-----------|-----------|
| Flange | Diameter | A | 6.969 | 177.0 |
| | Thickness | W2 | 0.717 | 18.2 |
| | Space Between Flange | W1 | 0.504 | 12.8 |
| Hub | Outer Diameter | N | 2.283 | 58.0 |
| | Arbor Hole Diameter | C | 0.512 | 13.0 |
| | Key Slit Width | B | 0.079 | 2.0 |
| | Key Slit Diameter | D | 0.787 | 20.0 |

Tape and Reel Information – Tape Length and Label Placement



- Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
 2. Labels are placed on the flange opposite the sprockets in the carrier tape.