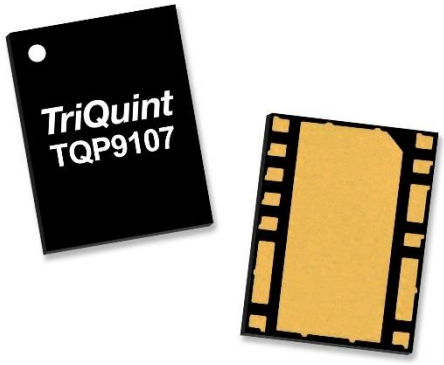
TQP9107

600 – 960 MHz 2-stage Power Amplifier

General Description

The TQP9107 is a high-efficiency two-stage power amplifier in a low-cost surface-mount package. The amplifier is able to achieve 31% power added efficiency at +27 dBm output power while operating with a low 84 mA idle current. The amplifier is designed to ensure that all odd-order IMD products are below −17 dBm at all output power levels below +24 dBm/tone.

The TQP9107 integrates two high performance amplifier stages onto a module to allow for a compact system design and requires very few external components for operation. The amplifier is bias adjustable allowing the amplifier's power consumption to be optimized. The TQP9107 is available in a lead-free/RoHS-compliant 13-pin 3.5 x 4.5mm surface mount package and is pin-compatible to the higher frequency band version in the family with the TQP9108 (1.70-2.17 GHz).

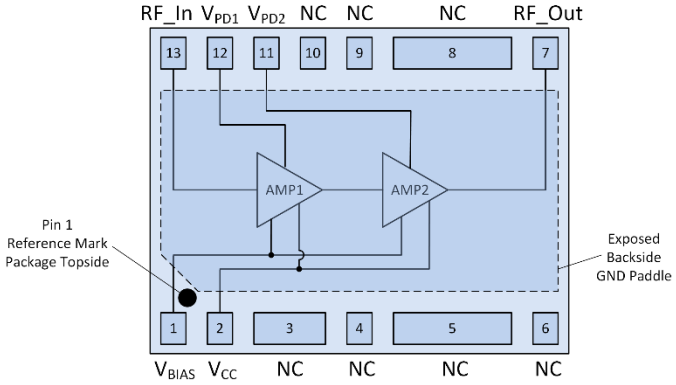


3.5 x 4.5 mm Leadless SMT Package

Product Features

- 600 – 960 MHz Frequency Range
- 35.5 dB gain
- +46 dBm Output IP3 at Pout = +24 dBm/tone
- 31% PAE at +27 dBm Pout
- Internally Matched
- Integrated Inter-Stage Matching
- Bias Adjustable
- Low idle current

Functional Block Diagram



Top View

Applications

- Wireless Infrastructure
- Repeaters, Boosters, DAS
- High Power Amplifiers
- Small cell BTS

Ordering Information

Part No.	Description
TQP9107	699 − 960 MHz Power Amplifier
TQP9107-PCB	Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−55 to +150 °C
RF Input Power, CW, 50 Ω, T=25 °C	+7 dBm
Supply Voltage (V_{CC})	+6 V

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{CC}		+4.3	+5.0	V
V_{BIAS}		+3.9	V_{CC}	V
V_{PD1}, V_{PD2}		+4.0	V_{CC}	V
T_{CASE}	−40		+105	°C
Tj for >10^6 hours MTTF			+170	°C

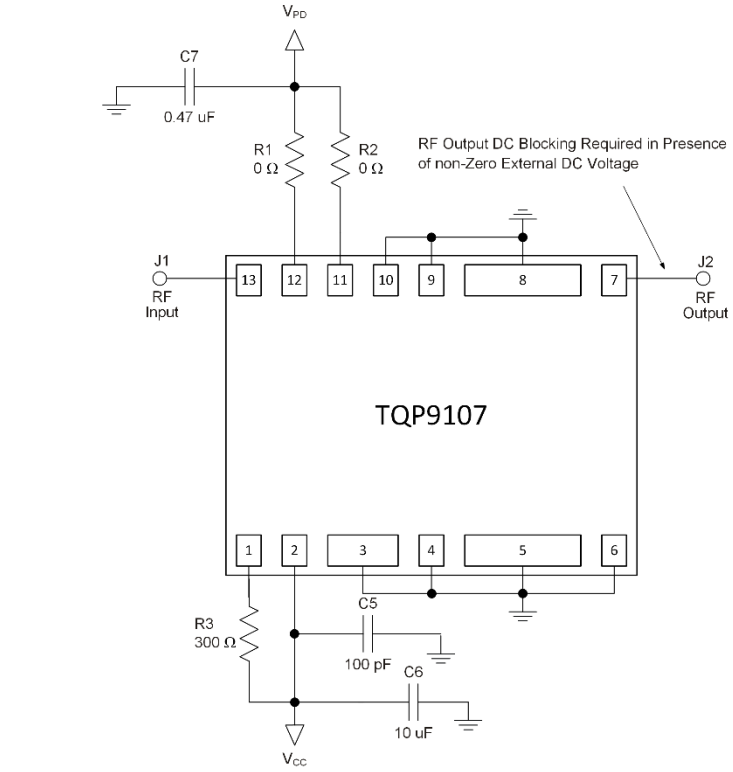
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

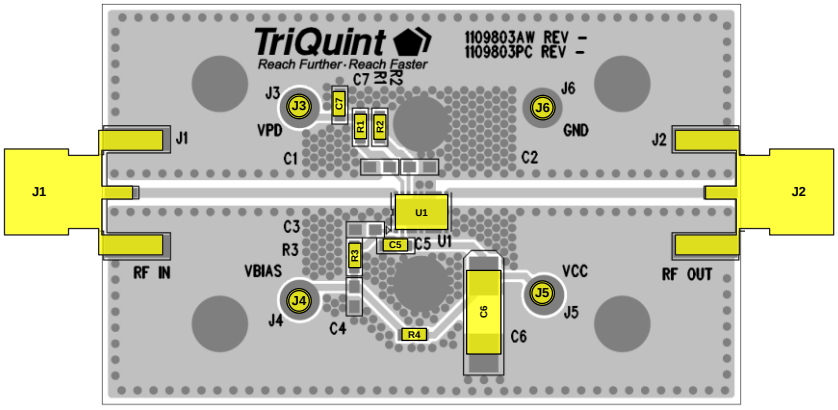
Electrical Specifications

Parameter	Conditions[1]	Min	Typ	Max	Units
Operational Frequency Range		600		960	MHz
Test Frequency			849		MHz
Gain		28.8	35.5		dB
Noise Figure			5		dB
Output P1dB			30.5		dBm
Output IP3	Pout = +23 dBm/tone, Δf = 600 kHz	+43	+46		dBm
IMD3, IMD5, IMD7	All power levels ≤ 23 dBm / tone			−17	dBm
Current, I_{CC}	Pout = +27 dBm		370		mA
Power Added Efficiency	Pout = +27 dBm		31		%
Idle Current	No RF Input Power		84		mA
VSWR Survivability	Pout = P1dB, Signal: CW All Phases		10:1		–
	Pout = +28 dBm, All Phases Signal: 20 MHz LTE 1C, PAR = 9.5 dB		6:1		–
Thermal Resistance, θ_{jc}	Junction to backside GND paddle		30.1		°C/W

Notes:
1. Test conditions unless otherwise noted: V_{CC} = +4.3 V, V_{PD1} = V_{PD2} = +4.0 V, Temp = +25 °C, 50 Ω system.

Application Circuit Schematic and Layout – TQP9107-PCB : 700 MHz to 960 MHz





Bill of Material – TQP9107-PCB : 700 MHz to 960 MHz

Reference Des.	Value	Description	Manuf.	Part Number
n/a		PCB, Nelco FR4, APP BOARD	Qorvo	1109803PC
U1		AMP, 2-Stage Power Amplifier	Qorvo	TQP9107
C5	100 pF	CAP, 0603, 5%, 50V, NPO	various	
C6	10 µF	CAP, 6032, 20%, 50V, Tantalum	various	
C7	0.47 µF	CAP, 0603, 50V, X7R, 5%	various	
R1, R2, R4	0 Ω	RES, 0603, 5%, 1/16W, Chip	various	
R3	300 Ω	RES, 0603, 5%, 1/16W, Chip	various	

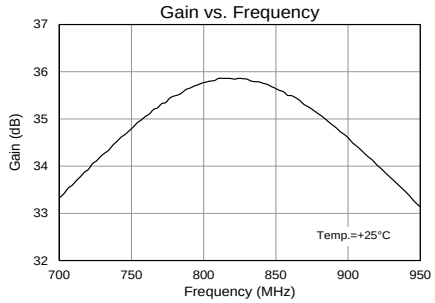
Typical Performance – TQP9107-PCB : 700 MHz to 960 MHz

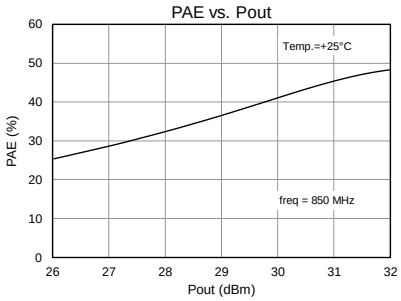
Parameter	Conditions[1]	Typical Value				Units
Frequency		760	820	850	920	MHz
Gain		35.0	35.8	35.7	34.1	dB
IM3	Pout= +27 dBm, Δf= 600 KHz	-30	-27	-24	-17	dBm
IM5	Pout= +27 dBm, Δf= 600 KHz	-22	-21	-20	-21	dBm
Quiescent Collector Current, I_{CQ}	V_{PD} = +4 V	84				mA

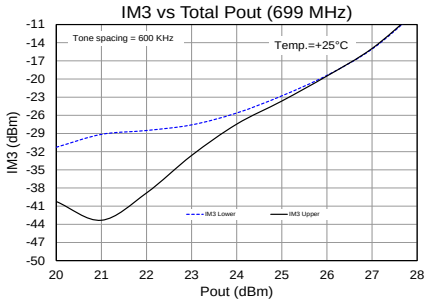
Notes:
1. Test conditions unless otherwise noted: V_{CC} = +4.3 V, V_{PD1}= V_{PD2} = +4.0V, Temp.=+25 °C

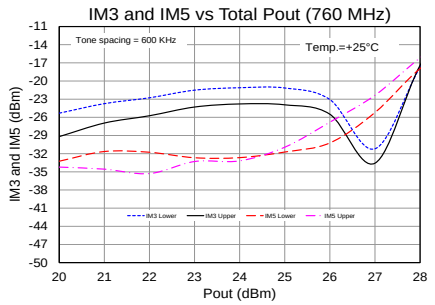
Performance Plots – TQP9107-PCB : 700 MHz to 960 MHz

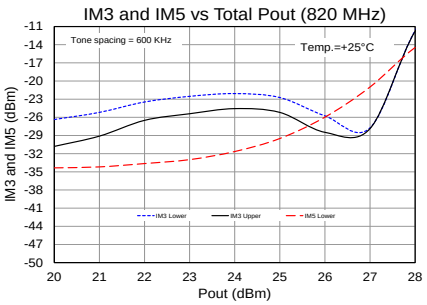
Test conditions unless otherwise noted: V_{CC} = +4.3 V, V_{PD1}= V_{PD2} = +4.0V, Temp.=+25 °C

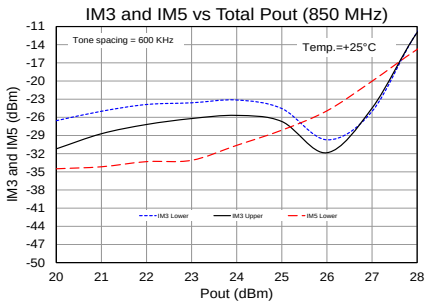


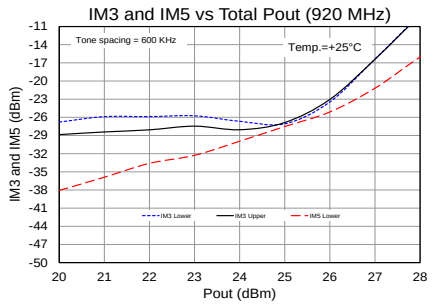


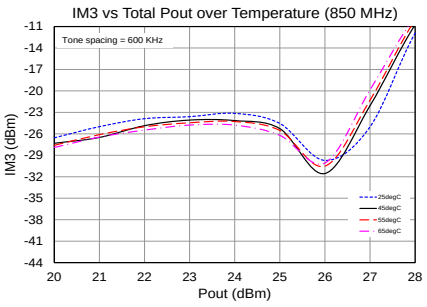


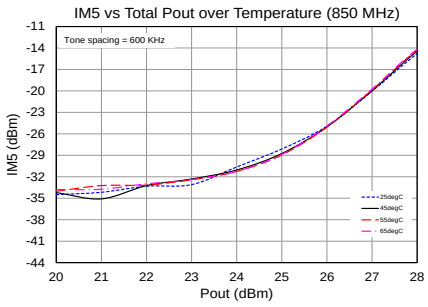


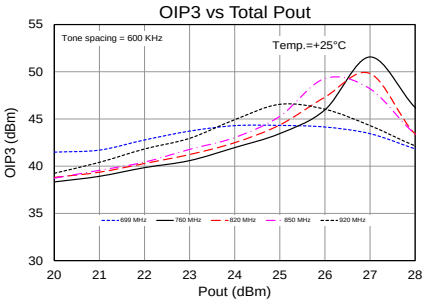












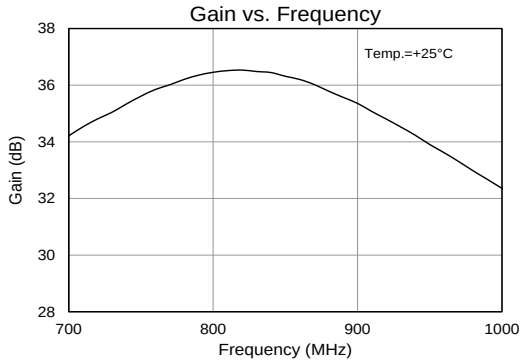
Typical Performance – V_{CC} +5.0 V & V_{PD} +4.3 V

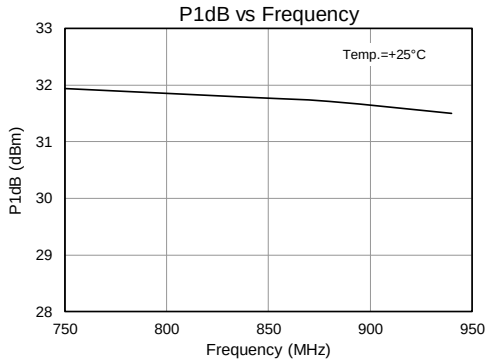
Parameter	Conditions[1]	Typical Value				Units
Frequency		750	840	880	940	MHz
Gain		35.5	36.2	35.8	34.0	dB
Input Return Loss		-13	-9	-9	-10	dB
Output P1dB		+31.9	+31.7	+31.6	+31.5	dBm
Output IP3	Pout= +24 dBm, Δf= 1 MHz	+42.1	+43.5	+44.0	+46.2	dBm
Quiescent Collector Current, I_{CQ}	V_{PD} = +4.3 V	108				mA

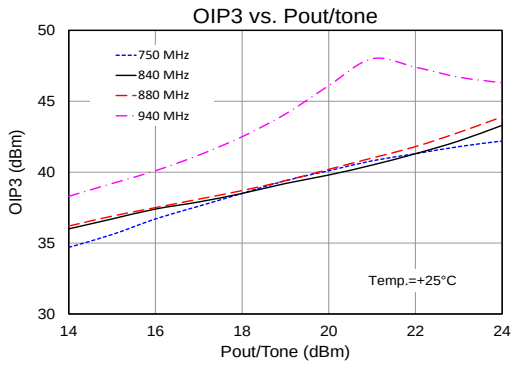
Notes:
1. Test conditions unless otherwise noted: V_{CC} = +5.0 V, V_{PD1}= V_{PD2} = +4.3V, Temp.=+25 °C

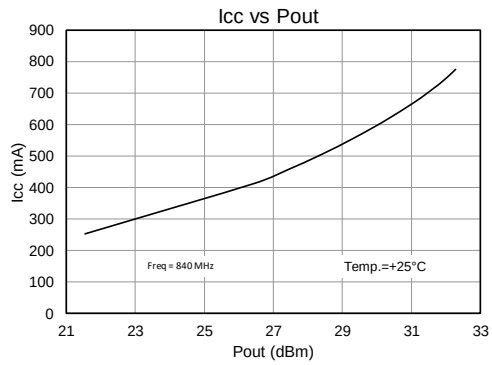
Performance Plots – VCC +5.0 V & V_{PD} +4.3 V

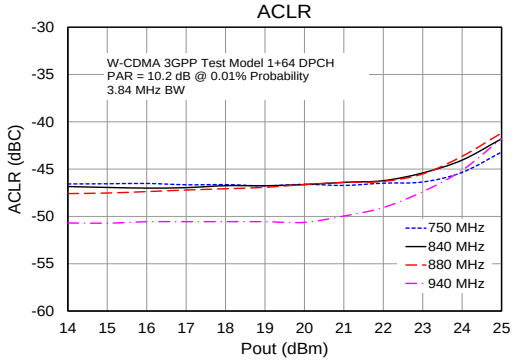
Test conditions unless otherwise noted: V_{CC} = +5.0 V, V_{PD1}= V_{PD2} = +4.3V, Temp.=+25 °C



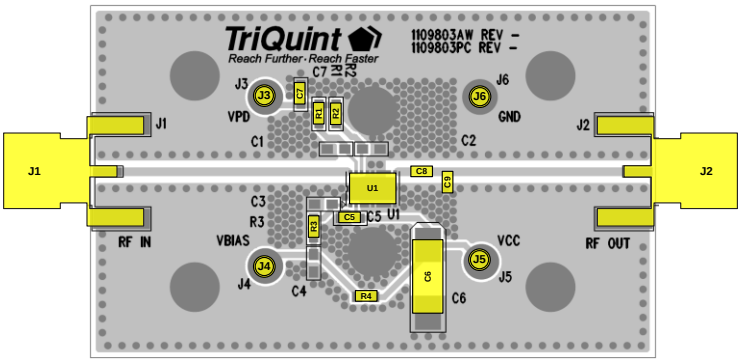


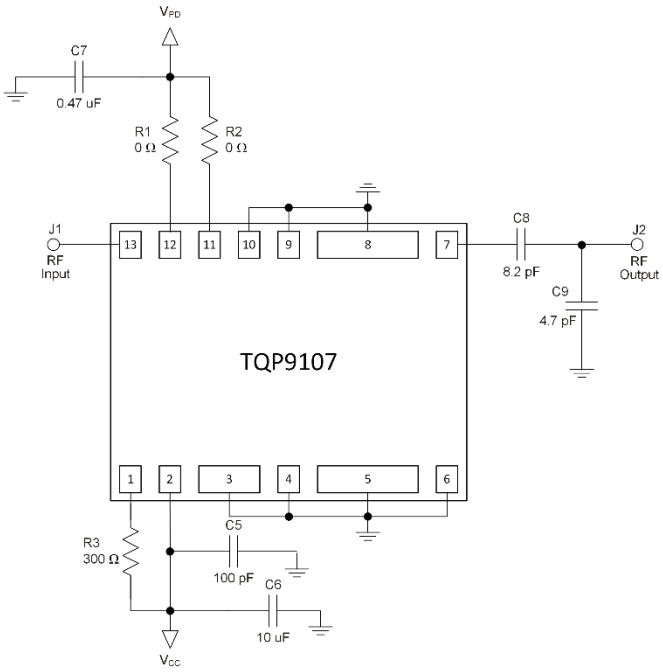






Evaluation Board and Schematic – 600 to 650 MHz





Notes:

1. All components are of 0603 size unless stated on the schematic.
2. The recommended component values are dependent upon the frequency of operation.
3. Critical component placement locations:
    - Distance between U1 (right edge) to C8 (left edge): 60 mil
    - Distance between U1 (right edge) to C9 (left edge): 160 mil

Bill of Material – 600 to 650MHz

Reference Des.	Value	Description	Manuf.	Part Number
n/a		PCB, Nelco FR4, APP BOARD	Qorvo	1109803PC
U1		AMP, 2-Stage Power Amplifier	Qorvo	TQP9107
C5	100 pF	CAP, 0603, 5%, 50V, NPO	various	
C6	10 µF	CAP, 6032, 20%, 50V, Tantalum	various	
C7	0.47 µF	CAP, 0603, 50V, X7R, 5%	various	
R1, R2, R4	0 Ω	RES, 0603, 5%, 1/16W, Chip	various	
R3	300 Ω	RES, 0603, 5%, 1/16W, Chip	various	
C8	8.2 pF	CAP, +/-0.1pF, 0603, 50V, COG	various	
C9	4.7 pF	CAP, +/-0.1pF, 0603, 50V, COG	various	

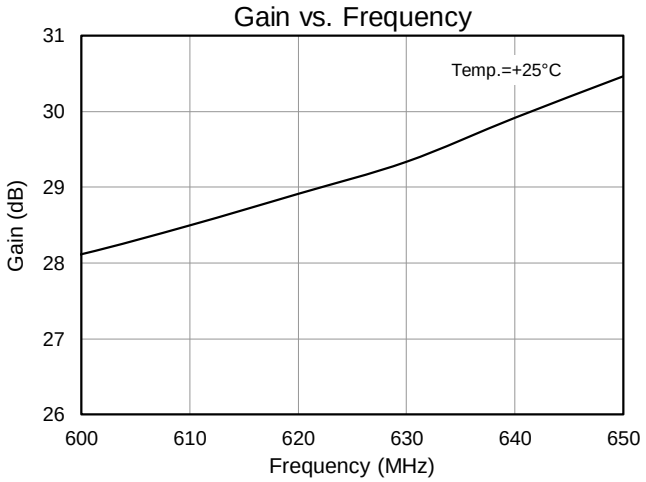
Typical Performance – 600 to 650 MHz, V_{CC} +5 V & V_{PD} +4.3 V

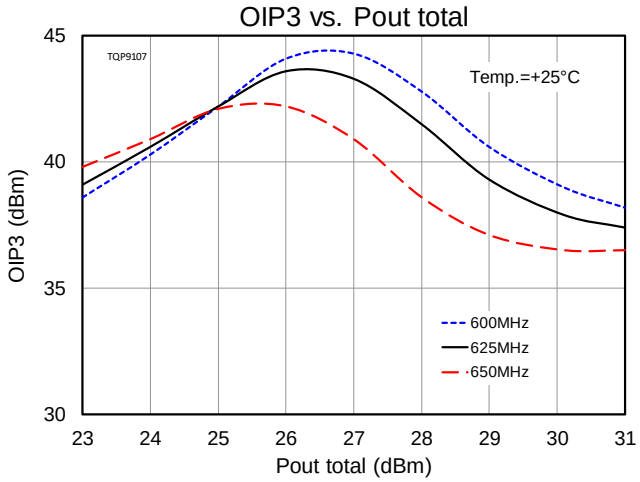
Parameter	Conditions	Typical Value			Units
Frequency		600	625	650	MHz
Gain		28.1	29.1	30.5	dB
Output P1dB		+31.7	+31.3	+30.6	dBm
Output IP3	Pout total = +26 dBm, Δf= 1 MHz	+44.1	+43.6	+42.2	dBm
Quiescent Collector Current, I_{CQ}		86			mA

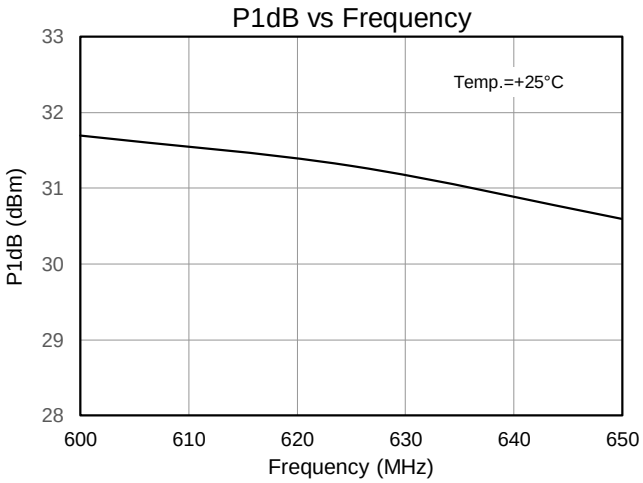
Notes:
1. Test Conditions: V_{CC}=+5.0 V, V_{PD} = +4.3V, Temp.=+25°C, 50Ω System

Performance Plot – 600 to 650 MHz, V_{CC} +5 V & V_{PD} +4.3 V

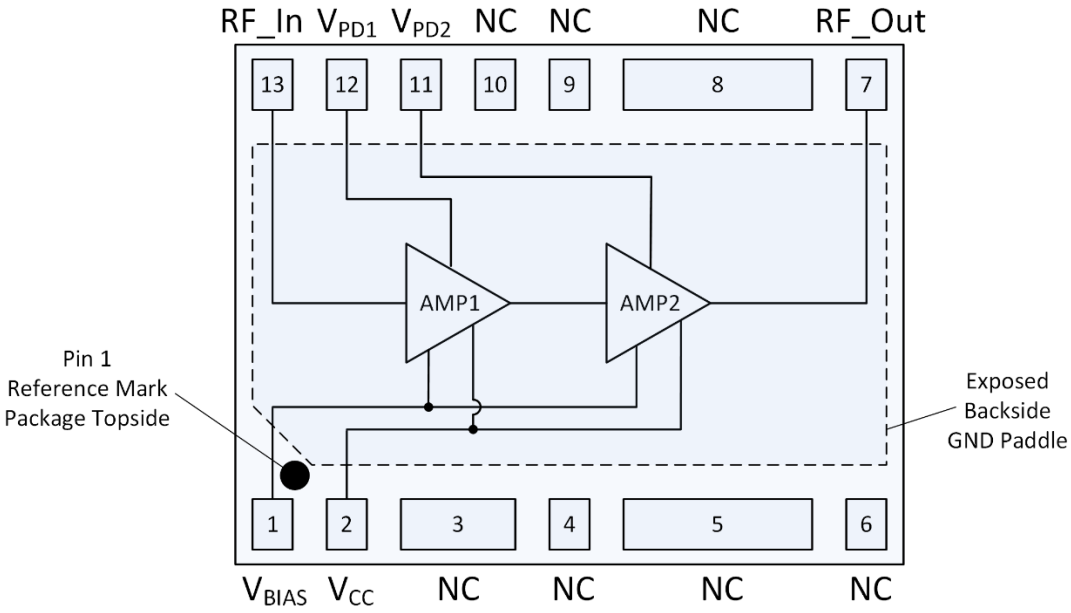
Test Conditions: V_{CC}=+5.0 V, V_{PD} = +4.3V, Temp.=+25°C, 50Ω System







Pin Configuration and Description

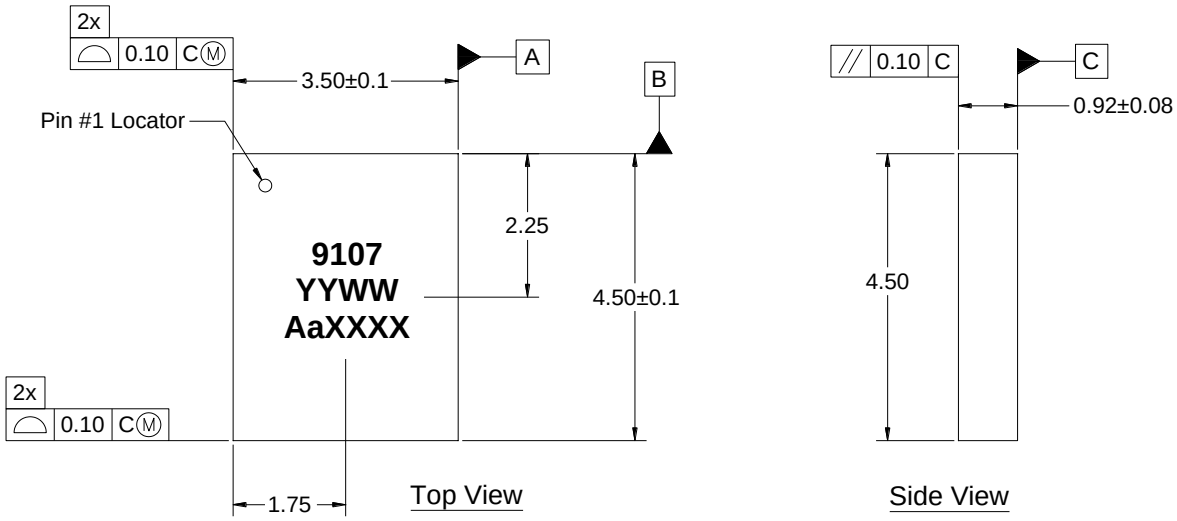


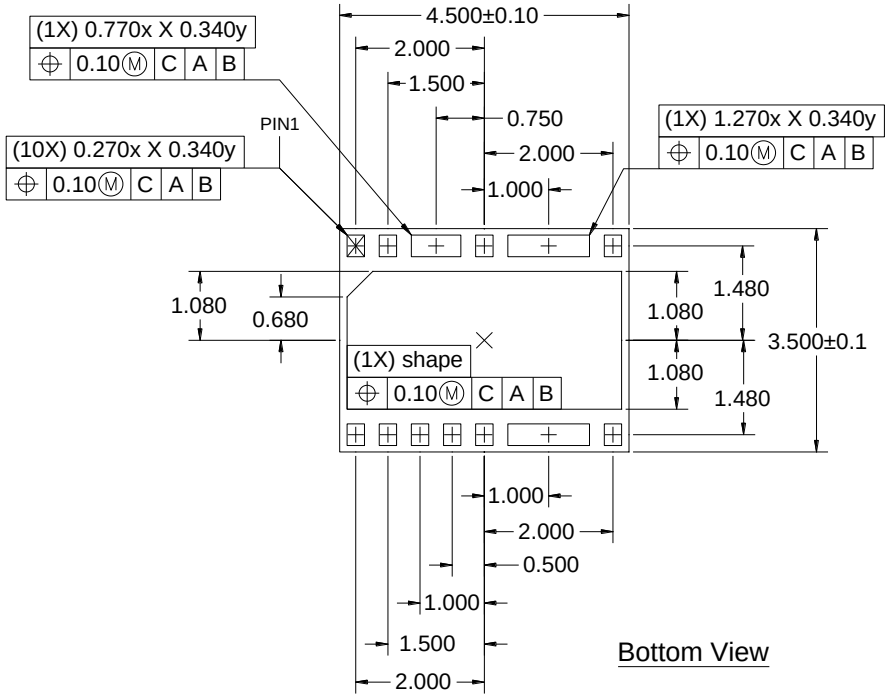
Top View

Pad No.	Label	Description
1	V_{BIAS}	DC voltage supply input for active biasing circuit
2	V_{CC}	DC voltage supply input for AMP1 and AMP2
3, 4, 5, 6, 8, 9, 10	NC	No internal connection, grounded land pads for PCB mounting integrity
7	RF_Out	RF output, DC blocking required in the presence of external non-zero DC Voltage
11	V_{PD2}	DC voltage input, AMP2 quiescent current reference, 0 Volt AMP2 power down
12	V_{PD1}	DC voltage input, AMP1 quiescent current reference, 0 Volt AMP1 power down
13	RF_In	RF input, Internally DC blocked
Backside Pad	GND	RF/DC ground. Use recommended via hole pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Package Marking and Dimensions

Marking: Part Number – TQP9107
Date – YYWW
Lot Code - AaXXXX

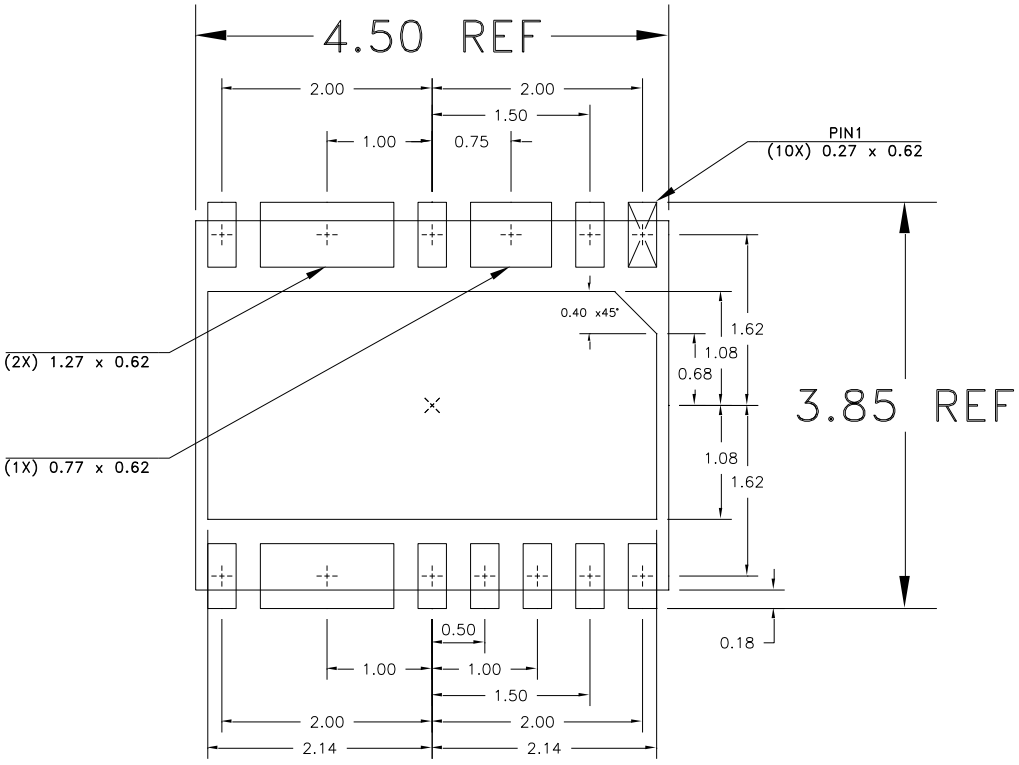




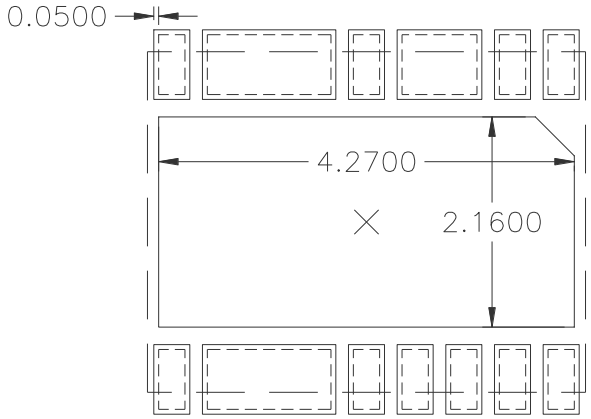
Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Contact plating: Au over Ni

PCB Mounting Pattern

Recommend PCB land-pad pattern metallization (Top View)



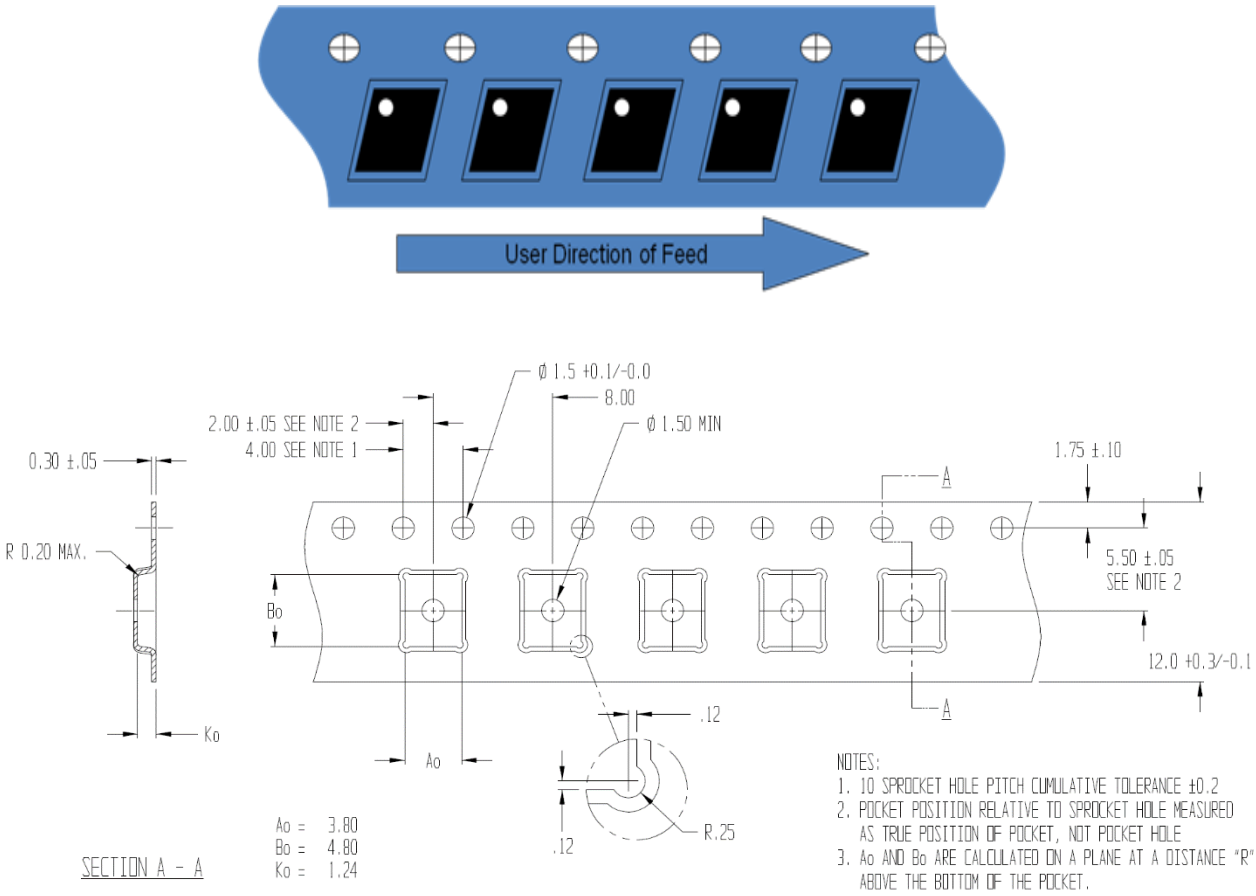
Recommended PCB solder mask opening (Top View)



Notes:

1. A heat sink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal via holes are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135”) diameter drill and have a final plated thru diameter of .25 mm (.010”).
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

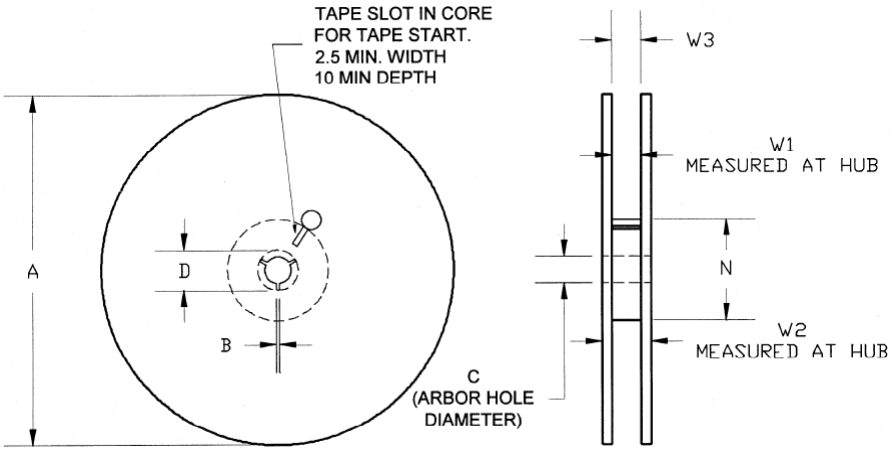
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.150	3.80
	Width	B0	0.199	4.80
	Depth	K0	0.049	1.24
	Pitch	P1	0.315	8.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.00

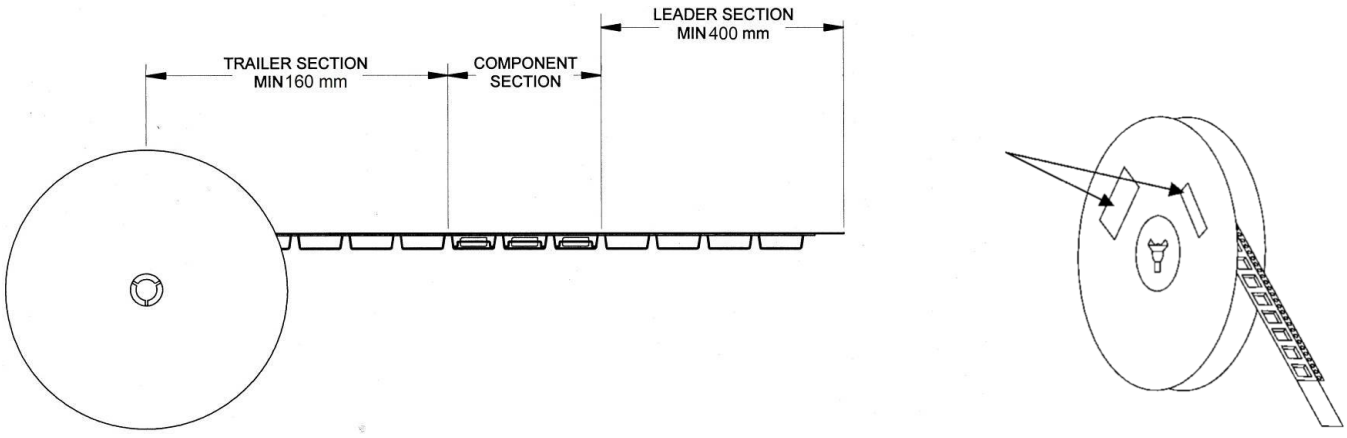
Tape and Reel Information – Reel Dimensions (13”)

Standard T/R size = 2,500 pieces on a 13” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.