TQP9218

High Linearity 0.25 W Small Cell PA

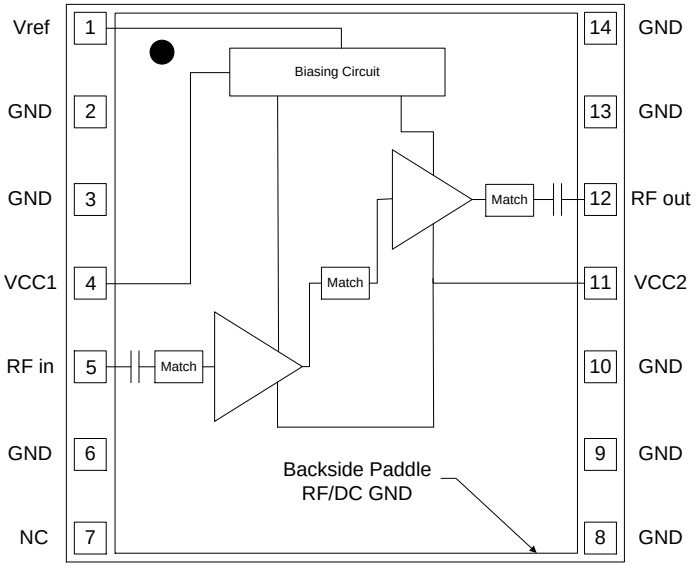
General Description

The TQP9218 is a high-linearity two-stage power amplifier in a low-cost surface-mount package with on-chip bias control and temperature compensation circuits. The amplifier provides 31.5 dB gain over the 1805 – 1880 MHz frequency range and be utilized without the need of linearization circuitry such as DPD It is able to achieve −48 dBc ACLR at +24 dBm output power using 20 MHz LTE signal (9.5 dB PAR).

The TQP9218 integrates two high performance amplifier stages onto a module to allow for a compact system design and requires very few external components for operation. The product is bias adjustable allowing the amplifier's power consumption to be optimized and is available in a lead-free/RoHS-compliant 7 x 7 mm surface mount package.

The TQP9218 is targeted for small cell or enterprise Femtocell basestation applications, distributed antenna systems (DAS), repeaters, and/or booster amplifiers.

Functional Block Diagram



Top View

14 Pin 7 x 7 mm Leadless SMT Package

Product Features

- 1805 – 1880 MHz Frequency Range
- Fully integrated, 2-Stage Power Amplifier
- Internally Matched 50 Ω Input/Output
- −48 dBc ACLR at Pavg = +24 dBm
- 31.5 dB Gain
- 15% PAE at +24 dBm
- >15dB Input / Output return Loss
- 212 mA Quiescent Current
- On-chip Control Bias and Temp. Comp Circuit
- RoHS compliant
- Covers Bands 3, 9

Applications

- Small Cell / Picocell
- Enterprise Femtocell
- Customer Premises Equipment (CPE)
- Data Cards and Terminals
- Distributed Antenna Systems (DAS)
- Booster Amps, Repeaters

Ordering Information

Part No.	Description
TQP9218	2,500 pieces on a 13" reel (standard)
TQP9218-PCB	1805 −1880 MHz Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−55 to +150 °C
RF Input Power, CW, 50Ω, T=+25 °C	+13 dBm
Supply Voltage (V_{CC})	6 V
V_{REF}	+3.5 V

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{CC1}, V_{cc2}	+3.6	+4.5	+5.25	V
V_{ref}	+2.75	+2.85	+2.95	V
T_{CASE}	−40		+85	°C
Tj at T_{CASE} max			+165	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

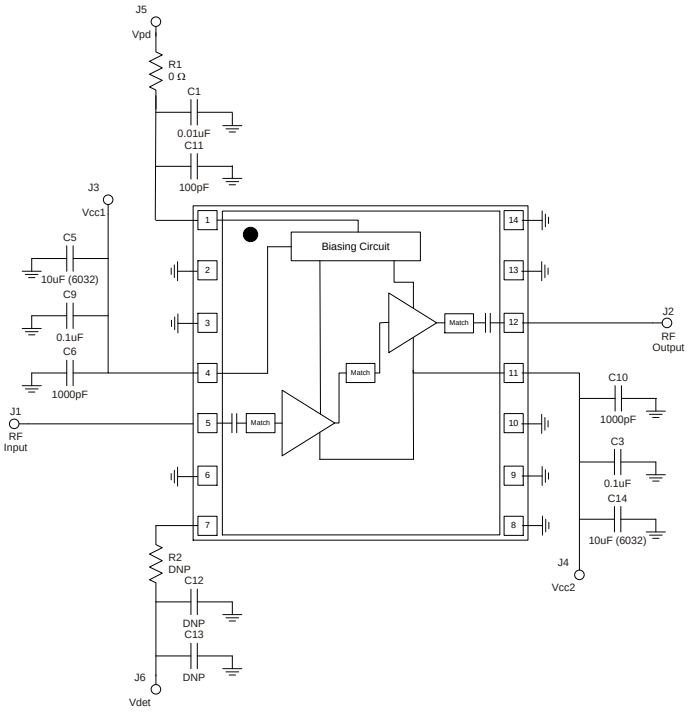
Parameter	Conditions[1]	Min	Typ	Max	Units
Frequency Range		1805		1880	MHz
Test Frequency			1840		MHz
Gain		28.5	31.5	34.5	dB
Input Return Loss		10	17		dB
Output Return Loss		10	16		dB
Output P1dB			+33		dBm
ACLR	P_{out} = +24 dBm, 20 MHz LTE E-TM1.1, 9.5 dB PAR		−48	-45	dBc
ACLR	P_{out} = +24 dBm, 2X20 MHz LTE E-TM1.1, 9.5 dB PAR		-40		dBc
ACLR	P_{out} = +24 dBm, 15 MHz LTE E-TM1.1, 9.5 dB PAR		−52		dBc
ACLR	P_{out} = +24 dBm, 10 MHz LTE E-TM1.1, 9.5 dB PAR		−52		dBc
ACLR	P_{out} = +24 dBm, 5 MHz LTE E-TM1.1, 9.5 dB PAR		−52		dBc
Efficiency	P_{out} = +24 dBm, 20 MHz LTE E-TM1.1, 9.5 dB PAR	13	15.2		%
Spurious Output Level	P_{out} = +24 dBm, 10:1 VSWR		<60		dBc
VSWR Survivability	No degradation or failure	10:1			-
Quiescent Current	V_{CC1} + V_{CC2}	160	212	280	mA
Reference Current	Temp = −40°C to +85°C, V_{REF} = +2.85V		6.5	10	mA
Leakage current	VCC = +4.5V, Vref = 0V		1.5	5	µA
Operational Current	Pout = +24 dBm		365	460	mA
Switching Speed	10% to 90% Rise time		620		ns
	90% to 10% Fall time		610		ns
Harmonics	$2F_0$ at +24dBm, CW signal		-43	-38	dBc
	$3F_0$ at +24dBm, CW signal		-61	-56	dBc
	$4F_0$ at +24dBm, CW signal		-58	-53	dBc
Thermal Resistance, θ_{jc}	Module (junction to case)			37	°C/W

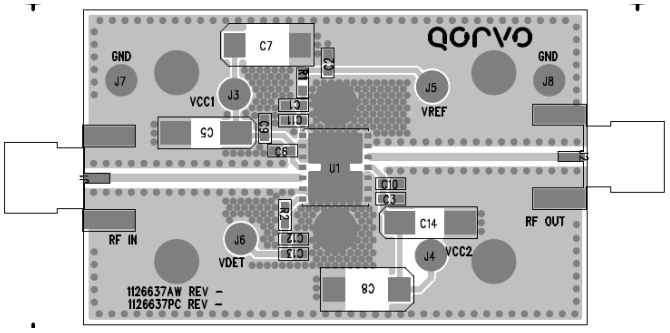
Notes:
1. Test conditions unless otherwise noted: V_{CC1} = V_{CC2} = +4.5 V, V_{REF} = +2.85V, Temp = +25 °C, 50 Ω system.

Parameter	Conditions	-40°C	+25°C	+85°C	Units
Gain	Small Signal	33.0	31.5	30.0	dB
ACLR	P_{OUT} = +24 dBm, 20 MHz LTE E-TM1.1, 9.5dB PAR	-50	-48	-46	dBc
PAE	P_{OUT} = +24 dBm, 20 MHz LTE E-TM1.1, 9.5dB PAR	16	15	14	%

Test Frequency = 1840MHz

Evaluation Board – TQP9218-PCB





Bill of Material – TQP9218-PCB

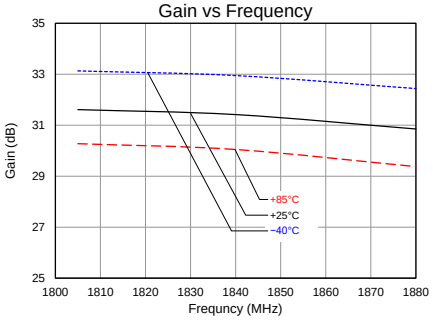
Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board		
U1	n/a	High Linearity 0.25 W Power Amplifier	Qorvo	TQP9218
R1	0 Ω	Resistor, Chip, 0603, 5%	various	
C1	0.01 uF	Capacitor, Chip, 0603, 5%	various	
C11	100 pF	Capacitor, Chip, 0603, 5%	various	
C3, C9	0.1 uF	Capacitor, Chip, 0603, 5%	various	
C5, C14	10 uF	Capacitor , Chip, 6032, 10%, Tantalum	various	
C6, C10	1000 pF	Capacitor , Chip, 0603, NPO/COG, 5%	various	

Vcc1=Vcc2=4.5V, Pout=24.5dBm, Signal PAR=9.5dB, F = 1840MHz					
LTE signal BW	5MHz	10MHz	15MHz	20MHz	Units
ACLR1-Low	-50.0	-51.5	-51.5	-51.5	dBc
ACLR1-high	-51.5	-51.5	-50.0	-50.5	dBc

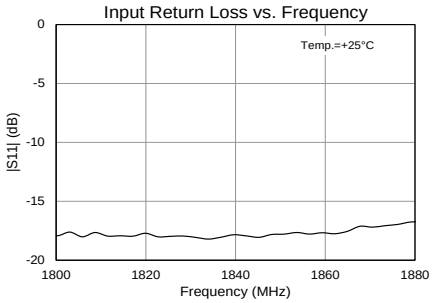
Performance Plots – TQP9218-PCB

Test conditions unless otherwise noted: V_{CC1} = V_{CC2} = +4.5V, V_{REF} = +2.85 V, I_{CQ} = 212mA, I_{REF} = 6.5mA, Temp.= +25 °C

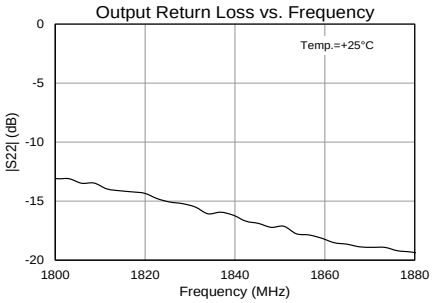
Gain vs Frequency



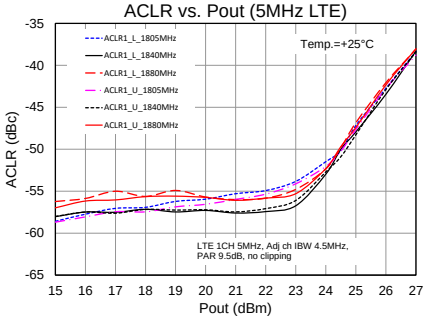
Input Return Loss vs. Frequency



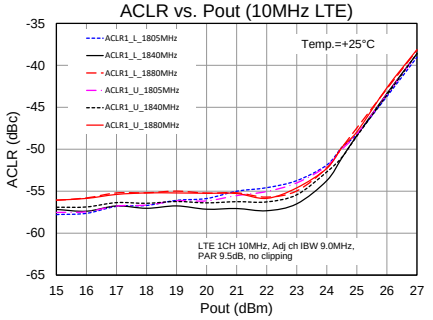
Output Return Loss vs. Frequency



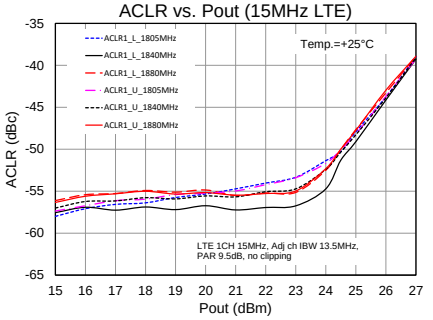
ACLR vs. Pout (5MHz LTE)



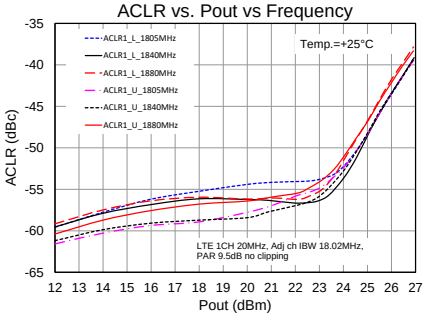
ACLR vs. Pout (10MHz LTE)



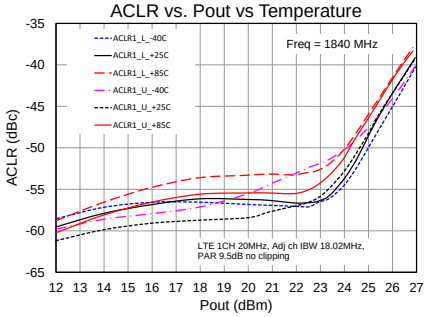
ACLR vs. Pout (15MHz LTE)



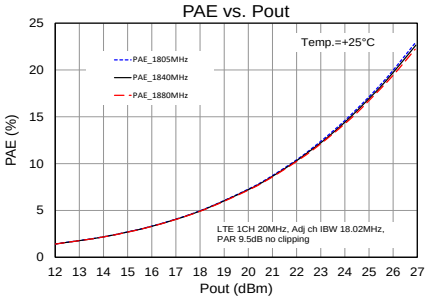
ACLR vs. Pout vs Frequency



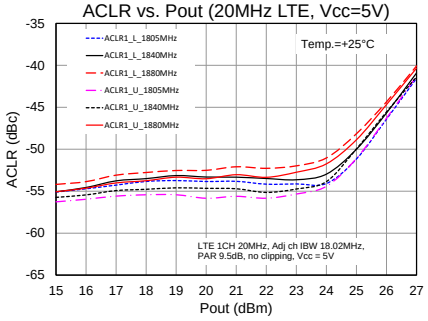
ACLR vs. Pout vs Temperature



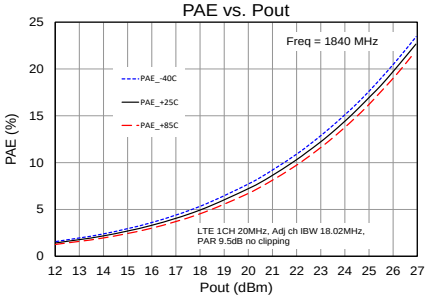
PAE vs. Pout



ACLR vs. Pout (20MHz LTE, Vcc=5V)



PAE vs. Pout

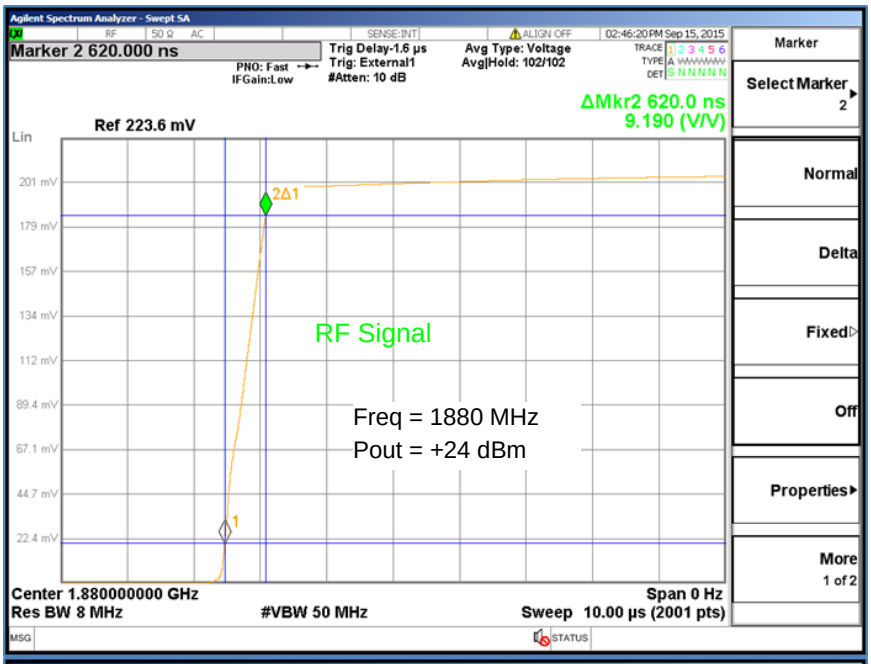


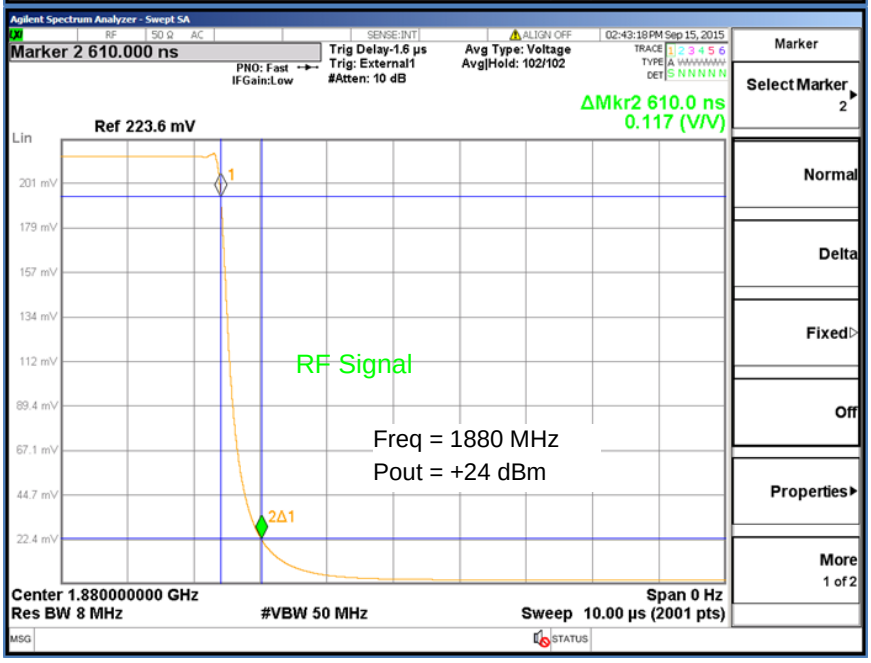
Switching Speed

Switching Time Measurement based on TQP9218 Application Board

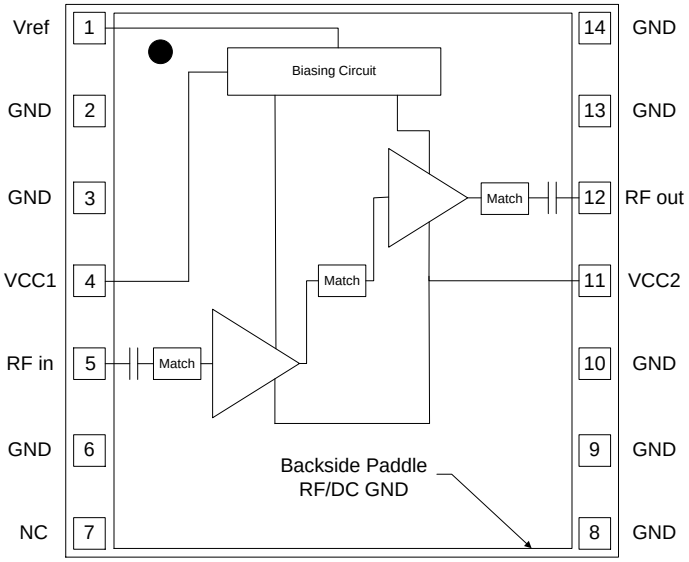
Using Shutdown Circuit: V_{REF}=2.85V, Vcc=4.5V, C1=NL

Parameter	
Turn-on Transition (10% RF – 90% RF)	620nS
Turn-off Transition (90% RF – 10% RF)	610nS





Pin Configuration and Description

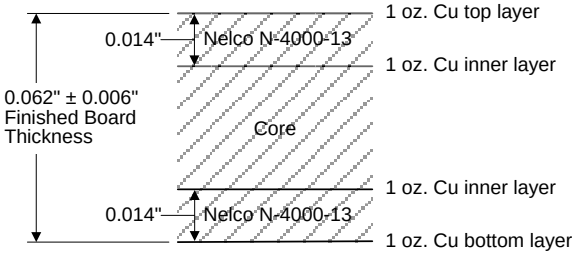


Top View

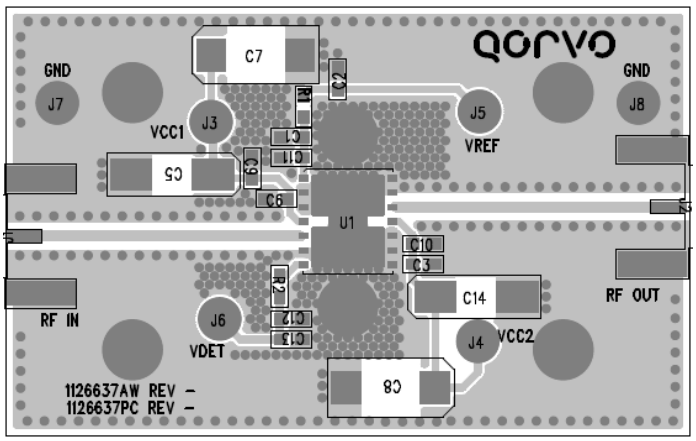
Pad No.	Label	Description
1	V_{REF}	Sets the bias current for the amplifiers. It can also be used to power down the device.
2, 3, 6, 8, 9, 10, 13, 14	GND	RF and DC ground.
4	$V_{CC}1$	Voltage supply for the active bias circuitry.
5	RFin	RF input pin. The DC is internally blocked at this pin.
7	NC	No internal connection.
11	$V_{CC}2$	DC voltage supply connection for AMP1 and AMP2.
12	RFout	RF output pin. The DC is internally blocked at this pin.
Backside Paddle	RF/DC GND	RF/DC ground. See PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

Qorvo PCB 1126637 Material and Stack-up

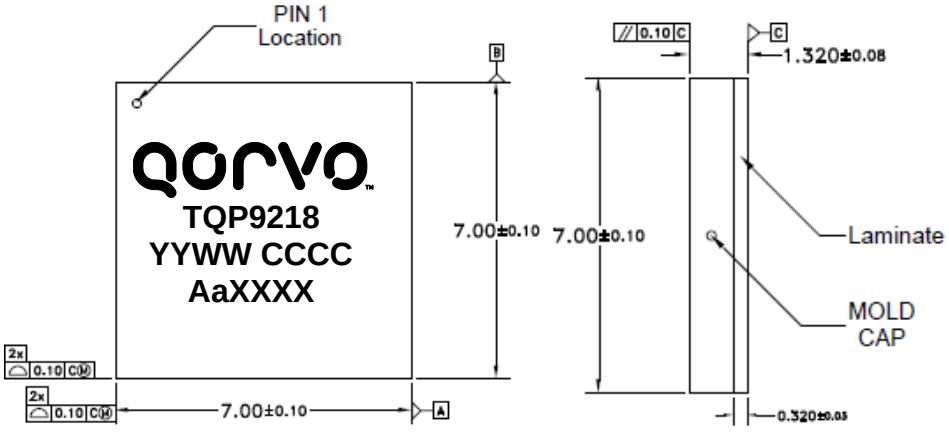


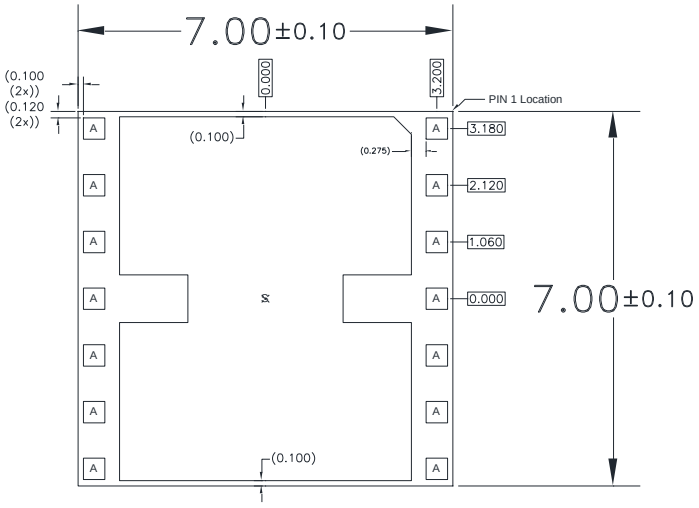
50 ohm line dimensions: width = .028”
spacing = .028”.

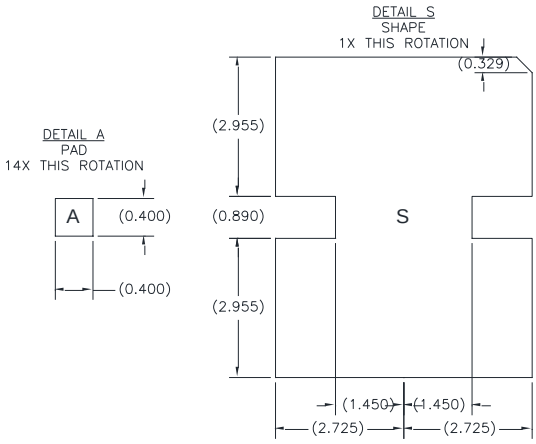


Package Marking and Dimensions

Marking: Part number – TQP9218
Assembly Code – YYWW
Country Code - CCCC
Lot code – AaXXXX



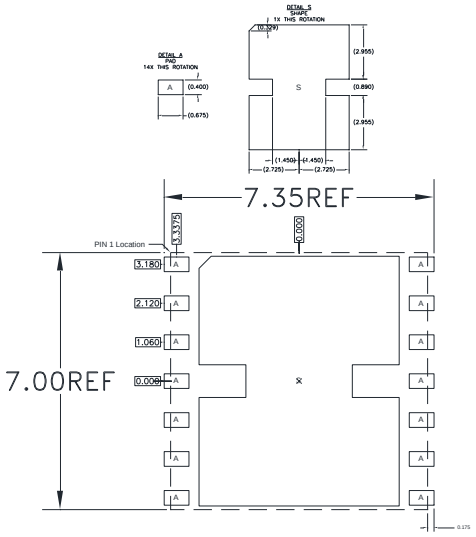




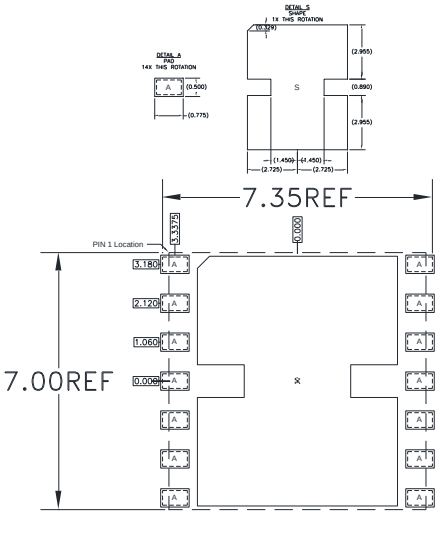
Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



RECOMMENDED
LAND PATTERN

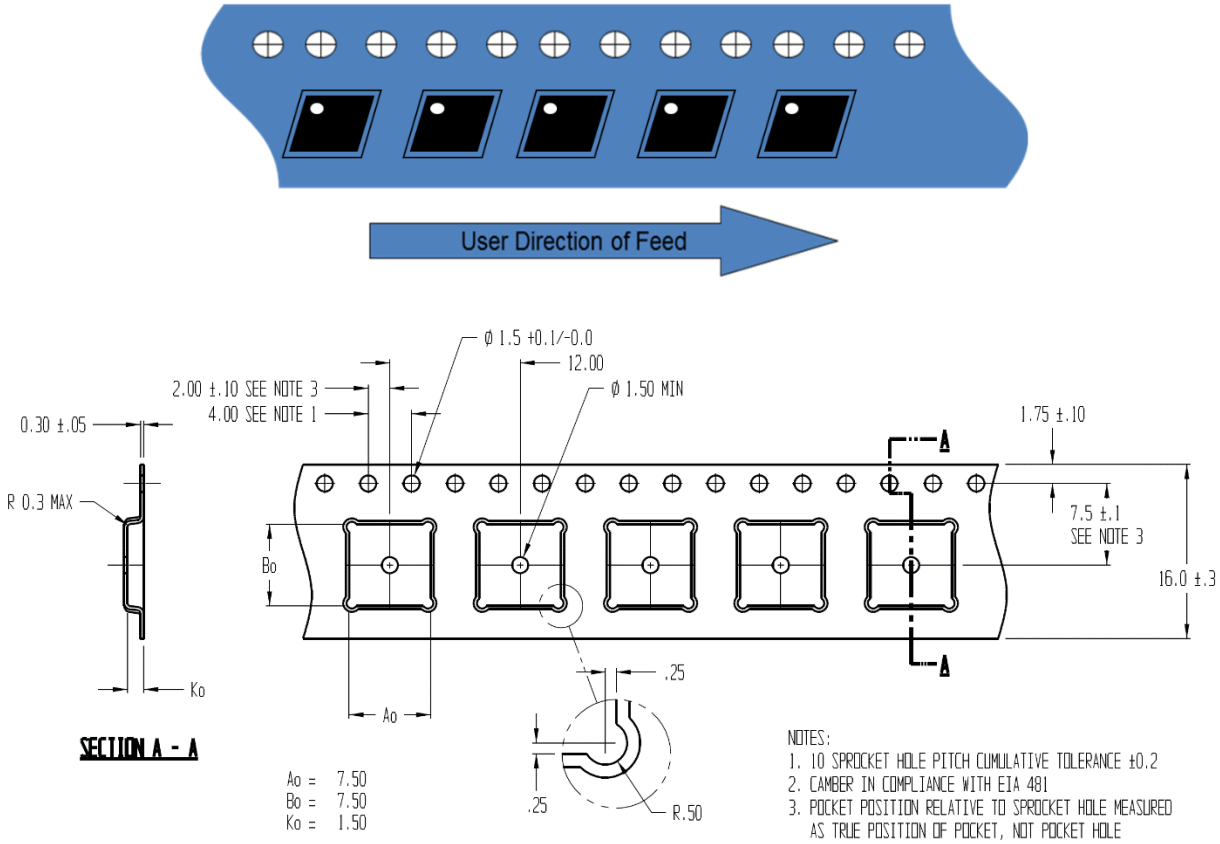


RECOMMENDED
LAND PATTERN MASK

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

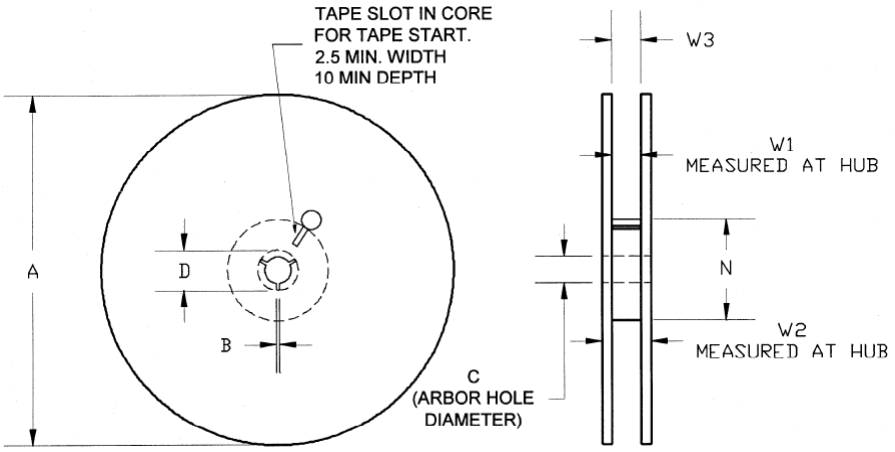
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.295	7.50
	Width	B0	0.295	7.50
	Depth	K0	0.059	1.50
	Pitch	P1	0.472	12.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.295	7.50
Cover Tape	Width	C	0.524	13.30
Carrier Tape	Width	W	0.630	16.0

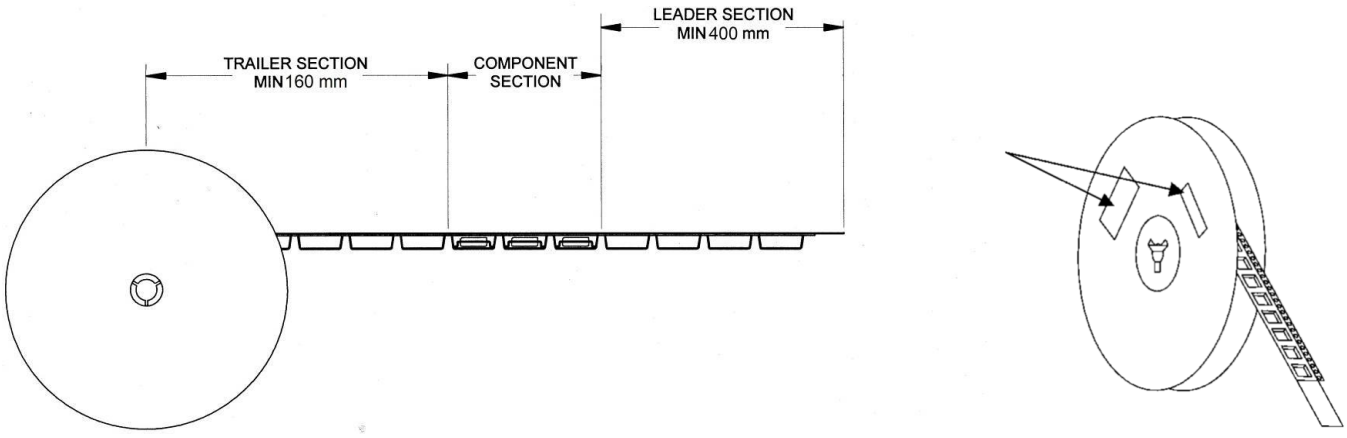
Tape and Reel Information – Reel Dimensions (13”)

Standard T/R size = 2,500 pieces on a 13” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.874	22.2
	Space Between Flange	W1	0.661	16.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.