TQP9309

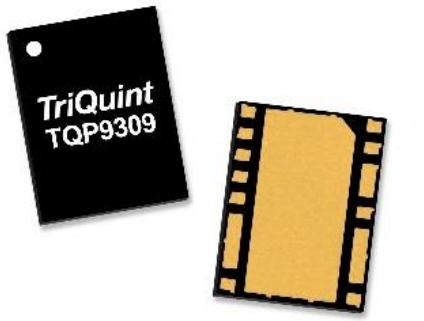
High Efficiency 0.5W Small Cell Power Amplifier

General Description

The TQP9309 is a high-efficiency two-stage power amplifier in a low-cost surface-mount package with on-chip bias control and temperature compensation circuitry, suitable for small cell base station applications.

TQP9309 provides 32 dB gain and >+28 dBm linear power with pre-distortion correction over the 0.7-1.0 GHz frequency range for Bands 5, 6, 8, 12, 13, 14, 17, 20, 26, 27, 28, and 29. With pre-distortion, the amplifier is able to achieve -50dBc ACLR at 28 dBm output power using a 20 MHz LTE signal.

The TQP9309 integrates two high performance amplifier stages onto a module to allow for a compact system design and requires very few external components for operation. The amplifier is bias adjustable allowing the amplifier's power consumption to be optimized. The TQP9309 is available in a lead-free RoHS-compliant 3.5x4.5mm surface mount package and is pin-compatible to the 1.8-2.2 GHz TQP9321 and 2.5-2.7 GHz TQP9326.

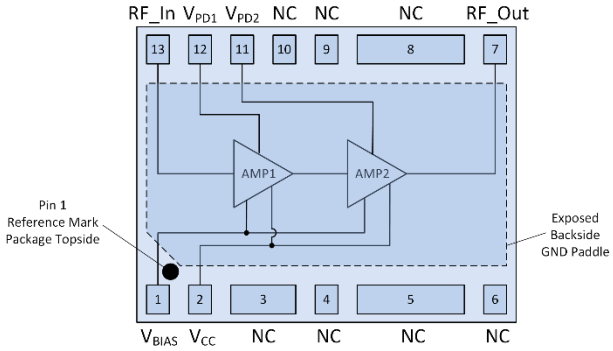


3.5 x 4.5 mm Leadless SMT Package

Product Features

- Frequency Range : 0.7-1.0 GHz
- Covers multiple bands with one component
- Fully integrated, 2-stage Power Amplifier
- Internally matched 50 Ω input/output
- -50dBc ACLR (DPD corrected) @ +28 dBm Pavg
- 32 dB Gain
- 27% PAE @ +28 dBm Pavg
- In-built Control Bias and Temp. Comp Circuit
- Single Supply Voltage : 5V
- Lead-free / RoHS compliant
- POE Capable

Functional Block Diagram



Top View

Applications

- Small-Cell Base Stations
- Enterprise Femtocell
- Bands 5, 6, 8, 12, 13, 14, 17, 20, 26, 27, 28, 29

Ordering Information

Part No.	Description
TQP9309TR13	2500 pieces on a 13" reel
TQP9309EVB-01	Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−40 to +150 °C
Supply Voltage (V_{CC})	+6 V
RF Input Power, CW, 50 Ω, T=25 °C	+10 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V_{DD})		+5		V
T_{CASE}	−40	+25	+85	°C
Tj for >10^6 hours MTTF			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{CC} =+5V, Vpd = +5V, Temp= +25°C, Test Frequency : 900MHz

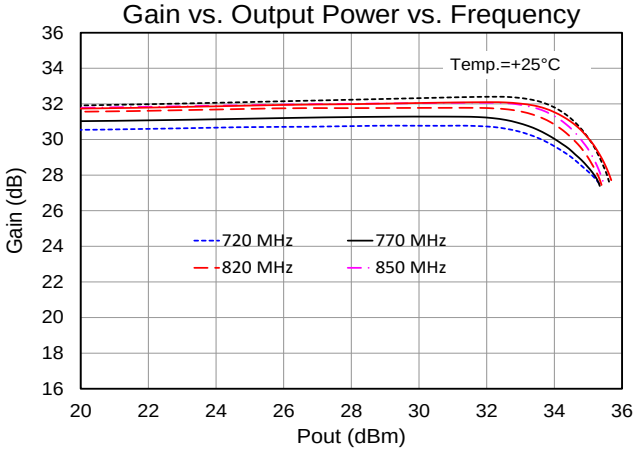
Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		700		960	MHz
Output Channel Power			+28		dBm
Gain	700 - 800MHz	28.6	31		dB
	800 - 960MHz	**29.6**	**32**	**33.3**	dB
Gain Temperature Coefficient			-0.026		dB/°C
ACLR Uncorrected	See note 1		-37		dBc
ACLR DPD Corrected	See note 1		-50		dBc
Power Added Efficiency	See note 1		27		%
Noise Figure			4		dB
Output P3dB		**+33.9**	**+35**		dBm
P3dB Temperature Coefficient			-0.005		dBm/°C
Supply Voltage			5		V
Quiescent Current, I_{CQ}		**85**	**100**	**127**	mA
Operational Current, Icc			380		mA
VSWR Survivability	Pout = +26 dBm Signal : WCDMA 1C, PAR = 8 dB	7:1			–
Thermal Resistance, θ_{jc}	Module (junction to backside paddle)		28.3		°C/W

Notes:
1. Using LTE signal, 20MHz, IBW = 18.02 MHz, PAR 7.5dB, Pout = +28 dBm
2. Items in min/max columns in **bold** at guaranteed by production test at 900 MHz
3. Items in min/max columns that are not a bold font are guaranteed by design characterization.

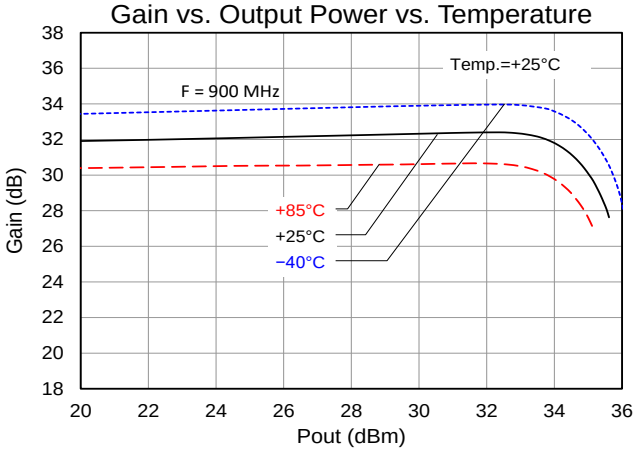
Performance Plots

Test conditions unless otherwise noted: V_{CC} =+5V, Vpd = +5V, Temp= +25°C

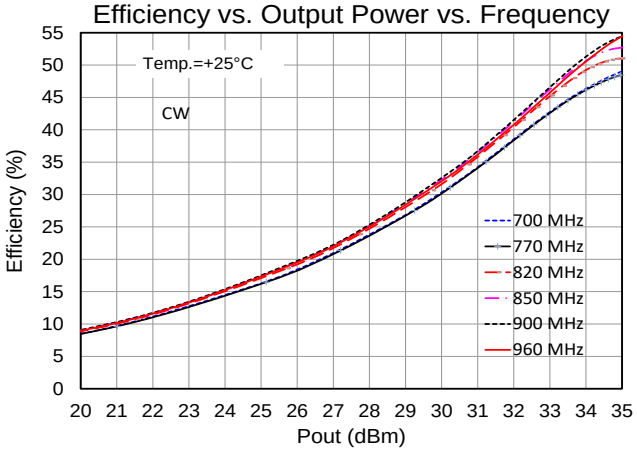
Gain vs. Output Power vs. Frequency



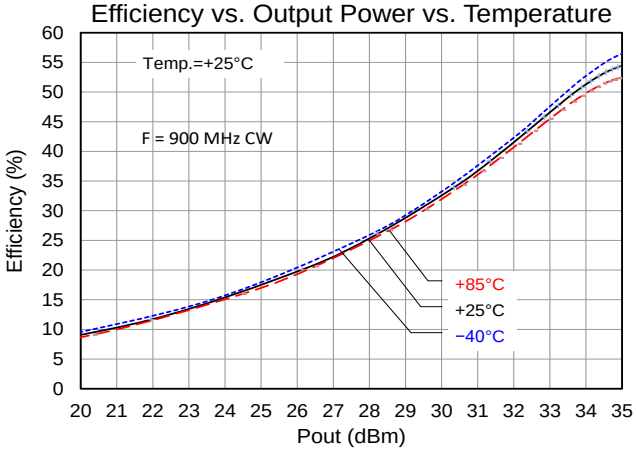
Gain vs. Output Power vs. Temperature



Efficiency vs. Output Power vs. Frequency

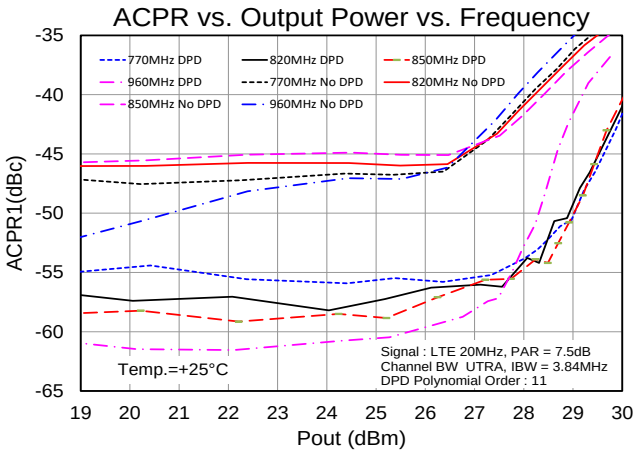


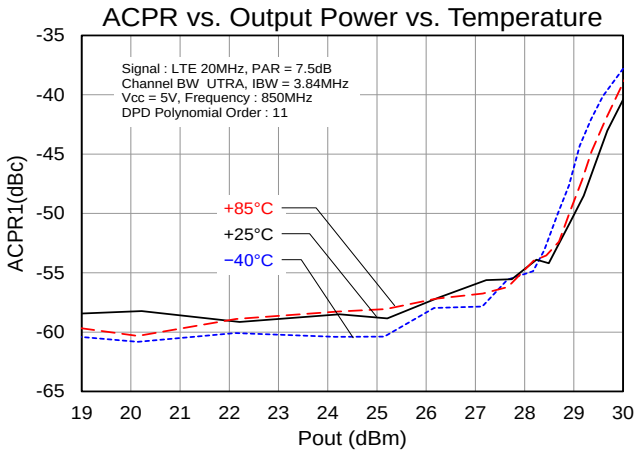
Efficiency vs. Output Power vs. Temperature

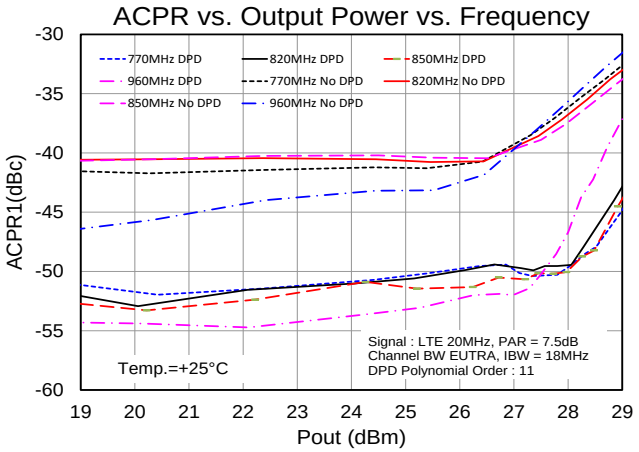


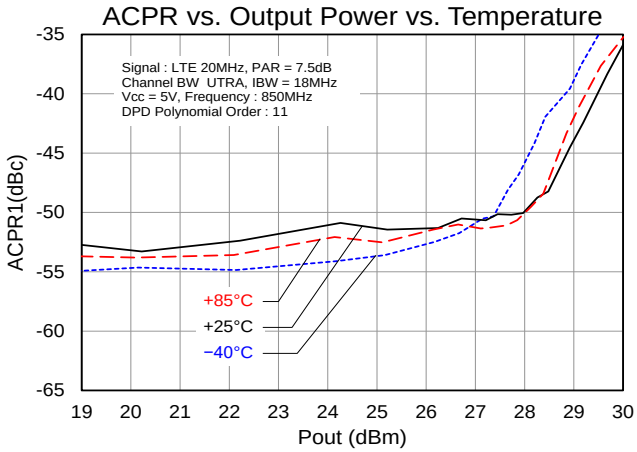
Performance Plots (continued)

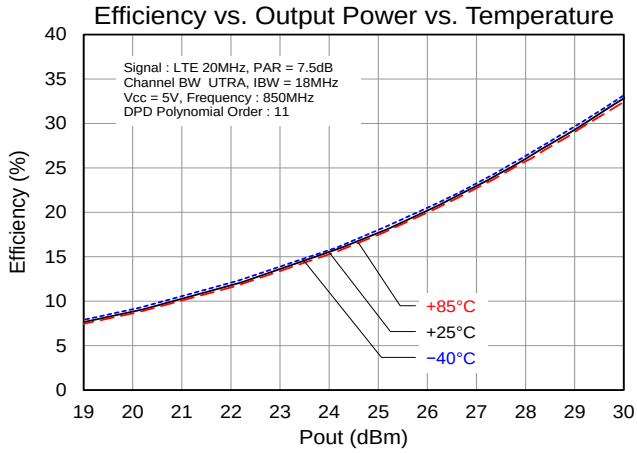
Test conditions unless otherwise noted: V_{CC} =+5V, Vpd = +5V, Temp= +25°C



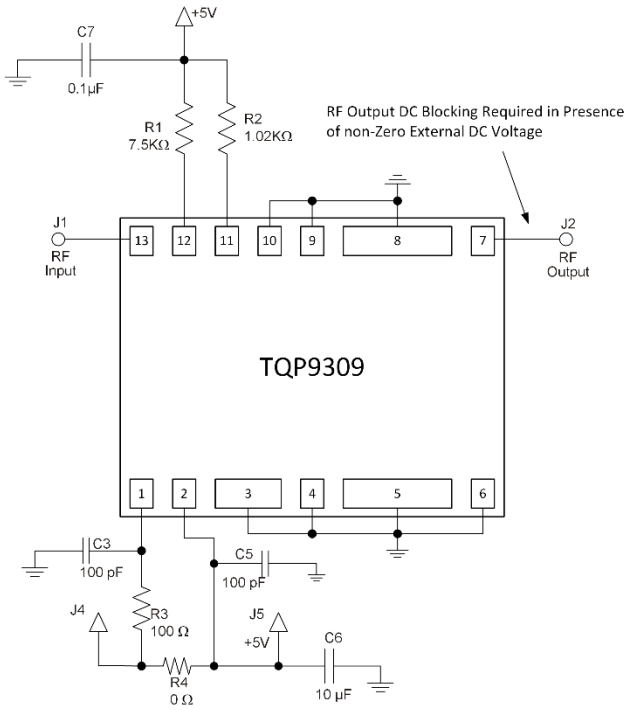


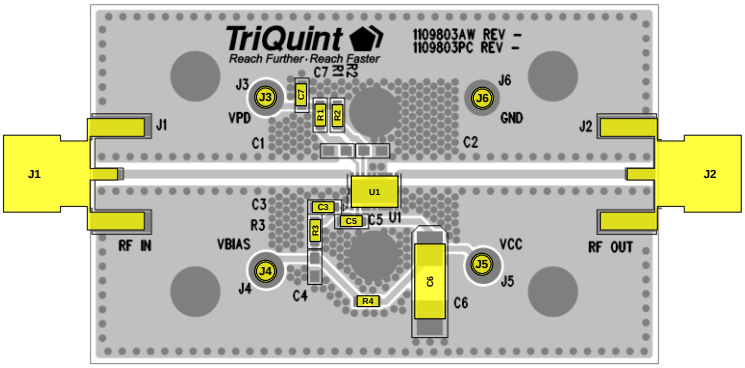






Application Circuit – TQP9309EVB-01

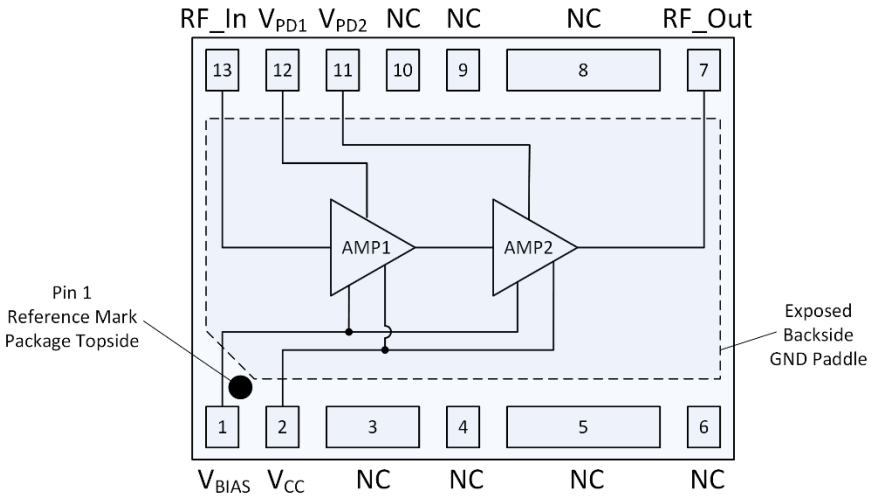




Bill of Material – TQP9309EVB-01

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	-	1109803
U1	n/a	High Efficiency 2-stage PA	Qorvo	TQP9309
R3, R4	0 Ω	Resistor, Chip, 0603, 5%	various	
R3	100 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
C7	0.1 µF	Capacitor, Chip, 0603, 5%	various	
C6	10 µF	Capacitor, Chip, 6032, 10%, Tantalum	various	
C3, C5	100 pF	Capacitor, Chip, 0603, NPO/COG, 5%	various	
R2	1.0 KΩ	Resistor, Chip, 0603, 5%, 1/16W	various	
R1	7.5 KΩ	Resistor, Chip, 0603, 5%, 1/16W	various	
C1, C2, C4		Do Not Place		

Pin Configuration and Description

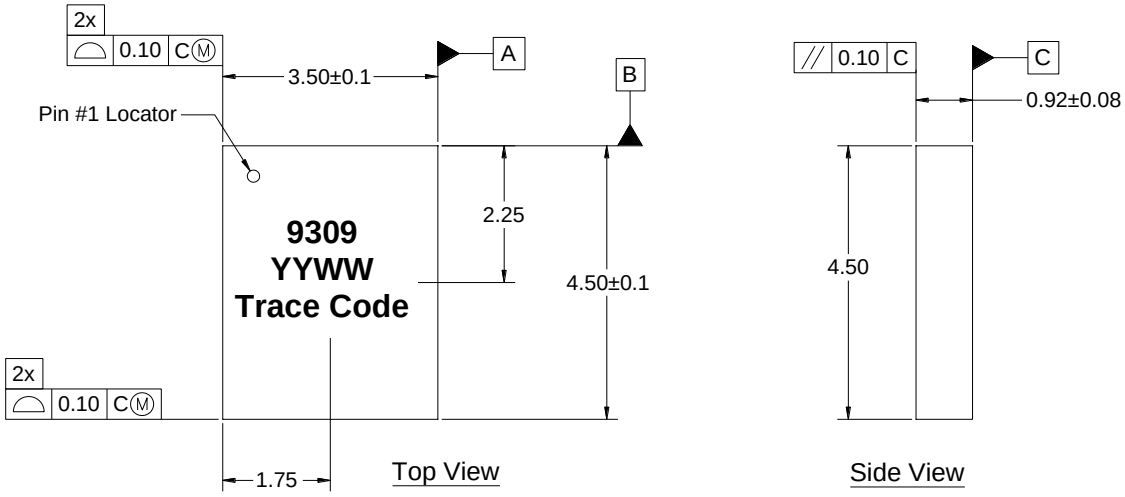


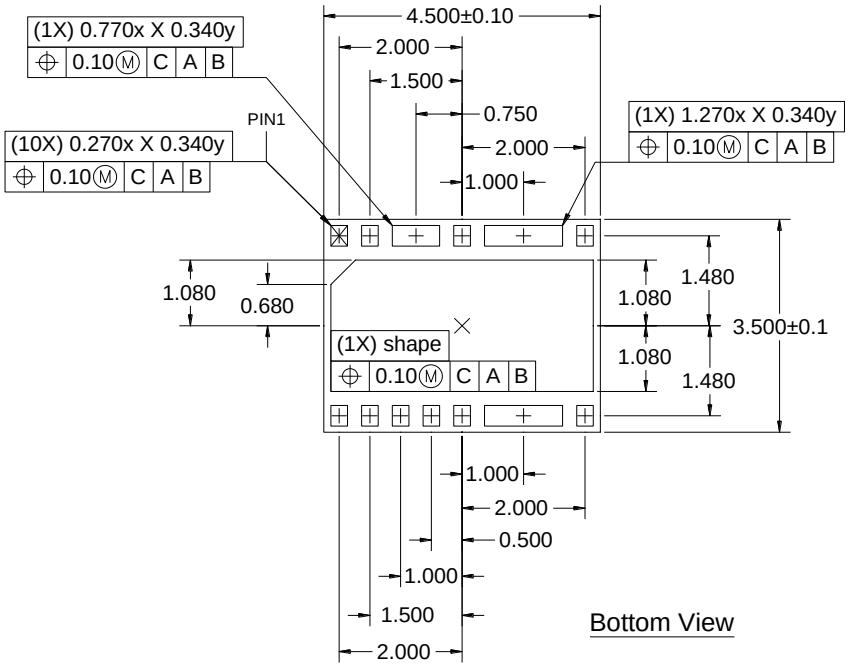
Pin No.	Label	Description
1	V_{BIAS}	DC voltage supply input for internal active biasing circuit
2	V_{CC}	DC voltage supply input for AMP1 and AMP2
3, 4, 5, 6, 8, 9, 10	NC	No internal connection. Provide grounded land pads for PCB mounting integrity
7	RF_Out	RF output, DC blocking required in the presence of external non-zero DC voltage
11	V_{PD2}	DC voltage input, AMP2 quiescent current reference, 0 Volt AMP2 power down
12	V_{PD1}	DC voltage input, AMP1 quiescent current reference, 0 Volt AMP1 power down
13	RF_In	RF input, Internally DC blocked
Backside Paddle	-	RF & DC ground. Use recommended via hole pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Mechanical Information

Package Marking and Dimensions

Marking: Part number – 9309
Assembly Code - YYWW

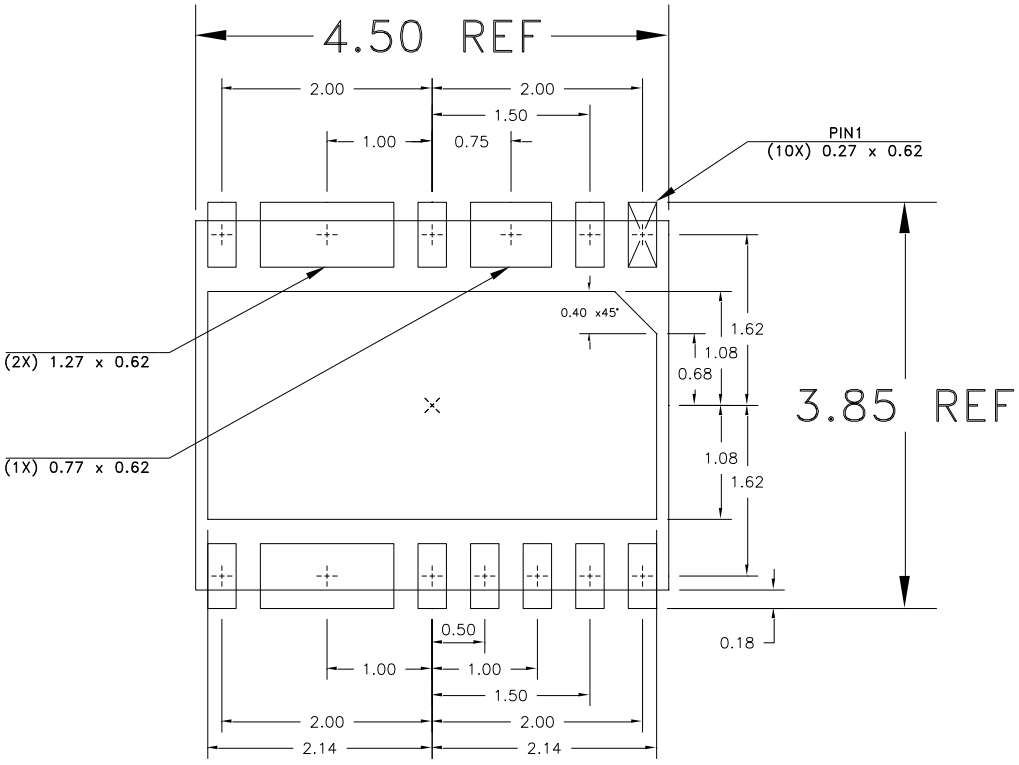




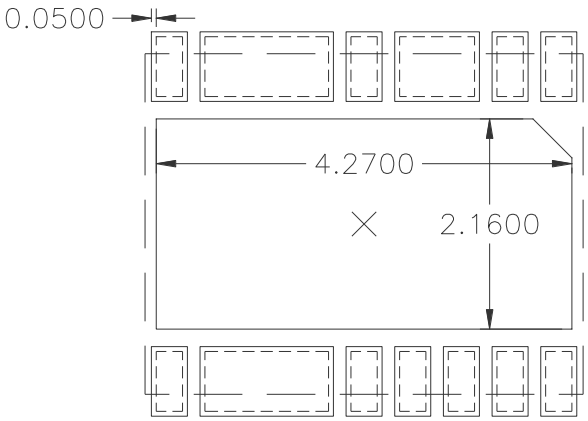
Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern

Recommend PCB land-pad pattern metallization (Top View)



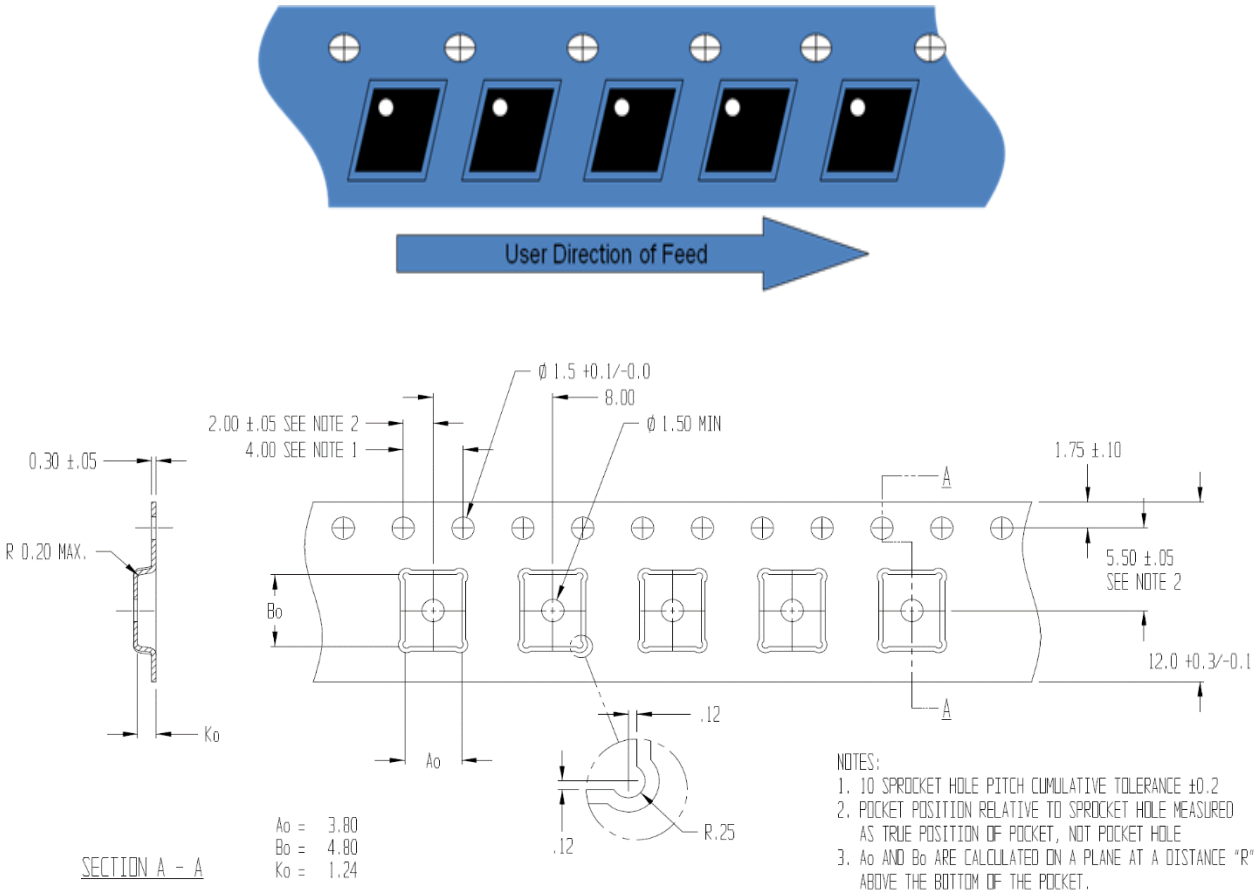
Recommended PCB solder mask opening (Top View)



Notes:

1. A heat sink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

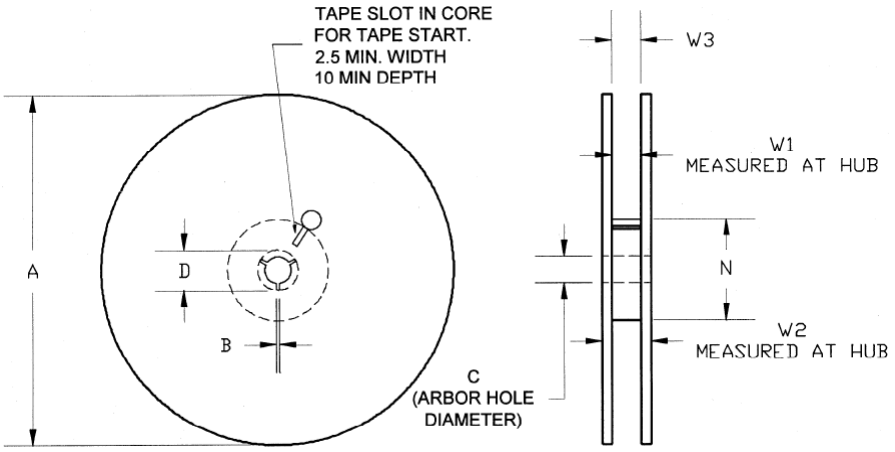
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.150	3.80
	Width	B0	0.199	4.80
	Depth	K0	0.049	1.24
	Pitch	P1	0.315	8.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.00

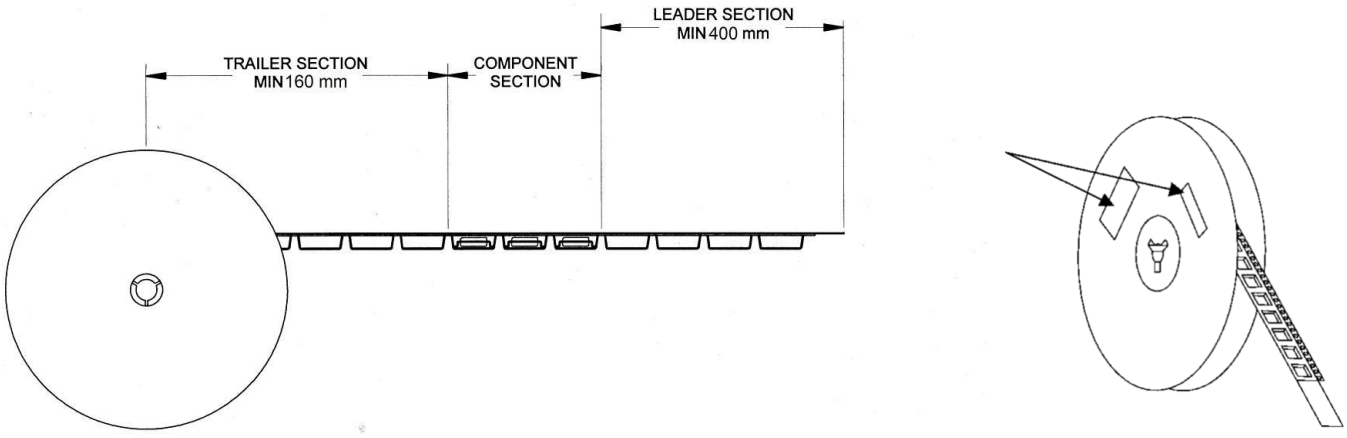
Tape and Reel Information – Reel Dimensions (13”)

Standard T/R size = 2,500 pieces on a 13” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.