Wide Input High Efficiency Charger for Li-Ion Batteries

POWER MANAGEMENT

Brief Description

The TS55101 is a DC/DC synchronous switching lithium-ion (Li-Ion) battery charger with fully integrated power switches, internal compensation, and extensive fault protection.

Its switching frequency of 1MHz enables the use of small filter components, resulting in smaller board space and reduced BOM costs.

The TS55101 utilizes constant current trickle charge in Pre-Charge mode. In Full-Charge Constant-Current Mode, the regulation is for constant current (CC). Once termination voltage is reached, the regulator operates in voltage mode. When the regulator is disabled (the EN pin is low), the device draws 10µA (typical) quiescent current. The Leakage current from the battery is below 1µA.

The TS55101 includes supervisory reporting through the NFLT (inverted fault) open-drain output to interface other components in the system. Device programming is achieved by an I²C™ interface through the SCL and SDA pins.

Benefits

- Up to 2.0A of continuous output current in Constant-Current (CC) Mode
- High efficiency – up to 92% with typical loads
- High programmability for custom charge parameters

Available Support

- Evaluation Kit
- Application Notes

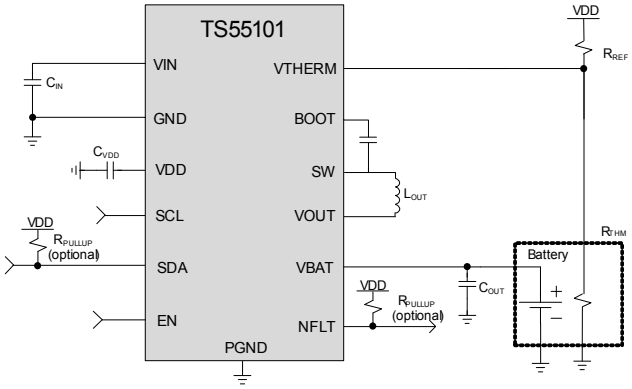
Features

- Internal charge current sensing
- VBAT reverse-current blocking
- Programmable temperature-compensated termination voltage: 3.9V to 4.5V ± 0.6%
- User programmable maximum charge current: 200mA to 2000mA
- Current mode PWM control in constant voltage
- Supervisor for VBAT reported at the nFLT pin
- Input supply under-voltage lockout
- Extensive protection for over-current, over-temperature, VBAT over-voltage, charging and pre-charging timeout
- Charge status indication
- I^2C™ program interface with EEPROM registers
- Integrated 50mA LDO output

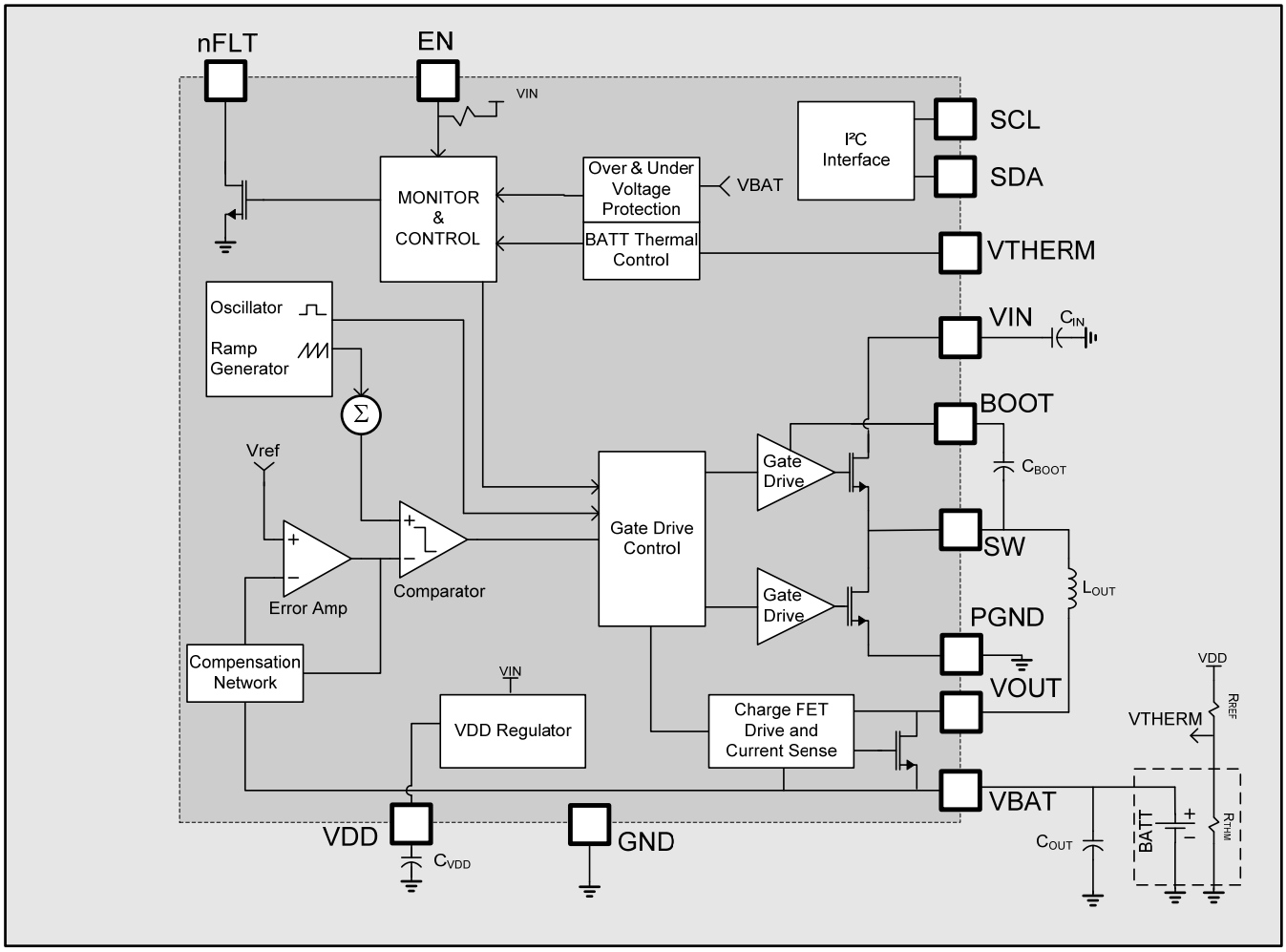
Physical Characteristics

- Wide input voltage range: V_{BAT} + 0.3V (4.4V min.) to 16.5V
- Junction operating temperature: -40°C to 125°C
- Package: 16-pin PQFN (3mm x 3mm), Lead-free, fully WEEE and RoHS compliant

TS55101 Application Circuit



TS55101 Block Diagram



1 TS55101 Characteristics

Important: Stresses beyond those listed under “Absolute Maximum Ratings” (section 1.1) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

1.1. Absolute Maximum Ratings

Over operating ambient temperature range unless otherwise noted.

Table 1.1 Absolute Maximum Ratings

Parameter	Value [1)]	Unit
VDD, EN, NFLT, SCL, SDA, VTHERM, VBAT	-0.3 to 5.5	V
VIN	-0.3 to 20	V
BOOT	-0.3 to 25	V
SW	-1 to 20	V
Maximum Junction Temperature, T_{JMAX}	150	°C
Storage Temperature Range, T_{STOR}	-65 to 150	°C
Electrostatic Discharge – Human Body Model [2)] – NFLT pin	±1.9k	V
Electrostatic Discharge – Human Body Model [2)] – all other pins	±2.0k	V
Electrostatic Discharge – Machine Model [2)]	+/-200	V
Peak IR Reflow Temperature (10s to 30s))	260	°C

1) All voltage values are with respect to network ground terminal.

2) ESD testing is performed according to the respective JESD22 JEDEC standard.

1.2. Thermal Characteristics

Table 1.2 Thermal Characteristics

Parameter	Symbol	Value [1)]	Unit
Thermal Resistance Junction to Ambient [1)]	θ_{JA}	33-36	°C/W
Thermal Resistance Junction to Case	θ_{JC}	1.2-3.9	°C/W

1) Assumes a 3x3mm QFN-16 in 1 in^2 area of 2 oz. copper and 25°C ambient temperature with 4 thermal vias beneath pad

1.3. Recommended Operating Conditions

Table 1.3 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input Operating Voltage at VIN Pin	V_{IN}	4.6	12	16.5	V
Thermal Reference Resistor	R_{REF}		10		kΩ
Output Filter Inductor Typical Value [1)]	L_{OUT}		4.7		µH
Output Filter Capacitor Typical Value [2)]	C_{OUT}		4.7		µF
Output Filter Capacitor ESR	$C_{OUT-ESR}$			100	mΩ
Input Supply Bypass Capacitor Value [3)]	C_{IN}		10		µF
VDD Supply Bypass Capacitor Value [2)]	C_{VDD}		2.2	10	µF
Bootstrap Capacitor	C_{BOOT}		22		nF
Operating Ambient Temperature	T_A	-40		85	°C
Operating Junction Temperature	T_J	-40		125	°C

1) For best performance, use an inductor with a saturation current rating higher than the maximum V_{BAT} load requirement plus the inductor current ripple.

2) For best performance, use a low ESR ceramic capacitor.

3) For best performance, use a low ESR ceramic capacitor. If C_{IN} is not a low ESR ceramic capacitor, add a 0.1µF ceramic capacitor in parallel to C_{IN}. Input supply cap has to be chosen to limit voltage ripple to <10% of VIN.

1.4. Electrical Characteristics

Electrical characteristics T_J = -40°C to 125°C, VIN = 12V, (unless otherwise noted)

Table 1.4 Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
VIN Supply Voltage						
Voltage Input	V_{IN}	Ensure that Vin > VBAT + 0.3V	4.6	12	16.5	V
Quiescent Current Normal Mode	$I_{CC-NORM}$	I_{LOAD} = 0A, no switching EN ≥ 2.2V (HIGH)		3		mA
Quiescent Current Disabled Mode	$I_{CC--DISABLE}$	EN = 0V		10	50	µA
VBAT Leakage						
Leakage Current From Battery	$I_{BAT-LEAK}$	EN = 0V, V_{VBAT} = 4.1V, V_{IN} = 12V Tj=25C		1		µA
		EN = 0V, V_{VBAT} = 4.1V T_J = -40°C to 125°C			5	
VIN Under-Voltage Lockout						
Input Supply Under-Voltage Threshold	V_{IN-UV}	V_{IN} increasing, minimum value to guarantee startup in all conditions	4.07	4.4	4.6	V
Input Supply Under-Voltage Threshold Hysteresis	V_{IN-UV_HYST}			165		mV
OSC						
Oscillator Frequency	f_{OSC}		0.9	1	1.1	MHz
NFLT Open Drain Output						
High-Level Output Leakage	$I_{OH-NFLT}$	V_{NFLT} = VDD		0.1		µA
Low-Level Output Voltage	$V_{OL-NFLT}$	I_{NFLT} = -1mA			0.4	V
EN/SCL/SDA Input Voltage Thresholds						
High Level Input Voltage	V_{IH}	Internal Pull-up resistance EN pin only: (125kΩ…195kΩ) to 4.2V internal supply rail.	2.2			V
Low Level Input Voltage	V_{IL}				0.6	V
Input Hysteresis – EN, SCL, SDA Pins	V_{HYST}			200		mV
Input Leakage – EN Pin	I_{IN-EN}	V_{EN}=VDD		2		µA
		V_{EN}=0V		-2.0		µA
Input Leakage – SCL Pin	I_{IN-SCL}	V_{SCL}=VDD		90		µA
		V_{SCL}=0V		-0.1		µA
Input Leakage – SDA Pin	I_{IN-SDA}	V_{SDA}=VDD		0.1		µA
		V_{SDA}=0V		-0.1		µA
Low-Level Output Voltage	V_{OL-SDA}	I_{SDA} = -1mA			0.4	V
Thermal Shutdown						

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal Shutdown Junction Temperature	T_{SD}		130	150		°C
TSD Hysteresis	$T_{SD-HYST}$			10		°C
Pre-Charge End						
Pre-charge Voltage Threshold	V_{PRECHG}		2.9	3.0	3.1	V
Pre-charge Voltage Hysteresis	$V_{PC-HYST}$			130		mV
Charge Restart						
Voltage Below Termination for Charging Restart	$V_{RESTART}$			60		mV+
VDD LDO Output						
LDO Output Voltage	V_{LDO}	At VIN > 5.5V	4.75	5.0	5.25	V
LDO Output Current	I_{LDO}				50	mA
LDO Drop Out	LDO_{DO}	VIN=5V, Iout=50mA			400	mV
Charging Regulator with L_{OUT} =4.7µH and C_{OUT}=4.7µF						
Output Current Limit Tolerance in Full-Charge Mode[1]	$I_{BAT-FC1}$	1500mA Setting	1400	1500	1600	mA
Output Current Limit Tolerance in Full-Charge Mode[1]	$I_{BAT-FC2}$	800mA Setting	720	800	880	mA
Termination Voltage Tolerance in Top-Off Mode	V_{BAT-TO}	0°C < T_J < 60°C VTERM = 4.20V V_{BAT} is user programmable; see section 2.7.	4.175 -0.6%	4.20	4.225 0.6%	V
Top-Off Mode Time Out	t_{TO}		0		120	Minutes
Full-Charge Timer	t_{FC}		60		600	Minutes
Pre-Charge Timer	t_{PC}		60		240	Minutes
Timer Accuracy	t_{ACC}		-10%		+10%	
High Side Switch On Resistance	R_{DSON}	I_{SW} = -1A, T_J=25°C		105	125	mΩ
Low Side Switch On Resistance		I_{SW} = 1A, T_J=25°C		80		mΩ
Battery FET Switch On Resistance	R_{DSON}	I_{charge}=1A, T_j=25C		50		mΩ
Maximum Output Current	I_{BAT}			1.5	2	A
Over-Current Detect	I_{OCD}	HS switch current	2.5			A
V_{BAT} Over-Voltage Threshold	V_{BAT-OV}	V_{BAT} = 3.9V	100.5	102.5	104.5	%
Maximum Duty Cycle	$DUTY_{MAX}$			98		%

1) The 200mA and 300mA settings will typically be around 15% higher than shown in table.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermistor (V_{TH_REF} = 5V)						
Thermistor: 10KΩ Temperature Thresholds – β=3434K						
0°C VTHERM Threshold	10°C	Increasing Temp.	63.8	64.8	65.8	%VTH_REF
10°C VTHERM Threshold	11°C	Increasing Temp.	62.8	63.8	64.8	%VTH_REF
45°C VTHERM Threshold	45°C	Increasing Temp.	31.6	32.6	33.6	%VTH_REF
50°C VTHERM Threshold	50°C	Increasing Temp.	28.1	29.1	30.1	%VTH_REF
60°C VTHERM Threshold	60°C	Increasing Temp.	21.9	22.9	23.9	%VTH_REF
50°C VTHERM Threshold	50°C	Decreasing Temp.	28.1	29.1	30.1	%VTH_REF
50°C VTHERM Threshold	49°C	Decreasing Temp.	28.8	29.8	30.8	%VTH_REF
45°C VTHERM Threshold	44°C	Decreasing Temp.	32.4	33.4	34.4	%VTH_REF
10°C VTHERM Threshold	10°C	Decreasing Temp.	63.8	64.8	65.8	%VTH_REF
0°C VTHERM Threshold	0°C	Decreasing Temp.	73.2	74.2	75.2	%VTH_REF
Thermistor: 100KΩ Temperature Thresholds – β=4311K						
0°C VTHERM Threshold	10°C	Increasing Temp.	67.3	68.3	69.3	%VTH_REF
10°C VTHERM Threshold	11°C	Increasing Temp.	66.1	67.1	68.1	%VTH_REF
45°C VTHERM Threshold	45°C	Increasing Temp.	27.7	28.7	29.7	%VTH_REF
50°C VTHERM Threshold	50°C	Increasing Temp.	23.6	24.6	25.6	%VTH_REF
60°C VTHERM Threshold	60°C	Increasing Temp.	16.9	17.9	18.9	%VTH_REF
50°C VTHERM Threshold	50°C	Decreasing Temp.	23.6	24.6	25.6	%VTH_REF
50°C VTHERM Threshold	49°C	Decreasing Temp.	24.4	25.4	26.4	%VTH_REF
45°C VTHERM Threshold	44°C	Decreasing Temp.	28.5	29.5	30.5	%VTH_REF
10°C VTHERM Threshold	10°C	Decreasing Temp.	67.3	68.3	69.3	%VTH_REF
0°C VTHERM Threshold	0°C	Decreasing Temp.	78.0	79.0	80.0	%VTH_REF

1.5. I²C™ Interface Timing Requirements

Electrical characteristics T_J = -40°C to 125°C, VIN = 12V. See Figure 2.6 for an illustration of the timing specifications given in Table 1.5.

Table 1.5 I²C™ Interface Timing Characteristics

Parameter	Symbol	Standard Mode		Fast Mode [1]		Unit
		Min	Max	Min	Max	
I²C™ Clock Frequency	f_{scl}	0	100	0	400	kHz
I²C™ Clock High Time	t_{sch}	4		0.6		µs
I²C™ Clock Low Time	t_{scl}	4.7		1.3		µs
I²C™ Tolerable Spike Time [2]	t_{sp}	0	50	0	50	ns
I²C™ Serial Data Setup Time	t_{sds}	250		250		ns
I²C™ Serial Data Hold Time	t_{sdh}	0		0		µs
I²C™ Input Rise Time [2]	t_{icr}		1000		300	ns
I²C™ Input Fall Time [2]	t_{icf}		300		300	ns
I²C™ Output Fall Time; 10pF to 400pF Bus [2]	t_{ocf}		300		300	ns
I²C™ Bus Free Time Between Stop and Start	t_{buf}	4.7		1.3		µs
I²C™ Start or Repeated Start Condition Setup Time	t_{sts}	4.7		0.6		µs
I²C™ Start or Repeated Start Condition Hold Time	t_{sth}	4		0.6		µs
I²C™ Stop Condition Setup Time [2]	t_{sps}	4		0.6		µs

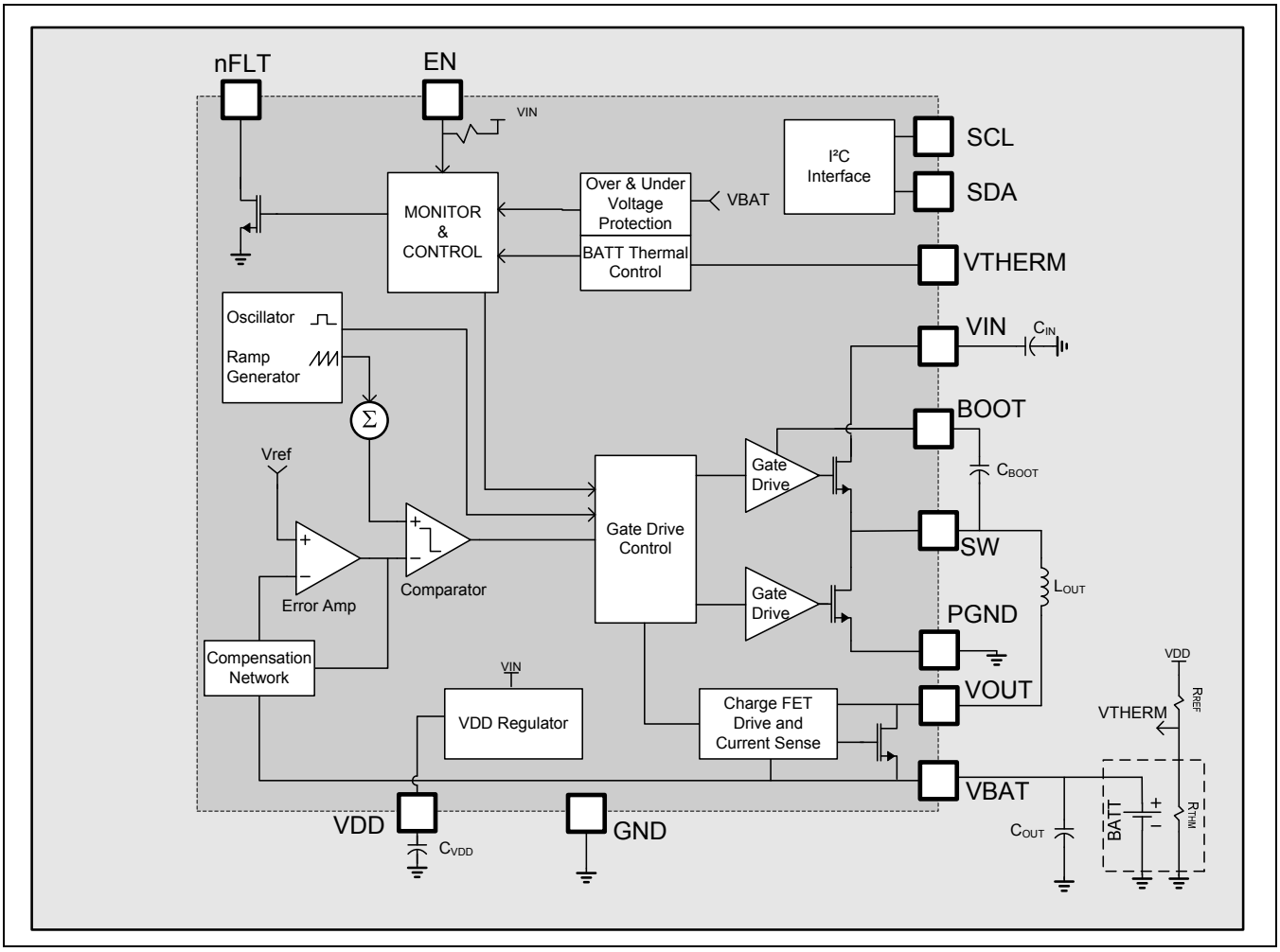
1) The I²C™ interface will operate in either standard or fast mode.

2) Parameter not tested in production.

2 Functional Description

The TS55101 is a fully-integrated Li-Ion battery charger IC based on a highly-efficient switching topology. It is configurable for termination voltage, charge current, and additional variables to allow optimum charging conditions for a wide range of Li-Ion batteries. The 1MHz internal switching frequency facilitates low-cost LC filter combinations. Figure 2.1 provides a block diagram for the TS55101.

Figure 2.1 TS55101 Block Diagram



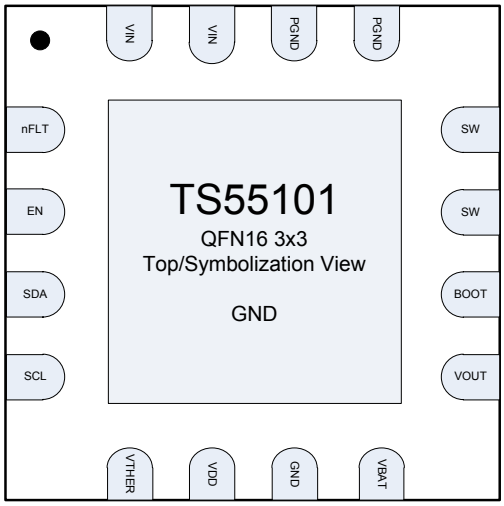
When the battery voltage is below 3.0 volts, the TS55101 enters a pre-charge state and applies a small charge current to safely charge the battery to a level for which full-charge current can be applied. This pre-charge phase is limited by a customer programmable pre-charge timer and current. Once the Full-Charge Mode has been initiated, the regulation will be for constant current (CC). When the battery voltage has increased enough to go into maintenance mode, the PWM control loop will force a constant voltage across the battery. Once in constant voltage mode, current is monitored to determine when the battery is fully charged. See Figure 2.3 for a diagram of the charging states.

This regulation voltage, as well as the 1C charging current, can be set to change based on the battery temperature. There are four temperature ranges for which the regulation voltage can be set independently: 0°C to 10°C, 10°C to 45°C, 45°C to 50°C, and 50°C to 60°C. The TS55101 will stop charging if the temperature passes the descending temperature threshold at 0°C or the ascending threshold at 60°C. These thresholds have 10 degrees of hysteresis. The intermediate points have 1 degree of hysteresis.

The device also incorporates a top off charge mode. The top off charge maximizes the usable battery capacity but increases the total charging time. If the top off timer is set to 0 the charging is terminated at the end-of-charge current level or after the 1C timer elapsed. If the timer is disabled the charging is terminated at the top-off-end current level or if the 1C timer elapsed. Setting a specific time in this register will cause the device to continue charging for this period after the EOC current was reached.

2.1. Pin-Out Assignments

Figure 2.2 TS55101 Pin Assignments



2.2. Pin Description

Table 2.1 Pin Description

Pin #	Name	Function	Description
1	nFLT	Inverted Fault	Open-drain output.
2	EN	Enable Input	When EN is high (> 2.2V), the device is enabled. Ground the pin to disable the device. Includes internal pull-up.
3	SDA	Data Input/Output	I2C data open-drain output
4	SCL	Clock Input	I2C clock input.
5	VTHERM	Battery Temperature Sensor	Node for the thermistor which is located in close proximity to the battery.
6	VDD	5.0V Supply Output	Connected to 100nF capacitor to GND
7	GND	Ground	Primary ground for the majority of the device except the low-side power FET.

Pin #	Name	Function	Description
8	VBAT	Battery Input	Regulator Feedback Input
9	VOUT	System Output Voltage	Positive input for the charge current loop. Connected to 100nF capacitor to GND
10	BOOT	Bootstrap Pin	Connected through 22nF capacitor to SW pin
11	SW	Switching Voltage Node	Connected to 4.7uH (typical) inductor
12	SW	Switching Voltage Node	Connected to 4.7uH (typical) inductor
13	PGND	Power Ground	GND supply for internal low-side FET/integrated diode
14	PGND	Power Ground	GND supply for internal low-side FET/integrated diode
15	VIN	Input Voltage	Power Supply Input voltage
16	VIN	Input Voltage	Power Supply Input voltage
17	GND	Thermal Pad	Tie thermal pad to GND

2.3. Internal Protection

2.3.1. VIN Under-Voltage Lockout (STATUS1, D1)

The device is held in the off state until the EN pin voltage is HIGH (≥ 2.2V) and VIN rises above 4.4V. There is a 200mV (typ) hysteresis on this input, which requires the input to fall below 4.2V (typ) before the device will disable.

2.3.2. Internal Current Limit

The current through the inductor L_{OUT} is sensed on a cycle-by-cycle basis and if the current limit (I_{OCD}; see section 1.4) is reached, the TS55101 will abbreviate the cycle. The current limit is always active when the regulator is enabled.

2.3.3. Thermal Shutdown (STATUS1, D3)

If the junction temperature of the TS55101 exceeds 150°C (typical), the SW output will tri-state to protect the device from damage. The NFLT and all other protection circuitry will stay active to inform the system of the failure mode. Once the device cools to 140°C (typical), the device will attempt to start up again. If the device reaches 150°C, the shutdown/restart sequence will repeat.

2.3.4. VBAT Over-Voltage Protection (STATUS1, D7)

The TS55101 has a battery protection circuit designed to shut down the charging profile if the battery voltage is greater than the termination voltage. The termination voltage can change based on user programming, so the protection threshold is set to 2% above the termination voltage. Shutting down the charging profile puts the TS55101 in a fault condition.

2.3.5. Pre-charge protection Timer (STATUS2, D5)

At the start of the pre charge action the pre charge timer is initialized. If the device is not able to charge the battery up to 3V in the user programmable limited time (CONFIG4, D4/D5), the charging is terminated and the fault is indicated in the corresponding status bit.

2.3.6. 1C protection Timer (STATUS1, D6)

Once the charger enters the CC charge the customer programmable 1C timer (CONFIG4, D6/D7) in initialized. This 1C timer will terminate the charge after it expires. If the cell Voltage is below the programmed termination Voltage minus the Hysteresis a fault is indicated and the charging is blocked. If the Voltage is above that threshold only the dedicated status bit is set, the charging will restart again once the battery voltage passes the threshold.

2.4. Fault Handling

2.4.1. NFLT Pin Functionality and Fault handling

In the event of a battery over-voltage, this will be registered as a fault condition. When 1C timer expires, if VBAT > $V_{RESTART}$ threshold voltage, it is regarded as a warning; if VBAT < $V_{RESTART}$ threshold voltage, it will be registered as a fault. Both TEMP 0C and TEMP 60C are registered as faults; i.e., battery temperature below 0C or above 60C. The Pre-charge timer is also registered as a fault.

Upon detecting a fault, charging stops and the NFLT pin is pulled low. When the fault condition is no longer present, the device will enter the INITIALIZE state (see Figure 2.3). This state is held and the NFLT pin will remain low until the corresponding STATUS1 or 2 register (00_{HEX} or 01_{HEX}) is read (see Table 2.3 and Table 2.4). When the corresponding STATUS1 or 2 register is read, the NFLT pin will go high and charging will restart until a new fault is detected.

For the event of an EEPROM parity error, NFLT will be pulled low and will remain low even if the STATUS2 register is read by the user.

2.4.2. Other warnings

When an open thermistor, thermal shut down, VIN under-voltage, or top-off time-out are detected, charging immediately stops and the corresponding bit in the STATUS1 register (00_{HEX}) is set. The device enters the INITIALIZE state until the warning state is no longer detected.

The open thermistor, TEMP 0C and TEMP 60C faults can be disabled in the corresponding programmable bit in the CONFIG1 register if no thermistor is used.

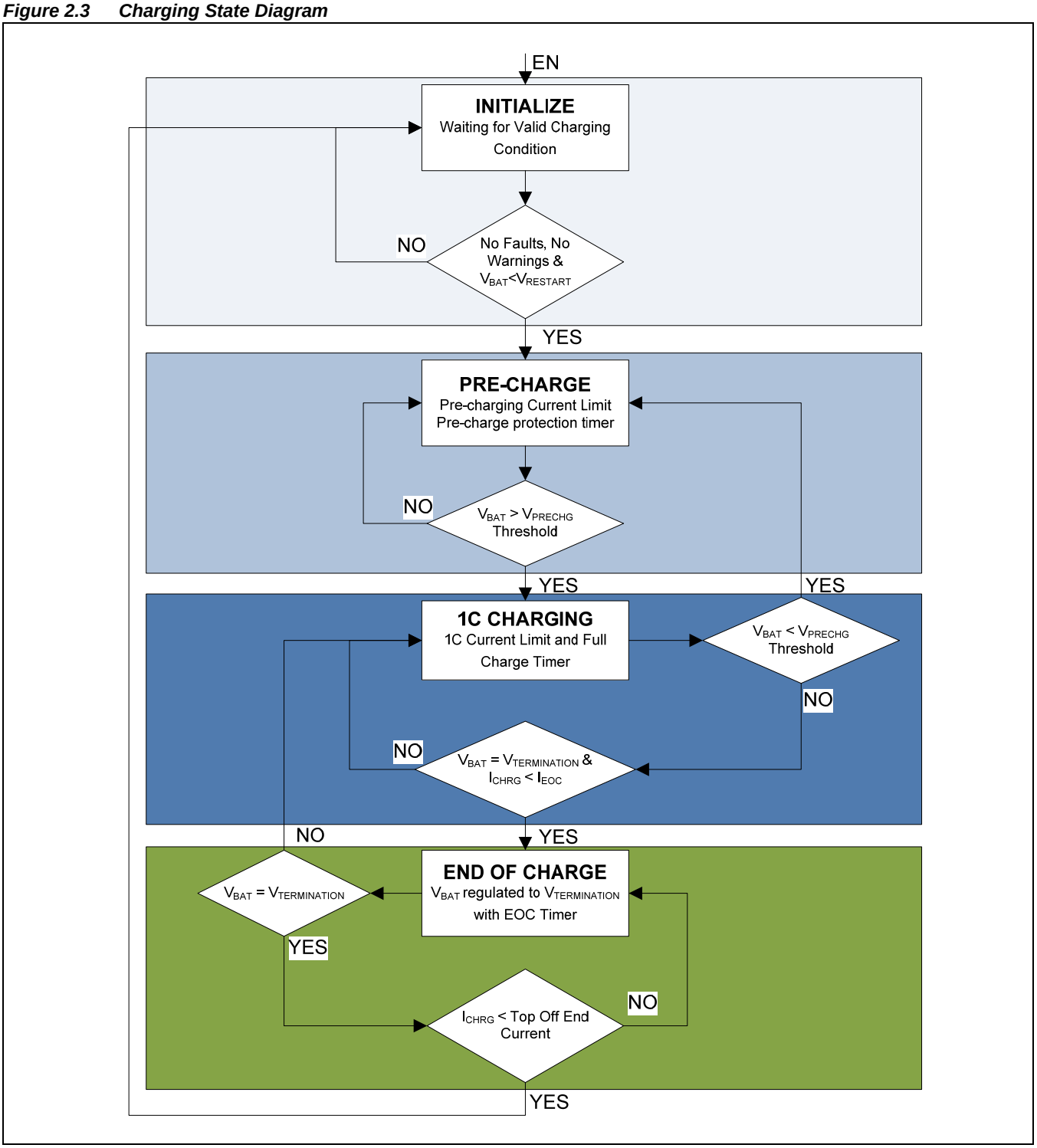
In warning states, the NFLT signal is not pulled to low. Operation will automatically resume after warning condition disappears.

2.5. EEPROM Programing Sequence

The following is a procedure for EEPROM programming in case this is required in an application or make the device default to different charge profile for a different battery.

1. Power up VIN to 9.5V;
2. Write x01 to Register 17, this allows customer register access;
3. Write desired values to Registers 2-7;
4. Write x02 to Register 18, this starts EEPROM erase;
5. Wait at least 100ms;
6. Write x00 to Register 18, this stops the EEPROM erase;
7. Write x01 to Register 18, this starts EEPROM write;
8. Wait at least 100ms;
9. Write x00 to Register 18, this stops EEPROM write;
10. Power cycle;
11. Write x01 to Register 17 to enable customer access;
12. Read back Registers 2-7 to verify.

Figure 2.3 Charging State Diagram



2.6. Serial Interface

The TS55101 features an I²C™ slave interface that offers advanced control and diagnostic features. It supports standard and fast mode data rates and auto-sequencing, and it is compatible with I²C™ standard version 3.0.

I²C™ operation offers configuration control for termination voltages, charge currents, and charge timeouts. This configurability allows optimum charging conditions in a wide range of Li-Ion batteries. I²C™ operation also offers fault and warning indicators. Whenever a fault is detected, the associated status bit in the STATUS1 or STATUS2 register is set and the NFLT pin is pulled low. Whenever a warning is detected, the associated status bit in the STATUS1 register is set, but the NFLT pin is not pulled low. Reading the STATUS1 or STATUS2 register resets the fault and warning status bits, and the NFLT pin is released after all fault status bits have been reset.

2.6.1. I²C™ Sub_address Definition

Figure 2.4 Subaddress in I²C™ Transmission

Slave Adress + R/nW										Subaddress									Data									
Start	G3	G2	G1	G0	A2	A1	A0	R/nW	ACK	S7	S6	S5	S4	S3	S2	S1	S0	ACK	D7	D6	D5	D4	D3	D2	D1	D0	ACK	Stop

Start – Start Condition
G(3:0) – Group ID: Address fixed at 1001b
A(2:0) – Device ID: Address fixed at 001b
R/nW – Read / not Write select bit

ACK - Acknowledge
S(7:0) – Subaddress: Defined per the address register map
D(7:0) – Data: Data to be transmitted with the device
Stop – Stop Condition

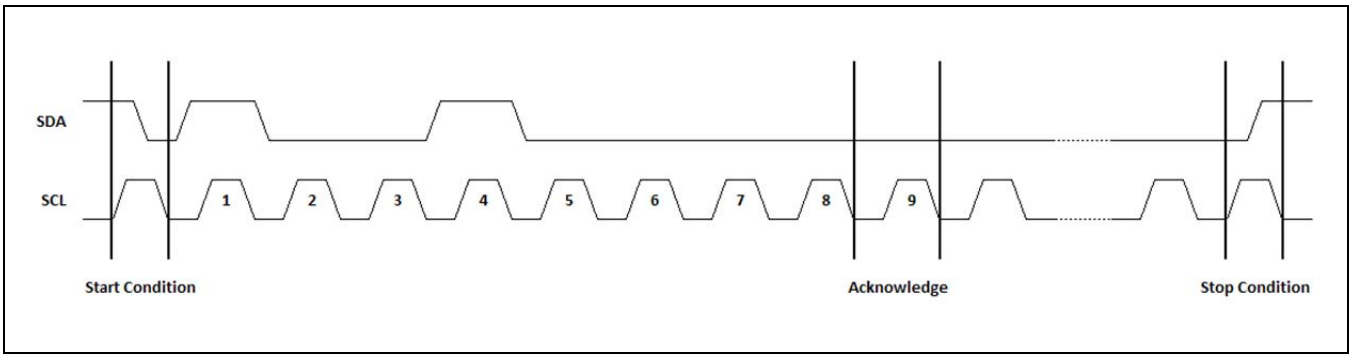
2.6.2. I²C™ Bus Operation

The TS55101's I²C™ is a two-wire serial interface; the two lines are serial clock (SCL) and serial data (SDA) (see Figure 2.5). SDA must be connected to a positive supply (e.g., the VDD pin) through an external pull-up resistor. The devices communicating on this bus can drive the SDA line low or release it to high impedance. To ensure proper operation, setup and hold times must be met (see Table 1.5). The device that initiates the I²C™ transaction becomes the master of the bus.

Communication is initiated by the master sending a START condition, which is a high-to-low transition on SDA while the SCL line is high. After the START condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (read = 1; write = 0). After receiving the valid address byte, the device responds with an acknowledge (ACK). An ACK is a low on SDA during the high of the ACK-related clock pulse. On the I²C™ bus, during each clock pulse, only one data bit is transferred. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as START or STOP control conditions. A low-to-high transition on SDA while the SCL input is high indicates a STOP condition and is sent by the master.

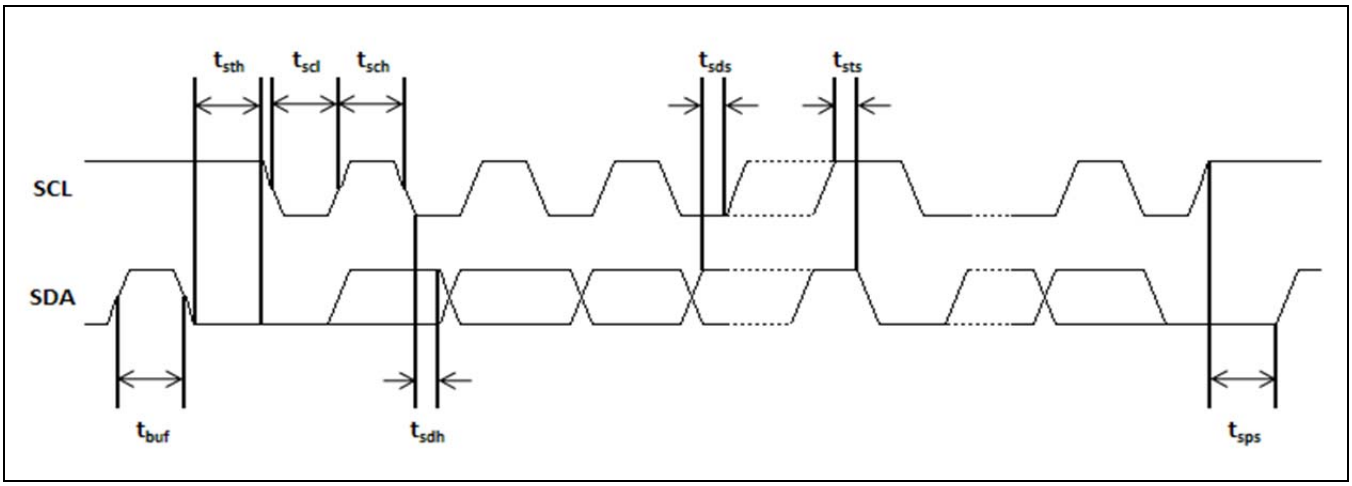
Any number of data bytes can be transferred from the transmitter to receiver between the START and the STOP conditions. Each byte of eight bits is followed by one ACK bit from the receiver. The SDA line must be released by the transmitter before the receiver can send an ACK bit. The receiver that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. An end of data is signaled by the master receiver to the slave transmitter by not generating an acknowledge after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. The transmitter must then release the data line to enable the master to generate a STOP condition.

Figure 2.5 I²C™ Start / Stop Protocol



See Table 1.5 for the definitions and specifications for the timing parameters labeled in Figure 2.6.

Figure 2.6 I²C™ Data Transmission Timing



2.7. Status and Configuration Registers

Table 2.2 Register Descriptions (Device Address = 49_{HEX})

Register	Address	Name	Default	Description
0	00_{HEX}	STATUS1	00_{HEX}	Status bit register
1	01_{HEX}	STATUS2	00_{HEX}	Charging status register
2	02_{HEX}	CONFIG1 0	EEPROM	Configuration register
3	03_{HEX}	CONFIG2 0	EEPROM	Configuration register
4	04_{HEX}	CONFIG3 0	EEPROM	Configuration register
5	05_{HEX}	CONFIG4 0	EEPROM	Configuration register
6	06_{HEX}	CONFIG5 0	EEPROM	Configuration register
7	07_{HEX}	CONFIG6 0	EEPROM	Configuration register
8-16	N/A	N/A	N/A	Registers not implemented
17	11_{HEX}	CONFIG_ENABLE	00_{HEX}	Enable configuration register access
18	12_{HEX}	EEPROM_CTRL 0	00_{HEX}	EEPROM control register

CONFIGx and EEPROM_CTRL registers are only accessible when the CONFIG_ENABLE register is written with the EN_CFG bit set to 1 (see Table 2.11)

Table 2.3 STATUS1 Register—Address 00_{HEX}

Note: All of the STATUS register bits are READ-only.

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	BATT_OV	1C_TO	TEMP_0C	TEMP_60C	TSD	TOP_TO	VIN_UV	TH_OPEN

FIELD NAME	BIT DEFINITION [1)]	Category
BATT_OV	VBAT over-voltage	Fault[1)]
1C_TO	Full charge timer has timed out.	Warning[1)] if VBAT > Vterm - hysteresis otherwise Fault[1)]
TEMP_0C	Thermistor indicates battery temperature < 0°C.	Fault[1)]
TEMP_60C	Thermistor indicates battery temperature > 60°C.	Fault[1)]
TSD	Thermal shutdown.	Warning[1)]
TOP_TO	Top-off timer has timed out.	Warning[1)]
VIN_UV	VIN under-voltage.	Warning[1)]
TH_OPEN	Thermistor open (battery not present).	Warning[1)]

1) Faults are defined as BATT_OV, 1C_TO, PRE_CHG_TO, P_ERR, TEMP_0C and TEMP_60. Warnings are defined as TSD, TOP_TO, VIN_UV, and TH_OPEN. Faults cause the NFLT pin to be pulled low. Warnings do not cause the NFLT pin to be pulled low. All status bits are cleared after STATUS1 or 2 register is read provided the fault no longer exists. The NFLT pin will go to high impedance (open-drain output) and the charging will restart after the STATUS1 or 2 register has been read and all fault bits have been reset. Please also refer to Functional Description 2.4 for 1C_TO fault and warning differentiation.

Table 2.4 STATUS2 Register—Address 01_{HEX}

Note: All of the STATUS register bits are READ-only.

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	P_ERR		PRE_CHG_TO	TERM	EOC	1C_CHG	PRE_CHG	INIT

FIELD NAME	BIT DEFINITION [1)]	Category
P_ERR	Error (parity) in EEPROM memory	Fault[1)]
PRE_CHG_TO	Pre-charge timer has timed out.	Fault[1)]
TERM	Charging Terminated	Status
EOC	End of Charge - Constant voltage mode	Status
1C_CHG	1C Charging – Charging at 1C charging current (programmed value)	Status
PRE_CHG	Pre-Charging – Charging at pre-charge current, battery voltage below 3.0V	Status
INIT	Initialize – Not Charging, waiting for valid charging conditions	Status

A P_ERR fault causes the NFLT pin to be pulled low and charging to stop. NFLT in this condition remains so long as the parity error exists. Parity errors are checked at startup and will block every charging action.

Table 2.5 Configuration Register CONFIG1—Address 02_{HEX}

Note: All of the CONFIG1 register bits are READ/WRITE.

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	PRE_CHRG[1:0]		TOP_END	TEMP_FAULT_DIS	V_TERM_0_10[4:0]			

FIELD NAME	BIT DEFINITION	
PRE_CHRG[1:0] 1)	Pre-charging configuration	00_{BIN} – 50 mA 01_{BIN} – 100 mA 10_{BIN} – 150 mA 11_{BIN} – 200 mA
TOP_END2)	Top Off end configuration	0 – 25mA 1 – 50mA
TEMP_FAULT_DIS3)	Temperature Fault disable	0 – NTC used 1 – NTC not used – disable generated faults
V_TERM_0_10[3:0] 3)	Voltage termination offset: 0-10°C configuration	Input Offset Applied in DEC & BIN 0000 – -0 = -0000; 1000 – -8 = -1000 0001 – -1 = -0001; 1001 – -9 = -1001 0010 – -2 = -0010; 1010 – -10 = -1010 0011 – -3 = -0011; 1011 – -11 = -1011 0100 – -4 = -0100; 1100 – -12 = -1100 0101 – -5 = -0101; 1101 – -13 = -1101 0110 – -6 = -0110; 1110 – -14 = -1110 0111 – -7 = -0111; 1111 – -15 = -1111

1) *PRE_CHRG Note: Maximum output current when 1.7 < V_{out} < 3.0 V.Below 1.7V a constant charge current of 50mA will be supplied to the battery*

2) *TOP_END Note: Charging stops when Vbat = Vtermination and Iout < Top Off end, assuming charging has continued to this point.*

3) *V_TERM Note: There are separate settings for battery temperatures 0-10°C, 10-45°C, 45-50°C , and 50-60°C (see Table 2.5 to Table 2.8 for temperature dependent settings). For <0°C and >60°C, charging is disabled and a fault is indicated. The 10-45°C setting is the base set point for the termination voltage. The other settings are programmed as negative offsets. The '11111' 4.50V base setting cannot be modified by the programmable offset.*

4) *TEMP_FAULT_DIS, if this bit is set high, then under 0°C fault and above 60°C fault will be disabled.*

Table 2.6 Configuration Register CONFIG2—Address 03_{HEX}

Note: All of the CONFIG2 register bits are READ/WRITE.

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	EOC[1:0]		TH	V_TERM_10_45[4:0]				

FIELD NAME	BIT DEFINITION	
EOC[1:0] [1)]	End of charge configuration	00_{BIN} – 50 mA 01_{BIN} – 100 mA 10_{BIN} – 150 mA 11_{BIN} – 200 mA
TH[2)]	Thermistor Configuration	0 – 10kΩ 1 – 100kΩ
V_TERM_10_45[4:0] [3)]	Voltage termination: 10-45°C configuration	00000 – 3.90 V 00001 – 3.92V 00010 – 3.93 V 00011 – 3.95V 00100 – 3.97V 00101 – 3.98V 00110 – 4.00V 00111 – 4.02 V 01000 – 4.03V 01001 – 4.05V 01010 – 4.07V 01011 – 4.09V 01100 – 4.11V 01101 – 4.12V 01110 – 4.14 V 01111 – 4.16V 10000 – 4.18 V 10001 – 4.20V 10010 – 4.22V 10011 – 4.24V 10100 – 4.26 V 10101 – 4.28V 10110 – 4.30 V 10111 – 4.32V 11000 – 4.34V 11001 – 4.36V 11010 – 4.38V 11011 – 4.41V 11100 – 4.43V 11101 – 4.45 V 11110 – 4.47V 11111 – 4.50 V

1) EOC Note: If the EOC current is reached the EOC Status bit will get set (Note: if TOP_TO is not programmed to 000)

2) TH Note: Thermistor characteristic can be programmed with this bit

3) V_TERM Note: There are separate settings for battery temperatures 0-10°C, 10-45°C, 45-50°C , and 50-60°C (see Table 2.5 to Table 2.8 for temperature dependent settings). For <0°C and >60°C, charging is disabled and a fault is indicated. The 10-45°C setting is the base set point for the termination voltage. The other settings are programmed as negative offsets. The '11111' 4.50V base setting cannot be modified by the programmable offset.

Example: *V_TERM computed value using offsets for battery temperature ranges: 0-10°C, 45-50°C and 50-60°C*.

If base code 01000 = 4.03V is set in V_TERM_10_45 and if offset code 0101 = -5 is set in V_TERM_0_10, then the termination code to be used when in temperature range 0-10°C is computed as the base code plus the offset code. Thus the effective code is 01000+(-0101) = 00011 and the value is 3.95V. Note the effective code stops at 00000 regardless of offset.

Table 2.7 Configuration Register CONFIG3—Address 04_{HEX}

Note: All of the CONFIG3 register bits are READ/WRITE.

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	TOP_TO			PARITY	V_TERM_45_50[3:0]			

FIELD NAME	BIT DEFINITION	
TOP_TO[2:0] [1)]	Top Off timer – time out configuration	000 – 0 minutes 001 – 20 minutes 010 – 40 minutes 011 – 60 minutes 100 – 80 minutes 101 – 100 minutes 110 – 120 minutes 111 – Disable time out timer
PARITY	Calculated parity bit based on customer registers (CONFIG1-6) **Important note:** Customer must set this bit after programming for correct operation If this bit is programmed wrong the charging will never start.	
V_TERM_45_50[3:0] [3)]	Voltage termination offset: 45-50°C configuration	Input Offset Applied in DEC & BIN 0000 – -0 = -0000 0001 – -1 = -0001 0010 – -2 = -0010 0011 – -3 = -0011 0100 – -4 = -0100 0101 – -5 = -0101 0110 – -6 = -0110 0111 – -7 = -0111 1000 – -8 = -1000 1001 – -9 = -1001 1010 – -10 = -1010 1011 – -11 = -1011 1100 – -12 = -1100 1101 – -13 = -1101 1110 – -14 = -1110 1111 – -15 = -1111

1) *TOP_TO Note: Timer starts when Vbat= Vtermination and Iout < EOC. If the EOC current is desired to terminate the charging this timer must be set to 0. If the timer is disabled the charging will be terminated at the TOP_END current limit.*

2) *V_TERM Note: There are separate settings for battery temperatures 0-10°C, 10-45°C, 45-50°C , and 50-60°C (see Table 2.5 to Table 2.8 for temperature dependent settings). For <0°C and >60°C, charging is disabled and a fault is indicated. The 10-45°C setting is the base set point for the termination voltage. The other settings are programmed as negative offsets. The '11111' 4.50V base setting cannot be modified by the programmable offset.*

Table 2.8 Configuration Register CONFIG4—Address 05_{HEX}

Note: All of the CONFIG4 register bits are READ/WRITE.

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	1C_TO[1:0]		PRE_CHG_TO		V_TERM_50_60[3:0]			

FIELD NAME	BIT DEFINITION	
1C_TO[1:0] [1)]	Full charge timer time out configuration	00 – Disable full charge timer 01 – 60 minutes 10 – 120 minutes 11 – 600 minutes
PRE_CHG_TO	Pre charge timer time out configuration	00 – 60 minutes 01 – 90 minutes 10 – 120 minutes 11 – 240 minutes
V_TERM_50_60[3:0] [3)]	Voltage termination offset: 50-60°C configuration	Input Offset Applied in DEC & BIN 0000 – -0 = -0000 0001 – -1 = -0001 0010 – -2 = -0010 0011 – -3 = -0011 0100 – -4 = -0100 0101 – -5 = -0101 0110 – -6 = -0110 0111 – -7 = -0111 1000 – -8 = -1000 1001 – -9 = -1001 1010 – -10 = -1010 1011 – -11 = -1011 1100 – -12 = -1100 1101 – -13 = -1101 1110 – -14 = -1110 1111 – -15 = -1111

1) *1C_TO Note: Timer starts when Vbat > 3.0V.*

2) *V_TERM Note: There are separate settings for battery temperatures 0-10°C, 10-45°C, 45-50°C , and 50-60°C (see Table 2.5 to Table 2.8 for temperature dependent settings). For <0°C and >60°C, charging is disabled and a fault is indicated. The 10-45°C setting is the base set point for the termination voltage. The other settings are programmed as negative offsets. The '11111' 4.50V base setting cannot be modified by the programmable offset.*

Table 2.9 Configuration Register CONFIG5—Address 06_{HEX}

Note: All of the CONFIG5 register bits are READ/WRITE.

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	MAX_CHRG_CURR_0_10[3:0]				MAX_CHRG_CURR_10_45[3:0]			

FIELD NAME		BIT DEFINITION	
MAX_CHRG_CURR_0_10[3:0] 1)	Maximum charge current 0-10°C configuration	0000 – 200 mA 0001 – 300 mA 0010 – 400 mA 0011 – 500 mA 0100 – 600 mA 0101 – 700 mA 0110 – 800 mA 0111 – 900 mA	1000 – 1000 mA 1001 – 1100 mA 1010 – 1200 mA 1011 – 1300 mA 1100 – 1400 mA 1101 – 1500 mA 1110 – 1700 mA 1111 – 2000 mA
MAX_CHRG_CURR_10_45[3:0] 1)	Maximum charge current 10-45°C configuration	0000 – 200 mA 0001 – 300 mA 0010 – 400 mA 0011 – 500 mA 0100 – 600 mA 0101 – 700 mA 0110 – 800 mA 0111 – 900 mA	1000 – 1000 mA 1001 – 1100 mA 1010 – 1200 mA 1011 – 1300 mA 1100 – 1400 mA 1101 – 1500 mA 1110 – 1700 mA 1111 – 2000 mA

1) MAX_CHRG_CURR Note: Unique settings available for battery temperatures 0-10°C, 10-45°C, 45-50°C, and 50-60°C. For <0°C and >60°C, charging is disabled and a fault is indicated.

Table 2.10 Configuration Register CONFIG6—Address 07_{HEX}

Note: All of the CONFIG5 register bits are READ/WRITE.

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	MAX_CHRG_CURR_45_50[3:0]				MAX_CHRG_CURR_50_60[3:0]			

FIELD NAME		BIT DEFINITION	
MAX_CHRG_CURR_45_50[3:01)] 1)	Maximum charge current 45-50°C configuration	0000 – 200 mA 0001 – 300 mA 0010 – 400 mA 0011 – 500 mA 0100 – 600 mA 0101 – 700 mA 0110 – 800 mA 0111 – 900 mA	1000 – 1000 mA 1001 – 1100 mA 1010 – 1200 mA 1011 – 1300 mA 1100 – 1400 mA 1101 – 1500 mA 1110 – 1700 mA 1111 – 2000 mA
MAX_CHRG_CURR_50_60[3:0] 1)	Maximum charge current 50-60°C configuration	0000 – 200 mA 0001 – 300 mA 0010 – 400 mA 0011 – 500 mA 0100 – 600 mA 0101 – 700 mA 0110 – 800 mA 0111 – 900 mA	1000 – 1000 mA 1001 – 1100 mA 1010 – 1200 mA 1011 – 1300 mA 1100 – 1400 mA 1101 – 1500 mA 1110 – 1700 mA 1111 – 2000 mA

1) MAX_CHRG_CURR Note: Unique settings available for battery temperatures 0-10°C, 10-45°C, 45-50°C, and 50-60°C. For <0°C and >60°C, charging is disabled and a fault is indicated.

Table 2.11 Enable Configuration Register CONFIG_ENABLE—Address 11_{HEX}

Note: The reset value for all of the CONFIG_ENABLE register bits is 0.

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	Not used	Not used	Not used	Not used	Not used	Not used	EN_CFG
READ/WRITE	R	R	R	R	R	R	R	R/W

FIELD NAME	BIT DEFINITION
EN_CFG	Enable-access control bit for configuration registers CONFIG1 through CONFIG5 (addresses 02_{HEX} to 06_{HEX}) 0_{BIN} – Disable access 1_{BIN} – Enable access

Table 2.12 EEPROM Control Register EEPROM_CTRL—Address 12_{HEX}

Note: The reset value for all of the EEPROM_CTRL register bits is 0.

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	Not used	Not used	Not used	Not used	Not used	EE_ERASE	EE_PROG
READ/WRITE	R	R	R	R	R	R	R/W	R/W

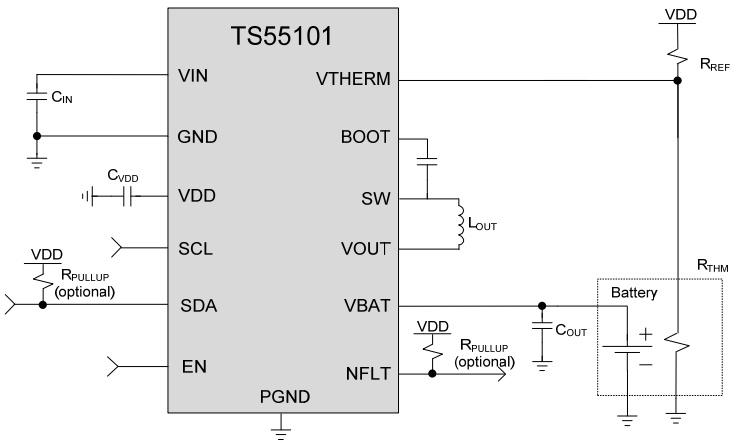
FIELD NAME	BIT DEFINITION
EE_PROG [1)]	EEPROM program control bit for configuration registers CONFIG1 through CONFIG5 (addresses 02_{HEX} to 06_{HEX}) 0_{BIN} – Disable EEPROM programming 1_{BIN} – Enable EEPROM programming with data from configuration registers CONFIG1 through CONFIG5 (addresses 02_{HEX} to 06_{HEX})

1) EE_PROG Note: Inputs VIN and EN must be present for 200ms.

3 Application Circuits

3.1. Typical Application Circuit

Figure 3.1 Typical Application Circuit for Charging a Lithium-Ion Battery



3.2. Selection of External Components

Note that the internal compensation is optimized for a 4.7µF output capacitor (C_{OUT}) and a 4.7µH output inductor (L_{OUT}). Table 1.3 provides recommended ranges for most of the following components.

3.2.1. C_{OUT} Output Capacitor

The 4.7uF capacitor with small ESR can be used for Cout, placed near IC.

3.2.2. L_{OUT} Output Inductor

For best performance, an inductor with a saturation current rating higher than the maximum V_{OUT} load requirement plus the inductor current ripple should be used for the 4.7µH output filter inductor.

3.2.3. C_{IN} Bypass Capacitor

For best performance, a low ESR ceramic capacitor should be used for the 10 µF input supply bypass capacitor. If it is not a low ESR ceramic capacitor, a 0.1µF ceramic capacitor should be added in parallel to C_{IN}. Input supply cap has to be chosen to limit voltage ripple to <10% of VIN.

3.2.4. C_{VDD} Bypass Capacitor for VDD Internal Reference Voltage Output

For best performance, a low ESR ceramic capacitor should be used for the 2.2µ F bypass capacitor from the VDD pin to ground.

3.2.5. Pull-up Resistors

For proper function of the I²C™ interface, the SDA pin must be connected to a positive supply (e.g., the VDD pin) through an external pull-up resistor.

For proper function of the fault warning signal on the NFLT pin, it must be connected to a positive supply (VDD) through an external pull-up resistor.

3.2.6. R_{THM} Thermistor

The internal temperature bins described in Table 1.4 are valid with respect to two different programmable temperature characteristics:

NTC 10k with β=3434K (use a 10k Pullup with this NTC)

NTC 100k with β=4311K (use a 100k Pullup with this NTC)

Of course different NTCs can be used. The general relation of the thermistors resistance can be derived as following: $R_T = R_{25} * e^{\beta(\frac{1}{T+273}*\frac{1}{298})}$

R_T is the resistance of the thermistor at T degree in Celsius, while R_{25} is the initial NTC resistance and β the corresponding temperature coefficient of the NTC.

By choosing a β = 4500 and a parallel 100k to the thermistor for example, the upper temperature protection limit can be reduced by roughly 10K to 50°C (instead of 60°C).

If no thermistor wants to be used, the function must be disabled in the corresponding register.

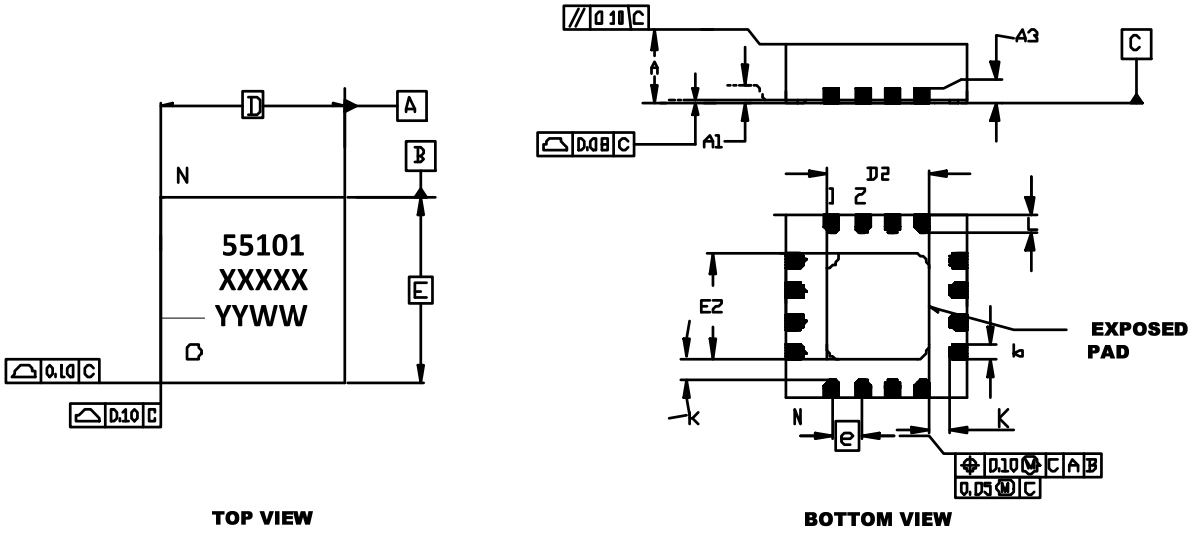
3.2.7. C_{POUT} Pre-Output Capacitor

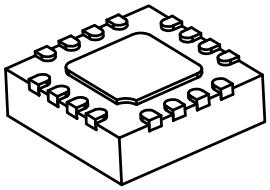
The capacitor on the Output pin of the IC is optional. A low ESR ceramic capacitor is recommended with 100nF if it is used. The Capacitor should be placed close to the IC from VOUT to GND. The evaluation board did not use this capacitor and it is operating properly.

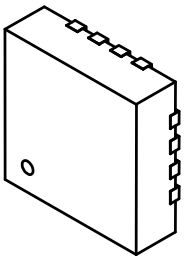
4 Mechanical Specifications

4.1. TS55101 Package Dimensions

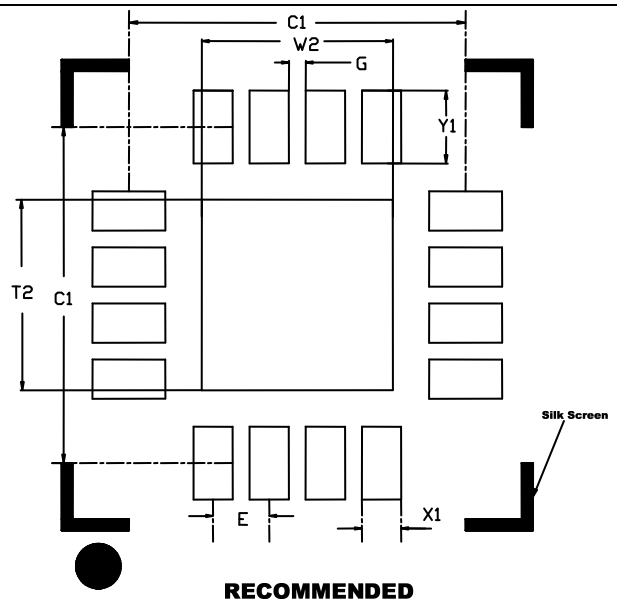
Figure 4.1 PQFN-16 Package Dimensions







Units		MILLIMETERS		
Dimensions Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Width	E2	1.55	1.70	1.80
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.55	1.70	1.80
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.30	0.40
Contact-to-Exposed Pad	K	0.20	-	-



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2	-	-	1.70
Optional Center Pad Length	T2	-	-	1.70
Contact Pad Spacing	C1	-	3.00	-
Contact Pad Spacing	C2	-	3.00	-
Contact Pad Width (X16)	X1	-	-	0.35
Contact Pad Length (X16)	Y1	-	-	0.65
Distance Between Pads	G	0.15	-	-

Notes:
Dimensions and tolerances per ASME Y14.5M. BSC: Basic Dimension. Theoretically exact values shown without tolerances. REF: Reference Dimension, usually without tolerance, for information only.

Pb-Free (RoHS): The TS55101 is Lead-free, fully WEEE and RoHS compliant

MSL, Peak Temp: The TS55101 has a Moisture Sensitivity Level (MSL) 1 rating per JEDEC J-STD-020D.

5 Layout Recommendations

The Layout of the PCB will have big impact on the performance of the TS55101. Care should be taken during the design phase.

It is recommended to maximize the copper area connected to the thermal pad, to dissipate the heat

In a Multi-Layer Layout thermal vias underneath the chip can be used to distribute heat to multiple layers

The output current rating for the linear regulators might need to be de-rated for ambient temperatures above 85°C. The de-rated value will depend on calculated worst case power dissipation and the thermal management implementation in the application.

Improper thermal design of the PCB might lead to thermal shutdown. This will significantly reduce the performance of the system.

Minimizing the loop area of commutation paths can reduce the emitted noise level.

A Layout proposal can be found in the TS55101 Evaluation Kit documentation

6 Ordering Information

Ordering Code	Description	Package
TS55101-QFNR	TS55101 High-Efficiency Charger for Li-Ion Batteries	16-pin PQFN Reel (3,300 pcs)
TS55101EVB	TS55101 evaluation board with USB Dongle and GUI	