DATASHEET

PORTABLE CONSUMER CODEC

LOW-POWER, HIGH-FIDELITY INTEGRATED CODEC

TSCS454xx

DESCRIPTION

The TSCS454xx is a low-power, high-fidelity CODEC with integrated fixed audio DSP's targeted to portable applications such as portable games, personal navigation devices, and personal audio appliances.

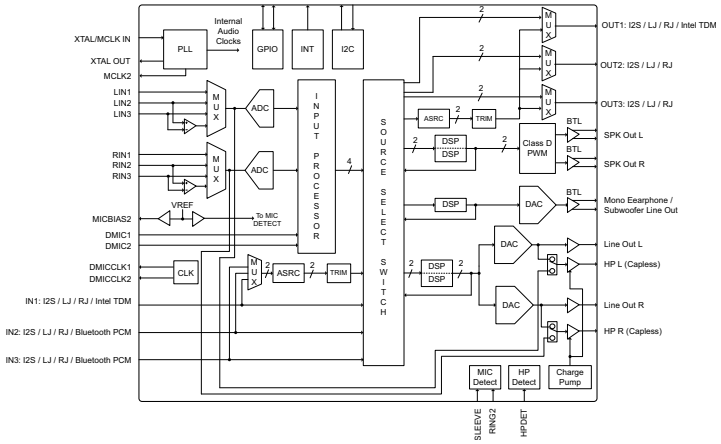
In addition to a high-fidelity low-power CODEC, the device integrates a fixed audio DSP, stereo speaker amplifier, mono earpiece amplifier, and a true cap-less stereo headphone amplifier.

Beyond high-fidelity for portable systems, the device offers an enriched "audio presence" through built-in audio processing capability.

The device has been designed with rapid customization in mind. Tempo is able to rapidly provide varying levels of integration, additional audio processing, according to the needs of large markets or customers.

TARGET APPLICATIONS

- UltraBook, Laptops, Slates, Tablets
- Portable Audio Devices
- Portable Gaming Devices
- Personal Media Players
- Multimedia handsets
- Digital Cameras/Camcorders



FEATURES

- **On-chip Class-H True Cap-less Stereo Headphone Driver**
  - 40 mW output power (16Ω), < 1% THD+N
  - Charge-pump allows true ground centered outputs
  - Headphone/Headset detection logic
  - Global Headset detection logic
  - SNR (A-weighted no active signal) -124dB
  - DNR (A-weighted -60db active signal) -102dB
- **Separate Stereo Line Outputs**
- **High-Fidelity 32-bit ADCs / DACs**
  - 1 Stereo ADC: SNR (A-weighted) 95dB
  - 1 Stereo DAC: SNR (A-weighted) 124dB
  - 1 Mono DAC: SNR (A-weighted) 124dB
- **24-bit Audio Output Processing DSP Engine**
  - Independent processing for up to five audio channels
  - 3D Stereo Enhancement
  - 12-Band Stereo Parametric Equalizers
  - Wideband DRC
  - Pro-Style, Multiband Compressor / Limiter / Expander
  - Psychoacoustic Bass Enhancement
  - High-frequency restoration for compressed audio content
- **Three 32-bit I2S/LJ/RJ input ports & output ports**
  - 8kHz ~ 96kHz Fs support
  - All ports can support I2S / LJ / RJ modes
  - Stereo Asynchronous Sample Rate Converters (In/Out)
  - 1 port can support Intel® TDM formatted data
  - 2 ports can support Bluetooth™ PCM formatted data
- **Stereo Class-D Speaker Driver**
  - Up to 3W/channel 4Ω (10% THD+N)
  - DDX Class-D Technology achieves low EMI while delivering high efficiency
  - Constant output power mode
  - Anti-Pop circuitry
  - Filterless architecture reduces BOM cost
- **Mono Earpiece Amplifier Speaker Driver / Subwoofer Line Output**
  - 40mW output power (16Ω), < 1% THD+N
  - Also capable of driving up to 1Vrms (10KΩ)
- **Microphone/line-in interface**
  - Analog / Digital microphone or Line-in inputs
  - Up to 2 analog mics & 2 digital mics or 4 digital mics
  - Automatic Level Control
  - Dual mic bias generators
- **Low-power with built in power management**
  - 1.6 V CODEC supports 1Vrms output
  - Ultra low standby and no-signal power consumption
  - 1.6V digital / 1.7V analog supply for low power
- **Package**
  - 68-pin, 8x8mm, QFN, 0.4mm pitch

1. OVERVIEW

1.1. Block Diagram

The TSCS454xx is an advanced low power codec with integrated fixed audio DSP's and Class-D amplifiers.To support the design of audio subsystems in a portable device, the TSCS454 features an intelligent codec architecture with fixed audio DSP functions, an integrated true cap-less Class-H headphone amplifier, programmable PLL's, 3W/channel filter-less stereo Class D amplifier, Mono Earpiece channel Class AB amplifier, cap less stereo line out and analog and digital microphone interfaces with programmable gain.

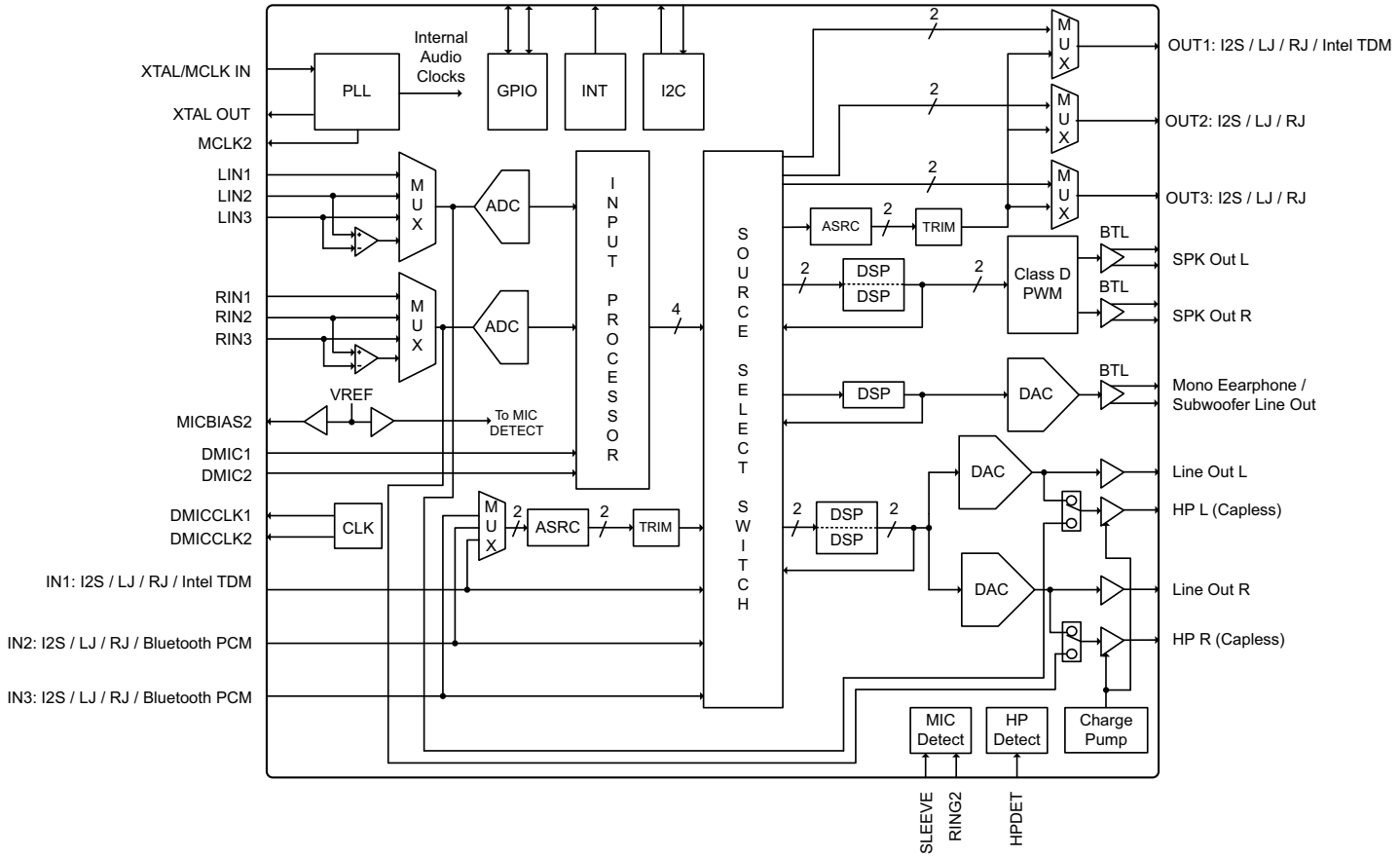


Figure 1. Block Diagram

1.2. Audio Outputs

The TSCS454xx provides multiple outputs for analog sound. Audio outputs include:

- A cap less stereo headphone port (40mw) with ground referenced outputs, capable of driving headphones without requiring an external DC blocking capacitor.
- A cap less stereo docking (line output port) with ground referenced outputs, capable of driving 10K ohm loads without requiring an external DC blocking capacitor.
- A mono, 40mw, Class AB output for driving a headset earpiece or for driving an external earpiece amplifier.
- A stereo 3W /channel filter-less class D amplifier. This amplifier is capable of driving the speakers typically found in portable equipment, providing high fidelity, high efficiency, and excellent sound quality

Outputs feature independent volume controls, including a soft-mute capability which can slowly ramp up or down the volume changes to avoid unwanted audio artifacts.
The TSCS454xx output signal paths consist of digital filters, DACs and output drivers. The digital filters and DACs are enabled when the TSCS454xx is in ‘playback only’ or ‘record and playback’ mode. The output drivers can be separately enabled by individual control bits.

The digital filter and audio processing block processes the data to provide volume control and numerous sound enhancement algorithms. High performance sigma-delta audio DACs convert the digital data into analog.
The digital audio data is converted to over-sampled bit streams using 24-bit digital interpolation filters, which then enters sigma-delta DACs, and become converted to high quality analog audio signals.

To enhance the sound available from the small, low-power speakers typically found in a portable device, the TSCS454xx provides numerous audio enhancement capabilities. The TSCS454xx features dual, independent, programmable Psychoacoustic bass and treble enhancement algorithms achieve a rich, full tone even from originally compressed content, and even with speakers generally unable to play low-frequency sounds, left/right 6-band equalization, allowing the system designer to provide an advanced system equalizer to accommodate the specific speakers and enclosure design. A multi-band compressor features programmable attack and release thresholds, enabling the system designer to attenuate loud noise excursions to avoid speaker artifacts, thus allowing the underlying content to be played at a louder volume without distortion. For compressed audio, a programmable expander is available to help restore the dynamic range of the original content. A programmable limiter provides protection for driving power limited loudspeaker drivers. A stereo depth enhancement algorithm allows common left/right content (e.g. dialog) to be attenuated separately from other content, providing a perceived depth separation between background and foreground audio.

1.3. Audio Inputs

The TSCS454xx provides multiple audio analog and digital inputs. Audio inputs include:

- Three mux selectable stereo analog line/microphone inputs with selectable differential input option.
- Four digital microphone inputs via two stereo input pins.
- Three stereo PCM, I2S type digital audio inputs, with programmable format and Asynchronous Sample Rate Converter. Analog Line Input to Headphone Output bypass path.

A maximum of four input streams can be processed simultaneously through the Input Processor.
The Input Processor provides automatic level control and various gain and volume control functions.

1.4. Digital Audio Interface

Three bi-directional digital audio ports are provided, with one input and output able to go to an ASRC, supporting I2S, Left Justified, Right Justified. these I2S input and/or bluetooth PCM can be configures as TDM type interfaces.

1.5. On-Chip PLLs

Beyond audio processing, the TSCS454xx also provides a higher level of system integration. It contains a low-power, low-jitter clock synthesizer. Using a single fundamental mode crystal the TSCS454xx has two PLLs that can be used to provide internal timing as well as generate a reference output to drive a local applications processor and other peripherals.

2. POWER MANAGEMENT

2.1. Registers

The TSCS454xx has control registers to enable system software to control which functions are active. To minimize power consumption, unused functions should be disabled. To avoid audio artifacts, it is important to enable or disable functions in the correct order

2.1.1. Power Management Register 0

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 51 - 33h PWRM0	7	RSVD	R	0	Reserved
	6	INPROC3PU	RW	0	Input Processor Channel 3 0 = Power down 1 = Power up
	5	INPROC2PU	RW	0	Input Processor Channel2 0 = Power down 1 = Power up
	4	INPROC1PU	RW	0	Input Proceesor Channel 1 0 = Power Down 1 = Pouwer Up
	3	INPROC0PU	RW	0	Input Proceesor Channel 0 0 = Power Down 1 = Pouwer Up
	2	MICB2PU	RW	0	MICBIAS2 0 = Power down 1 = Power up
	1	MICB1PU	RW	0	MICBIAS1 0 = Power down 1 = Power up
	0	MCLKPEN	RW	1	Master clock enable 0: master clock disabled 1: master clock enabled

Table 1. PWRM0 Register

2.1.2. Power Management Register 1

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 52 - 34h PWRM1	7	SUBPU	RW	0	SUB Output Buffer Enable 0 = Power down 1 = Power up
	6	HPLPU	RW	0	Left Headphone Output Buffer 0 = Power down 1 = Power up
	5	HPRPU	RW	0	Right Headphone Output Buffer 0 = Power down 1 = Power up
	4	SPKLPU	RW	0	Left Speaker Output Buffer Enable 0 = Power down 1 = Power up
	3	SPKRPU	RW	0	Right Speaker Output Buffer Enable 0 = Power down 1 = Power up
	2	D2S2PU	RW	0	Analog in D2S2 AMP Power Down 0 = Power down 1 = Power up
	1	D2S1PU	RW	0	Analog in D2S1 AMP Power Down 0 = Power down 1 = Power up
	0	RSVD	R	0	RVSD

Table 2. PWRM1 Register

2.1.3. Power Management Register 2

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 53 - 35h PWRM2	7:6	RSVD	R	0	Reserved
	5	I2S3OPU	RW	0	I2S3 Output Power Down 0 = I2S3 Output Powered down 1 = I2S3 Output Powered up
	4	I2S2OPU	RW	0	I2S2 Output Power Down 0 = I2S2 Output Powered down 1 = I2S2 Output Powered up
	3	I2S1OPU	RW	0	I2S1 Output Power Down 0 = I2S Output Powered down 1 = I2S Output Powered up
	2	I2S3IPU	RW	0	I2S3 Input Power Down 0 = I2S Input Powered down 1 = I2S Input Powered up
	1	I2S2IPU	RW	0	I2S2 Input Power Down 0 = I2S Input Powered down 1 = Input Powered up
	0	I2S1IPU	RW	0	I2S1 Input Power Down 0 = I2S Input Powered down 1 = I2S Input Powered up

Table 3. PWRM2 Register

2.1.4. Power Management Register 3

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 54 - 36h PWRM3	7	RSVD	R	0	Reserved
	6	BGSBUP	RW	0	Bandgap and self bias power up 0 = Powered Up 1 = Powered Down
	5	VGBAPU	RW	0	Input path VGB amplifier power up 0 = Powered Up 1 = Powered Down
	4	LLINEPU	RW	0	Left Line Output Buffer 0 = Power down 1 = Power up
	3	RLINEPU	RW	0	Right Line Output Buffer 0 = Power down 1 = Power up
	2:0	RSVD	R	0	Reserved

Table 4. PWRM3 Register

2.1.5. Power Management Register 4

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 55 - 37h PWRM4	7-5	RSVD	R	0	Reserved
	4	OPSUBPU	RW	0	Output Processor Sub Channel Power Down 0 = Powered Down 1 = Powered Up
	3	OPHPLPU	RW	0	Output Processor Headphone Left Channel Power Down 0 = Powered Down 1 = Powered Up
	2	OPHPRPU	RW	0	Output Processor Headphone Right Channel Power Down 0 = Power Down 1 = Power Up
	1	OPSPKLPU	RW	0	Output Processor Speaker Left Channel Power Downr 0 = Power Down 1 = Power Up
	0	OPSPKRPU	R	0	Output Processor Speaker Right Channel Power Downr 0 = Power Down 1 = Power Up

Table 5. PWRM4 Register

3. OUTPUT AUDIO PROCESSING

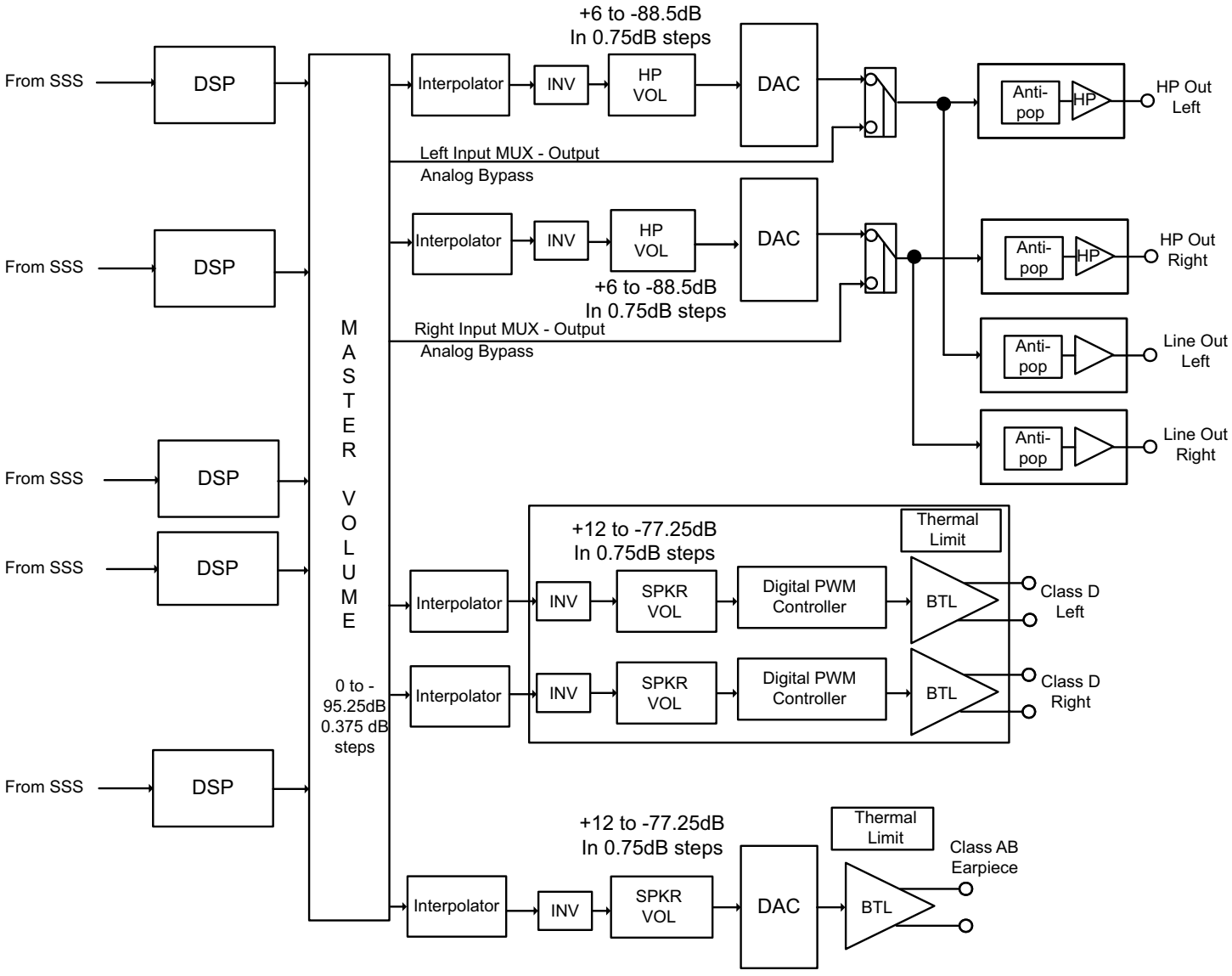


Figure 2. Output Processing Flow

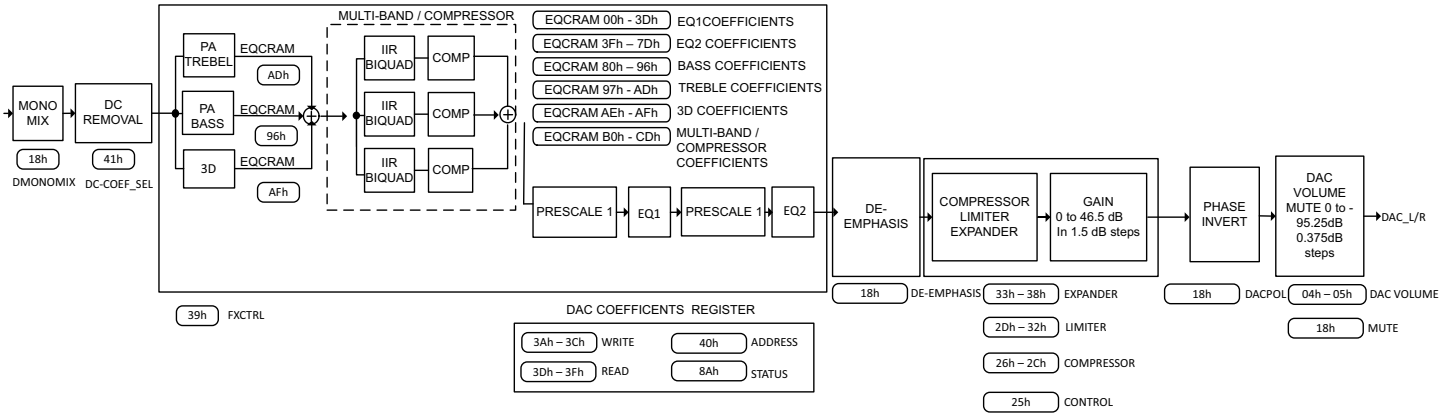


Figure 3. Output Audio DSP Processor

Note: The Output Processor's audio processing functions can exceed the available DSP processing cycles when operating at audio sample rates above 48KHz. When operating at sample rates above 48KHz the number of audio processing functions that can be enabled simultaneously will be limited by the total number of DSP processing cycles available. The maximum number of DSP processing cycles is 383.The number of DSP processing cycles required for each function. When operating at audio sample rates above 48KHz the total number of used DSP processing cycles must be less than 383.

DSP Processing Block	DSP Processing Cycles
Bass Enhancement	77
Treble Enhancement	65
3D	7
Multi-band Compressor Band 1	50
Multi-band Compressor Band 1	50
Multi-band Compressor Band 1	50
EQ1	83
EQ2	83
De-emphasis	13
Compressor-Expander-Limiter	21

Table 6. DSP Processing Cycles

3.1. DC Removal

Before processing, a DC removal filter removes the DC component from the incoming audio data. The DC removal filter is programmable.

Register Address	Bit	Label	Type	Default	Description
PAGE 2, Reg 4 - 4h DCCON	D7	SUBDCBP	RW	0	SUB DC Removal Bypass 0 = not bypassed 1 = bypassed
	D6	DACDCBP	RW	0	DAC DC Removal Bypass 0 = not bypassed 1 = bypassed
	D5	SPKDCBP	RW	0	Speaker DC Removal Bypass 0 = not bypassed 1 = bypassed
	D4:D3	RSVD	R	0	Reserved

	D2-D0	DCCOEFSEL[2:0]	RW	101	DC Offset
					0: dc_offset = 24'h100000; //2^^-3 = 0.125
					1: dc_offset = 24'h040000;
					2: dc_offset = 24'h010000;
					3: dc_offset = 24'h004000;
					4: dc_offset = 24'h001000;
					5: dc_offset = 24'h000400;
					6: dc_offset = 24'h000100; //2^^-15 = 0.00030517
					7: dc_offset = 24'h000040; //2^^-17

Table 7. DCCON Register

3.2. Volume Control Functions

The Volume Update bits control the updating of volume control data; when a bit is written as ‘0’, the Left Volume control associated with that bit is updated whenever the left volume register is written and the Right Volume control is updated when ever the right volume register is written. When a bit is written as ‘1’, the left volume data is placed into an internal holding register when the left volume register is written and both the left and right volumes are updated when the right volume register is written. This enables a simultaneous left and right volume update

Register Address	Bit	Label	Type	Default	Description
Page 2 , Reg 6 - 6h OVOLCTLU	7:5	RSVD	R	0	Reserved
	4	DACFADE	RW	1	1 = volume fades between old/new value 0 = volume/mute changes immediately
	3	SUBVOLU	RW	0	0 = SUB speaker volume updated immediately 1 = SUB speaker volume held until right speaker volume register written.
	2	DACVOLU	RW	0	0 = Left DAC volume updated immediately 1 = Left DAC volume held until right DAC volume register written.
	1	SPKVOLU	RW	0	0 = Left Speaker volume updated immediately 1 = Left Speaker volume held until right DAC volume register written.
	0	HPVOLU	RW	0	0 = Left headphone volume updated immediately 1 = Left headphone volume held until right headphone volume register written.

Table 8. OVOLCTLU Register

The output path may be muted automatically when a long string of zero data is received. The length of zeros is programmable and a detection flag indicates when a stream of zero data has been detected.

Register Address	Bit	Label	Type	Default	Description
Page 2, Reg 7 - 7h MUTEC	7	ZEROSTAT	R	0	1 = zero detect length exceeded.
	6	RSVD	R	0	Reserved for future use.
	5:4	ZDETLEN[1:0]	RW	2	Enable mute if input consecutive zeros exceeds this length. 0 = 512, 1 = 1k, 2 = 2k, 3 = 4k samples
	3	RSVD	R	0	Reserved for future use.
	2	AMUTE	RW	1	1 = auto mute if detect long string of zeros on input
	1:0	RSVD	R	0	Reserved for future use.

Table 9. MUTEC Register

3.3. Master Volume Control

The signal volume can be controlled digitally, across a gain and attenuation range of -95.25dB to 0dB (0.375dB steps). The level of attenuation is specified by an eight-bit code, 'MVOLx', where 'x' is L, or R. The value "00000000" indicates mute; other values select the number of 0.375dB steps above -95.625dB for the volume level.

In each Output Processor block there is a digital volume control that is mapped to this control register. Changing the value in this register will adjust the volume of all the outputs (Speaker, Headphone, Earpiece) simultaneously. The signal volume can be controlled digitally, across a gain and attenuation range of -95.25dB to 0dB (0.375dB steps). The level of attenuation is specified by an eight-bit code, 'MVOL_x', where 'x' is L, or R. The value "00000000" indicates mute; other values select the number of 0.375dB steps above -95.625dB for the volume level.

Register Address	Bit	Label	Type	Default	Description
Page 2, Reg 8 - 8h MVOLL	7:0	MVOL_L [7:0]	RW	FF (0dB)	Left Master Volume Level 0000 0000 = Digital Mute 0000 0001 = -95.25dB 0000 0010 = -94.875dB ... 0.375dB steps up to 1111 1111 = 0dB Note: If DACVOLU is set, this setting will take effect after the next write to the Right Input Volume register.
Page 2, Reg 9 - 9h MVOLR	7:0	MVOL_R [7:0]	RW	FF (0dB)	Right Master Digital Volume Level 0000 0000 = Digital Mute 0000 0001 = -95.25dB 0000 0010 = -94.875dB ... 0.375dB steps up to 1111 1111 = 0dB

Table 10. MVOLL/MVOLR Register

3.4. Effects Processing

The TSCS454xx offers Bass enhancement, Treble enhancement, Stereo Depth enhancement. The output effects processing is outlined in the following sections.

3.4.1. Effects Control (xFXCTL) Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 53 - 35h xFXCTL	7:5	RSVD	R	000	Reserved
	4	3DEN	RW	0	3D Enhancement Enable 0 = Disabled 1 = Enabled
	3	TEEN	RW	0	Treble Enhancement Enable 0 = Disabled 1 = Enabled
	2	TNLFBYP	RW	0	Treble Non-linear Function Bypass: 0 = Enabled 1 = Bypassed
	1	BEEN	RW	0	Bass Enhancement Enable 0 = Disabled 1 = Enabled
	0	BNLFBYP	RW	0	Bass Non-linear Function Bypass: 0 = Enabled 1 = Bypassed

Table 11. xFXCTL Register

Note 1: 3D Enhancement is not available for the Earpiece processing channel.

3.4.2. Stereo Depth (3D) Enhancement

The TSCS454xx has a digital depth enhancement option to artificially increase the separation between the left and right channels, by enabling the attenuation of the content common to both channels. The amount of attenuation is programmable within a range. The input is prescaled (fixed) before summation to prevent saturation. The Earpiece channel, due to its mono nature, does support this function.

The 3D enhancement algorithm is a tried and true algorithm that uses two principles.

1 If the material common to the two channels is removed, then the speakers will sound more 3D.

2 If the material for the opposite channel is presented to the current channel inverted, it will tend to cancel any material from the opposite channel on the current ear. For example, if the material from the right channel speaker is presented to the left ear inverted, it will cancel some of the material from the right ear that is leaking to the left ear. This is commonly referred to as crosstalk cancellation

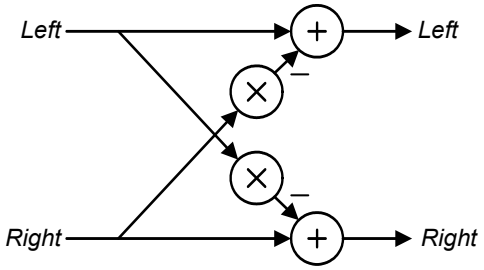


Figure 4. 3D Mixer Diagram

3D_Mix specifies the amount of the common signal that is added from the left and right channels. This number is a fractional amount between -1 and 1. For proper operation, this value is typically negative.

3.4.3. Psychoacoustic Bass Enhancement

One of the primary audio quality issues with small speaker systems is their inability to reproduce significant amounts of energy in the bass region (below 200Hz). While there is no magic mechanism to make a speaker reproduce frequencies that it is not capable of, there are mechanisms for fooling the ear into thinking that the bass material is being heard.

The psychoacoustic bass processor relies on a psychoacoustic principle called “missing fundamental”. If the human ear hears a proper series of harmonics for a particular bass note, the listener will hear the fundamental of that series, even if it is not present.

3.4.4. Psychoacoustic Treble Enhancement

One of the mechanisms used to limit the bit rate for compressed audio is to first remove high frequency information before compression. When these files like low bit rate MP3 are decompressed, this can lead to dull sounding audio. The Tempo treble enhancement replaces these lost high frequencies.

The psychoacoustic treble processor relies on a psychoacoustic principle called “missing fundamental”. If the human ear hears a proper series of harmonics for a particular treble note, the listener will hear the fundamental of that series, even if it is not present

3.5. Multi-band Compressor

The TSCS454xx output processing includes a multi-band compressor that improves sound from small loudspeakers typically used in portable devices. Three independent compressor blocks are each preceded by a, 2-stage, Bi-quad processing block that filters the incoming audio so that each compressor operates on a select range of audio frequencies. The advantage of multiband compression over full-bandwidth (full-band, or single-band) compression is that audible gain "pumping" can be reduced. When using single band compressors high energy audio content in a narrow range of frequencies can cause the volume of the entire audio frequency band to be affected thus causing the audio signal level to audibly “pump”. This pumping of the audio signal level can be distracting. A multi-band compressor can effectively eliminate or reduce the pumping to insignificant levels.

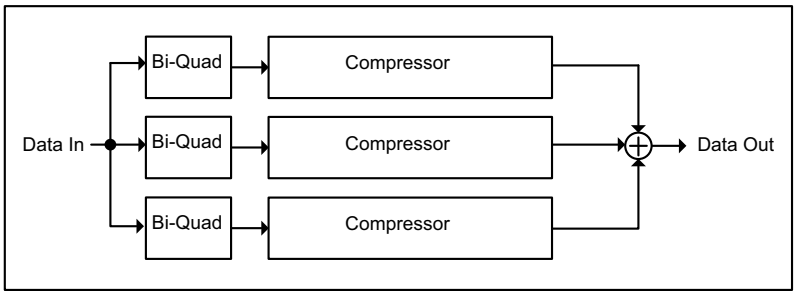


Figure 5. Block Diagram Multiband Compressor

Each band in the Multi-band Compressor is comprised of a single stage 6-tap IIR (Bi-quad) filter followed by a compressor block. The BI-quad filter coefficients are written using the Parametric Equalizer Registers. The purpose of the Bi-quad block is to provide a bandpass filter function for each Compressor band.

For a description of the Compressor function please see Gain, Limiting, and Dynamic Range Control

3.5.1. Multi-band_Compressor Registers

3.5.1.1. Multi-band_Compressor Enable Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 10 - 0Ah xMBCEN	7:3	RSVD	R	0h	Reserved
	2	xMBCEN3	RW	0	1 = enable compressor band 3
	1	xMBCEN2	RW	0	1 = enable compressor band 2
	0	xMBCEN1	RW	0	1 = enable compressor band 1

Table 12. xMBCEN Register

3.5.1.2. x_Multi-band_Compressor Control (xMBCCTL)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 11 - Bh xMBCCTL	7:6	RSVD	R	0h	Reserved
	5	LVLMODE3	RW	0	Compressor Level Detection Mode Band 3 0 = Average 1 = Peak
	4	WINSEL3	RW	0	Window width selection for level detection Band 3 0 = equivalent of 512 samples of selected Base Rate (~10-16ms) 1 = equivalent of 64 samples of selected Base Rate (~1.3-2ms)
	3	LVLMODE2	RW	0	Compressor Level Detection Mode Band 2 0 = Average 1 = Peak
	2	WINSEL2	RW	0	Window width selection for level detection Band 2 0 = equivalent of 512 samples of selected Base Rate (~10-16ms) 1 = equivalent of 64 samples of selected Base Rate (~1.3-2ms)
	1	LVLMODE1	RW	0	Compressor Level Detection Mode Band 1 0 = Average 1 = Peak
	0	WINSEL1	RW	0	Window width selection for level detection Band1 0 = equivalent of 512 samples of selected Base Rate (~10-16ms) 1 = equivalent of 64 samples of selected Base Rate (~1.3-2ms)

Table 13. xMBCCTL Register

3.5.1.3. x_Multi-band_Compressor Make-up Gain Band 1(xMBCMUG1) Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 12 - Ch xMBCMUG1	7:6	RSVD	R	0h	Reserved
	5	PHASE	RW	0h	Phase of Compressor Band Output 0 = Not inverted 1 = Inverted
	4:0	MUGAIN1[4:0]	RW	0h	0dB...46.5dB in 1.5dB steps

Table 14. xMBCMUG1 Register

3.5.1.4. x_Multi-band_Compressor Threshold Band 1(xMBCTHR1)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 13 - Dh xMBCTHR1	7:0	THRESH[7:0]	RW	00h	FFh...00h = 0dB...95.625dB in 0.375dB steps.

Table 15. xMBCTHR1 Register

3.5.1.5. x_Multi-band_Compression Ratio Band 1(xMBCRAT1)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 14 - Eh xMBCRAT1	7:5	RSVD	R	000	Reserved
	4:0	RATIO[4:0]	RW	00h	Compressor Ratio 00h = Reserved 01h = 1.5:1 02h...14h = 2:1...20:1 15h...1Fh = Reserved

Table 16. xMBCRAT1 Register

3.5.1.6. x_Multi-band_Compressor Attack Time Constant Band 1(xMBCATK1L) (Low)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 15 - Fh xMBCATK1L	7:0	TCATKL[7:0]	RW	00h	Low byte of the time constant used to ramp to a new gain value during a compressor attack phase. 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 17. xMBCATK1L Register

3.5.1.7. x_Multi-band_Compressor Attack Time Constant Band 1(xMBCATK1H) (High)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 16 - 10h xMBCATK1H	7:0	TCATKH1[7:0]	RW	00h	High byte of the time constant used to ramp to a new gain value during a compressor attack phase. 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 18. xMBCATK1H Register

3.5.1.8. x_Multi-band_Compressor Release Time Constant Band 1(xMBCREL1L) (Low)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 17 - 11h xMBCREL1L	7:0	TCRELL1[7:0]	RW	00h	Low byte of the time constant used to ramp to a new gain value during a compressor release phase. 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 19. xMBCREL1L Register

3.5.1.9. x_Multi-band_Compressor Release Time Constant Band 1(xMBCREL1H) (High)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 18 - 12h xMBCREL1H	7:0	TCRELH1[15:8]	RW	00h	High byte of the time constant used to ramp to a new gain value during a compressor release phase. The time constant is [high byte, low byte] 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 20. xMBCREL1H Register

3.5.1.10. x_Multi-band_Compressor Make-up Gain Band 2(xMBCMUG2) Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 19 - 13h xMBCMUG2	7:6	RSVD	R	0h	Reserved
	5	PHASE2	RW	0h	0 = Not inverted 1 = Inverted
	4:0	MUGAIN2[4:0]	RW	0h	0dB...46.5dB in 1.5dB steps

Table 21. xMBCMUG2 register

3.5.1.11. x_Multi-band_Compressor Threshold Band 2(xMBCTHR2) Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 20 - 14h xMBCTHR2	7:0	THRESH2[7:0]	RW	00h	FFh...00h = 0dB...95.625dB in 0.375dB steps.

Table 22. xMBCTHR2 Register

3.5.1.12. x_Multi-band_Compression Ratio Band 2(xMBCRAT2) Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 21 - 15h xMBCRAT2	7:5	RSVD	R	000	Reserved
	4:0	RATIO2[4:0]	RW	00h	Compressor Ratio 00h = Reserved 01h = 1.5:1 02h...14h = 2:1...20:1 15h...1Fh = Reserved

Table 23. xMBCRAT2 Register

3.5.1.13. x_Multi-band_Compressor Attack Time Constant Band 2(xMBCATK2L) Register (Low)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 22 - 16h xMBCATK2L	7:0	TCATKL2[7:0]	RW	00h	Low byte of the time constant used to ramp to a new gain value during a compressor attack phase. 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 24. xMBCATK2L Register

3.5.1.14. x_Multi-band_Compressor Attack Time Constant Band 2(xMBCATK2H) Register (High)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 23 - 17h xMBCATK2H	7:0	TCATKH2[7:0]	RW	00h	High byte of the time constant used to ramp to a new gain value during a compressor attack phase. 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 25. xMBCATK2H Register

3.5.1.15. x_Multi-band_Compressor Release Time Constant Band 2(xMBCREL2L) Register (Low)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 24 - 18h xMBCREL2L	7:0	TCRELL2[7:0]	RW	00h	Low byte of the time constant used to ramp to a new gain value during a compressor release phase. 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 26. xMBCREL2L Register

3.5.1.16. x_Multi-band_Compressor Release Time Constant Band 2(xMBCREL2H) Register (High)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 25 - 19h xMBCREL2H	7:0	TCRELH2[15:8]	RW	00h	High byte of the time constant used to ramp to a new gain value during a compressor release phase. The time constant is [high byte, low byte] 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 27. xMBCREL2H Register

3.5.1.17. x_Multi-band_Compressor Make-up Gain Band 3(xMBCMUG3) Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 26 - 1Ah xMBCMUG3	7:6	RSVD	R	0h	Reserved
	5	PHASE3	RW	0h	0 = Not inverted 1 = Inverted
	4:0	MUGAIN3[4:0]	RW	0h	0dB...46.5dB in 1.5dB steps

Table 28. xMBCMUG3 Register

3.5.1.18. x_Multi-band_Compressor Threshold Band 3(xMBCPTHR3) Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 27 - 1Bh xMBCTHR3	7:0	THRESH3[7:0]	RW	00h	FFh...00h = 0dB...95.625dB in 0.375dB steps.

Table 29. xMBCTHR3 Register

3.5.1.19. x_Multi-band_Compressor Compression Ratio Band 3(xMBCRAT3) Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 28 - 1Ch xMBCRAT3	7:5	RSVD	R	000	Reserved
	4:0	RATIO3[4:0]	RW	00h	Compressor Ratio 00h = Reserved 01h = 1.5:1 02h...14h = 2:1...20:1 15h...1Fh = Reserved

Table 30. xMBCRAT3 Register

3.5.1.20. x_Multi-band_Compressor Attack Time Constant Band 3(xMBCATK3L) Register (Low)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 29 - 1Dh xMBCATK3L	7:0	TCATKL3[7:0]	RW	00h	Low byte of the time constant used to ramp to a new gain value during a compressor attack phase. 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 31. xMBCATK3L Register

3.5.1.21. x_Multi-band_Compressor Attack Time Constant Band 3(xMBCATK3H) Register (High)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 30 - 1E xMBCATK3H	7:0	TCATKH3[7:0]	RW	00h	High byte of the time constant used to ramp to a new gain value during a compressor attack phase. 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 32. xMBCATK3H Register

3.5.1.22. x_Multi-band_Compressor Release Time Constant Band 3(xMBCREL3L) Register (Low)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 31 - 1Fh xMBCREL3L	7:0	TCREL3L[7:0]	RW	00h	Low byte of the time constant used to ramp to a new gain value during a compressor release phase. 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 33. xMBCREL3L Register

3.5.1.23. x_Multi-band_Compressor Release Time Constant Band 3(xMBCREL3H) Register (High)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 32 - 20h xMBCREL3H	7:0	TCRELH3[15:8]	RW	00h	High byte of the time constant used to ramp to a new gain value during a compressor release phase. The time constant is [high byte, low byte] 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 34. xMBCREL3H Register

3.6. Parametric Equalizer

The TSCS454xx has a dual, 6-band, digital parametric equalizer to enable fine tuning of the audio response and preferences for a given system. For the Speaker and DAC output channels the EQ filters are stereo. For the Earpiece channel the EQ filters are mono. This difference is reflected in the coefficient RAM table mapping. See Table and Table 45. Each EQ may be enabled or disabled independently. Typically one EQ will be used for speaker compensation and disabled when only headphones are in use while the other EQ is used to alter the audio to make it more pleasing to the listener.This function operates on the digital audio data before it is converted back to analog by the audio DACs.

3.6.1. Prescaler & Equalizer Filter

The Equalizer Filter consists of a Prescaler and 6 IIR Filters. The Prescaler allows the input to be attenuated prior to the EQ filters in case the EQ filters introduce gain, and would thus clip if not prescaled.

Tempo provides a tool to enable an audio designer to determine appropriate coefficients for the equalizer filters. The filters enable the implementation of a parametric equalizer with selectable frequency bands, gain, and filter characteristics (high, low, or bandpass).

Prescaler & EQ Filters

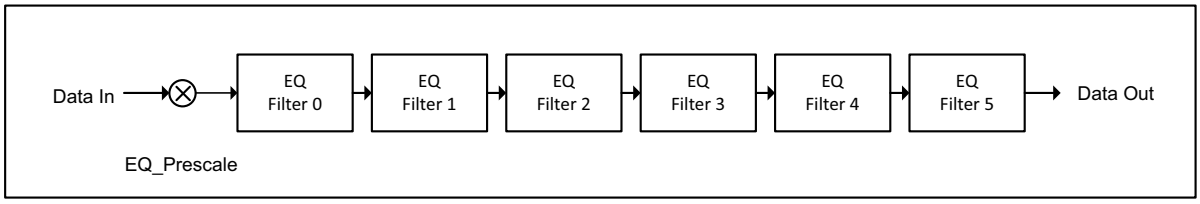


Figure 6. Prescale & Equalizer Filter Diagram

3.6.2. EQ Filter Register

3.6.2.1. EQ Filter Control (xEQFILT) Registers

Where x = SPK, DAC, SUB, y = Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 1 - 1h xEQFILT	7	EQ2_EN	R/W	0	EQ bank 2 enable 0 = second EQ bypassed 1 = second EQ enabled
	6:4	EQ2BE[2:0]	R/W	0	EQ2 band enable. When the EQ is enabled the following EQ stages are executed. 0 - Prescale only 1 - Prescale and Filter Band 0 ... 6 - Prescale and Filter Bands 0 to 5 7 - RESERVED
	3	EQ1EN	R/W	0	EQ bank 1 enable 0 = first EQ bypassed 1 = first EQ enabled
	2:0	EQ1BE[2:0]	R/W	0	EQ1 band enable. When the EQ is enabled the following EQ stages are executed. 0 - Prescale only ... 6 - Prescale and Filter Bands 0 to 5 7 - RESERVED

Table 35. xEQFILT Register

3.6.2.2. EQ Write/Read Data Coefficient Registers

These two 24-bit registers provide the 24-bit data holding registers used when doing indirect writes/reads to the EQ Coefficient RAM.

EQ Coefficient Write Data Low (xCRWDL) Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 2 -2h xCRWDL	7:0	WDATA_L[7:0]	R/W	0	**Low byte of a 24-bit data register, contains the values to be written to the EQ Coefficient RAM. The address written will have be specified by the EQ Coefficient RAM Address fields.**

Table 36. xCRWDL Register

EQ Coefficient Write Data Mid (xCRWDM) Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 3 - 3h xCRWDM	7:0	WDATA_M[15:8	R/W	0	Middle byte of a 24-bit data register, contains the values to be written to the **EQ Coefficient RAM**. The address written will have be specified by the **EQ Coefficient RAM** Address fields.

Table 37. xCRWDM Register

EQ Coefficient Write Data High (xCRWDH)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 4 - 4h xCRWDH	7:0	WDATA_H[23:16]	R/W	0	High byte of a 24-bit data register, contains the values to be written to the **EQ Coefficient RAM**. The address written will have be specified by the **EQ Coefficient RAM** Address fields.

Table 38. xCRWDH Register

EQ Coefficient Read Data Low (xCRRDL)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 5 -5h xCRRDL	7:0	RDATA_L[7:0]	R	0	Low byte of a 24-bit data register, contains the contents of the most recent **EQ Coefficient RAM** address read from the RAM. The address read will have been specified by the **EQ Coefficient RAM** Address fields.

Table 39. xCRRDL Register

EQ Coefficient Read Data Low (xCRRDM)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 6 - 6h xCRRDM	7:0	RDATA_M[15:8]	R	0	Middle byte of a 24-bit data register, contains the contents of the most recent **EQ Coefficient RAM** address read from the RAM. The address read will have been specified by the **EQ Coefficient RAM** Address fields.

Table 40. xCRRDM Register

EQ Coefficient Read Data HIgh (xCRRDH)

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 7 -7h xCRRDH	7:0	RDATA_H[23:16]	R	0	High byte of a 24-bit data register, contains the contents of the most recent **EQ Coefficient RAM** address read from the RAM. The address read will have been specified by the **EQ Coefficient RAM** Address fields.

Table 41. xCRRDH Register

3.6.2.3. Coefficient Address (xCRADD) Register

This 7-bit register provides the address to the internal RAM when doing indirect writes/reads to the EQ RAM.

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 8 - 8h xCRADD	7:0	ADDRESS[7:0]	R/W	0	Contains the address (between 0 and 255) of the **EQ Coefficient RAM** to be accessed by a read or write. This is not a byte address--it is the address of the 24-bit data item to be accessed from the **EQ Coefficient RAM**.This address is automatically incremented after writing to the xCRWD_H or reading from xCRRDH (and the 24 bit data from the next RAM location is fetched.)

Table 42. xCRADD Register

3.6.2.4. x_Coefficient Status (xCRS) Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

This control register provides the write/read enable when doing indirect writes/reads to the EQ RAM.

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 9 - 9h xCRS	7	xDACOEFR	R	0	1 = read/write to **EQ Coefficient RAM** in progress, cleared by HW when done.
	6:0	RSVD	R	0	Reserved

Table 43. xCRS Register

3.6.3. Equalizer, Bass, Treble Coefficient & Equalizer Prescaler RAM

The EQ Coefficient RAM is a single port 161x24 synchronous RAM. It is programmed indirectly through the I2C Control interface. Writing to the EQ coefficient RAM is done in the following manner as shown in the figure below:

1 Write EQ coefficient RAM target address to xCRADDregister. (EQ data is pre-fetched even if we don't use it)
- **a** I2C Start command followed by the I2C Device Address and Write flag
- **b** Write the Register Address for the xCRADD register
- **c** Write Register Data (EQ Coefficient RAM address)

2 Start a multiple write cycle
- **a** I2C Start command followed by the I2C Device Address and Write Flag
- **b** Register Address of the xCRADD register
- **c** Write D7:0 to the xCRWDL register
- **d** Write D15:8 to the xCRWDM register
- **e** Write D23:16 to the xCRWDH register

3 On successful receipt of the WDATA_H data, the part will automatically start a write cycle. The ACCSTAT bit will be set high to indicate that a write is in progress.

4 On completion of the internal write cycle, the ACCSTAT bit will be 0 (when operating the control interface at high speeds - TBD - software must poll this bit to ensure the write cycle is complete before starting another write cycle.)

5 The bus cycle may be terminated by the host or steps 2-3 may be repeated for writes to consecutive EQ RAM locations.

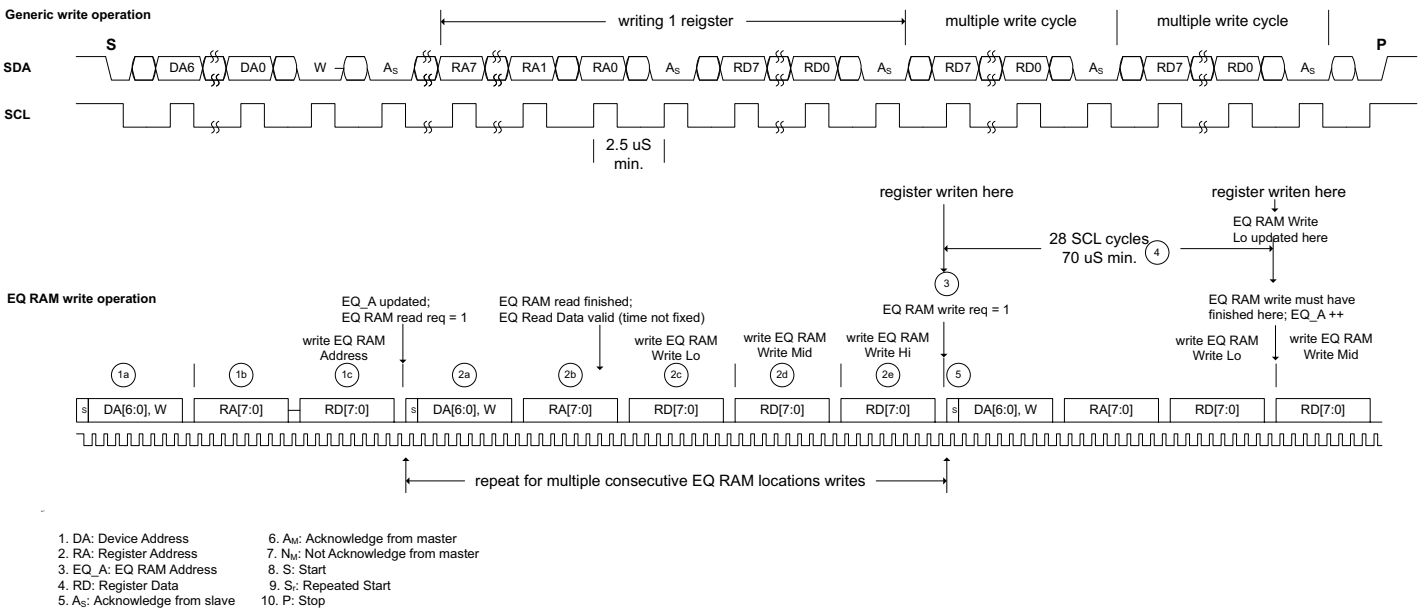


Figure 7. EQ Coefficient RAM Write Sequence

Reading back a value from the EQ Coefficient RAM is done in this manner:

1 Write target address to xCRADD register.(EQ data is pre-fetched for read even if we don't use it)
   - **a** I2C Start command followed by the I2C Device Address and Write flag
   - **b** Write the Register Address for the xCRADD register
   - **c** Write Register Data (EQ Coefficient RAM address)

2 I2C Start (or repeat start) a write cycle to xCRRDL and after the second byte (register address) is acknowledged, go to step 3. (Do not complete the write cycle.)
   - **a** I2C Start command followed by the I2C Device Address and Write Flag
   - **b** Write Register Address of the xCRRDL register

3 Signal a repeat start, provide the I2C device address, and indicate a read operation

4 Read D7:0 (register address incremented after ack by host)

5 Read D15:8 (register address incremented after ack by host)

6 Read D23:16 (register address incremented and next EQ location pre-fetched after ack by host)

7 The host stops the bus cycle

To repeat a read cycle for consecutive EQ RAM locations:

8 Start (or repeat start instead of stopping the bus cycle in step 7) a write cycle indicating xCRRDL as the target address.

9 After the second byte is acknowledged, signal a repeated start.

10 Indicate a read operation

11 Read the xCRRDL register as described in step 4

12 Read the xCRRDM register as described in step 5

13 Read the xCRRDH register as described in step 6

14 Repeat steps 8-13 as desire

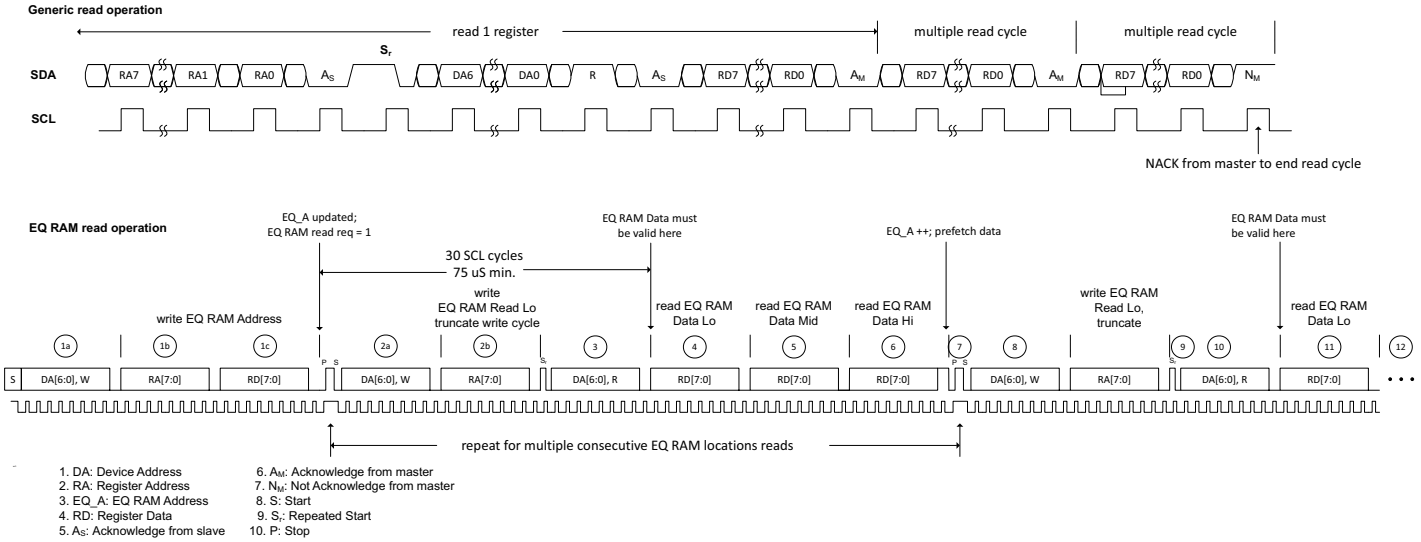


Figure 8. EQ Coefficient RAM Read Sequence

EQ 1				EQ2			
Address	**Channel 0 Coefficients**	**Address**	**Channel 1 Coefficients**	**Address**	**Channel 0 Coefficients**	**Address**	**Channel 1 Coefficients**
0x00	EQ_COEF_0F0_B0	0x20	EQ_COEF_1F0_B0	0x40	EQ_COEF_2F0_B0	0x60	EQ_COEF_3F0_B0
0x01	EQ_COEF_0F0_B1	0x21	EQ_COEF_1F0_B1	0x41	EQ_COEF_2F0_B1	0x61	EQ_COEF_3F0_B1
0x02	EQ_COEF_0F0_B2	0x22	EQ_COEF_1F0_B2	0x42	EQ_COEF_2F0_B2	0x62	EQ_COEF_3F0_B2
0x03	EQ_COEF_0F0_A1	0x23	EQ_COEF_1F0_A1	0x43	EQ_COEF_2F0_A1	0x63	EQ_COEF_3F0_A1
0x04	EQ_COEF_0F0_A2	0x24	EQ_COEF_1F0_A2	0x44	EQ_COEF_2F0_A2	0x64	EQ_COEF_3F0_A2
0x05	EQ_COEF_0F1_B0	0x25	EQ_COEF_1F1_B0	0x45	EQ_COEF_2F1_B0	0x65	EQ_COEF_3F1_B0
0x06	EQ_COEF_0F1_B1	0x26	EQ_COEF_1F1_B1	0x46	EQ_COEF_2F1_B1	0x66	EQ_COEF_3F1_B1
0x07	EQ_COEF_0F1_B2	0x27	EQ_COEF_1F1_B2	0x47	EQ_COEF_2F1_B2	0x67	EQ_COEF_3F1_B2
0x08	EQ_COEF_0F1_A1	0x28	EQ_COEF_1F1_A1	0x48	EQ_COEF_2F1_A1	0x68	EQ_COEF_3F1_A1
0x09	EQ_COEF_0F1_A2	0x29	EQ_COEF_1F1_A2	0x49	EQ_COEF_2F1_A2	0x69	EQ_COEF_3F1_A2
0x0A	EQ_COEF_0F2_B0	0x2A	EQ_COEF_1F2_B0	0x4A	EQ_COEF_2F2_B0	0x6A	EQ_COEF_3F2_B0
0x0B	EQ_COEF_0F2_B1	0x2B	EQ_COEF_1F2_B1	0x4B	EQ_COEF_2F2_B1	0x6B	EQ_COEF_3F2_B1
0x0C	EQ_COEF_0F2_B2	0x2C	EQ_COEF_1F2_B2	0x4C	EQ_COEF_2F2_B2	0x6C	EQ_COEF_3F2_B2
0x0D	EQ_COEF_0F2_A1	0x2D	EQ_COEF_1F2_A1	0x4D	EQ_COEF_2F2_A1	0x6D	EQ_COEF_3F2_A1
0x0E	EQ_COEF_0F2_A2	0x2E	EQ_COEF_1F2_A2	0x4E	EQ_COEF_2F2_A2	0x6E	EQ_COEF_3F2_A2
0x0F	EQ_COEF_0F3_B0	0x2F	EQ_COEF_1F3_B0	0x4F	EQ_COEF_2F3_B0	0x6F	EQ_COEF_3F3_B0
0x10	EQ_COEF_0F3_B1	0x30	EQ_COEF_1F3_B1	0x50	EQ_COEF_2F3_B1	0x70	EQ_COEF_3F3_B1
0x11	EQ_COEF_0F3_B2	0x31	EQ_COEF_1F3_B2	0x51	EQ_COEF_2F3_B2	0x71	EQ_COEF_3F3_B2
0x12	EQ_COEF_0F3_A1	0x32	EQ_COEF_1F3_A1	0x52	EQ_COEF_2F3_A1	0x72	EQ_COEF_3F3_A1
0x13	EQ_COEF_0F3_A2	0x33	EQ_COEF_1F3_A2	0x53	EQ_COEF_2F3_A2	0x73	EQ_COEF_3F3_A2
0x14	EQ_COEF_0F4_B0	0x34	EQ_COEF_1F4_B0	0x54	EQ_COEF_2F4_B0	0x74	EQ_COEF_3F4_B0
0x15	EQ_COEF_0F4_B1	0x35	EQ_COEF_1F4_B1	0x55	EQ_COEF_2F4_B1	0x75	EQ_COEF_3F4_B1
0x16	EQ_COEF_0F4_B2	0x36	EQ_COEF_1F4_B2	0x56	EQ_COEF_2F4_B2	0x76	EQ_COEF_3F4_B2
0x17	EQ_COEF_0F4_A1	0x37	EQ_COEF_1F4_A1	0x57	EQ_COEF_2F4_A1	0x77	EQ_COEF_3F4_A1
0x18	EQ_COEF_0F4_A2	0x38	EQ_COEF_1F4_A2	0x58	EQ_COEF_2F4_A2	0x78	EQ_COEF_3F4_A2
0x19	EQ_COEF_0F5_B0	0x39	EQ_COEF_1F5_B0	0x59	EQ_COEF_2F5_B0	0x79	EQ_COEF_3F5_B0
0x1A	EQ_COEF_0F5_B1	0x3A	EQ_COEF_1F5_B1	0x5A	EQ_COEF_2F5_B1	0x7A	EQ_COEF_3F5_B1
0x1B	EQ_COEF_0F5_B2	0x3B	EQ_COEF_1F5_B2	0x5B	EQ_COEF_2F5_B2	0x7B	EQ_COEF_3F5_B2
0x1C	EQ_COEF_0F5_A1	0x3C	EQ_COEF_1F5_A1	0x5C	EQ_COEF_2F5_A1	0x7C	EQ_COEF_3F5_A1
0x1D	EQ_COEF_0F5_A2	0x3D	EQ_COEF_1F5_A2	0x5D	EQ_COEF_2F5_A2	0x7D	EQ_COEF_3F5_A2
0x1E	-	0x3E	-	0x5E	-	0x7E	-
0x1F	EQ_PRESCALE0	0x3F	EQ_PRESCALE1	0x5F	EQ_PRESCALE2	0x7F	EQ_PRESCALE3

Table 44. EQ Coefficient RAM AddressesFor Speaker and DAC Channels

EQ 1			EQ2	
Address	**Channel Coefficients**		**Address**	**Channel Coefficients**
0x00	EQ_COEF_0F0_B0		0x20	EQ_COEF_1F0_B0
0x01	EQ_COEF_0F0_B1		0x21	EQ_COEF_1F0_B1
0x02	EQ_COEF_0F0_B2		0x22	EQ_COEF_1F0_B2
0x03	EQ_COEF_0F0_A1		0x23	EQ_COEF_1F0_A1
0x04	EQ_COEF_0F0_A2		0x24	EQ_COEF_1F0_A2
0x05	EQ_COEF_0F1_B0		0x25	EQ_COEF_1F1_B0
0x06	EQ_COEF_0F1_B1		0x26	EQ_COEF_1F1_B1
0x07	EQ_COEF_0F1_B2		0x27	EQ_COEF_1F1_B2
0x08	EQ_COEF_0F1_A1		0x28	EQ_COEF_1F1_A1
0x09	EQ_COEF_0F1_A2		0x29	EQ_COEF_1F1_A2
0x0A	EQ_COEF_0F2_B0		0x2A	EQ_COEF_1F2_B0
0x0B	EQ_COEF_0F2_B1		0x2B	EQ_COEF_1F2_B1
0x0C	EQ_COEF_0F2_B2		0x2C	EQ_COEF_1F2_B2
0x0D	EQ_COEF_0F2_A1		0x2D	EQ_COEF_1F2_A1
0x0E	EQ_COEF_0F2_A2		0x2E	EQ_COEF_1F2_A2
0x0F	EQ_COEF_0F3_B0		0x2F	EQ_COEF_1F3_B0
0x10	EQ_COEF_0F3_B1		0x30	EQ_COEF_1F3_B1
0x11	EQ_COEF_0F3_B2		0x31	EQ_COEF_1F3_B2
0x12	EQ_COEF_0F3_A1		0x32	EQ_COEF_1F3_A1
0x13	EQ_COEF_0F3_A2		0x33	EQ_COEF_1F3_A2
0x14	EQ_COEF_0F4_B0		0x34	EQ_COEF_1F4_B0
0x15	EQ_COEF_0F4_B1		0x35	EQ_COEF_1F4_B1
0x16	EQ_COEF_0F4_B2		0x36	EQ_COEF_1F4_B2
0x17	EQ_COEF_0F4_A1		0x37	EQ_COEF_1F4_A1
0x18	EQ_COEF_0F4_A2		0x38	EQ_COEF_1F4_A2
0x19	EQ_COEF_0F5_B0		0x39	EQ_COEF_1F5_B0
0x1A	EQ_COEF_0F5_B1		0x3A	EQ_COEF_1F5_B1
0x1B	EQ_COEF_0F5_B2		0x3B	EQ_COEF_1F5_B2
0x1C	EQ_COEF_0F5_A1		0x3C	EQ_COEF_1F5_A1
0x1D	EQ_COEF_0F5_A2		0x3D	EQ_COEF_1F5_A2
0x1E	-		0x3E	-
0x1F	EQ_PRESCALE0		0x3F	EQ_PRESCALE1

Table 45. EQ Coefficient RAM Addresses For Earpiece Channel

Address	Bass Coefficients	Address	Treble Coefficients	Address	3D Coefficients	Address	Multiband Coefficients
0x80	BASS_COEF_EXT1_B0	0x97	TREB_COEF_EXT1_B0	0xAE	3D_COEF	0xB0	MBC1_BQ1_COEFF0
0x81	BASS_COEF_EXT1_B1	0x98	TREB_COEF_EXT1_B1	0xAF	3D_MIX	0xB1	MBC1_BQ1_COEFF1
0x82	BASS_COEF_EXT1_B2	0x99	TREB_COEF_EXT1_B2			0xB2	MBC1_BQ1_COEFF2
0x83	BASS_COEF_EXT1_A1	0x9A	TREB_COEF_EXT1_A1			0xB3	MBC1_BQ1_COEFF3
0x84	BASS_COEF_EXT1_A2	0x9B	TREB_COEF_EXT1_A2			0xB4	MBC1_BQ1_COEFF4
0x85	BASS_COEF_EXT2_B0	0x9C	TREB_COEF_EXT2_B0			0xB5	MBC1_BQ2_COEFF0
0x86	BASS_COEF_EXT2_B1	0x9D	TREB_COEF_EXT2_B1			0xB6	MBC1_BQ2_COEFF1
0x87	BASS_COEF_EXT2_B2	0x9E	TREB_COEF_EXT2_B2			0xB7	MBC1_BQ2_COEFF2
0x88	BASS_COEF_EXT2_A1	0x9F	TREB_COEF_EXT2_A1			0xB8	MBC1_BQ2_COEFF3
0x89	BASS_COEF_EXT2_A2	0xA0	TREB_COEF_EXT2_A2			0xB9	MBC1_BQ2_COEFF4
0x8A	BASS_COEF_NLF_M1	0xA1	TREB_COEF_NLF_M1			0xBA	MBC2_BQ1_COEFF0
0x8B	BASS_COEF_NLF_M2	0xA2	TREB_COEF_NLF_M2			0xBB	MBC2_BQ1_COEFF1
0x8C	BASS_COEF_LMT_B0	0xA3	TREB_COEF_LMT_B0			0xBC	MBC2_BQ1_COEFF2
0x8D	BASS_COEF_LMT_B1	0xA4	TREB_COEF_LMT_B1			0xBD	MBC2_BQ1_COEFF3
0x8E	BASS_COEF_LMT_B2	0xA5	TREB_COEF_LMT_B2			0xBE	MBC2_BQ1_COEFF4
0x8F	BASS_COEF_LMT_A1	0xA6	TREB_COEF_LMT_A1			0xBF	MBC2_BQ2_COEFF0
0x90	BASS_COEF_LMT_A2	0xA7	TREB_COEF_LMT_A2			0xC0	MBC2_BQ2_COEFF1
0x91	BASS_COEF_CTO_B0	0xA8	TREB_COEF_CTO_B0			0xC1	MBC2_BQ2_COEFF2
0x92	BASS_COEF_CTO_B1	0xA9	TREB_COEF_CTO_B1			0xC2	MBC2_BQ2_COEFF3
0x93	BASS_COEF_CTO_B2	0xAA	TREB_COEF_CTO_B2			0xC3	MBC2_BQ2_COEFF4
0x94	BASS_COEF_CTO_A1	0xAB	TREB_COEF_CTO_A1			0xC4	MBC3_BQ1_COEFF0
0x95	BASS_COEF_CTO_A2	0xAC	TREB_COEF_CTO_A2			0xC5	MBC3_BQ1_COEFF1
0x96	BASS_MIX	0xAD	TREB_MIX			0xC6	MBC3_BQ1_COEFF2
						0xC7	MBC3_BQ1_COEFF3
						0xC8	MBC3_BQ1_COEFF4
						0xC9	MBC3_BQ2_COEFF0
						0xCA	MBC3_BQ2_COEFF1
						0xCB	MBC3_BQ2_COEFF2
						0xCC	MBC3_BQ2_COEFF3
						0xCD	MBC3_BQ2_COEFF4

Table 46. EQCRAM Multi-Band Compressor/Bass/Treble/3D Addresses

3.7. Gain, Limiting, and Dynamic Range Control

The gain for a given channel is controlled by the MVOL_x registers. The range of gain supported is from -95.625db to 0db in 0.375db steps. If the result of the gain multiply step would result in overflow of the 24-bit output word width, the output is saturated at the max positive or negative value. In addition to simple gain control, the TSCS454xx also provides sophisticated dynamic range control. The dynamic range control processing element implements limiting, dynamic range compression, and dynamic range expansion functions.

3.7.1. Limiter Compressor and Expander

The Limiter function will limit the audio output of the DSP module to the DAC's and Class-D outputs. If the signal is greater than 0dB it will saturate at 0dB as the final processing step within the DSP module.

There are times when the user may intentionally want the output Limiter to perform this saturation, for example +6dB of gain applied within the DSP gain control and then limited to 0dB when output to the Class-D module would result in a clipped signal driving the Speaker output. This clipped signal would obviously contribute to increased distortion on the Speaker output which from the user listening perception it would “sound louder”.

At other times, the system designer may wish to protect speakers from overheating or provide hearing protection by intentionally limiting the output level before full scale is reached. A limit threshold, independent of the compressor threshold is provided for this purpose. It is expected that the limit threshold is set to a higher level than the compressor threshold.

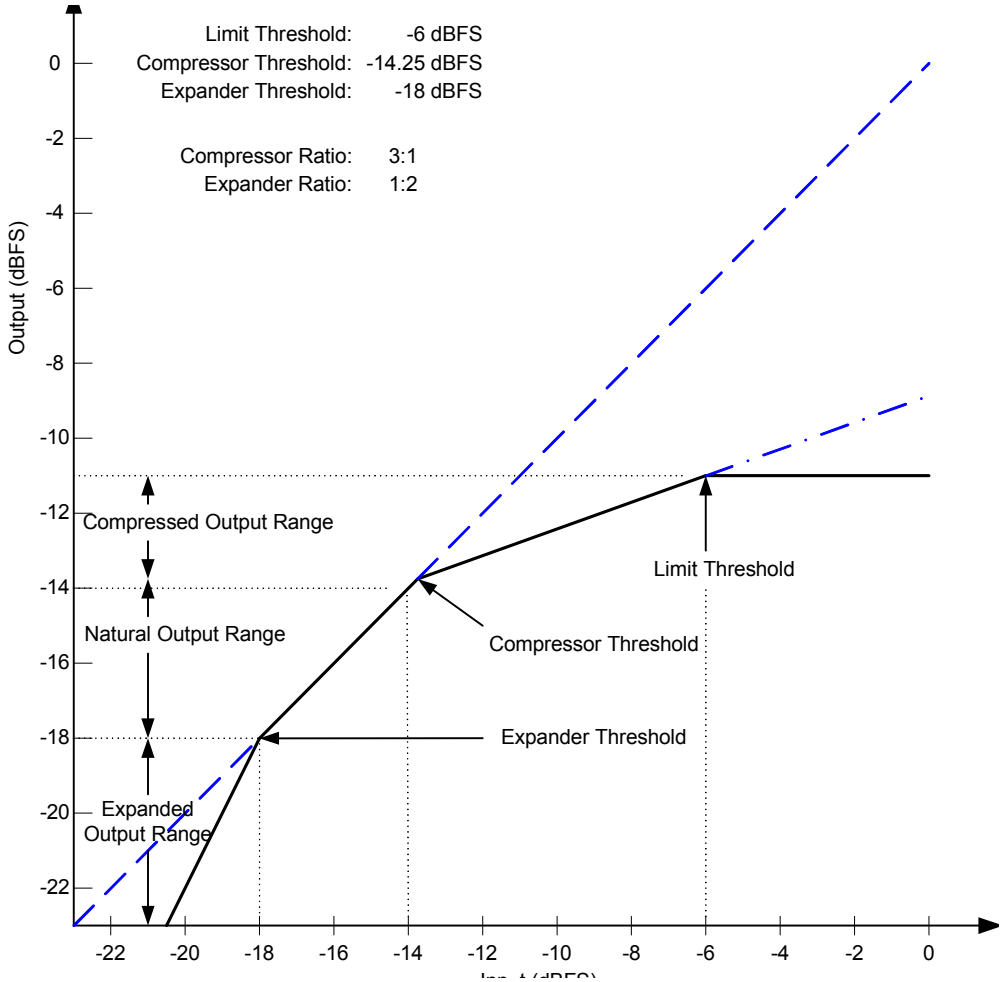


Figure 9. Compressor, Output vs Input Gain

The traditional compressor algorithm provides two functions simultaneously (depending on signal level). For higher level signals, it can provide a compression function to reduce the signal level. For lower level signals, it can provide an expansion function for either increasing dynamic range or noise gating.

The compressor monitors the signal level and, if the signal is higher than a threshold, will reduce the gain by a programmed ratio to restrict the dynamic range. Limiting is an extreme example of the compressor where, as the input signal level is increased, the gain is decreased to maintain a specific output level.

In addition to limiting the bandwidth of the compressed audio, it is common for compressed audio to also compress the dynamic range of the audio. The expansion function inTSCS454xx can help restore the original dynamics to the audio.

The expander is a close relative of the compressor. Rather than using signal dependent gain to restrict the dynamic range, the expander uses signal dependent gain to expand the dynamic range. Thus if a signal level is below a particular

threshold, the expander will reduce the gain even further to extend the dynamic range of the material.

A basic block diagram of the compressor is shown below:

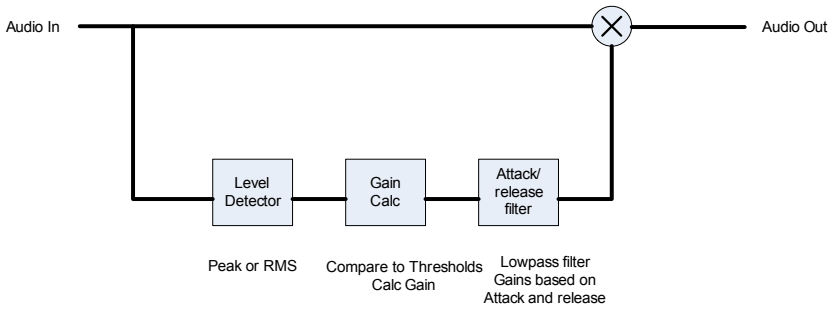


Figure 10. Compressor Diagram

As this diagram shows, there are 3 primary components of the compressor.

Compressor Level Detector

The level detector, detects the level of the incoming signal. Since the comp/limiter is designed to work on blocks of signals, the level detector will either find the peak value of the block of samples to be processed or the rms level of the samples within a block.

Compressor Gain Calculation

The gain calculation block is responsible for taking the output of the level detector and calculating a target gain based on that level and the compressor and expander thresholds.

The compressor recalculates the target gain value every block, typically every 10ms.

The gain calculation operates in 3 regions:

- Linear region – If the level is higher than the expander threshold and lower than the compression threshold, then the gain is 1.0
- Compression region – When the level is higher than the compressor threshold, then the comp/limiter is in the compression region. The gain is a function of the compressor ratio and the signal level.
- Expansion region – When the signal is lower than the expansion threshold, the comp/limiter is in the expansion region. In this region, the gain is a function of the signal level and the expansion ratio.

Compression region gain calculation

In the compression region, the gain calculation is:

```
Atten(in db) = (1-1/ratio)(threshold(in db) – level(in db);
```

For example,

- Ratio = 4:1 compression
- Threshold = -16db
- Level = -4 db

The required attenuation is: 9db or a gain coefficient of 0.1259.

Translating this calculation from log space to linear yields the formula:

$$Gain = (level/threshold)^{1/ratio} * (threshold/level)$$

Expansion region gain calculation

In the expansion region, the attenuation calculation is:

```
Atten(in db) = (1 - ratio)(threshold-level);
```

For example,

- Ratio = 3:1
- Threshold = -40db
- Level = -44 db

The resulting attenuation required is 8db or a gain value of 0.1585.

The linear equation for calculating the gain is:

$$Gain = (level/threshold)^{ratio} * (threshold/level)$$

If the calculated attenuation is more than the maximum possible attenuation(-96dB)the the target gain value will be 0.0 or -00dB, which effectively creates a noise gate function.

State Transitions

In addition to calculating the new gain for the compressor, the gain calculation block will also select the filter coefficient for the attack/release filter. The rules for selecting the coefficient are as follows:

- **In the compression region:**
  - If the gain calculated is less than the last gain calculated (more compression is being applied), then the filter coefficient is the compressor attack.
  - If the gain calculated is more than the last gain calculated (less compression), the filter coefficient is the compressor release.
- **In the expansion region:**
  - If the calculated gain is less than the last gain calculated (closing expander, the filter coefficient is the expander attack.
  - If the calculated gain is more than the last gain calculated, the filter coefficient is the expander release.
- **In the linear region:**

Modify gain until a gain of 1.0 is obtained.

- If the last non-linear state was compression, use the compressor release.
- If the last non-linear state was expansion, use the expander attack.

Attack/Release filter

In order to prevent objectionable artifacts, the gain is smoothly ramped from the current value to the new value calculated by the gain calculation block. In the PC-based comp/limiter, this is achieved using a simple tracking lowpass filter to smooth out the abrupt transitions. The calculation (using the coefficient (coeff) selected by the gain block) is:

```
Filtered_gain = coeff*last_filtered_gain + (1.0 - coeff)*target_gain;
```

This creates a exponential ramp from the current gain value to the new value.

3.7.2. Configuration

This compressor limiter provides the following configurable parameters.

- **Compressor/limiter**
  - Threshold – The threshold above which the compressor will reduce the dynamic range of the audio in the compression region.
  - Ratio – The ratio between the input dynamic range and the output dynamic range. For example, a ratio of 3 will reduce an input dynamic range of 9db to 3db.
  - Attack Time – The amount of time that changes in gain are smoothed over during the attack phase of the compressor.
  - Release Time – The amount of time that changes in gain are smoothed over during the release phase of the compressor.
  - Makeup gain – Used to increase the overall level of the compressed audio.

- **Expander**
  - Threshold – The threshold below which the expander will increase the dynamic range of the audio.
  - Ratio – The ratio between the input dynamic range and the output dynamic range of the audio in the expansion range. For example a ratio of 3 will take an input dynamic range of 9db and expand it to 27db.
  - Attack Time– The amount of time that changes in gain are smoothed over during the attack phase of the expander
  - Release Time
  - - The amount of time that changes in gain are smoothed over during the release phase of the expander.
  -
- **Two level detection algorithms**
  - RMS – Use an RMS measurement for the level.
  - Peak – Use a peak measurement for the level.

3.7.3. Controlling Parameters

In order to control this processing, there are a number of configurable parameters. The parameters and their ranges are:

- **Compressor/limiter**
  - Threshold - -40db to 0db relative to full scale.
  - Ratio – 1 to 20
  - Attack Time – typically 0 to 500ms
  - Release Time – typically 25ms to 2 seconds
  - Makeup gain – 0 to 40db
- **Expander**
  - Threshold - -30 to -60 dB
  - Ratio – 1 to 6
  - Attack Time – same as above
  - Release Time – same as above.
- **Two level detection algorithms**
  - RMS
  - Peak

3.7.4. Compressor/Limiter/Expander Control Registers

3.7.4.1. General Compressor/Limiter/Expander Control Registers

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 33 -21h xCLECTL	7:5	RSVD	R	0h	Reserved
	4	LVLMODE	RW	0	CLE Level Detection Mode: 0 = Average 1 = Peak
	3	WINSEL	RW	0	CLE Level Detection Window: 0 = Equivalent of 512 samples at the selected Base Rate (~10-16ms) 1 = Equivalent of 64 samples at the selected Base Rate (~1.3-2ms
	2	EXPEN	RW	0	Expander Enable: 0 = Disabled 1 = Enabled
	1	LIMEN	RW	0	Limiter Enable: 0 = Disabled 1 = Enabled
	0	COMPEN	RW	0	Compressor Enable: 0 = Disabled 1 = Enabled

Table 47. xCLECTL Register

3.7.4.2. x_Compressor Make-up Gain (xCLEMUG) Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 34 - 22h xCLEMUG	7:5	RSVD	R	0h	Reserved
	4:0	xMUGAIN[4:0]	RW	0h	0dB...46.5dB in 1.5dB steps

Table 48. xCLEMUG Register

3.7.4.3. x_Compressor Threshold (xCOMPTHR) Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 35 - 23h xCOMPTHR	7:0	xTHRESH[7:0]	RW	00h	FFh...00h = 0dB...95.625dB in 0.375dB steps.

Table 49. xCOMPTHR Register

3.7.4.4. x_Compressor Compression Ratio (xCOMPRAT) Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 36 -24h xCOMPRAT	7:5	RSVD	R	000	Reserved
	4:0	xRATIO[4:0]	RW	00h	Compressor Ratio 00h = Reserved 01h = 1.5:1 02h...14h = 2:1...20:1 15h...1Fh = Reserved

Table 50. xCOMPRAT Register

3.7.4.5. Compressor Attack Time Constant (xCOMPATKL) Register (Low)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 37 -25h xCOMPATKL	7:0	xTCATKL[7:0]	RW	00h	Low byte of the time constant used to ramp to a new gain value during a compressor attack phase. 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 51. xCOMPATKL Register

3.7.4.6. Compressor Attack Time Constant (xCOMPATKH) Register (High)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 38 - 26h xCOMPATKH	7:0	xTCATKH[7:0]	RW	00h	High byte of the time constant used to ramp to a new gain value during a compressor attack phase. 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 52. xCOMPATKH Register

3.7.4.7. Compressor Release Time Constant (xCOMPRELL) Register (Low)

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 39 - 27h xCOMPRELL	7:0	xTCRELL[7:0]	RW	00h	Low byte of the time constant used to ramp to a new gain value during a compressor release phase. 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 53. xCOMPRELL Register

3.7.4.8. Compressor Release Time Constant (xCOMPRELH) Register (High)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 40 - 28h xCOMPRELH	7:0	xTCRELH[15:8]	RW	00h	High byte of the time constant used to ramp to a new gain value during a compressor release phase. The time constant is [high byte, low byte] 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 54. xCOMPRELH Register

3.7.4.9. Limiter Threshold (xLIMTH) Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 41 - 29h xLIMTH	7:0	xTHRESH[7:0]	RW	00h	FFh...00h = 0dB...95.625dB in 0.375dB steps.

Table 55. xLIMTH Register

3.7.4.10. Limiter Target (xLIMTGT) Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 42 - 2Ah xLIMTGT	7:0	xTARGET[7:0]	RW	00h	FFh...00h = 0dB...95.625dB in 0.375dB steps.

Table 56. xLIMTGT Register

3.7.4.11. Limiter Attack Time Constant (xLIMATKL) Register (Low)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 43 2Bh xLIMATKL	7:0	xTCATKL[7:0]	RW	00h	Low byte of the time constant used to ramp to a new gain value during a limiter attack phase. 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 57. xLIMATKL Register

3.7.4.12. Limiter Attack Time Constant (xLIMATKH) Register (High)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 44 - 2Ch xLIMATKH	7:0	xTCATKH[15:8	RW	00h	High byte of the time constant used to ramp to a new gain value during a limiter attack phase. The time constant is [high byte, low byte] 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 58. xLIMATKH Register

3.7.4.13. Limiter Release Time Constant (xLIMRELL) Register (Low)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 45 - 2Dh xLIMRELL	7:0	xTCRELL[7:0]	RW	00h	Low byte of the time constant used to ramp to a new gain value during a limiter release phase. 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 59. xLIMRELL Register

3.7.4.14. Limiter Release Time Constant (xLIMRELH) Register (High)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 46 - 2Eh xLIMRELH	7:0	xTCRELH[15:8]	RW	00h	High byte of the time constant used to ramp to a new gain value during a limiter release phase. The time constant is [high byte, low byte] 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 60. xLIMRELH Register

3.7.4.15. Expander Threshold (xEXPTHR) Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 47 - 2Fh xEXPTHR	7:0	xTHRESH[7:0]	RW	00h	Expander threshold: 0...95.625dB in 0.375dB steps

Table 61. xEXPTHR Register

3.7.4.16. Expander Ratio (xEXPRAT) Register

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 48 - 30h xEXPRAT	7:3	RSVD	R	00h	Reserved
		xRATIO[2:0]	RW	000	Expander Ratio 0h...1h = Reserved 2h...7h = 1:2...1:7

Table 62. xEXPRAT Register

3.7.4.17. Expander Attack Time Constant (xEXPATKL) Register (Low)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 49 - 31h xEXPATKL	7:0	xTCATKL[7:0]	RW	00h	Low byte of the time constant used to ramp to a new gain value during a expander attack phase. 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 63. xEXPATKL Register

3.7.4.18. Expander Attack Time Constant (xEXPATKH) Register (High)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 50 - 32h xEXPATKH	7:0	xTCATKH[15:8]	RW	00h	High byte of the time constant used to ramp to a new gain value during a expander attack phase. The time constant is [high byte, low byte] 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 64. xEXPATKH Register

3.7.4.19. Expander Release Time Constant (xEXPRELL) Register (Low)

Where x = SPK, DAC, SUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 51 - 33h xEXPRELL	7:0	xTCRELL[7:0]	RW	0	Low byte of the time constant used to ramp to a new gain value during a expander release phase. 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 65. xEXPRELL Register

3.7.4.20. Expander Release Time Constant (xEXPRELH) Register (High)

Where x = SPK, DAC, SUBSUB, y= Page 3, 4, 5

Register Address	Bit	Label	Type	Default	Description
Page y, Reg 52 - 34h xEXPRELH	7:0	xTCRELH[15:8]	RW	0	High byte of the time constant used to ramp to a new gain value during a expander release phase. The time constant is [high byte, low byte] 0000h = 0 (instantaneous) 0001h = 0.96875 + 1/(2^21) 0002h = 0.96875 + 2/(2^21) ... (step = 1/(2^21)) FFFEh = [(2^21)-2]/(2^21) FFFFh = [(2^21)-1]/(2^21)

Table 66. xEXPRELH Register

3.8. Mute and De-Emphasis and Phase Inversion

The TSCS454xx has a Soft Mute function, which is used to gradually attenuate the digital signal volume to zero. The gain returns to its previous setting if the soft mute is removed. At startup, the codec is muted by default; to enable audio play, the mute bit must be cleared to 0.

After the equalization filters, de-emphasis may be performed on the audio data to compensate for pre-emphasis that may be included in the audio stream. De-emphasis filtering is only available for 48kHz, and 44.1kHz sample rates.

Normal stereo operation converts left and right channel digital audio data to analog in separate DACs. However, it is also possible to have the same signal (left or right) appear on both analog output channels by disabling one channel. The DAC output defaults to non-inverted. Setting DACPOLL and DACPOLR bits will invert the DAC

See xCTL registers ((x = DAC, SPK and SUB) in the following sections for the control of the mute, de-emphasis and phase inversion.

3.9. Output Post Processing

Following the Output Processor the digital audio data is up-sampled and sent to the PWM/DAC blocks for analog conversion.

3.9.1. Interpolation and Filtering

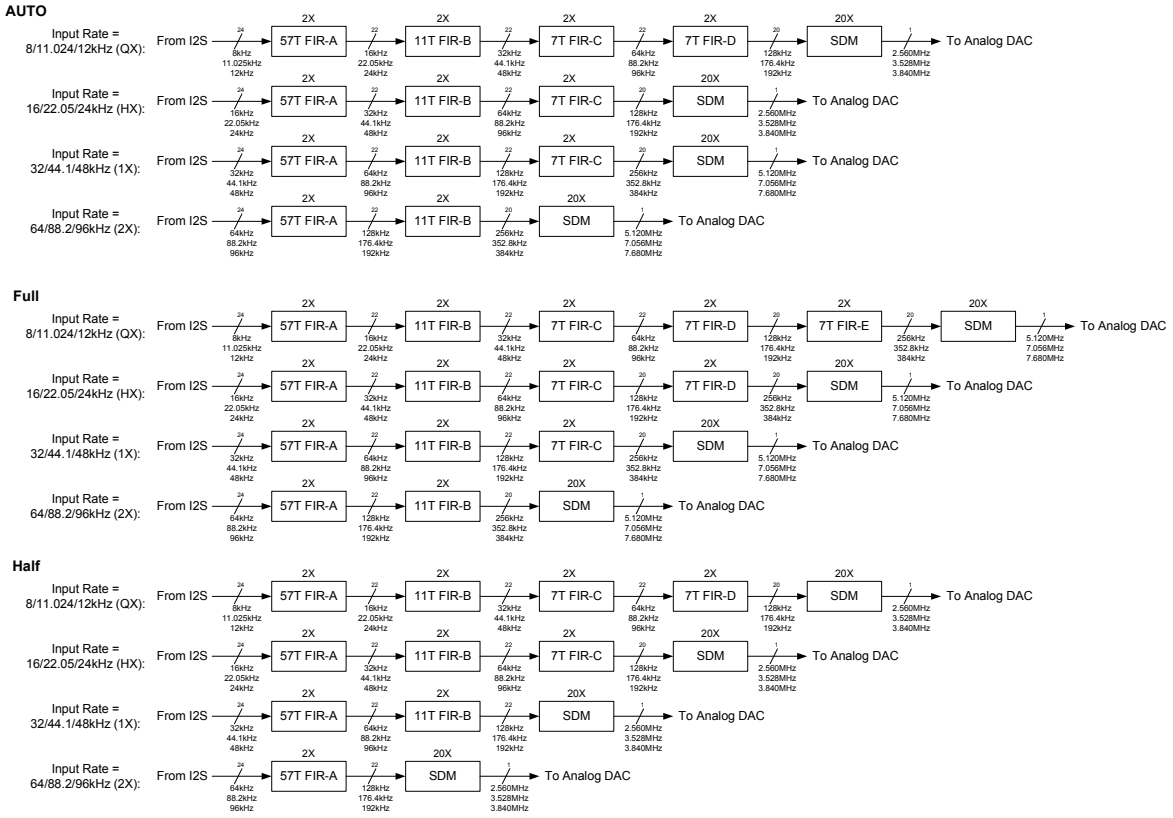


Figure 11. Output Interpolators and Filtering

3.10 Analog Audio Outputs

Refer to Figure 2, “Output Processing Flow,” on page 16. After the audio data is selected by the SSS the data is sent to the Output Processor, interpolator-filters, and finally to the DAC and output amplifiers for analog output generation. For digital audio data I2S PCM outputs are provided. A analog in bypass path exists that enables analog audio input via the Line Input1 to be sent directly and summed with the DAC output.

Following the Output Processor the digital audio data is up-sampled via the interpolator and sent to the PWM/DAC blocks for analog conversion.

The Analog Audio outputs are specified as follows:

- **Stereo, Class D, BTL Amplified Outputs - 1W into 8 ohms, 2W into 4 ohms**
- **Mono, Class AB, Earpiece Amplified Output - 40mw into 16 ohms**
- **Stereo, Class H, Headphone Amplified Outputs - 40mw into 16 ohms, Capless**
- **Stereo, Class AB, Line Level Output - 1VRMS into 10K ohm load, Capless**

3.10.1. Headphone Output

The HPOut pins can drive a 16Ω or 32Ω headphone. The signal volume of the headphone amplifier can be independently adjusted under software control by writing to HPVOL_L and HPVOL_R. Setting the volume to 0000000 will mute the output driver; the output remains at ground, so that no click noise is produced when muting or un-muting.

Gains above 0dB run the risk of clipping large signals.

To minimize artifacts such as clicks and zipper noise, the headphone outputs feature a volume fade function that smoothly changes volume from the current value to the target value.

3.10.1.1. DAC/Headphone Volume Control Register

Register Address	Bit	Label	Type	Default	Description
Page 2, Reg 10 -Ah HPVOLL	7	RSVD	R	0	Reserved
	6:0	HPVOL_L [6:0]	RW	1110111 (0dB)	Left Headphone Volume, 0.75dB per step 1111111 = +6dB 1111110 = +5.25dB … 1110111 = 0dB ... 0000001 = -88.5dB 0000000 = Analog mute Note: If HPVOLU is set, this setting will take effect after the next write to the Right Headphone Volume register.
Page 2, Reg 11 -Bh HPVOLR	7	RSVD	R	0	Reserved
	6:0	HPVOL_R [6:0]	RW	1110111	Right Headphone Volume, 0.75dB per step 1111111 = +6dB 1111110 = +5.25dB … 1110111 = 0dB ... 0000001 = -88.5dB 0000000 = Analog mute

Table 67. HPVOLL/HPVOLR Register

3.10.1.2. DAC Control Register

Register Address	Bit	Label	Type	Default	Description
Page 2, Reg 1 - 1h DACCTL	7	DACPOLR	RW	0	Invert DAC Right signal
	6	DACPOLL	RW	0	Invert DAC Left signal
	5:4	DACDITH	RW	00	DAC Dither Mode: 0h = Dynamic, Half Amplitude; 1h = Dynamic, Full Amplitude; 2h = Disabled; 3h = Static
	3	DACMU	RW	1	Digital Soft Mute 1 = mute 0 = no mute (signal active)
	2	DACDEM	RW	0	De-emphasis Enable 1 = De-emphasis Enabled 0 = No De-emphasis
	1	RSVD	R	0	Reserved
	0	ABYPASS	RW	0	Analog Bypass from MUXLIN, MUXRIN to HP Output 0 = Analog Bypass to Headphone Output Disabled 1 = Analog Bypass to Headphone Output Enabled

Table 68. DACCTL Register

3.10.1.3. Low Power Analog Input to Headphone Output Passthrough Mode.

A low power operating mode is provided that allows the output from the Input Analog Mux to be selected to drive the input to the headphone amplifier (DACCTL register, Bit 0 -ABYPASS). In this mode the TSCS454xx can be put into a very low power consumption state while allowing the selected analog audio input to be selected as the source for the headphone amplifier output.

3.10.2 Speaker Outputs

3.10.2.1. Speaker Volume Control

The LSPKOut (L+, L-) and RSPKOut (R+, R-) pins are controlled similarly, but independently of, the headphone output pins. They are intended to drive an 8 ohm speaker pair.

Register Address	Bit	Label	Type	Default	Description
Page 2, Reg 12 - Ch SPKVOLL	7	RSVD	R	0	Reserved
	6:0	SPKVOL_L [6:0]	RW	1101111 (0dB)	Left Speaker Volume 1111111 = +12dB 1111110 = +11.25dB … 1101111 = 0dB ... 0001000 to 0000001 = -77.25dB 0000000= Mute Note: If SPKVOLU is set, this setting will take effect after the next write to the Right Input Volume register.
Page 2, Reg 13 - Dh SPKVOLR	7	RSVD	R	0	Reserved
	6:0	SPKVOL_R [6:0]	RW	1101111 (0dB)	Right Speaker Volume 1111111 = +12dB 1111110 = +11.25dB … 1101111 = 0dB ... 0001000 to 0000001 = -77.25dB 0000000 = Mute

Table 69. SPKVOLL/ SPKVOLR Registers

3.10.2.2. Speaker Control Register

Register Address	Bit	Label	Type	Default	Description
Page 2, Reg 2 - 2h SPKCTL	7	SPKPOLR	RW	0	Speaker Right Polarity 0 = normal 1 = invert
	6	SPKPOLL	RW	0	Speaker Left Polarity 0 = normal 1 = invert
	5:4	RSVD	R	00	Reserved
	3	SPKMUTE	RW	1	Mute 1 = mute 0 = no mute (signal active)
	2	SPKDEM	RW	0	De-emphasis Enable 1 = De-emphasis Enabled 0 = No De-emphasis
	1:0	RSVD	R	00	Reserved

Table 70. SPKCTL Register

3.10.3. Earpiece Output

3.10.3.1. SUB Volume Control

The SUBOut (+, -) pins are controlled similarly, but independently of, the headphone output pins. They are intended to drive a 16 or 32 ohm speaker.

Register Address	Bit	Label	Type	Default	Description
Page 2, Reg 16 - 10h SUBVOL	7	RSVD	R	0	Reserved
	6:0	SUBVOL [6:0]	RW	1101111 (0dB)	SUB Speaker Volume 1111111 = +12dB 1111110 = +11.25dB … 1101111 = 0dB ... 0001000 to 0000001 = -77.25dB 0000000= Mute Note: If SPKVOLU is set, this setting will take effect after the next write to the Right Input Volume register.

Table 71. SUBVOL Register

3.10.3.2. SUB Speaker Output Control Register

Register Address	Bit	Label	Type	Default	Description
Page 2, Reg 3 - 3h SUBCTL	7	SUBPOL	RW	0	SUB Polarity 0 = normal 1 = invert
	6:4	RSVD	R	0	Reserved
	3	SUBMU	RW	1	Mute 1 = mute 0 = no mute (signal active)
	2	SUBDEM	RW	0	De-emphasis Enable 1 = De-emphasis Enabled 0 = No De-emphasis
	1	SUBMUX	RW	0	Selects Input Into SUB Amplifier 0 = Output Process 1 = Mix from Output Processor Left/2 + Right/2
	0	SUBILDIS	R	0	Sub Output Current Limiter 1 = Disable 0 = Enable

Table 72. SUBCTL Register

3.10.4. Class D Audio Processing

For additional information on the DDX^{TM} Class D solution, please see the application note on www.Temposemi.com.

The DDX^{TM} Class D PWM Controller performs the following signal processing:

- Feedback filters are applied to shape any noise. The filters move noise from audible frequencies to frequencies above the audio range.
- The PWM block converts the data streams to tri-state PWM signals and sends them to the power stages.
- Finally, the Class-D controller block adjusts the output volume to provide constant output power across supply voltage.

The power stages boost the signals to higher levels, sufficient to drive speakers at a comfortable listening level.

3.10.4.1. Constant Output Power Mode

In normal operation the BTL amplifier is rated at 0.5W (full scale digital with 6dB BTL gain) into an 8 ohm load at 3.6V but will vary from about 0.38W to about 1.2W across a 3.1V to 5.5V supply range. However, when constant output power mode is enabled, the full scale output is held constant from 3.1V to 5.5V

The BTL amplifier in TSCS454xx will continuously adjust to power supply changes to ensure that the full scale output power remains constant. This is not an automatic level control. Rather, this function prevents sudden volume changes when switching between battery and line power. Please note, when in this mode the amplifier efficiency may be reduced and decreases with higher supply voltages and lower target values.

A simple 5-bit ADC is used to monitor PVDD. As PVDD raises or lowers, the analog circuit will send a 5-bit code to the digital section that will average and then calculate a gain adjustment. The BTL audio signal will be multiplied by this gain value (in addition to the user volume controls).

The user will select a target value for the circuit. The constant output function will calculate a gain adjustment that will provide approximately the same full scale output voltage as provided when PVDD causes the same code value. So, if the

target is 9 then a PVDD voltage of about 3.7V would generate a code value of 9 and a full scale output power of about 630mW into 8 ohms. If PVDD should rise to 4V, generating a code of 13, then the constant output power circuit would reduce the gain by 0.75dB (4 codes * 0.1875dB) to keep the full scale output at the target level.

The circuit may be configured to add gain, attenuation, or both to maintain the full-scale output level. If the needed adjustment falls outside of the range of the circuit (only attenuation is enabled and gain is needed, for example) then the circuit will apply as much correction as it is able. Through the use of gain, attenuation, and target values, different behaviors may be implemented:

- **a** Attenuation only, target set to mimic a low supply voltage - Constant output level across battery state with constant quality (THD/SNR)
- **b** Attenuation only, target set to mimic a moderate supply voltage - Output limiting to an approximate power level. Level will decrease at lower supply voltages but won't increase beyond a specific point.
- **c** Gain only, target at or near max - Output will remain relatively constant but distortion will increase as PVDD is lowered. This mimics the behavior of common class-AB amplifiers.
- **d** Gain and attenuation - Output remains at a level below the maximum possible at the highest supply voltage and above the theoretical full scale at minimum supply. Full scale PCM input clips when the supply voltage is low but won't become too loud when the supply voltage is high.

In addition to maintaining a constant output level, PVDD may be monitored for a large, sudden, change. If the High Delta function is enabled and PVDD changes more than 4 code steps since the last cycle, the output will be rapidly reduced then gradually increased to the target level.

When using this circuit, please take note of the following:

- **a** The full scale output power may be limited by the supply voltage.
- **b** Full scale output power is affected by other gain controls in the output path including the EQ and compressor/limiter.
- **c** The Constant Output Power function is intended to help maintain a constant output level, not an exact output level. The output level for a specific target may vary part to part. If limiting is required for safety or other reasons, be conservative and set the target well below the maximum allowable level.
- **d** Noise on the PVDD supply may cause erratic behavior. Use the recommended supply decoupling caps and verify that the power supply can support the peak currents demanded by a class-D amplifier.

Constant Output Power error (dB) relative to a target of 8 for an ideal part and the output error if left uncorrected across a 3.1 to 5.5V supply range.

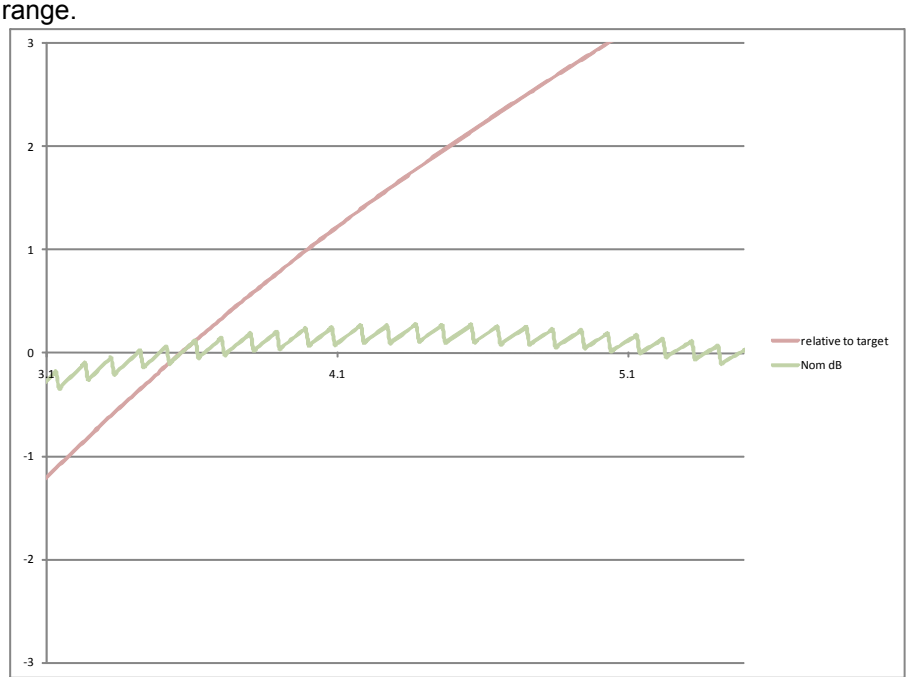


Figure 12. Uncorrected & Corrected Constant Output Power

Constant Output Power for nominal and high/low reference across a 3.1 to 5.5V supply range.(Uncorrected power shown for reference) A target of 8 roughly corresponds to 0.5W at 3.6V into 8 ohms.

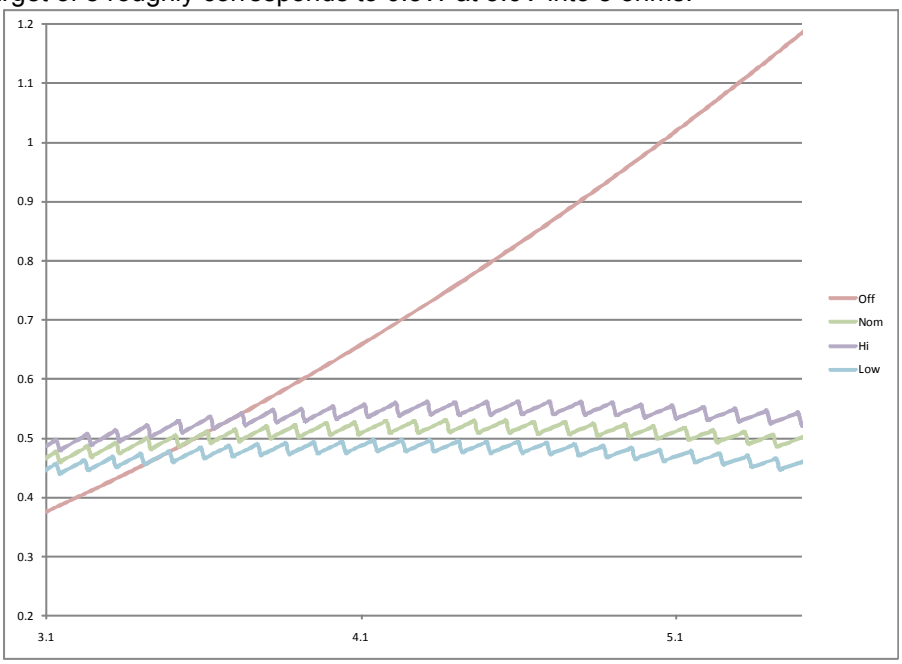


Figure 13. Corrected Constant Output Power

3.10.4.2. Under Voltage Lock Out

When the PVDD supply becomes low, the BTL amplifier may be disabled to help prevent undesirable amplifier operation (overheat) or system level problems (battery under-voltage.)

The same circuit that monitors the PVDD supply to help maintain a constant output power is used to monitor the PVDD supply for a critical under-voltage situation. If the sense circuit consistently returns a 0 code then the PVDD supply is less than the minimum required for proper operation. To prevent accidental shutdown due to a noisy supply at the minimum operating range, the output of the PVDD sense circuit will be averaged for at least 200ms.

3.10.4.3. Constant Output Power 0 (COP0) Register

Register Address	Bit	Label	Type	Default	Description
Page 2, Reg 17 - 11h COP0	7	COPATTEN	RW	0	1 = Constant Output Power function will attenuate the BTL output if the PVDD sense circuit returns a code higher than the target value.
	6	COPGAIN	RW	0	1 = Constant Output Power function will increase the BTL output if the PVDD sense circuit returns a code higher than the target value.
	5	HDELTA	RW	0	1 = If the PVDD code value has changed more than 4 counts since the last gain adjustment, the output will be reduced rapidly then slowly returned to the target level.
	4:0	COPTARGET[4:0]	RW	8h	5-bit target for the Constant Output Power function.

Table 73. COP0 Register

3.10.4.4. Constant Output Power 1 (COP1) Register

Register Address	Bit	Label	Type	Default	Description
Page 2 ,Reg 18 - 12h COP1	7	RSVD	R	0	Reserved
	6	HDCOMPMODE	RW	0	0 = Compare current poll value to last average to detect high delta event. 1 = Compare current poll value to last poll value to detect high delta event.
	5:2	AVGLENGTH[3:0]	RW	0000	Number of sense cycles to average: 0000 = 1 0001 = 2 0010 = 4 0011 = 8 0100 = 16 0101 = 32 0110 = 64 0111 = 128 1000 = 256 1001 = 512 1010 - 1111 = Reserved
	1:0	MONRATE[2:0]	RW	10	Rate the PVDD supply is monitored: 00 = 0.25ms 01 = 0.5ms 10 = 1ms 11 = 2ms

Table 74. COP1 Register

3.10.4.5. Constant Output Power Status (COPSTAT) Register

Register Address	Bit	Label	Type	Default	Description
Page 2, Reg 19 - 13h COPSTAT	7	HDELTADET	R	0	1 = A high delta situation has been detected (positive code change > 4) and the constant output power function is adjusting.
	6	UV	R	0	1 = PVDD is below the under voltage lockout threshold.
	5:0	COPADJ[5:0]	R	0h	Amount that the Constant Output Power function is adjusting the signal gain. Value is 2s compliment with each step equal to 0.1875dB. The approximate range is +/- 6dB

Table 75. COPSTAT Register

3.10.4.6. PWM Control 0 Register

Register Address	Bit	Label	Type	Default	Description
Page 2, Reg 20 - 14h PWM0	7:6	SCTO[1:0]	RW	11	Class-D Short Circuit Detect Time-out 00 = 10uS 01 = 100uS 10 = 500uS 11 = 100mS
	5	UVLO	RW	0	Under Voltage Lock Out 1 = BTL output disabled if PVDD sense circuit returns code 0
	4		R	1	Reserved
	3	BFDIS	RW	0	1 = disable binomial filter
	2	PWMMODE	RW	1	PWM Modulation Type: 0 = Binary; 1 = Ternary
	1		R	0	Reserved
	0	NOOFFSET	RW	0	PWM Frame Offset Disable: 0 = Right Frame Offset from Left; 1 = Left & Right Frames Alligned

Table 76. PWM0 Register

3.10.4.7. PWM Control 0 Register

Register Address	Bit	Label	Type	Default	Description
Page 2, Reg 20 - 14h PWM0	7:6	SCTO[1:0]	RW	11	Class-D Short Circuit Detect Time-out 00 = 10uS 01 = 100uS 10 = 500uS 11 = 100mS
	5	UVLO	RW	0	Under Voltage Lock Out 1 = BTL output disabled if PVDD sense circuit returns code 0
	4		R	1	Reserved
	3	BFDIS	RW	0	1 = disable binomial filter
	2	PWMMODE	RW	1	PWM Modulation Type: 0 = Binary; 1 = Ternary
	1		R	0	Reserved
	0	NOOFFSET	RW	0	PWM Frame Offset Disable: 0 = Right Frame Offset from Left; 1 = Left & Right Frames Alligned

Table 77. PWM0 Register

3.10.4.8. PWM Control 1 Register

Register Address	Bit	Label	Type	Default	Description
Page 2 , Reg 21 - 15h PWM1	7	RSVD	R	0	Reserved
	6:4	DITHPOS[4:0]	RW	0	PWM Dither Position: 0h = Full Dither; 1h = 1/2 Dither; 2h = 1/4 Static Only; 3h = 1/8 Static Only; 4h = 1/16 Static Only; 5h .. 7h = Reserved
	3:2		R		Reserved
	1	DYNDITH	RW	1	PWM Dynamic Dither: 0 = Static Dither; 1 = Dynamic Dither
	0	DITHDIS	RW	0	PWM Dither clear: 0 = Dither not cleared; 1 = Dither cleared

Table 78. PWM1 Register

NOTE: Dither is currently not implemented/working. This register retained for future revisions.

3.10.4.9. PWM Control 3 Register

Register Address	Bit	Label	Type	Default	Description
Page 4, Reg 23 - 17h PWM3	7:6	PWMMUX[1:0]	RW	00	pwm output muxing 0 = normal 1 = swap 0/1 2 = ch0 on both 3 = ch1 on both
	5:3		R	00	Reserved
	2:0	CVALUE[5:0]	RW	03h	tristate constant field, must be even and not 0

Table 79. PWM3 Register

3.11. Thermal Shutdown

To avoid overpower and overheating the codec when the amplifier outputs are driving large currents, the TSCS454xx incorporates a thermal protection circuit. If enabled, and the device temperature reaches approximately 150°C, the speaker and headphone amplifier outputs will be disabled. Once the device cools, the outputs will be automatically re-enabled.

3.11.1. Algorithm description:

There are 2 trip points, “high” and “low”. High indicates a critical overheat requiring a reduction in volume to avoid damage to the part. Low is set for a slightly lower temperature point, indicating that the current level is safe but that increased volume would result in a critical overheat condition.

Normally, the overheat bits are polled every 8ms but may be polled at 4ms, 8ms, 16ms, or 32ms by adjusting the Poll value. Reductions in volume will be allowed to happen at the Poll rate. Increases in volume are programmable to happen every 1, 2, 4, or 8 Poll cycles and in steps of 0.75dB to 6dB. This allows a full scale volume increase in a range of 10s of milliseconds to 10s of seconds.

When both overheat bits are 0, the volume is allowed to increment by the IncStep size, unless the volume has already reached the maximum value allowed. Any subsequent increment will be held off until the programmed number of polling cycles have occurred.

When the low overheat bit is 1 and the high overheat bit is 0, this indicates that the volume is currently at a safe point but the temperature is higher than desired and incrementing the volume may cause severe overheating. The volume is held at the current value.

When the high overheat bit is 1, damage could occur, so the volume setting will be immediately reduced by the Decrement Step value. As the overheat bits are re-polled, this volume reduction will continue until the high overheat bit drops to 0 or the volume value reaches the minimum setting. If the high overheat bit remains 1 even at the minimum setting, then the mute control bit will be asserted. If the high overheat bit persists even after mute, then the BTL amp will be powered down.

3.11.2. Thermal Trip Points.

The high and low trip points can be adjusted to suit the needs of a particular system implementation. There is a “shift” value (TripShift) which sets the low trip point, and there is a “split” value (TripSplit) that sets how many degrees above the low trip point the high trip point is.

By default:

TripShift = 2 (140 degrees C)
TripSplit = 0 (15 degrees C)

Therefore:

High Trip Point = 155°C.
Low Trip Point = 140°C.

3.11.3. Instant Cut Mode

This mode can be used to make our algorithm react faster to reduce thermal output but will cause more pronounced volume changes. If enabled:

- Only the high overheat is used, the low overheat is ignored.
- Whenever polled, if the high overheat is 1, then the volume setting will immediately be set to 0h.
- Conversely, if the high overheat is 0, the volume setting will immediately be set to the MaxVol value.
- Both volume clear and volume set events occur at the polling rate.

During this mode, the algorithm still possesses the ability to mute and then power down the BTL amp if the high overheat continues to be 1.

This mode is disabled by default.

3.11.4. Thermal Shutdown Registers

3.11.4.1. Temp Sensor Control/Status

The temperature sensor circuit is configured and monitored using the Temp Sensor Control/Status Register

Register Address	Bit	Label	Type	Default	Description
Page 2, Reg 25 - 19h THERMTS	7	TRIPHS	R	0	Temp sensor high trip point status 0 = Normal Operation 1 = Over Temp Condition
	6	TRIPLS	R	0	Temp sensor low trip point status 0 = Normal Operation 1 = Over Temp Condition
	5:4	TRIPSPLIT[1:0]	RW	0h	Temp sensor “split” setting. Determines how many degrees above the low trip point the high trip is set: 0h = 15 Degrees C 1h = 30 Degrees C 2h = 45 Degrees C 3h = 60 Degrees C.
	3:2	TRIPSHIFT[1:0]	RW	2h	Temp sensor “shift” setting. Determines the low trip temperature: 0h = 110 Degrees C 1h = 125 Degrees C 2h = 140 Degrees C 3h = 155 Degrees C.
	1:0	TSPOLL[1:0]	RW	1h	Temp sensor polling interval 0h = 4ms 1h = 8ms 2h = 16ms 3h = 32ms

Table 80. THERMTS Register

3.11.4.2. Speaker Thermal Shutdown Control Register

The thermal shutdown algorithm is configured using the Speaker Thermal Algorithm Control Register

Register Address	Bit	Label	Type	Default	Description
Page 2, Reg 26 - 1Ah THERMSPK	7	FORCEPWD	RW	1	Force powerdown enable for the speaker thermal algorithm: 0 = Speaker will remain powered up even if the temp sensor continues to report an overheat condition at minimum volume (mute) 1 = Speaker will be powered down if the temp sensor reports an overheat at the minimum volume (mute)
	6	INSTCUTMD	RW	0	Instant Cut Mode 0 = Both temp sensor status bits used to smoothly adjust the volume. 1 = Only the high temp sensor status bit will be used to set the volume. volume will be set to the full volume or mute (IncStep and DecStep are ignored.)
	5:4	INCRATIO[1:0]	RW	0h	Increment interval ratio. Determines the ratio between the speaker volume increment interval and the speaker volume decrement interval (increment rate is equal to or slower than decrement rate): 0h = 1:1 1h = 2:1 2h = 4:1 3h = 8:1
	3:2	INCSTEP[1:0]	RW	0h	Increment step size for the speaker thermal control algorithm (occurs at the temp sensor polling rate X the increment interval ratio.) 0h = 0.75dB 1h = 1.5dB 2h = 3.0dB 3h = 6.0dB
	1:0	DECSTEP[1:0]	RW	1h	Decrement step size for the speaker thermal control algorithm (occurs at the temp sensor polling rate.) 0h = 3dB 1h = 6dB 2h = 12dB 3h = 24dB

Table 81. THERMSPK Register

3.11.4.3. Speaker Thermal Algorithm Status Register

The thermal shutdown algorithm is monitored using the Speaker Thermal Algorithm Status Register

Register Address	Bit	Label	Type	Default	Description
Page 2, Reg 27 - 1Bh THRMSTAT	7	FPWDS	R	0	0: Speaker not powered down due to thermal algorithm 1: Speaker has been powered down because overtemp condition was present even though the speaker was muted.
	6:0	VOLSTAT[6:0]	R	NA	Current speaker volume value. If no overheat is being reported by the temperature sensor, this value should be equal to the greater of the left or right speaker volume setting.

Table 82. THRMSTAT Register

3.12. Short Circuit Protection

To avoid damage to the outputs if a short circuit condition should occur, both the headphone and BTL amplifiers implement short circuit protection circuits. The headphone output amplifier will detect the load current and limit its output if in an over current state. The BTL amplifier will sense a short to PVDD, ground, or between its +/- outputs and disable its output if a short is detected. After a brief time, controlled by SCTO[1:0], the amplifier will turn on again. If a short circuit condition is still present, the amplifier will disable itself again.

Register Address	Bit	Label	Type	Default	Description
Page 2 Reg 28 - 1Ch SCSTAT	7:5	Reserved	R	0h	Reserved
	4:3	ESDF	R	0h	ESD fault detected
	2	CPF	R	0h	charge pump fault detected
	1:0	CLSDF	R	0h	Class D fault detected

Table 83. SCSTAT Register

3.13. Analog Input to DAC/Headphone Bypass Path

A low power mode exists to allow the output from the analog input multiplexer to be selected as an input to the Headphone/Line Out amplifier. See A mux is used to control the source selection for the HP/LineOut amplifier. The MUX selection is controlled by the ABYPASS bit.

3.14. Headphone Switch

The HPDET pin is used to detect connection of a headphone when this pin is connected to a mechanical switch located within the headphone jack. When headphone insertion into the headphone jack is detected, the codec can automatically disable the speaker outputs and enable the headphone outputs. Control bits determine the meaning and polarity of the input.

3.14.1. Headphone Switch Control Register

Register Address	Bit	Label	Type	Default	Description
Page 2, Reg 24 - 18h HPSW	7:5	RSVD	R	0	Reserved
	4	HPDSTATE	R	0	HP-DET Pin State 0 = HP_DET pin low 1 = HP_DET pin high
	3:2	HPSWEN[1:0]	RW	00b	Headphone Switch Enable 00 =: Headphone switch disabled 01 =: Headphone switch enabled for Speaker Outputs 10 and 11 are Reserved
	1	HPSWPOL	RW	0	Headphone Switch Polarity 0: HPDETECT high = headphone 1: HPDETECT high = speaker
	0	TSDEN	RW	0	Thermal Shutdown Enable 0: thermal shutdown disabled 1: thermal shutdown enabled

Table 84. HPSW Register

HPSWEN	HPSWPOL	HP_DET Pin state	HPOut	SPKOut	HeadPhone Enable	Speaker Enabled
00	X	X	0	0	no	no
00	X	X	0	1	no	yes
00	X	X	1	0	yes	no
00	X	X	1	1	yes	yes
01	0	0	X	0	no	no
01	0	0	X	1	no	yes
01	0	1	0	X	no	no
01	0	1	1	X	yes	no
01	1	0	0	X	no	no
01	1	0	1	X	yes	no
01	1	1	X	0	no	no
01	1	1	X	1	no	yes

Table 85. Headphone Operation

Note:HPOut = Logical OR of the HPL and HPR enable (power state) bits1.
Note:SPKOut = Logical OR of the SPKL and SPKR enable (power state) bits

4. ANALOG INPUT AUDIO PROCESSING

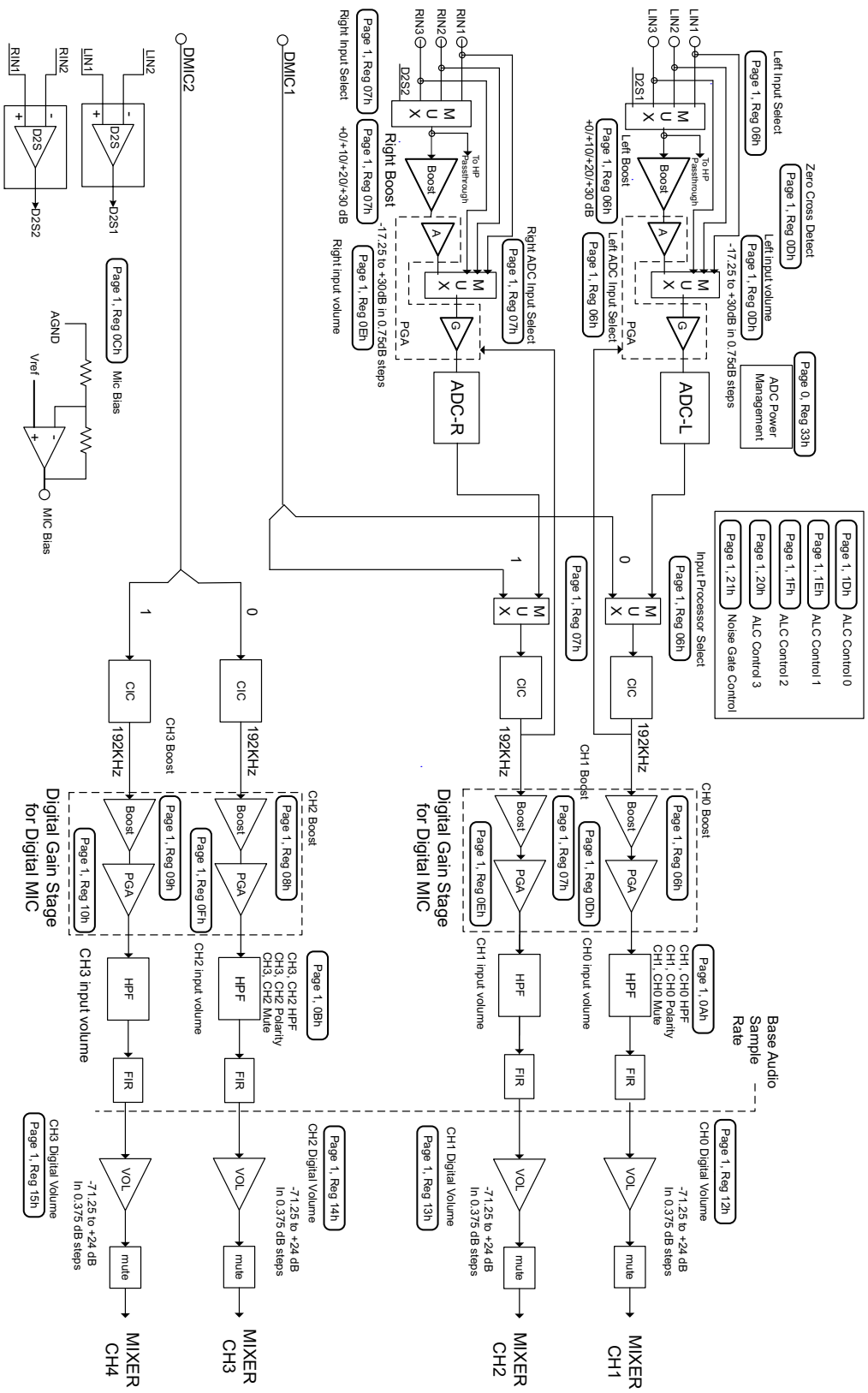


Figure 14. Input Audio Processing

4.1. Overview

The TSCS454xx supports three stereo analog and one stereo differential, four digital microphone inputs, and three digital, stereo I2S inputs,The analog and digital mic inputs of the TSCS454xx are processed and controlled through a four channel Input Processor. The first two channels of the Input Processor can process either the output from the ADC or the digital mic input from the DIGMIC1 input. The remaining two channels of the Input Processor are dedicated to the digital microphone input via the DIGMIC2 pin. The Input Processor supports volume control functions, ALC, high-pass filter, polarity, and mute functions for each channel.

4.2. Analog Audio Inputs

The TSCS454xx provides multiple high impedance, low capacitance AC-coupled analog inputs with an input signal path to the stereo ADCs. Prior to the ADC, there is a multiplexor that allows the system to select which analog input is selected for input to the ADC. Following the mux, there is a programmable gain amplifier (PGA) and also an optional microphone gain boost. The gain of the PGA can be controlled either by the system, or by the on-chip level control function. Signal inputs are biased internally so AC coupling capacitors are required when connecting microphones (due to the 2.5V microphone bias) or when offsets would cause unacceptable “zipper noise” or pops when changing PGA or boost gain settings. To avoid audio artifacts, the line inputs are kept biased to analog ground when they are muted or the device is placed into standby mode.

4.3. Input Processor Analog Input Control

The TSCS454xx Input Processor controls the selection of the analog input to the ADC, gain boost, microphone bias generation, and differential input control.

4.3.1. Channel 0 Input Audio Control Register

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 6 -6h CH0AIC	7:6	INSELL[1:0]	RW	00	Left Channel Analog Input Select 00 = LINPUT1 01 = LINPUT2 10 = LINPUT3 11 = D2S
	5:4	MICBST0[1:0]	RW	00	Left Channel Microphone Gain Boost 00 = Boost off (bypassed) 01 = 10dB boost 10 = 20dB boost 11 = 30dB boost
	3:2	LADCIN	RW	0	Left Channel ADC Input Select 00 = LINPUT1 Bypass 01 = LINPUT2 Bypass 10 = LINPUT3 Bypass 11 = Left Input MUX Output
	1	BYPSPGA0	RW	0	Bypass left channel PGA amplifier 1 = Bypass PGA amplifier 0 = PGA amplifier
	0	IPCH0S	RW	0	Input Processor Channel 0 Input Select - The Left ADC is powered when the DMIC input is selected. 0 = Select ADC Left 1 = Select DMIC Channel 0

Table 85. CH0AIC Register

4.3.2. Channel 1 Audio Input Control Register

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 7 - 7h CH1AIC	7:6	INSELR[1:0]	RW	00	Right Channel Analog Input Select 00 = RINPUT1 01 = RINPUT2 10 = RINPUT3 11 = D2S
	5:4	MICBST1[1:0]	RW	00	Right Channel Microphone Gain Boost 00 = Boost off (bypassed) 01 = 10dB boost 10 = 20dB boost 11 = 30dB boost
	3:2	RADCIN	RW	0	Right Channel ADC Input Select 00 = RINPUT1 Bypass 01 = RINPUT2 Bypass 10 = RINPUT3 Bypass 11 = Right Input MUX Output
	1	BYPSPGA1	RW	0	Bypass right channel PGA amplifier 1 = Bypass PGA amplifier 0 = PGA amplifier
	0	IPCH1S	RW	0	Input Processor Channel 1 Input Select - The Right ADC is powered when the DMIC input is selected. 0 = Select ADC Right 1 = Select DMIC Channel 1

Table 86. CH1AIC Register

4.3.3. Channel 2 Audio Input Control Register

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 8 -8h CH2AIC	7:6	RSVD	R	0	Reserved
	5:4	MICBST2[1:0]	RW	0	Right Channel Microphone Gain Boost 00 = Boost off (bypassed) 01 = 10dB boost 10 = 20dB boost 11 = 30dB boost
	3:0	RSVD	R	0	Reserved

Table 87. CH2AIC Register

4.3.4. Channel 3 Audio Input Control Register

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 9 - 9h CH3AIC	7:6	RSVD	R	0	Reserved
	5:4	MICBST3[1:0]	RW	0	Right Channel Microphone Gain Boost 00 = Boost off (bypassed) 01 = 10dB boost 10 = 20dB boost 11 = 30dB boost
	3:0	RSVD	R	0	Reserved

Table 88. CH3AIC Register

4.4. Input Processor Digital Processing

4.4.1. The Input Processor also provides control of polarity, mixing, volume/gain, limiting, and automatic level control. ***Input Processor Control Register 0***

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 10 - Ah ICTL0	7	IN1POL	RW	0	Input Channel 1 Polarity 0 = normal 1 = inverted
	6	IN0POL	RW	0	Input Channel 0 Polarity 0 = normal 1 = inverted
	5:4	INPCH10SEL[1:0]	RW	0	Input Processor Channel 1, 0 Select 00 = Stereo, Channel 0 = Left Channel 1 = Right 01 = Channel 0 output on Channels 1 and 0 10 = Channel 1 output on Channels 1 and 0 11 = 1/2 Channel 0 and 1/2 Channel 1 output on Channels 1 and 0
	3	IN1MUTE	RW	1	0 = Input channel 1 un-muted 1 = Input channel 1 muted
	2	IN0MUTE	RW	1	0 = Input channel 0 un-muted 1 = Input channel 0 muted
	1	IN1HP	RW	0	Input Channel 1 High Pass Filter Disable
	0	IN0HP	RW	0	Input Channel 0 High Pass Filter Disable

Table 89. ICTL0 Register

4.4.2. Input Processor Control Register 1

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 11 - Bh ICTL1	7	IN3POL	RW	0	Input Channel 3 Polarity 0 = normal 1 = inverted
	6	IN2POL	RW	0	Input Channel 2 Polarity 0 = normal 1 = inverted
	5:4	INPCH32SEL[1:0]	RW	0	Input Processor Channel 3, 2 Select 00 = Stereo, Channel 2 = Left Channel 3 = Right 01 = Channel 2 output on Channels 3 and 2 10 = Channel 3 output on Channels 3 and 2 11 = 1/2 Channel 2 and 1/2 Channel 3 output on Channels 3 and 2
	3	IN3MUTE	RW	1	0 = Input channel 3 un-muted 1 = Input channels 3 muted
	2	IN2MUTE	RW	1	0 = Input channel 2 un-muted 1 = Input channels 2 muted
	1	IN3HP	RW	0	Input Channel 3 High Pass Filter Disable
	0	IN2HP	RW	0	Input Channel 2 High Pass Filter Disable

Table 90. ICTL1 Register

4.5. Microphone Bias

The MICBIAS1,2 outputs are used to bias electric type microphones. They provide a low noise reference voltage used for an external resistor biasing network. The MICBx control bits are used to enable the individual outputs. A series 2.2K ohm resistor is provided in series with each MICBIAS output.

Each MICBIAS output can source up to 500uA of current

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 12 - Ch MICBIAS	7:6	MICBOV1[1:0]	RW	00b	Mic Bias 1 Output Voltage 00 = 2.5V 01 = 2.1V 10 = 1.8V 11 = Bypass, uses MICBIAS VDD Supply
	5:4	MICBOV2[1:0]	RW	00b	Mic Bias 2 Output Voltage 00 = 2.5V 01 = 2.1V 10 = 1.8V 11 = Bypass, uses MICBIAS VDD Supply
	3:0	RSVD	RW	00b	Reserved

Table 91. MICBIAS Register

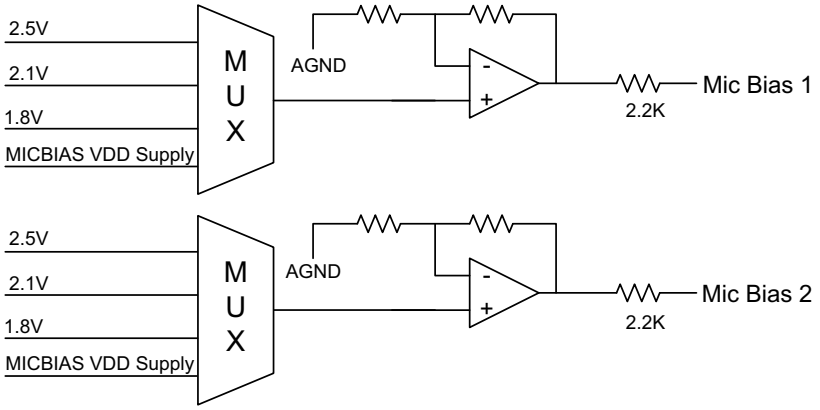


Figure 15. MIC Bias Generator

4.6. Programmable Gain Control

The Programmable Gain Amplifier (PGA) enables the input signal level to be matched to the ADC input range. Amplifier gain is adjustable across the range +30dB to –17.25dB (using 0.75dB steps). The PGA can be controlled directly by the system software using the PGA Control registers (PGACTL0, PGACTL1, PGACTL2 and PGACTL3), or alternately the Automatic Level Control (ALC) function can automatically control the gain. If the ALC function is used, writing to the PGA Control registers has no effect.

Left and right input gains are independently adjustable. By controlling the update bit PGAVOLU Page 1, Reg 28 - VOL-CTLU register, the left and right gain settings can be simultaneously updated. To eliminate zipper noise, PGA0ZC and PGA1ZC bits enable a zero-cross detector to insure changes only occur when the signal is at zero. A time-out for zero-cross is also provided, using TOEN in register Page 1, R17.

Software can also mute the inputs in the analog domain.

4.6.1. PGA Control Registers

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 13 - Dh PGACTL0	7	PGA0MUTE	RW	1	Channel 0 PGA Mute 1 = Mute 0 = Un mute
	6	PGA0ZC	RW	0	Channel 0 Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately Note: If PGAVOLU is set, this setting will take effect after the next write to the PGA0VOL[5:0]
	5:0	PGA0VOL[5:0]	RW	010111 (0dB)	Channel 0 Input Volume Control 111111 = +30dB 111110 = +29.25dB ... 0.75dB steps down to 000000 = -17.25dB
Page 1, Reg 14 - Eh PGACTL1	7	PGA1MUTE	RW	1	Channel 1 PGA Mute 1 = Mute 0 = Un mute
	6	PGA1ZC	R	0	Channel 1 Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately Note: If PGAVOLU is set, this setting will take effect after the next write to the PGA1VOL[5:0]
	5:0	PGA1VOL[5:0]	RW	010111 (0dB)	Channel 1 Input Volume Control 111111 = +30dB 111110 = +29.25dB ... 0.75dB steps down to 000000 = -17.25dB
Page 1, Reg 15 - Fh PGACTL2	7	PGA2MUTE	RW	1	Channel 2 PGA Mute 1 = Mute 0 = Un mute
	6	RSVD	R		Reserved
	5:0	PGA2VOL[5:0]	RW	010111 (0dB)	Channel 2 Input Volume Control 111111 = +30dB 111110 = +29.25dB ... 0.75dB steps down to 000000 = -17.25dB
Page 1, Reg 16 - 10h PGACTL3	7	PGA3MUTE	RW	1	Channel 3 PGA Mute 1 = Mute 0 = Un mute
	6	RSVD	R		Reserved
	5:0	PGA3VOL[5:0]	RW	010111 (0dB)	Channel 3 Input Volume Control 111111 = +30dB 111110 = +29.25dB ... 0.75dB steps down to 000000 = -17.25dB

Table 92. PGACTL0 Registers

4.6.2. PGA Zero Cross Control Register

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 17 - 11h PGAZ	7:2	RSVD	R	0	Reserved
	1	INHPOR	RW	0	Input High-Pass Filter Offset Result (applies to all 4 input processor channels) 0 = discard calculated offset when HPF disabled 1 = store and use last calculated offset when HPF disabled
	0	TOEN	RW	0	Zero Cross Time-out Enable 0: Time-out Disabled 1: Time-out Enabled - volumes updated if no zero cross event has occurred before time-out

Table 93. PGA Zero Cross Control Register

4.7. ADC Digital Filter

To provide the correct sampling frequency on the digital audio outputs, ADC filters perform true 24-bit signal processing and convert the raw multi-bit oversampled data from the ADC using the digital filter path illustrated below.

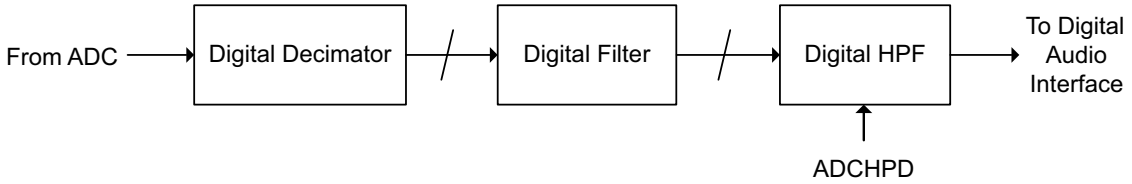


Figure 16. ADC Filter Data path

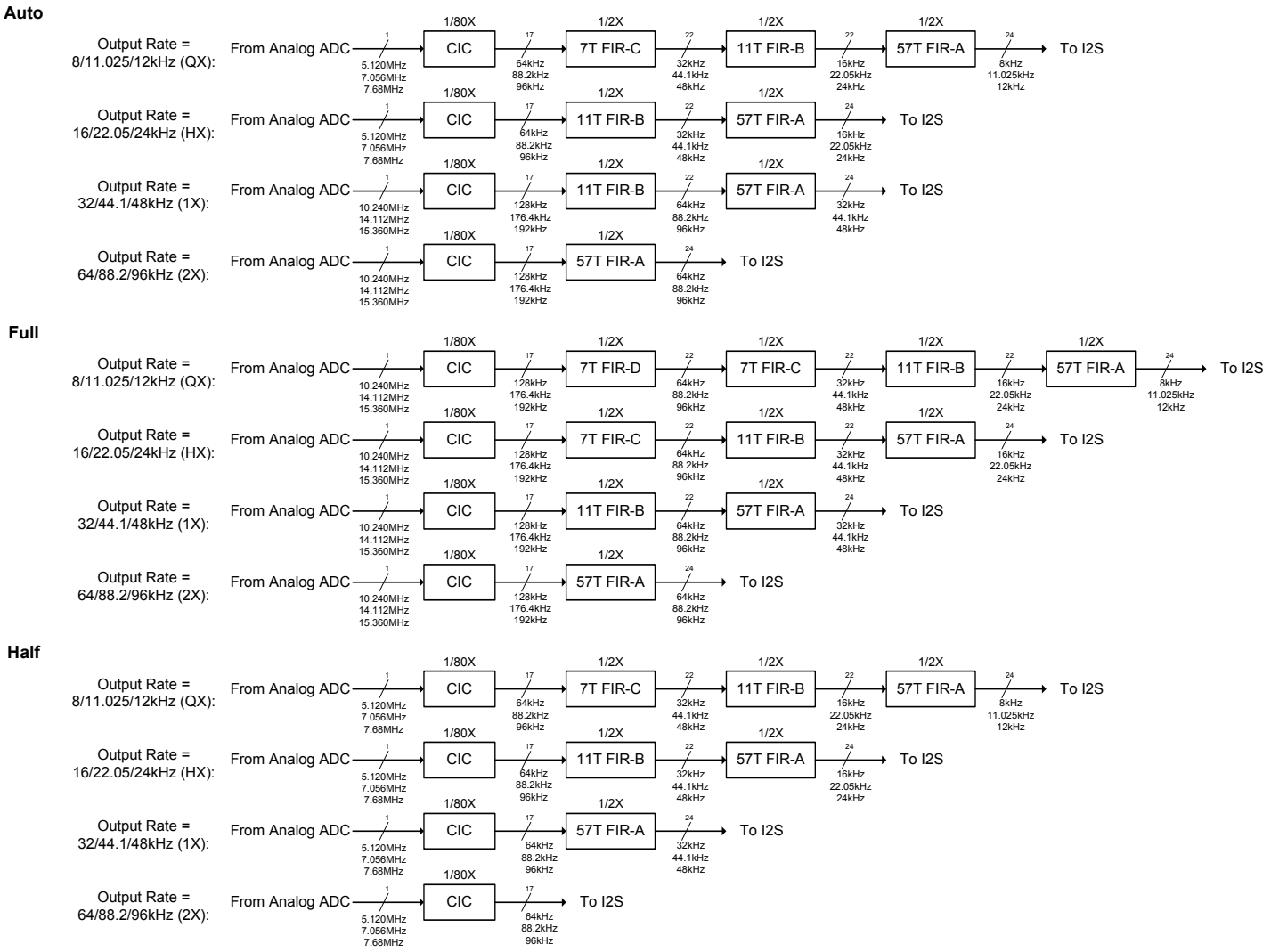


Figure 17. ADC Input processing

The ADC digital filters contain a software-selectable digital high pass filter. When the high-pass filter is enabled, the dc offset is continuously calculated and subtracted from the input signal. The HPOR bit enables the last calculated DC offset value to be stored when the high-pass filter is disabled; this value will then continue to be subtracted from the input signal. To provide support for calibration, the stored and subtracted value will not change unless the high-pass filter is enabled even if the DC value is changed. The high pass filter may be enabled separately for each of the left and right channels.

The output data format can be programmed by the system. This allows stereo or mono recording streams at both inputs. Software can change the polarity of the output signal.

4.8. Input Channel Volume Control

Channel volume can be controlled digitally, across a gain and attenuation range of -71.25dB to +24dB (0.375dB steps). The level of attenuation is specified by an eight-bit code ICH0VOL, ICH1VOL, ICH2VOL and ICH3VOL. The value “00000000” indicates mute; other values describe the number of 0.375dB steps above -71.25dB.

The INPVOLU bit (Section 7.3.1 “Input Volume Update” on page 117) controls the updating of digital volume control data. for the Input Channels. When INPVOLU is written as ‘0’, the ADC digital volume is immediately updated with the ICH0VOL data when the Left ADC Digital Volume register is written. When INPVOLU is set to ‘1’, the ICH0VOL data is held in an internal holding register until the ICH1VOL is written.

4.8.1. CH0, CH1 Input Volume Control Registers

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 18 - 12h ICH0VOL	7:0	ICH0VOL [7:0]	RW	10111111 (0dB)	Channel 0 Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -71.25dB 0000 0010 = -70.875dB ... 0.375dB steps up to 1111 1111 = +24dB Note: If INPVOLU is set, this setting will take effect after the next write to the ICH1VOL register.
Page 1, Reg 19 -13h ICH1VOL	7:0	ICH1VOL [7:0]	RW	10111111 (0dB)	Channel 1 Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -71.25dB 0000 0010 = -70.875dB ... 0.375dB steps up to 1111 1111 = +24dB

Table 94. ICH0VOL/ ICH1VOL Registers

4.8.2. CH2, CH3 Input Volume Control Register

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 20 - 14H ICH2VOL	7:0	ICH2VOL [7:0]	RW	10111111 (0dB)	Channel 2 Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -71.25dB 0000 0010 = -70.875dB ... 0.375dB steps up to 1111 1111 = +24dB Note: If IPNVOLU is set, this setting will take effect after the next write to theICH3VOL register.
Page 1, Reg 21 - 15h ICH3VOL	7:0	ICH3VOL [7:0]	RW	10111111 (0dB)	Channel 3 Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -71.25dB 0000 0010 = -70.875dB ... 0.375dB steps up to 1111 1111 = +24dB

Table 95. ICH2VOL/ ICH3VOL Registers

4.9. Automatic Level Control (ALC)

The TSCS454xx has an automatic level control to achieve recording volume across a range of input signal levels. The device uses a digital peak detector to monitor and adjusts the PGA gain to provide a signal level at the ADC input. A range of adjustment between –6dB and –28.5dB (relative to ADC full scale) can be selected. The device provides programmable attack, hold, and decay times to smooth adjustments. The level control also features a peak limiter to prevent clipping when the ADC input exceeds a threshold. Note that if the ALC is enabled, the input volume controls are ignored.

4.9.1. ALC Operation

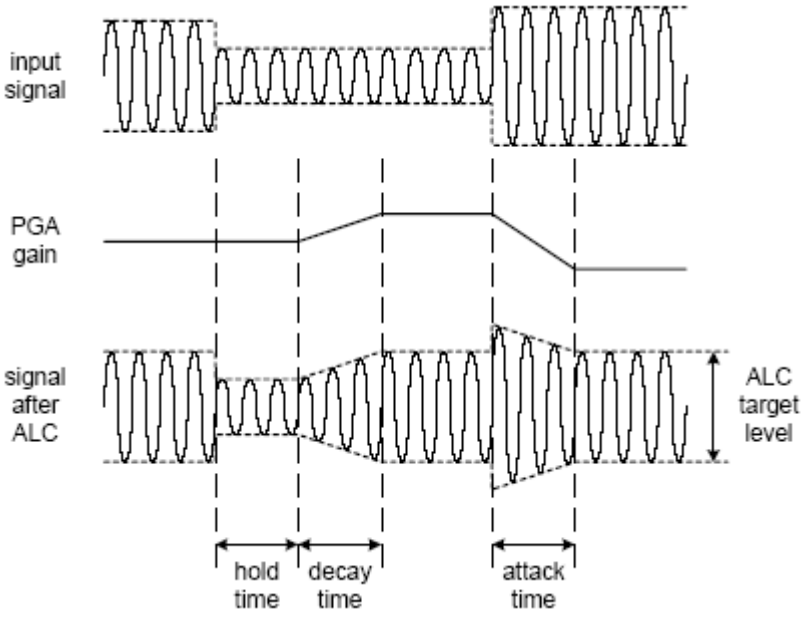


Figure 18. ALC Operation

When ALC is enabled, the recording volume target can be programmed between –6dB and –28.5dB (relative to ADC full scale). The ALC will attempt to keep the ADC input level to within +/-0.5dB of the target level. An upper limit for the PGA gain can also be imposed, using the MAXGAIN control bits.

Hold time specifies the delay between detecting a peak level being below target, and the PGA gain beginning to ramp up. It is specified as 2^n*2.67mS, enabling a range between 0mS and over 40s.; ramp-down begins immediately if the signal level is above the target.

Decay (Gain Ramp-Up) Time is the time that it takes for the PGA to ramp up across 90% of its range. The time is 2^n*24mS. The time required for the recording level to return to its target value therefore depends on the decay time and on the gain adjustment required.

Attack (Gain Ramp-Down) Time is the time that it takes for the PGA to ramp down across 90% of its range. Time is specified as 2^n*24mS. The time required for the recording level to return to its target value depends on both the attack time and on the gain adjustment required.

When operating ,the peak detector can be programmed to use a specific channel maximum peak value or take the maximum of the currently enabled processing channels,, and all the PGAs use the same gain setting. If the ALC function is only enabled on specific channels, only that PGA is controlled by the ALC mechanism, and the other channels runs independently using the PGA gain set through the control registers.

4.9.2. ALC Control Registers

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 29 - 1Dh ALCCTL0	7	ALCMODE	RW	0	ALC Mode Selection 0 = ALC Mode 1 = Limiter Mode
	6:4	ALC REF	RW	4h	ALC Reference Channel Selection 000: Channel 0 001: Channel 1 010: Channel 2 011: Channel 3 100-111: Peal Across All Enabled Channels
	3	ALCEN3	RW	0 (OFF)	Channel 3 ALC function select 0 = ALC off 1 = ALC On
	2	ALCEN2	RW	0 (OFF)	Channel 2 ALC function select 0 = ALC off 1 = ALC On
	1	ALCEN1	RW	0 (OFF)	Channel 1 ALC function select 0 = ALC off 1 = ALC On
	0	ALCEN0	RW	0 (OFF)	Channel 0 ALC function select 0 = ALC off 1 = ALC On
Page 1, Reg 30 - 1Eh ALCCTL1	7	RSVD	R	0	Reserved
	6:4	MAXGAIN [2:0]	RW	111 (+30dB)	Set Maximum Gain of PGA 111: +30dB 110: +24dB ….(-6dB steps) 001: -6dB 000: -12dB
	3:0	ALCL [3:0]	RW	1011 (-12dB)	ALC target – sets signal level at ADC input 0000 = -28.5dB fs 0001 = -27.0dB fs … (1.5dB steps) 1110 = -7.5dB fs 1111 = -6dB fs

Table 96. ALCCTL0 /ALCCTL1 Registers

Register Address	Bit	Label	Type	Default	Description
Page 3, Reg 31 - 1Fh ALCCTL2	7	ALCZC	RW	0 (zero cross off)	ALC uses zero cross detection circuit.
	6:4	MINGAIN[2:0]	RW	000	Sets the minimum gain of the PGA 000 = -17.25db 001 = -11.25 ... 110 = +18.75dB 111 = +24.75db where each value represents a 6dB step.
	3:0	HLD [3:0]	RW	0000 (0ms)	ALC hold time before gain is increased. 0000 = 0ms 0001 = 2.67ms 0010 = 5.33ms … (time doubles with every step) 1111 = 43.691s
Page 3, Reg 32 - 20h ALCCTL3	7:4	DCY [3:0]	RW	0011 (192ms)	ALC decay (gain ramp-up) time 0000 = 24ms 0001 = 48ms 0010 = 96ms … (time doubles with every step) 1010 or higher = 24.58s
	3:0	ATK [3:0]	RW	0010 (24ms)	ALC attack (gain ramp-down) time 0000 = 6ms 0001 = 12ms 0010 = 24ms … (time doubles with every step) 1010 or higher = 6.14s

Table 96. ALCCTL0 /ALCCTL1 Registers

4.9.3. Peak Limiter

To prevent clipping, the ALC circuit also includes a limiter function. If the ADC input signal exceeds 87.5% of full scale (–1.16dB), the PGA gain is ramped down at the maximum attack rate, until the signal level falls below 87.5% of full scale. This function is automatically enabled whenever the ALC is enabled.

4.9.4. Input Threshold

To avoid hissing during quiet periods, the TSCS454xx has an input threshold noise gate function that compares the signal level at the inputs to a noise gate threshold. Below the threshold, the programmable gain can be held , or the ADC output can be muted. The threshold can be adjusted in increments of 1.5dB.
The noise gate activates when the signal-level at the input pin is less than the Noise Gate Threshold (NGTH) setting. The ADC output can be muted. Alternatively, the PGA gain can be held .
The threshold is adjusted in 1.5dB steps. The noise gate only works in conjunction with the ALC, and always operates on the same channel(s) as the ALC.

Noise Gate Control Register

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 33 - 21h NGATE	7:3	NGTH [4:0]	RW	00000	Noise gate threshold (compared to ADC full-scale range) 00000 -76.5dBfs 00001 -75dBfs … 1.5 dB steps 11110 -31.5dBfs 11111 -30dBfs
	2:1	NGG [1:0]	RW	00	Noise gate type X0 = PGA gain held constant 01 = mute ADC output 11 = reserved (do not use this setting)
	0	NGAT	RW	0	Noise gate function enable 1 = enable 0 = disable

Table 97. NGATE Register

4.9.5Digital Microphone Support

TSCS454 supports input connection for up to four digital microphones via two stereo DMIC_x pins.

The digital microphone interface permits connection of a digital microphone(s) to the CODEC via the DMIC_x, and DMIC_CLK 2-pin interface. DMIC_DATx is an input that carries individual channels of digital microphone data to the Input Processor. In the event that a single microphone is used, the data is ported to both Input Processor channels. This mode is selected using a control bit and the left time slot is copied to the left and right inputs.

The DMIC_CLK output is synchronous to the internal clock and is adjustable in 4 steps. Each step provides a clock that is a multiple of the chosen internal ICLK base rate and modulator rate.The default frequency is and 80 times the base rate for 44.1KHz and 48KHz base rates.

4.9.5.1.DMIC Clock

SDM Rate	DMRate [1:0]	Base Rate	Internal CLK	DMIC_CLK divisor	DMIC_CLK
Full	00	44.1 KHz	56.448 MHz	16	3.528 MHz
		48 KHz	61.440 MHz	16	3.84 MHz
	01	44.1 KHz	56.448 MHz	20	2.8224 MHz
		48 KHz	61.440 MHz	20	3.072 MHz
	10	44.1 KHz	56.448 MHz	24	2.352 MHz
		48 KHz	61.440 MHz	24	2.56 MHz
	11	44.1 KHz	56.448 MHz	32	1.764 MHz
		48 KHz	61.440 MHz	32	1.92 MHz

Table 98. DMIC Clock

SDM Rate	DMRate [1:0]	Base Rate	Internal CLK	DMIC_CLK divisor	DMIC_CLK
Half	00	44.1 KHz	56.448 MHz	16	3.528 MHz
		48 KHz	61.440 MHz	16	3.84 MHz
	01	44.1 KHz	56.448 MHz	24	2.352 MHz
		48 KHz	61.440 MHz	24	2.56 MHz
	10	44.1 KHz	56.448 MHz	32	1.764 MHz
		48 KHz	61.440 MHz	32	1.92 MHz
	11	44.1 KHz	56.448 MHz	40	1.4112 MHz
		48 KHz	61.440 MHz	40	1.536 MHz

Table 98. DMIC Clock

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To conserve power, the analog portion of the ADC will be turned off if the D-mic input is selected. When switching from the digital microphone to an analog input to the ADC, the analog portion of the ADC will be brought back to a full power state and allowed to stabilize before switching from the digital microphone to the analog input. This should take less than 10mS.

If the ADC path is powered down, the DMIC_CLK output will be driven low to place the DMIC element into a low power state. (Many digital microphones will enter a low power state if the clock input is held at a DC level or toggled at a slow rate.)

The TSCS454xx device supports the following digital microphone configurations:

Digital Mics	Data Sample	Notes
0	N/A	No Digital Microphones
1	Single Edge	When using a microphone that supports multiplexed operation (2-mics can share a common data line), configure the microphone for “Left” and select mono operation. “Left” D-mic data is used for ADC left and right channels.
2	Double Edge	External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don’t support alternative clock edge (multiplexed output) capability.

Table 99. Valid Digital Mic Configuration

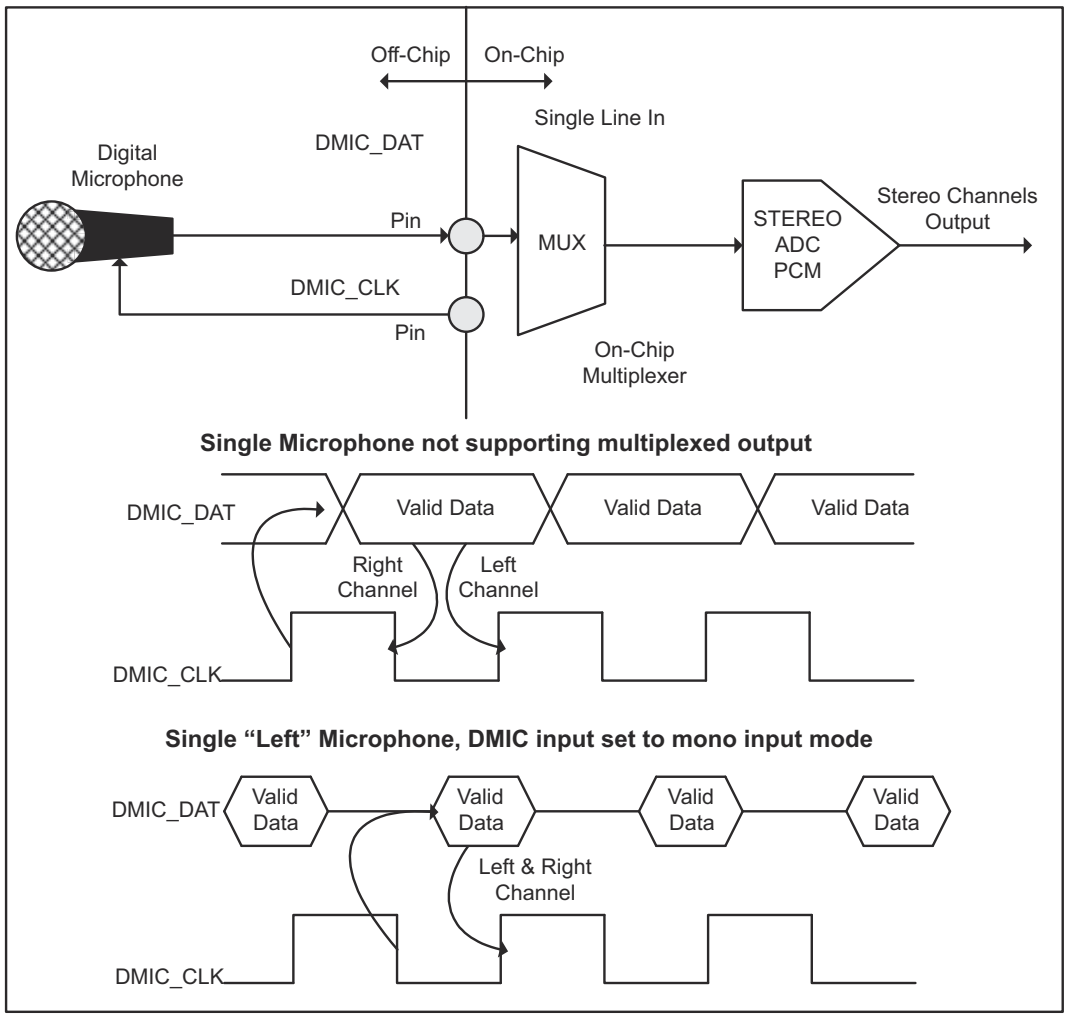


Figure 19. Mono Digital Microphone (data is ported to both left and right channels)

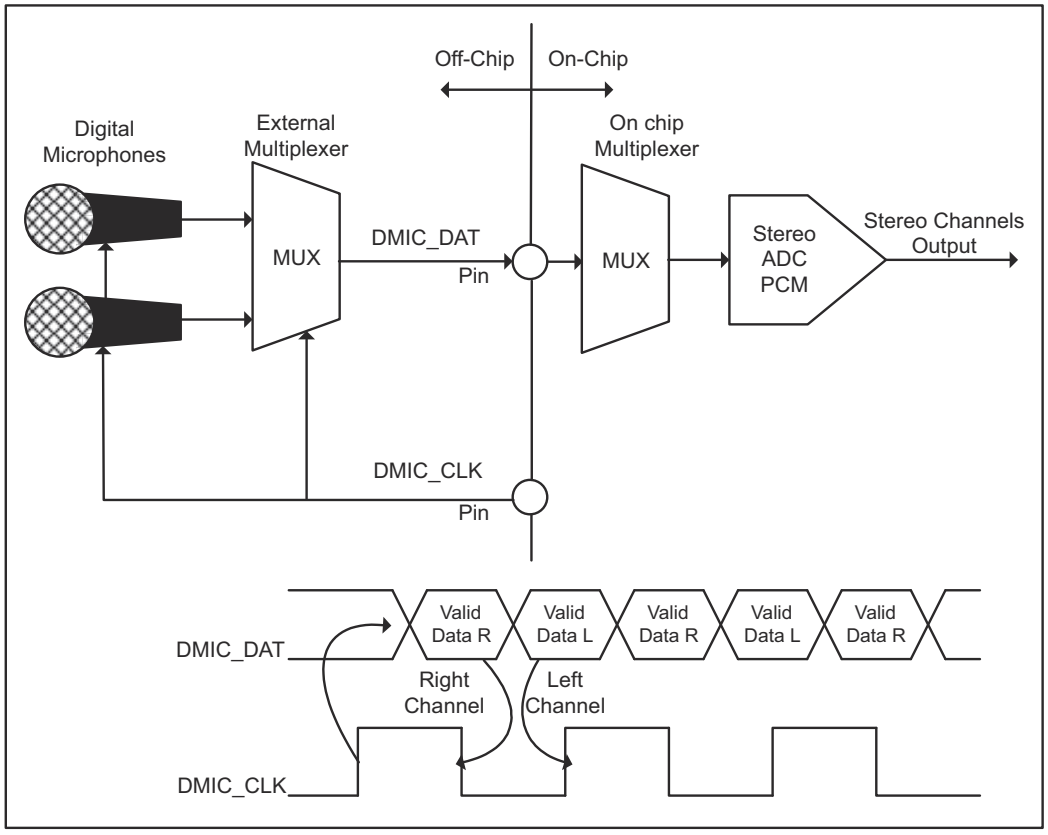


Figure 20. Stereo Digital Microphone

4.9.5.2.Digital Mic Control Register

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 34 - 22h DMICCTL	7	DMIC2EN	RW	0	Digital Microphone 2 Enable 0 = DMIC interface is disabled (DMIC_CLK2 low, DMIC muted) 1 = DMIC interface is enabled
	6	DMIC1EN	RW	0	Digital Microphone 1 Enable 0 = DMIC interface is disabled (DMIC_CLK1 low, DMIC muted) 1 = DMIC interface is enabled
	5	RSVD	R	00	Reserved
	4	DMONO	RW	0	0 = stereo operation, 1 = mono operation (left channel duplicated on right)
	3:2	DMDCLKj[1:0]	RW	00	Selects when the D-Mic data is latched relative to the DMIC_CLKx. 00 = Left data rising edge / right data falling edge 01 = Left data center of high / right data center of low 10 = Left data falling edge / right data rising edge 11 = Left data center of low / right data center of high
	1:0	DMRATE[1:0]	RW	00	Selects the DMIC clock rate: See DMIC clock table

Table 100. DMICCTL Register

5. DIGITAL AUDIO INPUT-OUTPUT

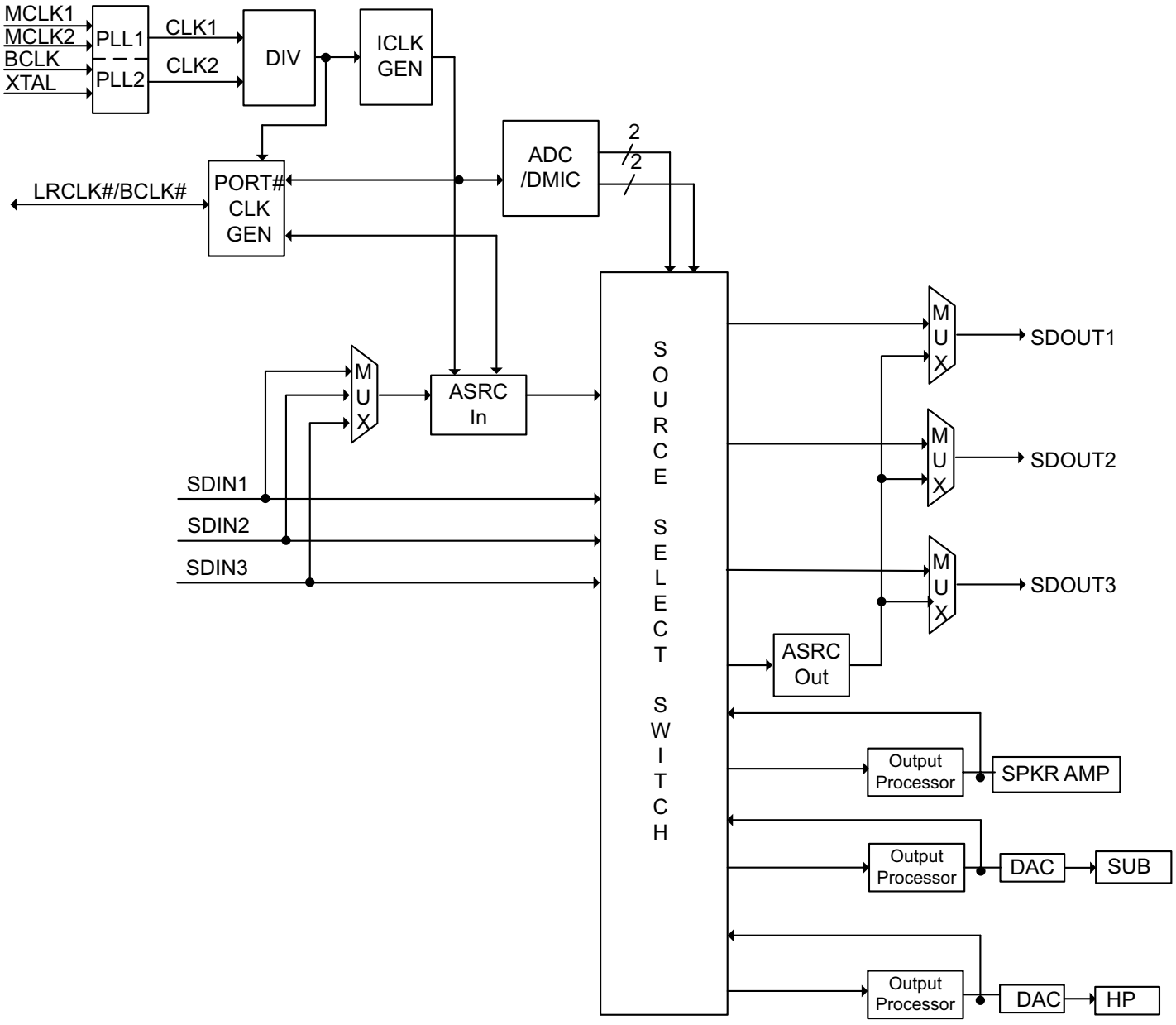


Figure 21. Digital Audio Interface Block Diagram

5.1. PCM Interfaces

- For digital audio data, the TSCS454xx uses four pins for each I2S/PCM audio interface.
- SDOUT1: I2S/TDM data output
- SDOUT2: I2S/PCM2 data output
- SDOUT3: I2S/PCM3 data output

- LRCLK1: I2S/TDM data alignment clock
- LRCLK2: I2S/PCM2 data alignment clock
- LRCLK3: I2S/PCM3 data alignment clock

- BCLK1: I2S1/TDM1 Bit clock, for synchronization
- BCLK2: I2S2/PCM2 Bit clock, for synchronization
- BCLK3: I2S3/PCM3 Bit clock, for synchronization

- SDIN1: I2S/PCM1 data input
- SDIN2: I2S/PCM2 data input
- SDIN3: I2S/PCM3 data input

	I2S AUDIO INTERFACES					
	INPUT	OUTPUT	INPUT	OUTPUT	INPUT	OUTPUT
I2S Port	I2S Port 1		I2S Port 2		I2S Port 3	
INPUT/OUTPUT Pins	SDIN1	SDOUT1	SDIN2	SDOUT2	SDIN3	SDOUT3
Master/Slave	Master/Slave	Master/Slave	Master/Slave	Master/Slave	Master/Slave	Master/Slave

Table 101. I2S Audio Interfaces

Different data formats are supported as below:

- I2S
  - Left justified
  - Right justified
- TDM
- PCM
  - Linear

All of these modes are MSB first.

5.1.1. PCM(I2S) Audio Input Interface Mapping

The PCM Inputs are connected to the functional blocks as follows:

I2S Audio Input	**Functional Blocks**			
SDIN1	I2S Input Port1	SSS	or ASRC In -->	SSS
SDIN2	I2S Input Port2	SSS	or ASRC In -->	SSS
SDIN3	I2S Input Port3	SSS	or ASRC In -->	SSS

Table 102. PCM(I2S) Audio Input Interface Mapping

The outputs of the I2S Inputs Ports 1-3 are connected to the ASRC's 1-3 respectively.

5.1.2. PCM(I2S) Audio Output Interface Mapping

Audio Data Source	I2S Output
Source Select Switch (SSS) or ASRC Out	SDOUT1
Source Select Switch (SSS) or ASRC Out	SDOUT2
Source Select Switch (SSS) or ASRC Out	SDOUT3

Table 103. PCM(I2S) Audio Output Interface Mapping

5.1.3. PCM control Register

Register Address	Bit	Label	Read/ Write	Reset Value	Description
Page 0, Reg 31 - 2Fh PCMPXCTL0	7:3	RSVD	R	0	Reserved
	2	PCMFLENPX	RW	0	PCM Frame Length in master mode, 0 = 128 bits peer frame, 1 = 256 bits per frame
	1	SLSYNCPX	RW	0	hort-Long Frame Sync, 0 = one clock wide, 1 = one slot wide
	0	BDELAYPX	RW	0	Data delay relative to start of frame in PCM mode, 0 = data not delayed relative to start of frame, 1 = data delayed by one clock relative to start of frame

Table 104. PCMPXCTL0 Register

Register Address	Bit	Label	Read/ Write	Reset Value	Description
Page 0, Reg 3 - 2Eh PCMPXCTL1	7	RSVD	R	0	Reserved
	6	PCMMOMP2	RW	0	PCM mono output mode, 0- When number of slots = 1, select left data for slot0, 1-select left data for slot0 = 1, select right data for slot0.
	5	PCMSOP2	RW	0	Number of Active Slots per PCM Output Frame, 0 = one, 1 = two
	4:3	PCMDSSP2	RW	0	PCM Data Slots Size, 00 = 16 bit, 01 =24 bit, 10 = 32 bit, 11=Reserved
	2		R	0	Reserved
	1	PCMMIMP2		0	PCM mono input mode, 0- When number of slots = 1, select left data for slot0, silence for slot1, 1-When number of slots = 1, select left and right data for slot0.
	0	PCMSIP2		0	Numver of Active Slots per PCM Input Frame, 0 = one, 1 = two;

Table 105. PCMOXCTL1 Register

5.2. ASRC Input/Output Volume Controls

These controls provide adjustment of volume for the PCM audio streams sourced by the ASRC's. The ASRCVOLU bit controls the updating of digital volume control data. for the ASRCs. When ASRCVOLU is written as '0', the digital volume is immediately updated with the ASRCxLVOL data when the Left ASRC Digital Volume register is written. When ASRCxVOLU is set to '1', the ASRCxLVOL data is held in an internal holding register until the Right ASRC Digital Volume Register is written.

5.2.1. Output Data Mux Control Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 3A AUDIOMUX1	7:6	ASRCIMUX	RW	0	Input ASRC MUX:00-no input asrc, 01-input asrc assigned to i2si1, 10-input asrc assigned to i2si2, 11-input asrc assigned to i2si3
	5:3	I2S2MUX	RW	00	I2S2 output Mux Control:3'h0-i2si1, 3'h2-i2si2, 3'h3-i2si3,3'h4-ADC/DMIC1,3'h5-dmic2,3'h6-classd dsp out,3'h6-dac dsp out-sub dsp out
	2:0	I2S1MUX	RW	00	I2S1 output Mux Control:3'h0-i2si1, 3'h2-i2si2, 3'h3-i2si3,3'h4-ADC/DMIC1,3'h5-dmic2,3'h6-classd dsp out,3'h6-dac dsp out-sub dsp out

Table 106. AUDIOMUX1 Register

5.2.2. Output Data Mux Control Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 3B AUDIOMUX2	7:6	ASRCOMUX	RW	0	Output ASRC MUX:00-no input asrc, 01-input asrc assigned to i2so1, 10-input asrc assigned to i2so2, 11-input asrc assigned to i2so3
	5:3	DACMUX	RW	00	
	2:0	I2S3MUX	RW	00	

Table 107. AUDIOMUX2 Register

5.2.3. Output Data Mux Control Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 3C AUDIOMUX3	7:3	SUBMUX	RW	0	Reserved
	2:0	CLASSDMUX	RW	00	

Table 108. AUDIOMUX3 Register

5.2.4. I2S Input Volume Control Register

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 22 - 16h ASRCILVOL	7:0	ASRCILVOL [7:0]	RW	11101111 (0dB)	ASRC Input Left Digital Volume Control - 0.375dB steps 0000 0000 = Mute 0000 0001 = -90.25dB 0000 0010 = 89.875dB 1111 1111 = +6dB Note: If ASRCVOLU is set, this setting will take effect after the next right to the Right Input Volume registers.
Page 1, Reg 23 - 17h ASRCIRVOL	7:0	ASRCIRVOL [7:0]	RW	11101111 (0dB)	ASRC Input Right Digital Volume Control - 0.375dB steps 0000 0000 = Mute 0000 0001 = -90.25dB 0000 0010 = 89.875dB 1111 1111 = +6dB Note: If ASRCVOLU is set, this setting will take effect after the next right to the Right Input Volume registers.
Page 1, Reg 24 - 18h ASRCOLVOL	7:0	ASRCOLVOL [7:0]	RW	11101111 (0dB)	ASRC Output Left Digital Volume Control - 0.375dB steps 0000 0000 = Mute 0000 0001 = -90.25dB 0000 0010 = 89.875dB 1111 1111 = +6dB Note: If ASRCVOLU is set, this setting will take effect after the next right to the Right Input Volume registers.
Page 1, Reg 25 - 19h ASRCORVOL	7:0	ASRCORVOL [7:0]	RW	11101111 (0dB)	ASRC Output Right Digital Volume Control - 0.375dB steps 0000 0000 = Mute 0000 0001 = -90.25dB 0000 0010 = 89.875dB 1111 1111 = +6dB Note: If ASRCVOLU is set, this setting will take effect after the next right to the Right Input Volume registers.

Table 109. ASRCILVOL/ASRCIRVOL and ASRCOLVOL/ASRCORVOL Register

5.2.5. Volume Update Register

Register Address	Bit	Label	Read/ Write	Reset Value	Description
Page 1, Reg 28 - 1Ch VOLCTLU	7:4	RSVD	R	0	Reserved
	3	IFADE	RW	1	1 = Input Processor volume fades between old/new value 0 = Input Processor volume/mute changes immediately
	2	INPVOLU	RW	0	1 = Left Input Processor volume held until right input volume register written 0 = Left Input Processor volume updated immediately
	1	PGAVOLU	RW	0	1 = Left PGA input volume held until right input volume register 0 = Left PGA input volume updated immediately
	0	ASRCVOLU	RW	0	1 = Left ASRC volume held until right input volume register written. This affects input and output ASRC volume controls. 0 = Left ASRC volume updated immediately

Table 110. VOLCTLU Register

5.3. Audio Interface Clocking Options

Three pairs of bit clock and frame signals (BCLK/LRCLK) are available for clocking the various I2S interface ports. I2S Ports 1-3 are associated with I2S inputs and the BCLK/LRCLK signals can be inputs (Slave operation) or outputs (Master Operation). .Each I2S port has register bits for controlling the I2S format, the number of bits, and the polarity of the BCLK and LRCLK signals.

5.4. Master and Slave Mode Operation

The TSCS454xx I2S ports can be used as either a master or slave device, selected by the PORTxMS Bits. Both the I2S inputs and outputs operate at the same rate. When an I2S Port is operating as a master, the TSCS454xx generates the bit clocks and frame clock signals. In slave mode, the TSCS454xx assumes the input audio data is aligned to clocks it receives.

5.5. Audio Data Formats

The TSCS454xx supports 4 common audio interface formats and programmable clocking that provides broad compatibility with DSPs, Consumer Audio and Video SOCs, FPGAs, handset chip sets, and many other products.

In all modes, depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition. If the converter word length is smaller than the number of clocks per sample in the frame then the DAC will ignore (truncate) the extra bits while the ADC will zero pad the output data. If the converter word length chosen is larger than the number of clocks available per sample in the frame, the ADC data will be truncated to fit the frame and the DAC data will be zero padded.

5.5.1. Left Justified Audio Interface

Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits are then transmitted in order. The LRCLK signal is high when left channel data is present and low when right channel data is present

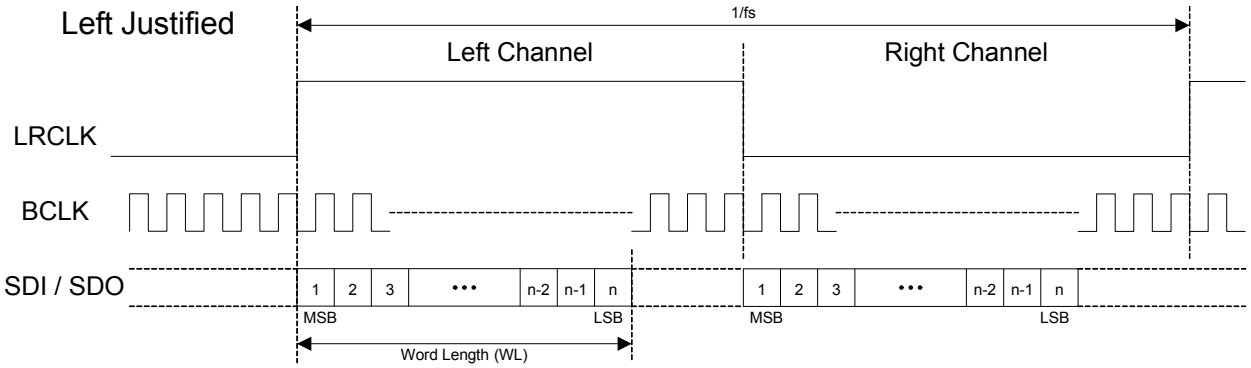


Figure 22. Left Justified Audio Format

5.5.2. Right Justified Audio Interface (assuming n-bit word length)

Right Justified mode, the LSB is available on the last rising edge of BCLK before a LRCLK transition. All other bits are transmitted in order. The LRCLK signal is high when left channel data is present and low when right channel data is present.

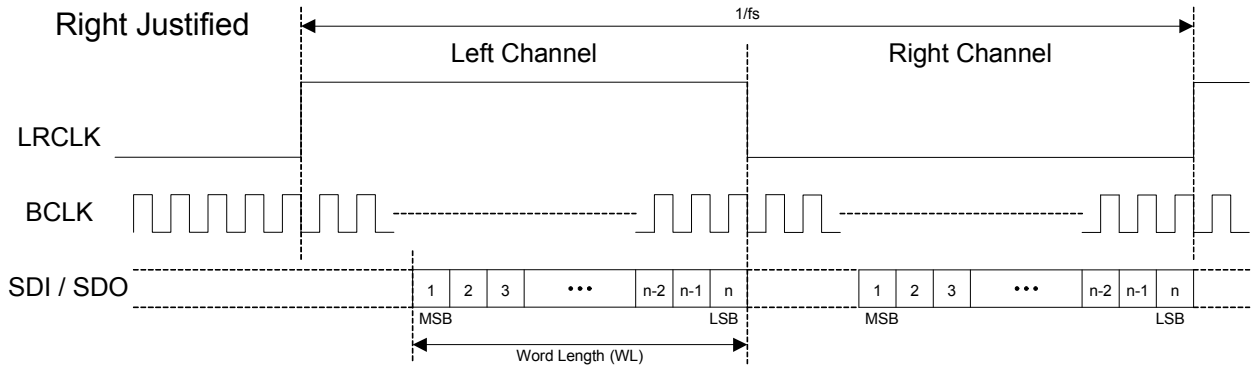


Figure 23. Right Justified Audio Format

5.5.3. I²S Format Audio Interface

I²S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order.

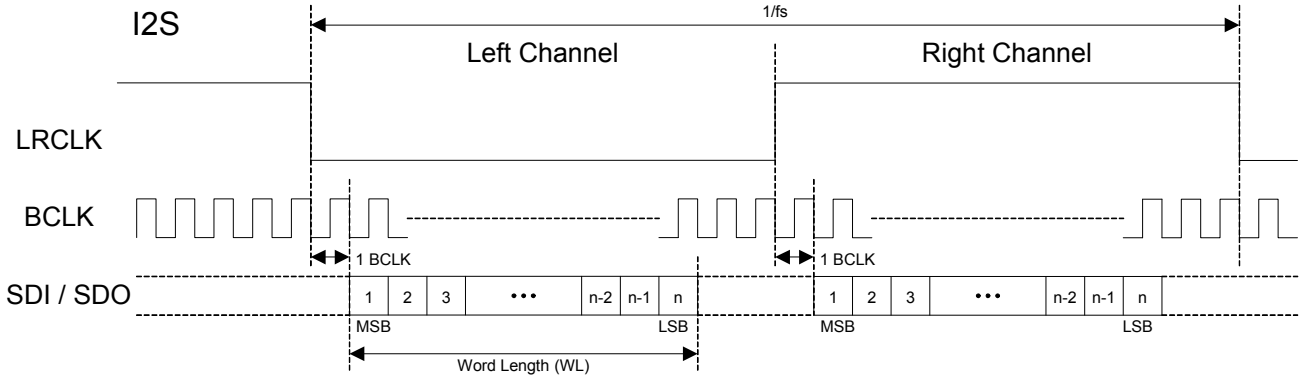


Figure 24. I²S Format AudioFormat

5.5.4. TDM (DSP) Format Audio Interface

TDM Mode is a time-division multiplexed format for transmitting and receiving multiple channels of audio information over a single data connection. When TDM mode is enabled the SDIN1 and SDOUT1 pins are used to input and output TDM data respectively. TDM data is transferred MSB first and the LRCLK/BCLK (frame clock/bit clock) ratio is fixed at two rates; 200Fs and 256Fs. Each digital audio input and output supports up to six,16, 24, or 32 bit time slots, with the audio data left justified within the time slot by padding the unused bits with zeros. Valid audio data word lengths are 16, 20, or 24.(MSB justified within a slot) The defined audio data word length is always the same for both TDM input and output. Short or Long frame syncs are supported. The data lines are tri-stated after the programmed number of data slots have been transmitted or received. The TDM interface operates in either slave or master mode. Data is sampled on the falling edge of the bit clock and transmitted on the rising edge. A control bit selects between a delayed and non-delayed data timing relative to the start of the frame sync. The BCLK invert bit is functional in this mode. The LRCLK is one bit clock long for a Short Frame Sync and one slot wide for a Long Frame Sync.Operating I2S Port 1 in TDM mode does not prevent the other I2S interfaces (Ports 2,3) to be used if four or fewer time slots are enabled.

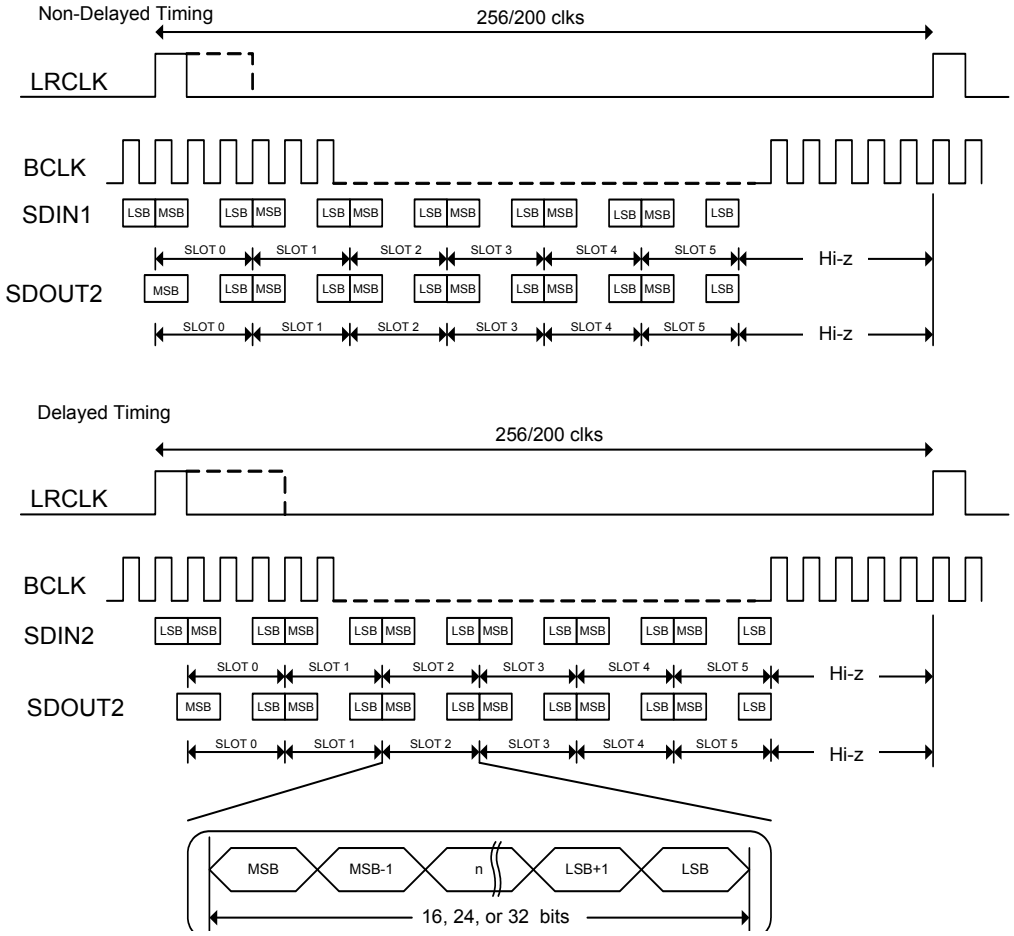


Figure 25. TDM Mode Timing

TDM Slot Mapping:

For TDM mode the audio data is mapped in slots according to the following table. The mapping is fixed. The TDM input data stream, via SDIN1, data slots are routed to the SSS via the same data path as the I2S inputs. Thus the SDIN2 and SDIN3 I2S inputs are not available in TDM mode when the TDM interface is programmed for more than 2 or 4 slots. The TDM output data stream is sourced from the data streams driving the I2S outputs

TDM Input Destination SDIN1		**TDM Output Source SDOUT1**	
SLOT1	DSPIN1	SDOUT1-L	SLOT1
SLOT2	DSPIN2	SDOUT1-R	SLOT2
SLOT3	DSPIN3	SDOUT2-L	SLOT3
SLOT4	DSPIN4	SDOUT2-R	SLOT4
SLOT5	DSPIN5	SDOUT3-L	SLOT5
SLOT6	DSPIN6	SDOUT3-R	SLOT6

Table 111. TDM Slot Mapping

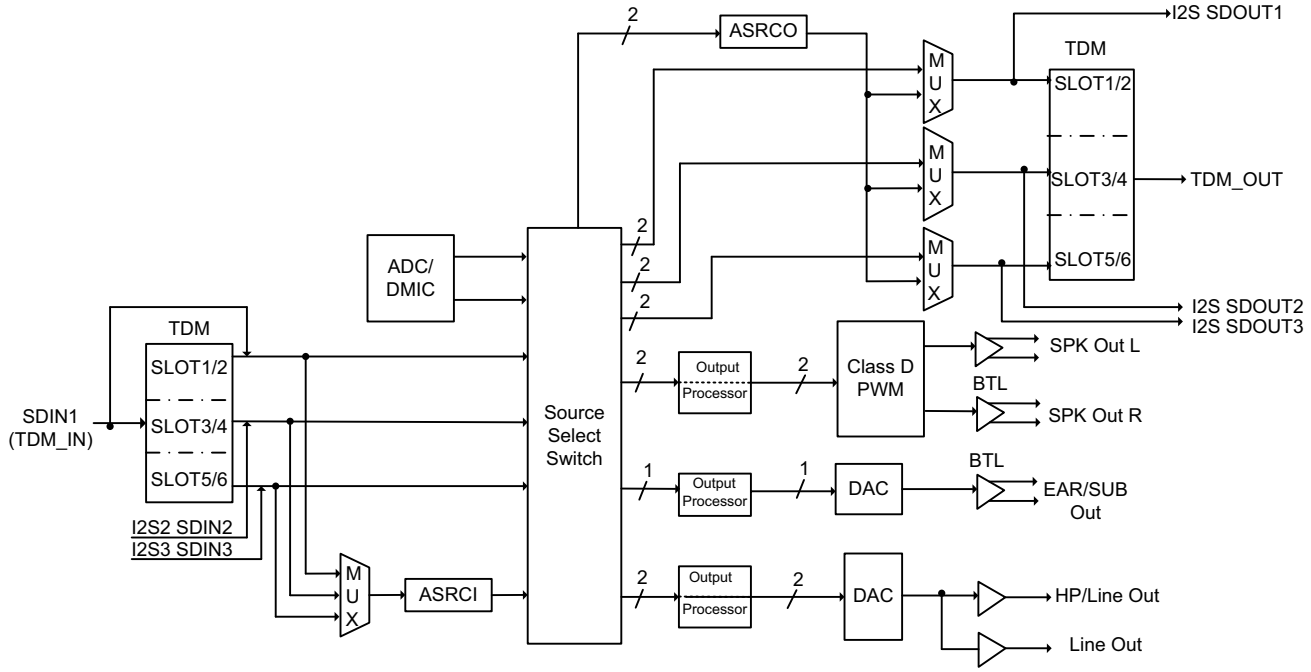


Figure 26. TDM Mode Data Source/Destination Diagram

5.6. Digital Audio Interface Registers

The register bits controlling audio format, word length and master / slave mode are shown below. In Master mode BCLK1:3, LRCK1:3, are outputs; in slave mode, they are inputs.

The I2S interface can be operated in either Master or Slave mode. When operating in Slave mode one input can be redirected towards ASRCI is active and will auto-detect the incoming audio sample rate and convert the audio sample rate to currently defined ASRC output sample rare. rate to the currently defined ASRC output sample rate.The ASRC can power down independently of I2S port.

5.6.1. LRCK and BLCK Mode Control

The TSCS454xx includes three input PCM audio interfaces labeled as TDM, PCM2, and PCM3. The clocking of data through the PCM/TDM interface is controlled by Frame Sync (LRCLK) and Bit Clock (BCLK) signals.

5.6.1.1. I2S Port 1 Control Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 26 - 1Ah I2SP1CTL	7	BCLK1STAT	RW	0	Valid when operating in “Slave Mode” Bit when set indicates a loss of the BCLK has occurred. This bit is sticky and is reset by writing a “1” to this bit. 0 = no loss of BCLK1 has occurred 1 = loss of BCLK1 has occurred
	6	BCLKP1	RW	0	BCLKP1 invert bit (for master and slave modes) 0 = BCLKP1 not inverted 1 = BCLKP1 inverted
	5	PORT1MS	RW	0	Port1 Master/Slave. 0 = Slave 1 = Master
	4	LRCLKP1	RW	0	Right, left and I^2S modes – LRCLKP1 polarity 0 = LRCLKP1 not inverted 1 = LRCLKP1 inverted
	3:2	WL1[1:0]	RW	10	Audio Data Word Length 11 = 32 bits 10 = 24 bits 01 = 20 bits 00 = 16 bits
	1:0	FORMAT1[1:0]	RW	10	Audio Data Format Select 11 = TDM Format 10 = I^2S Format 01 = Left justified 00 = Right justified

Table 112. I2SP1CTL Register

5.6.1.2. I2S Port 2 Control Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 27 - 1Bh I2SP2CTL	**7**	BCLK2STAT	RW	0	Valid when operating in “Slave Mode” Bit when set indicates a loss of the BCLK has occurred. This bit is sticky and is reset by writing a “1” to this bit. 0 = no loss of BCLK2 has occurred 1 = loss of BCLK2 has occurred
	6	BCLKP2	RW	0	BCLKP2 invert bit (for master and slave modes) 0 = BCLKP2 not inverted 1 = BCLKP2 inverted
	5	PORT2MS	RW	0	Port 2 Master/Slave. 0 = Slave 1 = Master
	4	LRCLKP2	RW	0	Right, left and I^2S modes – LRCLK2 polarity 0 = LRCLK2 not inverted 1 = LRCLK2 inverted
	3:2	WL2[1:0]	RW	10	Audio Data Word Length 11 = 32 bits 10 = 24 bits 01 = 20 bits 00 = 16 bits
	1:0	FORMAT2[1:0]	RW	10	Audio Data Format Select 11 =PCM Format 10 = I^2S Format 01 = Left justified 00 = Right justified

Table 113. I2SP2CTL Register

5.6.1.3. I2S Port 3 Control Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 28 - 1C I2SP3CTL	7	BCLK3STAT	RW	0	Valid when operating in “Slave Mode” Bit when set indicates a loss of the BCLK has occurred. This bit is sticky and is reset by writing a “1” to this bit. 0 = no loss of BCLK3 has occurred 1 = loss of BCLK3 has occurred
	6	BCLKP3	RW	0	BCLKP3 invert bit (for master and slave modes) 0 = BCLKP3 not inverted 1 = BCLKP3 inverted
	5	PORT3MS	RW	0	Port 3 Master/Slave. 0 = Slave 1 = Master
	4	LRCLKP3	RW	0	Right, left and I^2S modes – LRCLK3 polarity 0 = LRCLKP3 not inverted 1 = LRCLKP3 inverted
	3:2	WL3[1:0]	RW	10	Audio Data Word Length 11 = 32 bits 10 = 24 bits 01 = 20 bits 00 = 16 bits
	1:0	FORMAT3[1:0]	RW	10	Audio Data Format Select 11 = PCM Format 10 = I^2S Format 01 = Left justified 00 = Right justified

Table 114. I2SP3CTL Register

5.6.1.4. I2S Port 1 Master Sample Rate Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 29 - 1Dh I2S1MRATE	7	I2S1MCLKHALF	RW	0	I2S1 MCLK Divide By 2 0 = Divide by 2 1 = Divide by 1
	6:5	I2S1MCLKDIV[1:0]	RW	0	I2S1 MCLK Divider when I2S1MBR= 11 00 = 125 01 = 128 10 = 136 11 = 192
	4:3	I2S1MBR	RW	10	I2S1 Base Rate 00 = 32KHz 01 = 44.1KHz 10 = 48KHz 11 = MCLK2 mode
	2	RSVD	R	0	Reserved
	1:0	I2S1MBM	RW	10	I2S1 Base Rate Multiplier 00 = 0.25x 01 = 0.50x 10 = 1x 11 = 2x

Table 115. I2S1MRATE Register

5.6.1.5. I2S Port 2 Master Sample Rate Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 30 - 1Eh I2S2MRATE	7	I2S2MCLKHALF	RW	0	I2S2 MCLK Divide By 2 0 = Divide by 2 1 = Divide by 1
	6:5	I2S2MCLKDIV[1:0]	RW	0	I2S2 MCLK Divider when I2S1MBR= 11 00 = 125 01 = 128 10 = 136 11 = 192
	4:2	I2S2MBR	RW	10	I2S2 Base Rate 00 = 32KHz 01 = 44.1KHz 10 = 48KHz 11 = MCLK2 mode
	2	RSVD	R	0	Reserved
	1:0	I2S2MBM	RW	10	I2S2 Base Rate Multiplier 00 = 0.25x 01 = 0.50x 10 = 1x 11 = 2x

Table 116. I2S2MRATE Register

5.6.1.6. I2S Port 3 Master Sample Rate Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 31 - 1Fh I2S3MRATE	7	I2S3MCLKHALF	RW	0	I2S3 MCLK Divide By 2 0 = Divide by 2 1 = Divide by 1
	6:5	I2S3MCLKDIV[1:0]	RW	0	I2S3 MCLK Divider when I2S1MBR= 11 00 = 125 01 = 128 10 = 136 11 = 192
	4:2	I2S3MBR	RW	10	I2S3 Base Rate 00 = 32KHz 01 = 44.1KHz 10 = 48KHz 11 = MCLK2 mode
	2	RSVD	R	0	Reserved
	1:0	I2S3MBM	RW	10	I2S3 Base Rate Multiplier 00 = 0.25x 01 = 0.50x 10 = 1x 11 = 2x

Table 117. I2S3MRATE Register

5.6.1.7. I2S Input Data Mapping Control Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 56 - 38h I2S Input Data Mapping Control	7:6	RSVD	R	0	Reserved
	5:4	I2S3IDCTL[1:0]	RW	0	I2S 3 Input Data Mapping 00 = Normal 01 = Left on both Channels 10 = Right on both Channels 11 = Swap Left and Right Channels
	3:2	I2S2IDCTL[1:0]	RW	0	I2S 2 Input Data Mapping 00 = Normal 01 = Left on both Channels 10 = Right on both Channels 11 = Swap Left and Right Channels
	1:0	I2S1IDCTL[1:0]	RW	0	I2S 1 Input Data Mapping 00 = Normal 01 = Left on both Channels 10 = Right on both Channels 11 = Swap Left and Right Channels

Table 118. I2SIDCTLRegister

5.6.1.8. I2S Output Data Mapping Control Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 57 - 39h I2S Output Data Mapping Control	7:6	RSVD	R	0	Reserved
	5:4	I2S3ODCTL[1:0]	RW	0	I2S 3 Output Data Mapping 00 = Normal 01 = Left on both Channels 10 = Right on both Channels 11 = Swap Left and Right Channels
	3:2	I2S2ODCTL[1:0]	RW	0	I2S 2 Output Data Mapping 00 = Normal 01 = Left on both Channels 10 = Right on both Channels 11 = Swap Left and Right Channels
	1:0	I2S1ODCTL[1:0]	RW	0	I2S 1 Output Data Mapping 00 = Normal 01 = Left on both Channels 10 = Right on both Channels 11 = Swap Left and Right Channels

Table 119. I2SODCTL Register

5.6.2. Bit Clock Mode

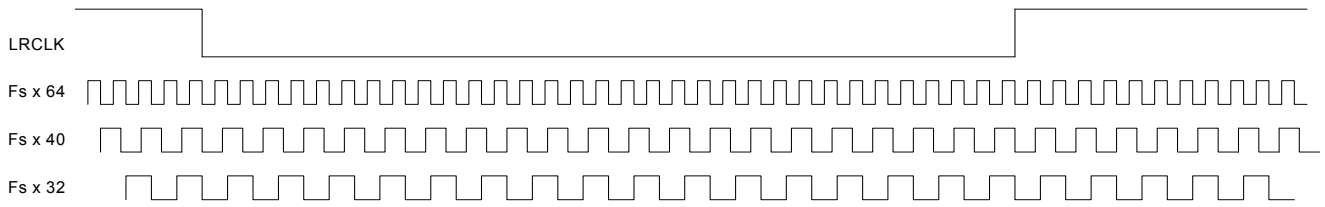
The default master mode bit clock generator for each I2S port automatically produces a bit clock frequency based on the sample rate and word length. When enabled by setting the appropriate BCM bits, the bit clock mode (BCM) function overrides the default master mode bit clock generator to produce the bit clock frequency shown below: Note that selecting a word length of 24-bits in Auto mode generates 64 clocks per frame (64fs).

5.6.2.1. I2S Ports Bit 1-3 Clock Mode Control Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 32 - 20h I2SP1-3CMC I2S Ports 1-3 Bit Clock Mode Control	7:6	RSVD	R	0	Reserved
	5:4	BCMP3[1:0]	RW	0	I2S Port 3 Bit Clock Mode 00 = Auto 01 = 32 x fs 10 = 40 x fs 11 = 64 x fs
	3:2	BCMP2[1:0]	RW	0	I2S Port 2 Bit Clock Mode 00 = Auto 01 = 32 x fs 10 = 40 x fs 11 = 64 x fs
	1:0	BCMP1[1:0]	RW	0	I2S Port 1 BIt Clock Mode 00 = Auto 01 = 32 x fs 10 = 40 x fs 11 = 64 x fs

Table 120. I2S Ports 1-3 Clock Mode Control Register

The BCM mode bit clock generator produces 16, 20, or 32 bit cycles per sample.



Note: The clock cycles are evenly distributed throughout the frame (true multiple of LRCLK not a gated clock.)

5.6.3. SCLK Underflow and Overflow

When the serial audio interface is configured in stereo mode, an SCLK overflow condition occurs when there are more than 32 SCLK cycles between consecutive edges of the LRCLK. Similarly, an SCLK underflow condition occurs when there are less than 32 SCLK cycles between consecutive edges of the LRCLK. In an SCLK overflow condition, the extra SCLK cycles are ignored. In an SCLK underflow condition, all remaining non-loaded data bits are filled with zeros.

5.6.4. Audio Interface Output Tri-state Control

TRI is used to tri-state the SDOUT3:1, LRCLK3:1, BCLK3:1 pins. The Tri-stated pins are pulled low with an internal I2Spull-down resistor unless that resistor is disabled.

5.6.5. I2S Pin Control 0 Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 34 - 22h I2SPINC0	7	SDO3TRI	RW	0	Tri-state pin. 0 = SDOUT3 is an output 1 = SDOUT3 is high impedance
	6	SDO2TRI	RW	0	Tri-state pin. 0 = SDOUT2 is an output 1 = SDOUT2 is high impedance
	5	SDO1TRI	RW	0	Tri-state pin. 0 = SDOUT1 is an output 1 = SDOUT1 is high impedance
	4:3	RSVD	R	0	Reserved
	2	PCM3TRI	RW	0	Tri-state pin. 0 = LRCK3, BCLK3 are inputs (slave mode) or outputs (master mode) 1 = LRCK3, BCLK3 are high impedance
	1	PCM2TRI	RW	0	Tri-state pin. 0 = LRCK2, BCLK2 are inputs (slave mode) or outputs (master mode) 1 = LRCK2, BCLK2 are high impedance
	0	PCM1TRI	RW	0	Tri-state pin. 0 = LRCK1, BCLK1 are inputs (slave mode) or outputs (master mode) 1 = LRCK1, BCLK1 are high impedance

Table 121. I2SPINC0 Register

5.6.6. Pin Control 1 Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 35 - 23h I2SPINC1	7:3	RSVD	R	0	Reserved
	2	SDO3PDD	RW	0	SDOUT3 Pull-Down Disable 0 = Pull-Down active when tri-stated 1 = Pull-Down always disabled
	1	SDO2PDD	RW	0	SDOUT2 Pull-Down Disable 0 = Pull-Down active when tri-stated 1 = Pull-Down always disabled
	0	SDO1PDD	RW	0	SDOUT1 Pull-Down Disable 0 = Pull-Down active when tri-stated 1 = Pull-Down always disabled

Table 122. I2SPINC1 Register

5.6.7. I2S Pin Control 2 Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 36 - 24h I2SPINC2	7:6	RSVD	R	0	Reserved
	5	LR3PDD	RW	0	LRCLK3 Pull-Down Disable 0 = Pull-Down active when configured as input 1 = Pull-Down always disabled
	4	BC3PDD	RW	0	BCLK3 Pull-Down Disable 0 = Pull-Down active when configured as input 1 = Pull-Down always disabled
	3	LR2PDD	RW	0	LRCLK2 Pull-Down Disable 0 = Pull-Down active when configured as input 1 = Pull-Down always disabled
	2	BC2PDD	RW	0	BCLK2 Pull-Down Disable 0 = Pull-Down active when configured as input 1 = Pull-Down always disabled
	1	LR1PDD	RW	0	LRCLK1 Pull-Down Disable 0 = Pull-Down active when configured as input 1 = Pull-Down always disabled
	0	BC1PDD	RW	0	BCLK1 Pull-Down Disable 0 = Pull-Down active when configured as input 1 = Pull-Down always disabled

Table 123. I2SPINC2 Register

5.6.8. TDM Control 0 Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 45 - 2Dh TDMCTL0	7:3	RSVD	R	0	Reserved
	2	TDMMODE	RW	0	TDM Mode 0 = 200 bits per frame 1 = 256 bits per frame
	1	SLSYNC	RW	0	Short-Long Frame Sync 0 = short frame sync, one clock wide 1 = long frame sync, half of frame wide
	0	BDELAY	RW	0	Bit Clock Delay relative to start of data in TDM mode 0 = bit clock not delayed relative to start of data 1 = bit clock delayed by one clock relative to start of data

Table 124. TDMCTL0 Register

5.6.9. TDM Control 1 Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 46 - 2Eh TDMCTL1	7	RSVD	R	0	Reserved
	6:5	TDMSO[1:0]	RW	01	Number of slots per TDM Output Frame 00 = 2 01 = 4 10 = 6 11 = Reserved
	4:3	TDMDSS	RW	0	TDM Data Slot Width 00 = 24 bit 01 = 16 bit 10 = 32 bit 11 = reserved
	2	RSVD	R	0	Reserved
	1:0	TDMSI[1:0]	RW	01	Number of slots per TDM Output Frame 00 = 2 01 = 4 10 = 6 11 = Reserved

Table 125. TDMCTL1 Register

5.7. ASRC's

The three digital I2S audio input ports can be muxed to one Asynchronous Sample Rate Converters (ASRC) to converter the incoming audio data streams from whatever sample rate they are running at to an internal known sample rate. The three digital I2S audio output ports can mux ASRC output which converts the internal audio data streams from a known sample rate to another sample rate. ASRC's can also provide attenuation of incoming audio source jitter which may improve the audio performance of the design.

5.7.1. Supported Input Sample Rates

The ASRC must support input sample rates from 8KHz to 96KHz.

5.7.1.1. Autorate Detection

Standard Audio Sample Input Rates		
8KHz	11.025KHz	12KHz
16KHz	22.050KHz	24KHz
32KHz	44.100KHz	48KHz
64KHz	88.2KHz	96KHz

Table 126. Standard Audio Sample Rates

The incoming audio sample rate is unknown when the audio interface is operating in slave mode and therefore must be estimated. Typically the audio frame period (sample rate) is determined by counting the number of clock pulses that occur during the frame. No programming should be required to support the range of input sample rates.

5.7.1.2. Master/Slave Operation

The ASRC can operates either in Master or Slave mode. In Master mode the audio sample rate and signal timing on the input side is defined by a set of registers based on internal clocks. In Slave mode the ASRC auto detects the incoming audio sample rate and adjusts the processing to match the defined ASRC output audio sample rate. In Slave mode operation Autorate detection of sample rate is required.

5.7.2. ASRC Output Rates

The ASRC's convert the incoming audio sample rate to one of two sample rates as specified by the System Clock Control and internal Sample Rate Control Register. See "Figure 34 shows the simplified block diagram. The TSCS454xx utilizes internal PLLs to generate the PLL clocks at 112.896 MHz (22.5792MHz *5) and122.880 MHz (24.576 *5). Intermediate clocks (61.44MHz, 40.96MHz, 56.448MHz) are then generated which are then used to generate the audio sample rates. There is one internal clock rate that can be specified to operate at 11.025KHz, 12 KHz, 22.050KHz, 24KHz, 44.1KHz, 48KHz,88.2KHz, and 96KHz. When changing sample rates a delay of up to 5mS may be needed for the part to properly lock PLLs, flush filters, etc." on page 122.

5.7.2.1. ASRC Bypass

The ASRC's may be bypassed. When the ASRC is bypassed it is put into a powered down state to save power. The ASRC's are bypassed via the ASRCx Bypass Bit when the incoming I2S rate is synchronized to the currently defined Internal ICLK audio rate. In this case the input clock (MCLK) to the TSCS454xx would need to be driven by the external master audio source and the timing of the I2S interface synchronized to this clock. The ASRC volume control function is Active in bypass mode

Note: this may require that the internal clock generation must support an external sync mode so that the internal clock timing of the TSCS454xx can be synchronized to an external I2S source when the ASRC's are bypassed.

5.7.3. ASRC Control

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 40 - 28h ASRC	7	ASRCOBW	RW	0	Output ASRC High-Bandwidth Support: 0 = Audio content is assumed to be 20kHz or less (filtering is limited for higher rates, to save cycles) 1 = Audio content can be as high as allowed by the sample rate
	6	ASRCIBW	RW	0	Input ASRC High-Bandwidth Support: 0 = Audio content is assumed to be 20kHz or less (filtering is limited for higher rates, to save cycles) 1 = Audio content can be as high as allowed by the sample rate
	5	ASRCOB	RW	0	Output ASRC1 Bypass 0 = Output ASRC Active 1 = Output ASRC Bypassed
	4	ASRCIB	RW	0	Input ASRC1 Bypass 0 = Input ASRC Active 1 = Input ASRC Bypassed
	3	ASRCOL	R	0	Output ASRC1 Lock Status 0 = Output ASRC Unlocked 1 = Output ASRC Locked
	2	ASRCIL	R	0	Input ASRC1 Lock Status 0 = Input ASRC Unlocked 1 = Input ASRC Locked
	1:0	RSVD	R	0	Reserved

Table 127. ASRC Register

6. HOST CONTROL, I²C, 2-WIRE CONTROL INTERFACE

The TSCS454xx device includes a 2-Wire I²C compatible interface for communicating with an external controller. This interface supports communication to external micro-controller or other I²C compatible peripheral chips. The I²C interface supports normal and fast mode operation. The TSCS454xx incorporates a Paged accessing scheme.

The device address can be set using hardware pin strapping via the GPIO0, GPIO1 pins or via a register. When using the hardware pin strapping method the Mixer device address is always offset from the register device address by + 0x2 The default I2C device address is 0xD2 for the registers. The TSCS454xx registers are accessed through a unique serial control interface using a multi-word protocol comprised of 8-bit words. The first 8 bits provide the device address and Read/Write flag. In a write cycle, the next 8 bits provide the register address; all Subsequent words contain the data, corresponding to the 8 bits in each control register.

The control interface operates as a slave device when communicating to an external controller.

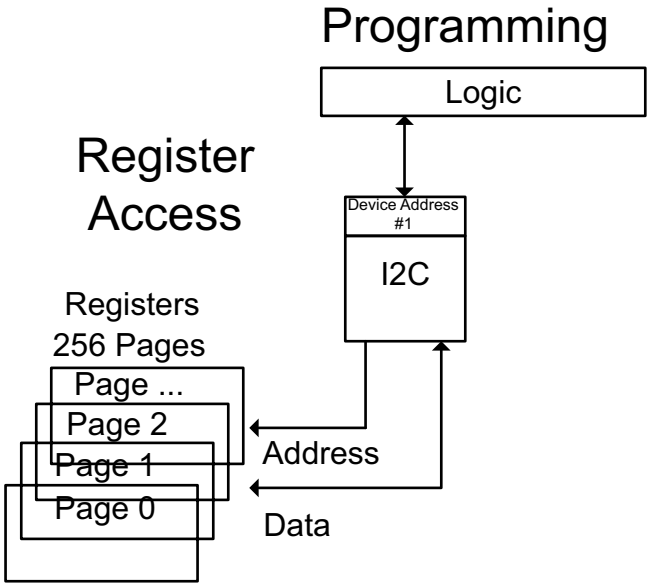


Figure 27. I2C Register-Mixer Access Diagram

6.1. I2C Device Addressing

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	0	1	A2	A1	1	R/W

Table 128. I2C Device Address Byte Format

The address byte format is shown in Table 128. The TSCS454xx slave addresses are set with the GPIO0/ADDR1, GPIO1/ADDR2 pins. The address resides in the first seven bits of the I2C write. The LSB of this byte sets either a read or write operation. Logic Level 1 corresponds to a read operation, and Logic Level 0 corresponds to a write operation. Bits 3 and 2 of the address are set by tying the GPIO1, GPIO0 pins of the TSCS454xx to Logic Level 0 or Logic Level 1.The state of these pins is latched on power-up via an internal power-valid signal. Once the device address has been configured, The SEL Bit 1 is generated by the host controller's I2C address and decoded by the TSCS454xx to access the Register address space. The device address mapping is shown below in Table 129

GPIO1	GPIO0	I2C Device Address
A2	**A1**	**SEL= 1**
0	0	0xD2
0	1	0xD6
1	0	0xDA
1	1	0xDE

Table 129. I2C Address Via Pin Strapping

The TSCS454xx default I2C slave address can be configured via the GPIO0/ADDR1, and GPIO1/ADDR2 pins but it may be necessary sometimes to use a different address. The TSCS454xx has a device address register for this purpose. The device address register can be updated by an external micro-controller. The device address can be uniquely specified for the Register address spaces. It should be noted that the TSCS454xx must be accessed via one of the default I2C device addresses as defined by the GPIO0/ADDR1, GPIO1ADDR2 pins in order for the device address to be changed.

Device Address Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 6 -6h DEVADD0	7:1	ADDR[7:1]	RW	See note	7-bit slave address for registers
	0	I2C_ADDRLK	RW	0	Locks I2C address if set to 1. Part must be powered down to reset this bit

Table 130. DEVADD0 Register

Note: The default setting is determined by the GPIO0/ADDR1 and GPIO1/ADDR2 pins on power-up. The state of the pins determines the default value for bits 3:2 of this register.

Device Identification Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 8 - 8h DEVID	7:0	DID[:7:0]	R	01000xxxb	8-bit device identification number. The least significant three bits reflect the state of the Bond-Out pins.

Table 131. DEVID Register

Device Revision Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 9 - 9h REVID	7:4	MAJ_REV[3:0]	R	0001	4-bit major revision number (all layer) currently = 1 (1st release) MMMM.mmmm currently = 1.0
	3:0	MNR_REV[3:0]	R	0000	4-bit minor revision number (metal revision) currently = 0 (no revisions-initial release)

Table 132. REVID Register

6.2. Page Register Write Cycle

The controller indicates the start of data transfer with a high to low transition on SDA while SCL remains high, signalling that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the TSCS454xx and the R/W bit is '0', indicating a write, then the TSCS454xx responds by pulling SDA low on the next clock pulse (ACK); otherwise, the TSCS454xx returns to the idle condition to wait for a new start condition and valid address. Once the TSCS454xx has acknowledged a correct device address, the controller sends the TSCS454xx register address. The TSCS454xx acknowledges the register address by pulling SDA low for one clock pulse (ACK). The controller then sends a byte of data (B7 to B0), and the TSCS454xx acknowledges again by pulling SDA low.

When there is a low to high transition on SDA while SCL is high, the transfer is complete. After receiving a complete address and data sequence the TSCS454xx returns to the idle state. If a start or stop condition is detected out of sequence, the device returns to the idle condition.

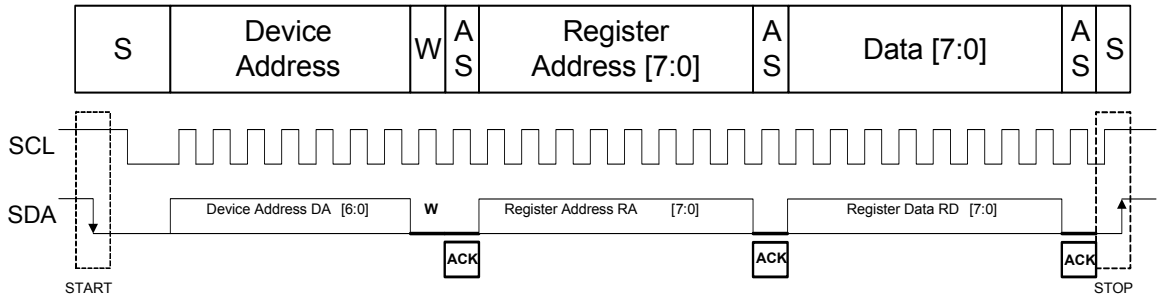


Figure 28. Page Register Write -2 Wire Serial Control Interface

6.3. Page Register Burst Write Cycle

The controller may write more than one register within a single write cycle. To write additional registers, the controller will not generate a stop or start (repeated start) command after receiving the acknowledge for the second byte of information (register address and data). Instead the controller will continue to send bytes of data. After each byte of data is received, the register address is incremented.

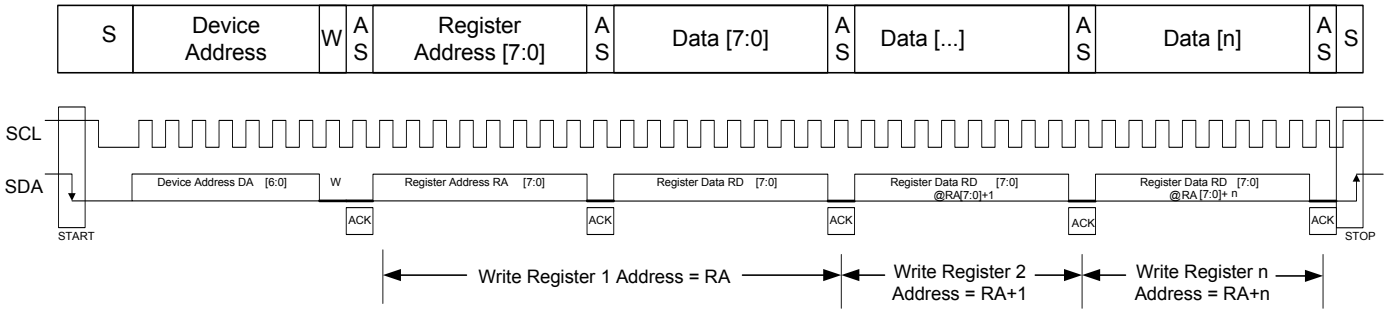


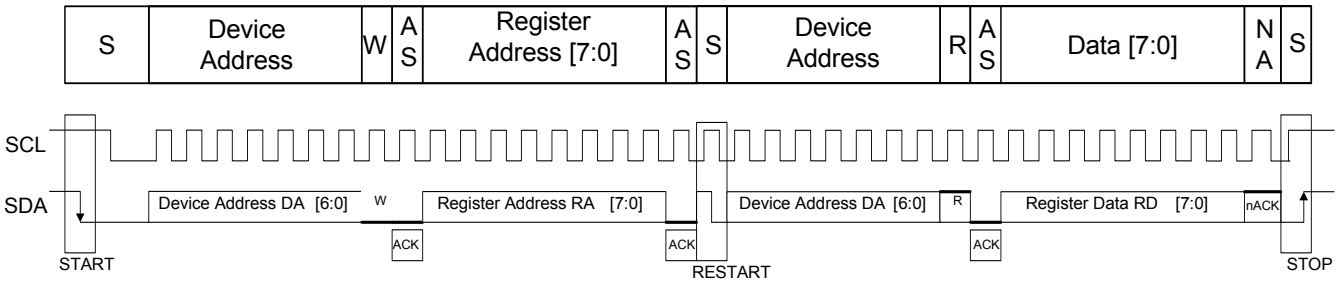
Figure 29. Page Register Burst Write Cycle

6.4. Page Register Read Cycle

The controller indicates the start of data transfer with a high to low transition on SDA while SCL remains high, signalling that a device address and data will follow. If the device address received matches the address of the TSCS454xx and the R/W bit is ‘0’, indicating a write, then the TSCS454xx responds by pulling SDA low on the next clock pulse (ACK); otherwise, the TSCS454xx returns to the idle condition to wait for a new start condition and valid address.

Once the TSCS454xx has acknowledged a correct address, the controller sends a restart command (high to low transition on SDA while SCL remains high). The controller then re-sends the devices address with the R/W bit set to ‘1’ to indicate a read cycle.The TSCS454xx acknowledges by pulling SDA low for one clock pulse. The controller then receives a byte of register data (B7 to B0).

For a single byte transfer, the host controller will not acknowledge (high on data line) the data byte and generate a low to high transition on SDA while SCL is high, completing the transfer. If a start or stop condition is detected out of sequence, the device returns to the idle condition.

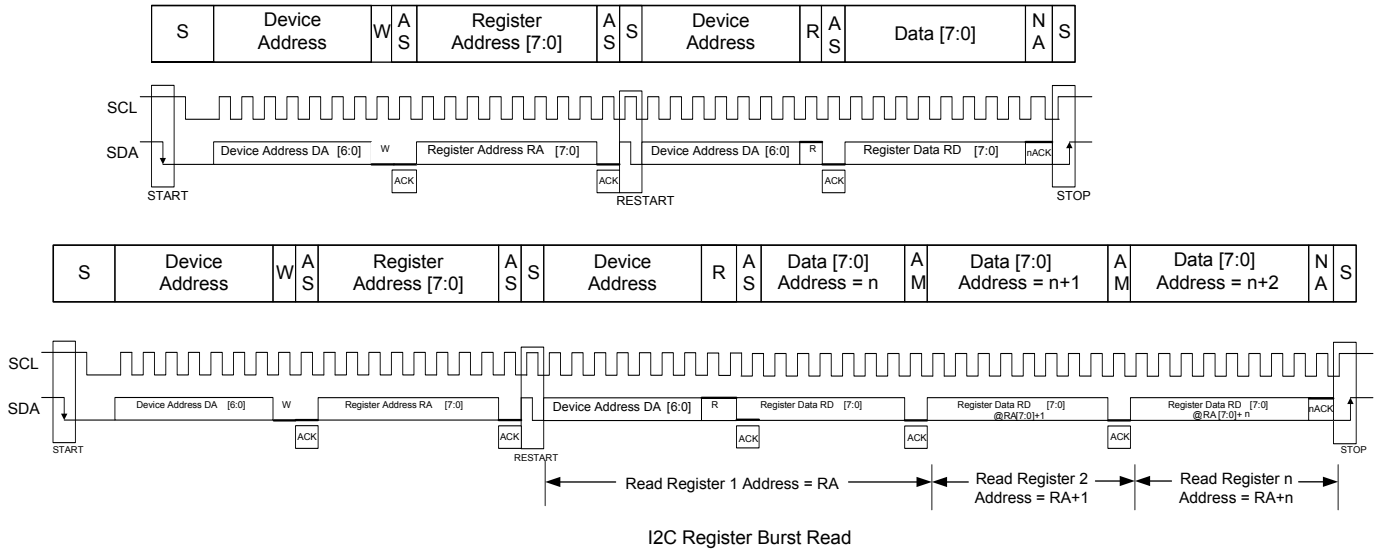


I2C Register Read

Figure 30. Page Register Single Byte Read Cycle

6.5. Page Register Burst Read Cycle

The controller may read more than one register within a single read cycle. To read additional registers, the controller will not generate a stop or start (repeated start) command after sending the acknowledge for the byte of data. Instead the controller will continue to provide clocks and acknowledge after each byte of received data. The TSCS454xx will automatically increment the internal register address after each register has had its data successfully read (ACK from host) but will not increment the register address if the data is not received correctly by the host (nACK from host) or if the bus cycle is terminated unexpectedly (however the EQ/Filter address will be incremented even if the register address is not incremented when performing EQ/Filter RAM reads). By automatically incrementing the internal register address after each byte is read, all the internal registers of the TSCS454xx may be read in a single read cycle.



I2C Register Burst Read

Figure 31. Page Register Burst Multi-byte) Read Cycle

6.6. GPIO's

Four GPIO's are available on the GPIO3-GPIO0 pins. These GPIO pins are accessed via register bits.The GPIO1-GPIO0 pins are also used to specify the I2C device address on power-up. The general-purpose input/output (GPIO) pins can be used as either inputs or outputs. These pins are readable and can be set or read through the control interface. These pins are useful for interfacing to external hardware.

6.6.1. GPIO Usage Summary

GPIO Pin	Function 1	Function 2	Pull-Up Pull-Down
GPIO0	I2C address 0	GPIO0 Register Bit	Pull-Down
GPIO1	I2C Address 1	GPIO1 Register Bit	Pull-Down
GPIO2	GPIO2 Register Bit	RSVD	Pull-Up
GPIO3	GPIO3 Register Bit	RSVD	Pull-Up

Table 133. GPIO Pin Usage Summary

6.6.2. GPIO Control Registers

6.6.2.1. GPIO Control 0 Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 25-25h GPIOCTL0	7	GPIO3INTP	RW	0	GPIO3 Interrupt Polarity 0 = generate interrupt on high going edge 1 = generate interrupt on low going edge
	6	GPIO2INTP	RW	0	GPIO2 Interrupt Polarity 0 = generate interrupt on high going edge 1 = generate interrupt on low going edge
	5	GPIO3CFG	RW	0	GPIO3 Configuration 0 = GPIO3 Configured as Input/Output 1 = GPIO3 Configured as Interrupt
	4	GPIO2CFG	RW	0	GPIO2 Configuration 0 = GPIO2 Configured as Input/Output 1 = GPIO2 Configured as Interrupt
	3	GPIO3IO	RW	0	GPIO3 Input/Output 0 = GPIO3 configured as input 1 = GPIO3 configured as output
	2	GPIO2IO	RW	0	GPIO2 Input/Output 0 = GPIO2 configured as input 1 = GPIO2 configured as output
	1	GPIO1IO	RW	0	GPIO1 Input/Output 0 = GPIO1 configured as input 1 = GPIO1 configured as output
	0	GPIO0IO	RW	0	GPIO0 Input/Output 0 = GPIO0 configured as input 1 = GPIO0 configured as output

Table 0-1.

Table 134. GPIOCTL0 Register

6.6.2.2. GPIO Control 1 Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 26-26h GPIOCTL1	7	GPIO3	RW	0	Register bit that is driven onto the GPIO3 pin
	6	GPIO2	RW	0	Register bit that is driven onto the GPIO2 pin
	5	GPIO1	RW	0	Register bit that is driven onto the GPIO1 pin
	4	GPIO0	RW	0	Register bit that is driven onto the GPIO0 pin
	3	GPIO3RD	R	0	Reports the state of the GPIO3 pin
	2	GPIO2RD	R	0	Reports the state of the GPIO2 pin
	1	GPIO1RD	R	0	Reports the state of the GPIO1 pin
	0	GPIO0RD	R	0	Reports the state of the GPIO0 pin

Table 135. GPIOCTL1 Register

6.7. Register Reset

The TSCS454xx registers may be reset to their default values using the reset register. Writing a special, non-zero value to this register causes all other registers to assume their default states. Device status bits will not necessarily change their values depending on the state of the device.

Reset Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 1-01h RESET	7:0	Reset[7:0]	RW	00h	Reset register Writing a value of 85h will cause registers to assume their default values. Reading this register returns 00h

Table 136. RESET Register

6.8. Interrupts

6.8.1 nINT/nTEST - Interrupt/Test Pin

The nINT interrupt pin is an open drain, active low, output that indicates a number of error conditions or chip states. The BTNDET, HDSINT, HDPNINT, EEND and CKSUM status bits are cleared by either issuing a RESET or by writing any value to the Interrupt Status Register.

When the nINT/nTEST is held low when the nRESET pin transitions high the device will enter TESTMODE operation.

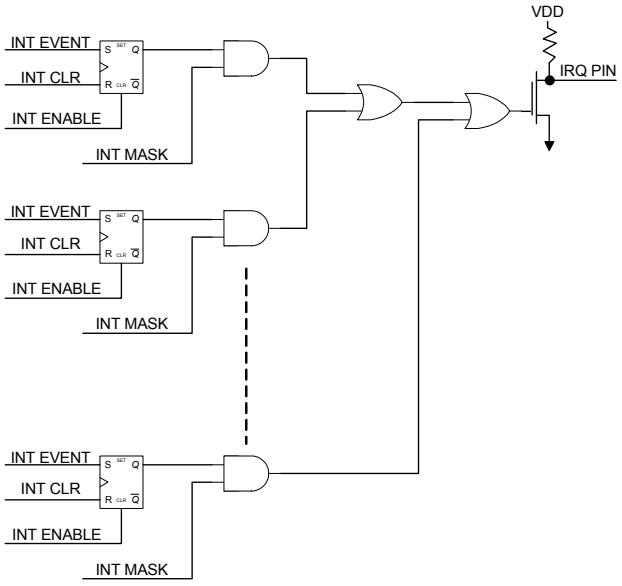
6.8.2 Interrupt Logic

The interrupt generation logic consists of a interrupt enable/disable control, an interrupt mask control, and a interrupt status/clear mechanism.

Each interrupt may be “Enabled/disabled” by the corresponding interrupt enable control bit located in the Interrupt Enable Register.

Each interrupt can be “Masked” from generating an interrupt on the IRQ pin by the corresponding interrupt mask bit located in the Interrupt Mask Register.

Each interrupt can be “Cleared” bit writing a “one” to the corresponding interrupt status bit located in the Interrupt Status Register.



6.8.3 Interrupt Sources

6.8.3.1. Thermal Protection Interrupt

An interrupt will be generated, if enabled, whenever the TSCS42xx device detects an over temperature condition. The THERMTS register can then be read to determine the thermal status.

6.8.3.2. Headphone/Headset Detection Interrupts

An interrupt can be generated by due to headphone and headset detection, or a headset button push

6.8.4. Interrupt Control Registers

6.8.4.1. Interrupt Enable Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 2-2h IRQEN	7	RSVD	R	0	Reserved
	6	THRMINTEN	RW	0	Thermal (Over Temp) Detect Interrupt Enable 0 = Interrupt Disabled 1 = Interrupt Enabled
	5	HBPINTEN	RW	0	Headset Button Push Detect Interrupt Enable
	4	HSDINTEN	RW	0	Headset Detected Interrupt Enable 0 = Interrupt Disabled 1 = Interrupt Enabled
	3	HPDINTEN	RW	0	Headphone Detected Interrupt Enable 0 = Interrupt Disabled 1 = Interrupt Enabled
	2	RSVD	R	0	Reserved
	1	GPIO3INTEN	RW	0	GPIO 3 Interrupt Enable 0 = Interrupt Disabled 1 = Interrupt Enabled
	1	GPIO2INTEN	RW	0	GPIO 2 Interrupt Enable 0 = Interrupt Disabled 1 = Interrupt Enabled

Table 137. IRQEN Register

6.8.4.2. Interrupt Mask Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 3-3h IRQMASK	7	RSVD	R	0	Reserved
	6	THRMIM	RW	0	Thermal (Over Temp) Detect Interrupt Mask 0 = Interrupt Disabled 1 = Interrupt Enabled
	5	HBPIM	RW	0	Button Push Detect Interrupt Mask
	4	HDDIM	RW	0	Headset Detection Interrupt Mask 0 = Interrupt Disabled 1 = Interrupt Enabled
	3	HDPIM	RW	0	Headphone Detection Interrupt Mask 0 = Interrupt Disabled 1 = Interrupt Enabled
	2	RSVD	R	0	Reserved
	1	GPIO3M	RW	0	GPIO 3 Interrupt Mask 0 = Interrupt Disabled 1 = Interrupt Enabled
	0	GPIO2M	RW	0	GPIO 2 Interrupt Mask 0 = Interrupt Disabled 1 = Interrupt Enabled

Table 138. IRQMASK Register

6.8.4.3. Interrupt Status Register

All interrupts are cleared by writing a one to the interrupt specific bits in this register.

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 4-4h IRQSTAT	7	RSVD	R	1	Reserved
	6	THRMIS	RW	0	Over Temperature Detect Interrupt Status
	5	HBPINT	RW	0	Headset Button Push Detect Interrupt Status. This is an “OR” of the Long and Short button push detect logic.
	4	HSDINT	RW	0	Headset Detected Interrupt Status
	3	HDPINT	RW	0	Headphone Detected Interrupt Status
	2	RSVD	R	0	Reserved
	1	GPIO3INT	RW	0	GPIO 3 Interrupt Status
	0	GPIO2INT	RW	0	GPIO 2 Interrupt Status

Table 139. IRQSTAT Register

6.9. Reset Pin

The Reset pin resets all internal registers to their default states and put the TSCS454xx into it’s lowest power state. While the Reset pin is held active the TSCS454xx should consume zero power.

7. CLOCK GENERATION

The TSCS454xx uses two PLL's to generate two high frequency reference clocks. The clock frequencies of each reference clock are based on multiples of 44.1KHz and 48KHz sample rates.The clock source for the PLL's can be the XTAL input, MCLK1 input via the XTAL_IN pin, the MCLK2 pin, or one of the I2S interface BCLK inputs. Each PLL can be independently powered down if the audio sample rates generated by that particular PLL are not required.

7.1. On-Chip PLLs

The TSCS454xx generates two high-quality, high-frequency clocks122.880MHz and 112.896MHz. The PLL's support a wide range of input clock frequencies. Some typical frequencies are 19.2Mhz, 22MHz, 22.5792MHz, 24MHz, 24.576 MHz, 27MHz, and 36MHz. It should be noted that some input clock frequencies may not result in being able to generate the 122.880MHz and 112.896Mhz clocks exactly resulting in an error in the audio sample rate.

Audio Clocks - Each PLL generates one of two clock frequencies based on two audio sample rates.

122.880 MHz (2560 x 48 KHz)
112.896 MHz (2560 x 44.1 KHz)

It is important that the crystal oscillator and needed PLLs remain on until all audio functions, including jack detection, are disabled.

For supporting System Master Clock (MCLK OUT) generation a 22.5792MHz,24.576MHz, or the PLL2 output may be selected to be output on the MCLK2 pin. This low jitter high frequency clock also can be used to drive external audio sources. The MCLK2 output frequency is limited to 50MHz. The MCLK2 pin can also be configured to input a high frequency clock from an external oscillator or other external clock source.

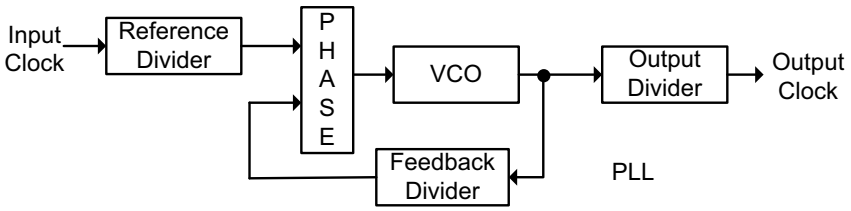


Figure 32. System Clock Diagram

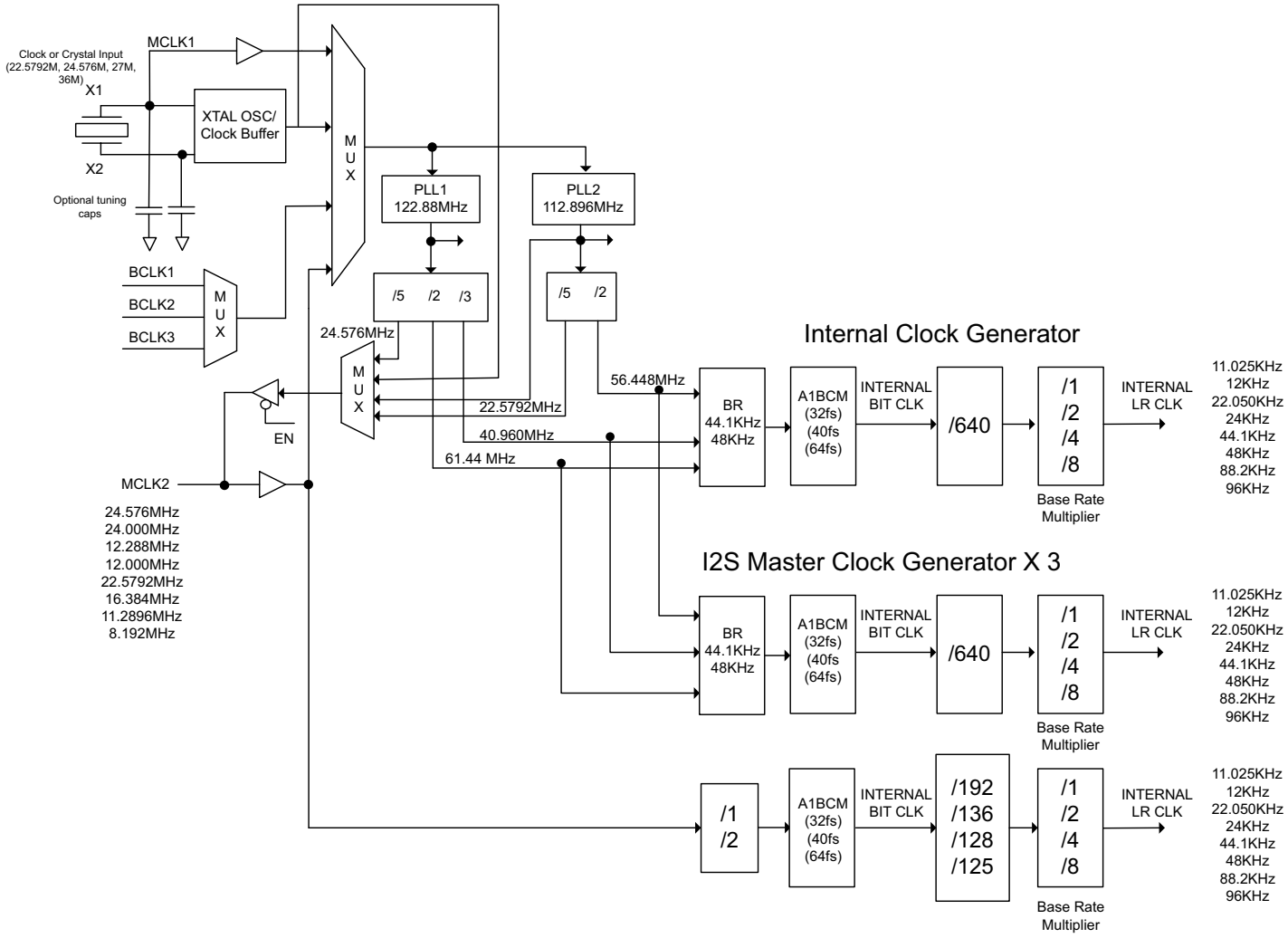


Figure 33. Clock Generation Diagram

7.2. System Clock Generation

The TSCS454xx supports an internal clock and audio sample rate that is selectable between 11.025KHz, 12 KHz, 22.050KHz, 24KHz, 44.1KHz, 48KHz, 88.2KHz, and 96KHz. ASRC's are used to sample rate convert the external audio source timing to the specified internal rate. Three bi-directional stereo I2S interfaces are available. Each I2S interface may operate as a slave or as a timing master. Separate input and output ASRC's are used. In Slave mode each ASRC will rate detect the incoming audio sample rate and adjust the ASRC automatically. In Master mode an internal timing generator is used to specify the audio sample rate. The sample rate specified in Master mode is independent from the internal clock rate.and the specified range is 8KHz to 96KHz. A variety of sample rates based on 44.1K, 48K and 32K are supported. A highly programmable PLL enables just about any input frequency to be used.

7.2.1 PLL Dividers

The chosen input frequency is multiplied up by the PLL's to generate the required output frequencies; 122.88MHz and 112.896MHz. It should be noted that it may not always be possible to generate the required output frequencies with zero error. Some values for the PLL dividers relative a specific input frequency are shown in the table below.

	Output Frequency									
	PLL1 - 122.88MHz					PLL2 - 112.896MHz				
Input Frequency (MHz)	Reference Divider	Feedback Divider	Output Divider	Freq Error ppm	VCO (MHz) Freq	Reference Divider	Feedback Divider	Output Divider	Freq Error ppm	VCO Freq (MHz)
1.4112	N/A	N/A	N/A	N/A	N/A	4	960	3	0	338.688
1.536	2	480	3	0	368.64	2	441	3	0	338.688
2.8224	N/A	N/A	N/A	N/A	N/A	3	360	3	0	338.688
3.072	7	840	3	0	368.64	7	1029	4	0	451.584
5.6448	N/A	N/A	N/A	N/A	N/A	14	840	3	0	338.688
6.144	5	300	3	0	368.64	8	441	3	0	338.688
12	25	768	3	0	368.64	25	1176	5	0	564.48
19.2	20	384	3	0	368.64	25	441	3	0	338.688
22	55	1536	5	0	614.4	38	585	3	-11.887	338.684
22.5792	49	800	3	0	368.64	29	435	3	0	338.688
24	25	384	3	0	368.64	25	588	5	0	564.48
24.576	29	435	3	0	368.64	24	441	4	0	451.584
25	55	811	3	-9.864	368.64	42	569	3	7.3111	338.688
27	45	1024	5	0	614.4	125	1568	3	0	338.688 PD= 210Khz
36	25	256	2	0	368.64	125	1176	3	0	338.688 PD= 280Khz

Table 140. Output Frequency

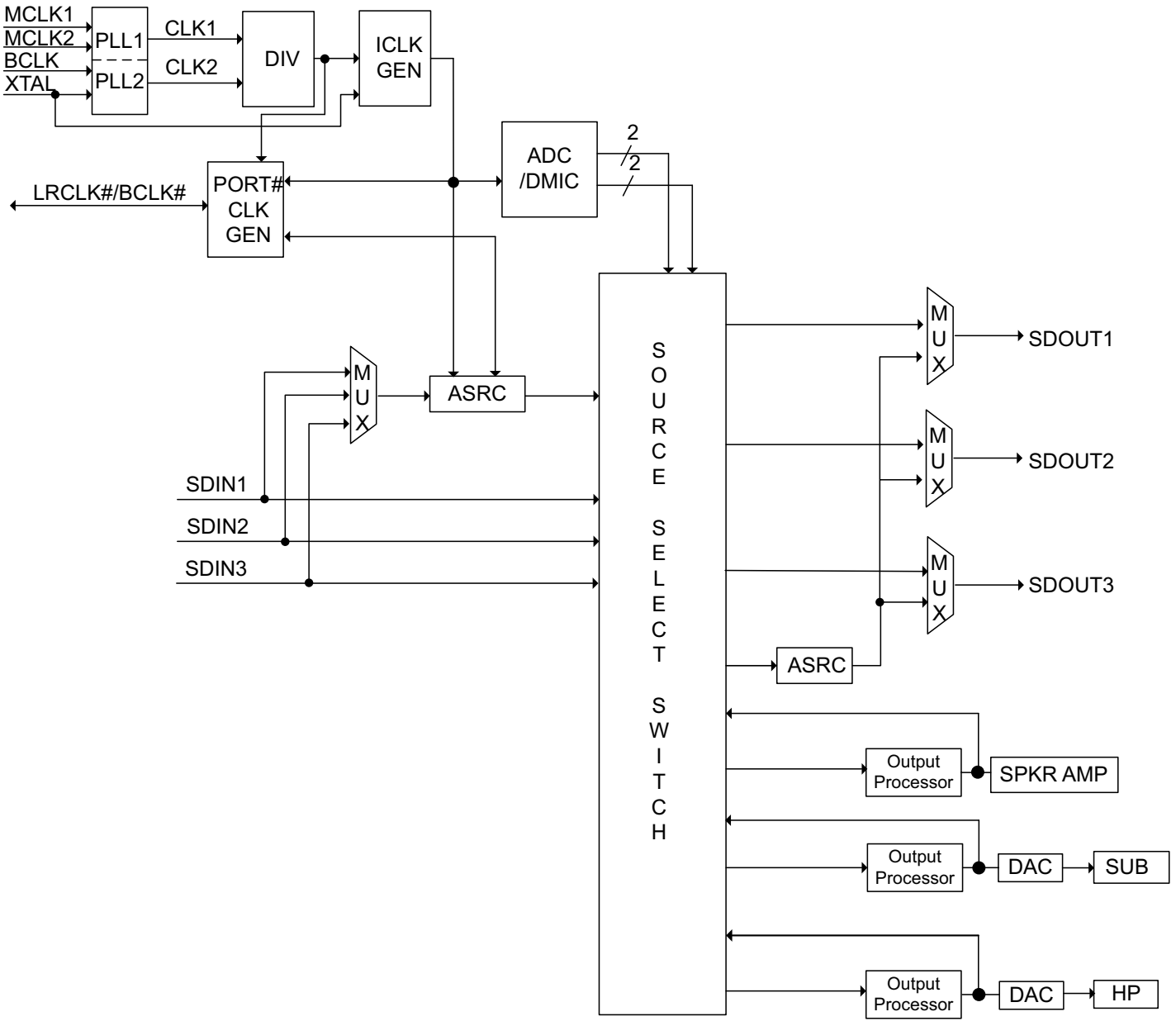


Figure 34. Simplified System Clock Block Diagram

The ADC internal processing blocks, DAC internal processing, Digital Mixer, input timing of the output ASRC's and output timing of the input ASRC's run at the ICLK (internal clock) rate. The sample rate of the audio source input to and out of the ASRC's is independent from the internal sample rate. The function of the ASCR's is to sample rate convert the incoming and outgoing audio to the fixed internal sample rate as defined by ICLK defined clock rate.

7.2.1.1. PLL Status Register

Register Address	Bit	Label	Type	Default	Description
Page 0 , Reg 10 - Ah PLLSTAT	7:2	RSVD	R	00h	Reserved
	1	PLL2LK	R	0	1 = PLL2 has obtained lock
	0	PLL1LK	R	0	1 = PLL1 has obtained lock

Table 141. PLLSTAT Register

7.2.1.2.PLL1 Control Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 11 - Bh PLL1CTL	7	RSVD	R	0	Reserved
	6:5	VCCI_PLL1	RW	1h	PLL1 voo/ico current setting
	4:3	RZ_PLL1	RW	2h	PLL1 Zero R setting
	2:0	CP_PLL1	RW	3h	PLL1 main charge pump current setting

Table 142. PLL1CTL Register

7.2.1.3.PLL1 Reference Clock Divider Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 12 - Ch PLL1RDIV	7:0	REFDIV_PLL1	RW	19h	PLL1 refclk divider

Table 143. PLL1RDIV Register

7.2.1.4.PLL1 Output Divider Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 13 - Dh PLL1ODIV	7:0	OUTDIV_PLL1	RW	03h	PLL1 output divider

Table 144. PPL1ODIV Register

7.2.1.5.PLL1 Feedback Divider Low Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 14 - Eh PLL1FDIVL	7:0	FBDIVL_PLL1	RW	80h	PLL1 feedback divider

Table 145. PLL1FDIVL Register

7.2.1.6.PLL1 Feedback Divider High Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 15 - Fh PLL1FDIVH	7:4	RSVD	R	0	Reserved
	3:0	FBDIVH_PLL1	RW	1h	PLL1 feedback divider

Table 146. PLL1FDIVH Register

7.2.1.7.PLL2 Control Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 16 - 10h PLL2CTL					
	7:6	VCCI_PLL2	RW	0	PLL2 voo/ico current setting
	5:3	RZ_PLL2	RW	1h	PLL2 Zero R setting
	2:0	CP_PLL2	RW	6h	PLL2 main charge pump current setting

Table 147. PLL2CTL Register

7.2.1.8. PLL2 Reference Clock Divider Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 17 - 11h PLL2RDIV	7:0	REFDIV_PLL2	RW	19h	PLL2 reference clock divider

Table 148. PLL2RDIV Register

7.2.1.9.PLL2 Output Divider Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 18 - 12h PLL2ODIV	7:0	OUTDIV_PLL2	RW	05h	PLL2 output divider

Table 149. PLL2ODIV Register

7.2.1.10.PLL2 Feedback Divider Low Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 19 - 13h PLL2FDIVL	7:0	FBDIVL_PLL2	RW	4ch	PLL2 feedback low divider

Table 150. PLL2FDIVL Register

7.2.1.11.PLL2 Feedback Divider High Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 20 - 14h PLL2FDIVH	7:4	RSVD	R	0	Reserved
	3:0	FBDIVH_PLL2	RW	2h	PLL2 feedback high divider

Table 151. PLL2FDIVH Register

7.2.1.12.PLL Control Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 21 - 15h PLLCTL	7	PU_PLL2	RW	0	Power Up PLL 2 1 = Power Up 0 = Power Down
	6	PU_PLL1	RW	0	Power Up PLL 1 1 = Power Up 0 = Power Down
	5	EN_PLL2	RW	0	Enable output of PLL 2 1 = Enable Output 0 = Disable Output
	4	EN_PLL1	RW	0	Enable output of PLL 1 1 = Enable Output 0 = Disable Output
	3:2	BCLKSEL	RW	00h	BCLK Input Select For PLL when PLLISEL = 11 00 = BCLK1 01 = BCLK2 10 = BCLK3 11= reserved
	1:0	PLLISEL	RW	0	Selects XTAL, MCLK1,MCLK2, I2S BCLK as PLL input 00 = XTAL selected as PLL input 01 = MCLK1 selected as PLL input 10 = MCLK2 selected as PLL input 11 = BCLK selected as PLL input

Table 152. PLLCTL Register

7.2.2 PLL Power Down Control

Each PLL can be powered down to save power if only one set of base audio rates is required. The base audio rates are defined as 44.1KHz based rates or 48KHz based rates. If support for either 44.1KHz or 48KHz based rates is not needed then the PLL associated with the unused rate can be powered down.

7.2.3 Audio Clock Generation

Figure 34 shows the simplified block diagram. The TSCS454xx utilizes internal PLLs to generate the PLL clocks at 112.896 MHz (22.5792MHz *5) and122.880 MHz (24.576 *5). Intermediate clocks (61.44MHz, 40.96MHz, 56.448MHz) are then generated which are then used to generate the audio sample rates. There is one internal clock rate that can be specified to operate at 11.025KHz, 12 KHz, 22.050KHz, 24KHz, 44.1KHz, 48KHz,88.2KHz, and 96KHz. When changing sample rates a delay of up to 5mS may be needed for the part to properly lock PLLs, flush filters, etc.

7.2.3.1.PLL Clock Source

The clock source for the PLL's can be selected from the XTAL input, MCLK1 input via the XTAL_IN pin, the MCLK2 pin or one of the I2S BCLK inputs via a selectable mux.

7.2.3.2. Internal Sample Rate Control Register

This register defines the internal sample rate.

Register Address	Bit	Label	Default	Description
Page 0, Reg 22 - 16h ISRC	7:3	RSVD	00h	Reserved
	2	IBR	1	ICLK Internal Base Rate 0 = 44.1KHz 1 = 48KHz
	1:0	IBM		ICLK Internal Base Rate Multiplier 00 = 0.25 01 = 0.5 10 = 1x 11 = 2x

Table 153. ISRC Register

Internal Sample Rates

IBR	xBM [1:0]	BASE RATE	SAMPLE RATE
0	00	56.448MHz	11.025kHz(MCLK/5120)
	01		22.050kHz(MCLK/2560)
	10		44.1 kHz (MCLK/1280)
	11		88.2 kHz (MCLK/640)
1	00	61.44 MHz	22kHz(MCLK/5120)
	01		24kHz(MCLK/2560)
	10		48 kHz (MCLK/1280)
	11		96 kHz (MCLK/640)

Table 154. Sample Rates

7.2.3.3. MCLK2 Pin

The MCLK2 pin can be configured to be an input or an output. When configured as an input it can provide a clock to drive the input to the PLL's or or the I2S Master Mode clock generators. When the MCLK2 pin is configured as an output it can provide either a 22.5792MHz, 24.576MHz, clock or when driven by PLL2 just about any desired clock frequency as can be programmed by the PLL2 registers.

MCLK2 Pin Control Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 33-21h MCLK2PINC	7:4	SLEWOUT[3:0]	RW	1000b	Slew rate setting for MCLK2 Output
	3	RSVD	R	0	Reserved
	2	MCLK2IO	RW	0	Configure MCLK2 as input or output. 0 = MCLK2 pin is an input 1 = MCLK2 pin is an output
	1:0	MCLK2OS[1:0]	RW	01b	MCLK2 Pin Output Clock Select 00 = 24.576 MHz 01 = 22.5792 MHz 10 = PLL2[1] 11 = Reserved

Table 155. MCLK2PINC Register

1.The maximum supported output frequency for MCLK2 is 50MHz

7.2.3.4. I2S Master Mode Clock Generation

Each I2S input audio source (PCM1, PCM2, and PCM3) can operate as a timing Slave or Master. When operated in Slave mode the ASRC will automatically detect the incoming audio sample rate and convert it to the current, internally defined, input/output sample rate. When operated in Master Mode an internal clock generator is used to produce the required bit and frame clocks to be driven out of the LRCLK and BCLK pins of each input I2S interface. The clock source for the I2S master clock generation can be selected between the PLL generated internal timing or an externally supplied clock via the MCLK2 input.

7.2.3.5. I2S Master Mode Sample Rate Control

These registers set the I2S Master Mode sample rates. For normal operation the PLL1 and PLL2 outputs are used for generating the timing for the I2S ports when operating in Master Mode. Optionally the MCLK2 input may be used for generating the timing for the I2S ports when operating in Master Mode. External MCLK timing mode is selected when the MBR[1:0] bits are set to 11. In this mode the MCLK/2 and MCLKDIV[1:0] bits become active. The MBM[2:0] bits are also active in this mode. The I2SxMBR bits set the base audio sample to be either 44.1Khz or 48KHz. The I2SxMBM bits are then used to set the base rate multiplier ratio. When the MCLK2 input is selected as a clocks source for the I2S Master Mode clock generation the I2SxMCLK/2 and I2SxMCLKDIV[1:0] bits are used to divide down the MCLK2 input to the desired audio sample rate.

7.2.3.6. I2S MasterMode Control Registers

Register Address	Bit	Label	Default	Description
Page 0, Reg 29, 30, 31 - 1Dh, 1Eh, 1Fh I2S1MRATE, I2S2MRATE, I2S3MRATE	7	I2SxMCLK/2	0	MCLK2 Pre-Divide 0 = MCLK2 divide = 1 1 = MCLK2 divide = 2
	6:5	I2SxMCLKDIV[1:0]	0	MCLK2 Mode Divide. When MBR[1:0] = 11 00 = 125 01 = 128 10 = 136 11 = 192
	4:3	I2SxMBR[1:0]	10	Base Rate 00 = reserved 01 = 44.1KHz 10 = 48KHz 11 = External MCLK Mode - MCLK2 input used for I2S master mode clock
	2	RSVD	0	Reserved
	1:0	I2SxMBM[2:0]	010	Base Rate Multiplier 00 = 0.25x 01 = 0.50x 10 = 1x 11 = 2x

Table 156. I2S1MRATE, I2S2MRATE, I2S3MRATE Register

Note: 1 x=1,2,3

Register Address	Bit	Label	Default	Description
Page 0, Reg 26, 30, 31 - 1Ah, 1Bh, 1Ch I2SP1CTL, I2SP2CTL, I2SP3CTL	7	BCLKxSTAT	0	I2Sx BClk Loss Status, Slave Mode (Clear by writing1): 0 = BClk not lost; 1 = BClk loss detected
	6	BCLKPx	0	I2Sx BClk Polarity: 0 = Not inverted; 1 = Inverted
	5	PORT1MS	0	I2Sx Master/Slave Selection: 0 = Slave; 1 = Master
	4	LRCLKP1	0	I2Sx LRClk Polarity: 0 = Not inverted; 1 = Inverted
	3:2	WLx1[1:0]	10	I2Sx Word Length: 0h = 16 bits; 1h = 20 bits; 2h = 24 bits; 3h = 32 bits
	1:0	FORMATx[1:0]	10	I2Sx Format: 0h = Right justified; 1h = Left justified; 2h = I2S format; 3h = TDM mode

Table 157. I2SP1CTL, I2SP2CTL, I2SP3CTL Register

Note: 1 x=1,2,3

The table below shows the typical I2S Master Mode Audio Sample Rates when using the MCLK2 input as the input clock source.

MCLK2(MHZ)	MCLK/2	MCLKDIV[1:0]	MBM [2:0]	SAMPLE RATE(KHz)	ERROR
24.576	/2	128	000	12	0
			001	24	0
			010	48	0
			011	96	0
		192	000	8	0
			001	16	0
			010	32	0
			011	64	0
12.288	/1	128	000	12	0
			001	24	0
			010	48	0
			011	96	0
		192	000	8	0
			001	16	0
			010	32	0
			011	64	0
24.000	/2	125	000	12	0
			001	24	0
			010	48	0
			011	96	0
		136	000	11.0294	.04%
			001	22.0588	.04%
			010	44.1176	.04%
			011	88.235	.04%

Table 158. I2S Master Mode Audio Sample Rates

MCLK2(MHZ)	MCLK/2	MCLKDIV[1:0]	MBM [2:0]	SAMPLE RATE(KHz)	ERROR
12.000	/1	125	000	12	0
			001	24	0
			010	48	0
			011	96	0
		135	000	11.0294	.04%
			001	22.0588	.04%
			010	44.1176	.04%
			011	88.235	.04%
22.5792	/2	128	000	11.025	0
			001	22.050	0
			010	44.1	0
			011	88.2	0
11.2896	/1	128	000	11.025	0
			001	22.050	0
			010	44.1	0
			011	88.2	0
16.384	/2	128	000	8.0	0
			001	16.0	0
			010	32.0	0
			011	64.0	0

Table 158. I2S Master Mode Audio Sample Rates

7.2.3.7. DAC/ADC Clock Control

The power consumption and audio quality may be adjusted by changing the converter modulator rate. By default the DAC and ADC Sigma-Delta modulators run at a high rate for the best audio quality. The modulator rates for the converters may be forced to run at half their nominal rate to conserve power. A third option allows the modulator rate to automatically drop to half rate when low sampling rates are chosen (1/2 or 1/4 the base rate.) The DACs and ADCs are independently controlled.

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 24 - 18h SCLKCTL	7:6	ASDM[1:0]	RW	10h	ADC Modulator Rate 00 = Reserved 01 = Half 10 = Full 11 = Auto
	5:4	DSDM[1:0]	RW	10h	DAC Modulator Rate 00 = Reserved 01 = Half 10 = Full 11 = Auto
	3:0	RSVD	R	0	Reserved

Table 159. SCLKCTL Register

ADC and DAC Modulator Rates

DSDM[1:0] ASDM[1:0]	BM [2:0]	Modulator Rate
00	NA	Reserved
01	000 (1/4x)	Half
	001 (1/2x)	
	010 (1x)	
	011 (2x)	
10	000 (1/4x)	Full
	001 (1/2x)	
	010 (1x)	
	011 (2x)	
11	000 (1/4x)	Auto (Half)
	001 (1/2x)	Auto (Half)
	010 (1x)	Auto (Full)
	011 (2x)	Auto (Full)

Table 160. ADC and DAC Modulator Rates

7.2.3.8.TMBASE - Timebase Register

Register Address	Bit	Label	Type	Default	Description
Page 0, Reg 27 - 19h TMBASE	7-0	TIMEBASE[7:0]	RW	2F	Internal Time Base Divider. This value should be programmed as [round(ref clock/256000)]-1

Table 161. TMBASE Register

8. HEADPHONE AND COMBO JACK DETECTION

The TSCS454xx supports headphone/headset detection, button press detection, and OMTP/CTIA type Headsets. The TSCS454xx can be programmed to generate an interrupt when headphone/headset insert/removal or a button press is sensed. In addition when headphone insertion is detected, the TSCS454xx can automatically disable the speaker outputs and enable the headphone outputs.

8.1. Headphone Switch and Plug Insertion Detection

The HPDET pin is used to detect connection of a headphone when this pin is connected to a isolated or non-isolated switch located inside the headphone jack. Alternately a non-switch detection mode is provided to support jack types without switches.

A 4 conductor (combo) jack with switch is typically used to support this feature in conjunction with the Headphone Detect (HPDET) pin. In the most common implementation, the 4 conductor plug has the same mechanical dimensions as a 3 conductor 3.5mm plug, but the sleeve portion has been split into two segments:S1 and S2. When a 4-conductor plug (headset) is inserted into the jack T (Tip) = Left headphone audio, R (Ring) = Right headphone audio, S1 (First half of sleeve) = microphone input, and S2 (Second half of sleeve) = return (GND). When a 3-conductor plug (headphones) is inserted into the jack; T (Tip) = Left audio, R (Ring) = Right audio, S1(sleeve) = return (GND). By monitoring the S1 connection to see if it is shorted to ground, we can distinguish between headsets and headphones. Please note that analog microphone plugs (3-conductor-Lmic/Rmic/GND) and optical SPDIF plugs are not supported.

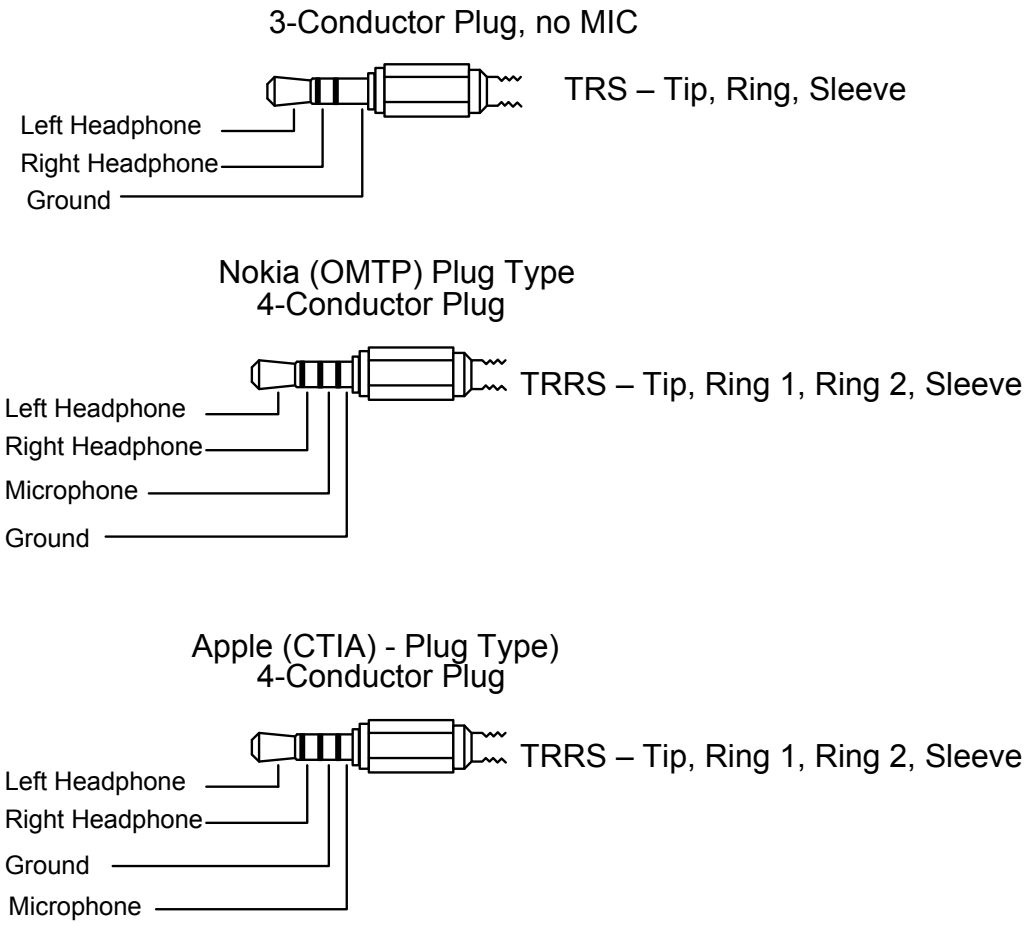


Figure 35. Headphone/Headset Plug Types

Requirements

Available pins include a Headphone detect pin (HPDET), Microphone Detect pin (MICDET), MICBIAS outputs, and analog line inputs.

Supports headphone output connections to Tip and Ring 1.

Supports TRS and TRRS plug types.

Plug insertion is reported on the headphone port using the switch integrated into the jack or by sensing the presence of signals that occur when a plug is inserted into a jack. The jack characteristics have a direct impact on what can be sensed thus a summary of various jack types and configurations will need to be provided.

The existing circuit monitors the voltage at various points on the jack to determine if a microphone is present on the Ring 2 or Sleeve. Both OMTP and CTIA plug types must be supported.

The non-microphone sensed Ring 2 or Sleeve connection must be connected to ground with minimal impedance.

Detection of a microphone is not reported unless plug insertion is also detected.

Provision should be made for preventing false detection by debouncing the headphone and microphone detection.

MIcrophone Bias output generator. Software may disable the MIC bias output to conserve power if the presence of a microphone is not detected.

Pops should be minimized when upon plug insertion/removal or when detecting the presence of a microphone.

8.2 Microphone Detection

The TSCS454xx supports detection of a microphone located on the “Sleeve” or Ring2 connection of a TRRS jack. The detection can be programmed to automatically control the MICBIAS, analog input selection, and ground switches or these can be controlled manually through register bits.

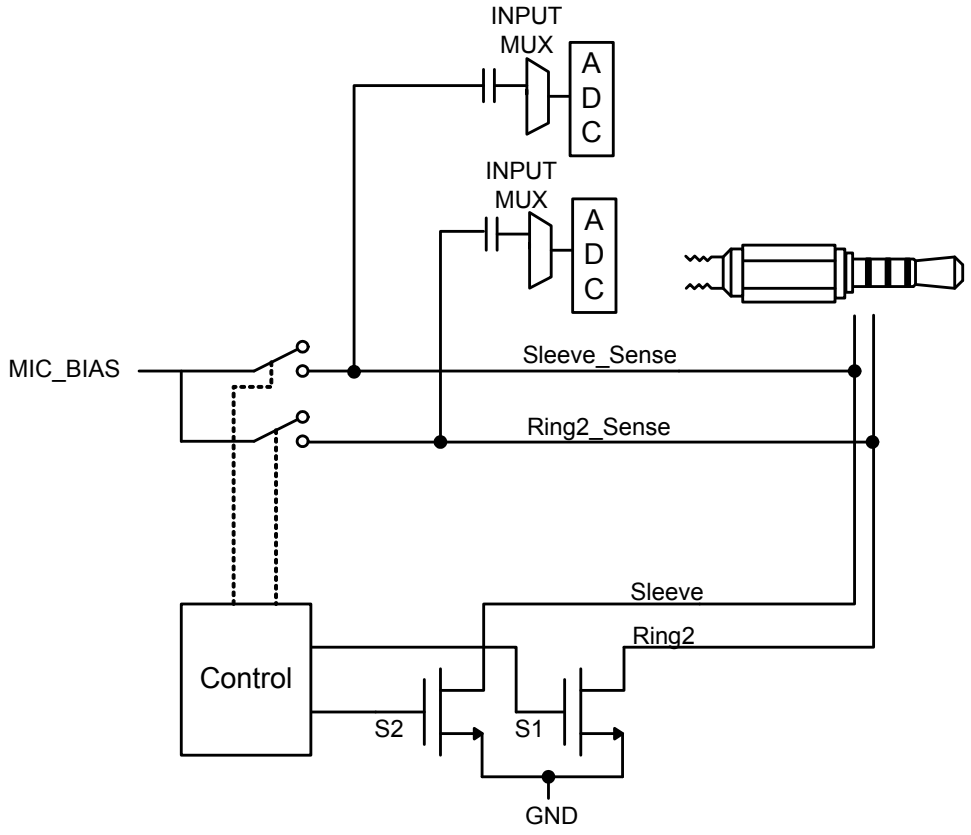


Figure 36. Example OMTP/CTIA Headset Detection Diagram

8.2.1. De-Glitch

To prevent anomalous plug insertion detect readings, a de-glitch circuit is provided. This logic circuit monitors the presence signal from the headset detection module (analog) for a transition (both positive and negative edges). The presence signal is considered valid if it remains stable for longer than a delay defined by the parameter T_STABLE. T_STABLE may be programmed as described in the table below.

T_STABLE [3:0]	Duration of de-glitch window
000	64ms
001	128ms
010	256ms(default)
011	512ms
100	1s
101	2s
110	4s
111	8s

Table 162. De-Glitch

Note: Assumes correct timebase settings

The detection result status bit is updated when the de-glitch circuitry has determined the impedance state is stable.If the de-glitch circuitry has determined that the impedance state is not stable then the headset presence bit will not be set.

8.2.2. Plug Insertion Before Headset Detection Is Enabled

Before Headset detection is enabled, the presence of a headphone inserted into the jack is determined by the HP_DET input. If a headphone is present when power is applied to the CODEC or if the CODEC is returning from a low power state, the CODEC will not detect a change in state and would normally not attempt to detect a microphone.To prevent this problem, the CODEC will automatically start a microphone detection cycle when Headset detection is enabled if the presence of the HP_DET detect true.

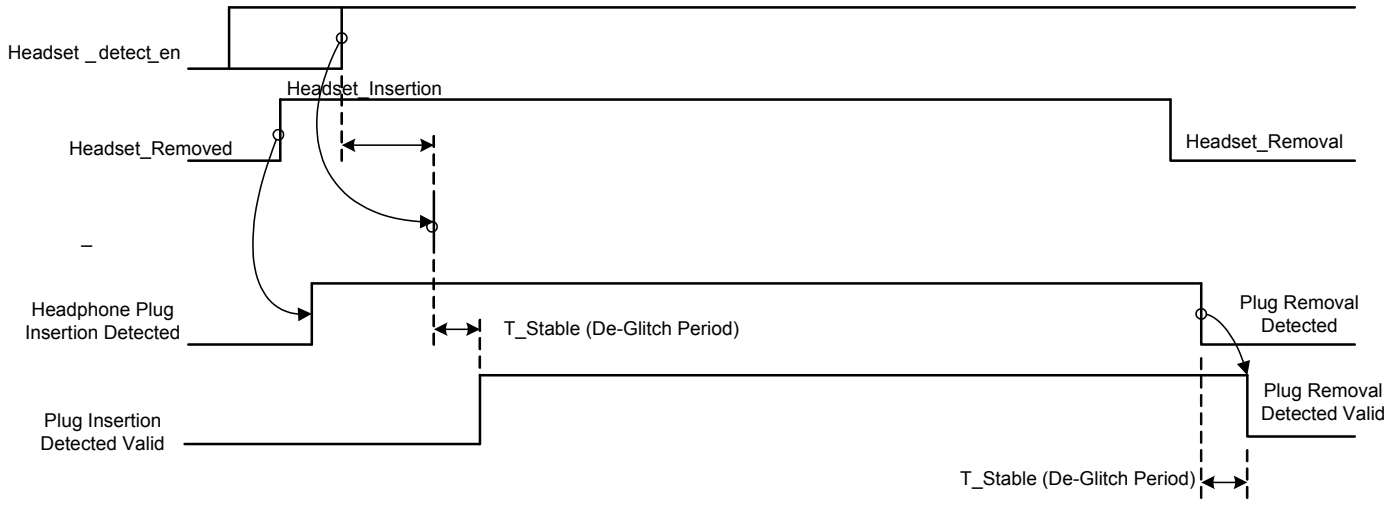


Figure 37. Headset present in jack when Combo-jack detection is enabled

The following diagrams show the connections to different headset jack configurations.

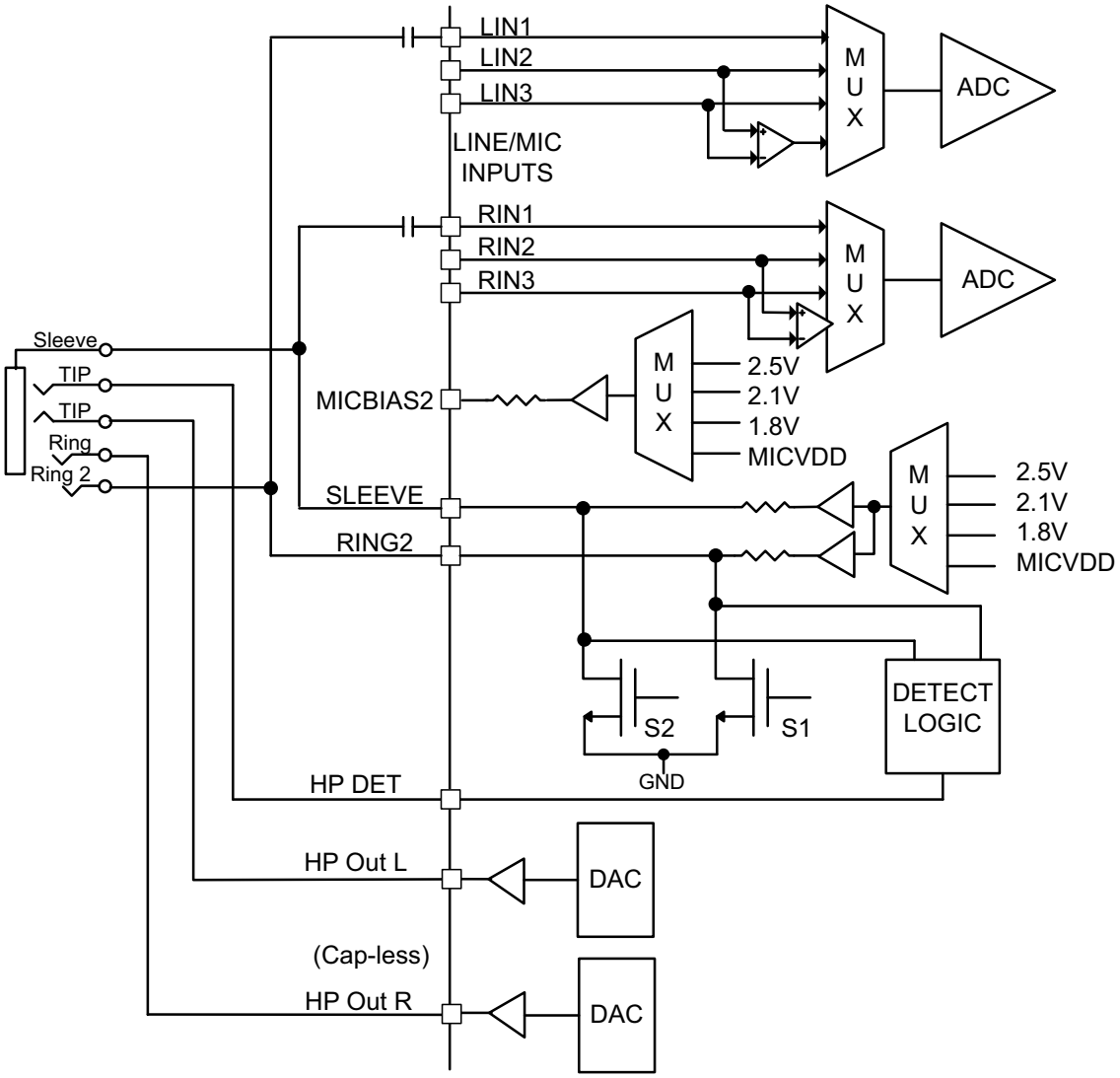


Figure 38. Pin Connection Diagram for 5 Terminal OMTP/CTIA Headset Support

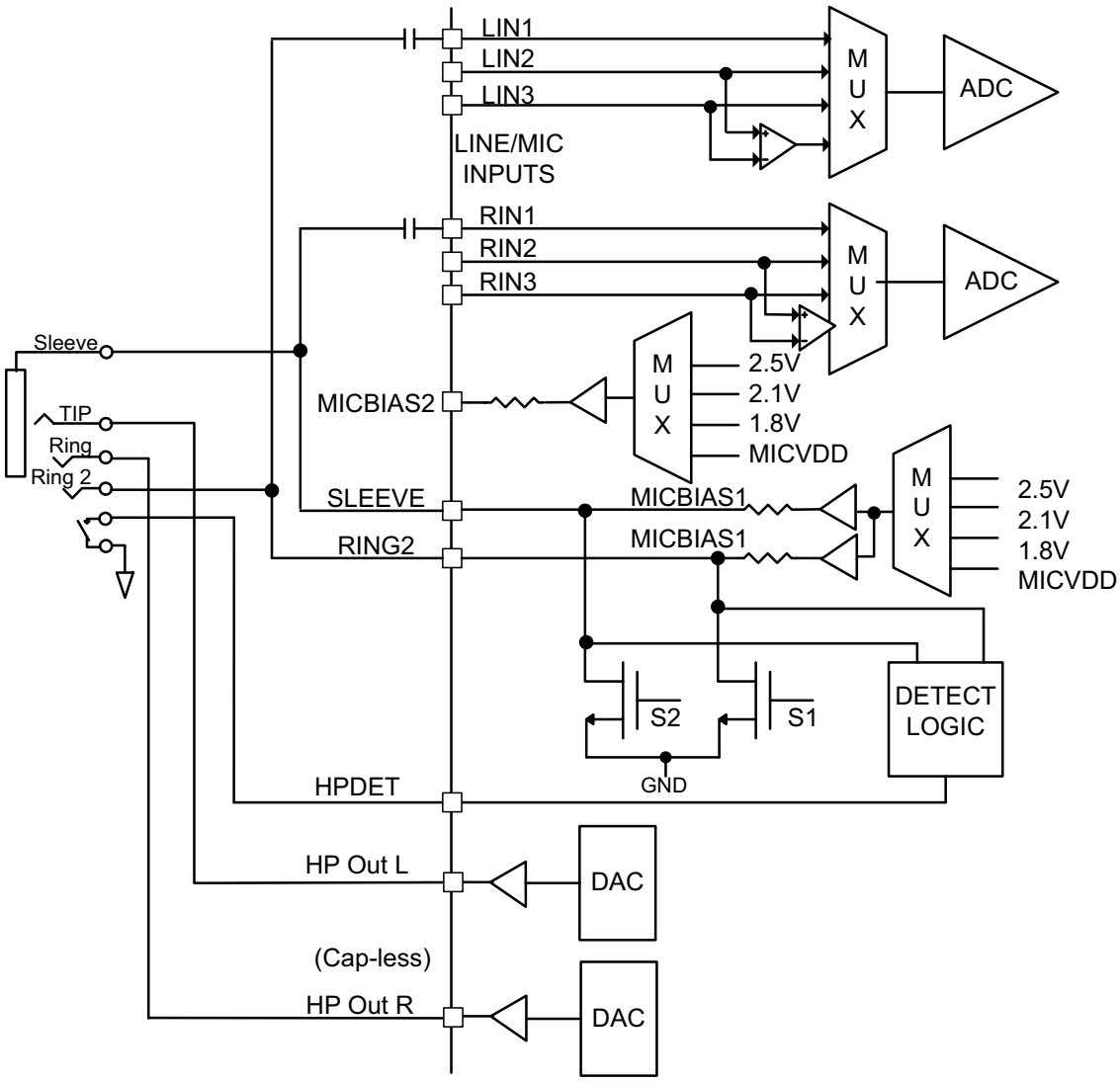


Figure 39. Pin Connection Diagram for 4 Terminal OMTP/CTIA Headset Support with isolated switch

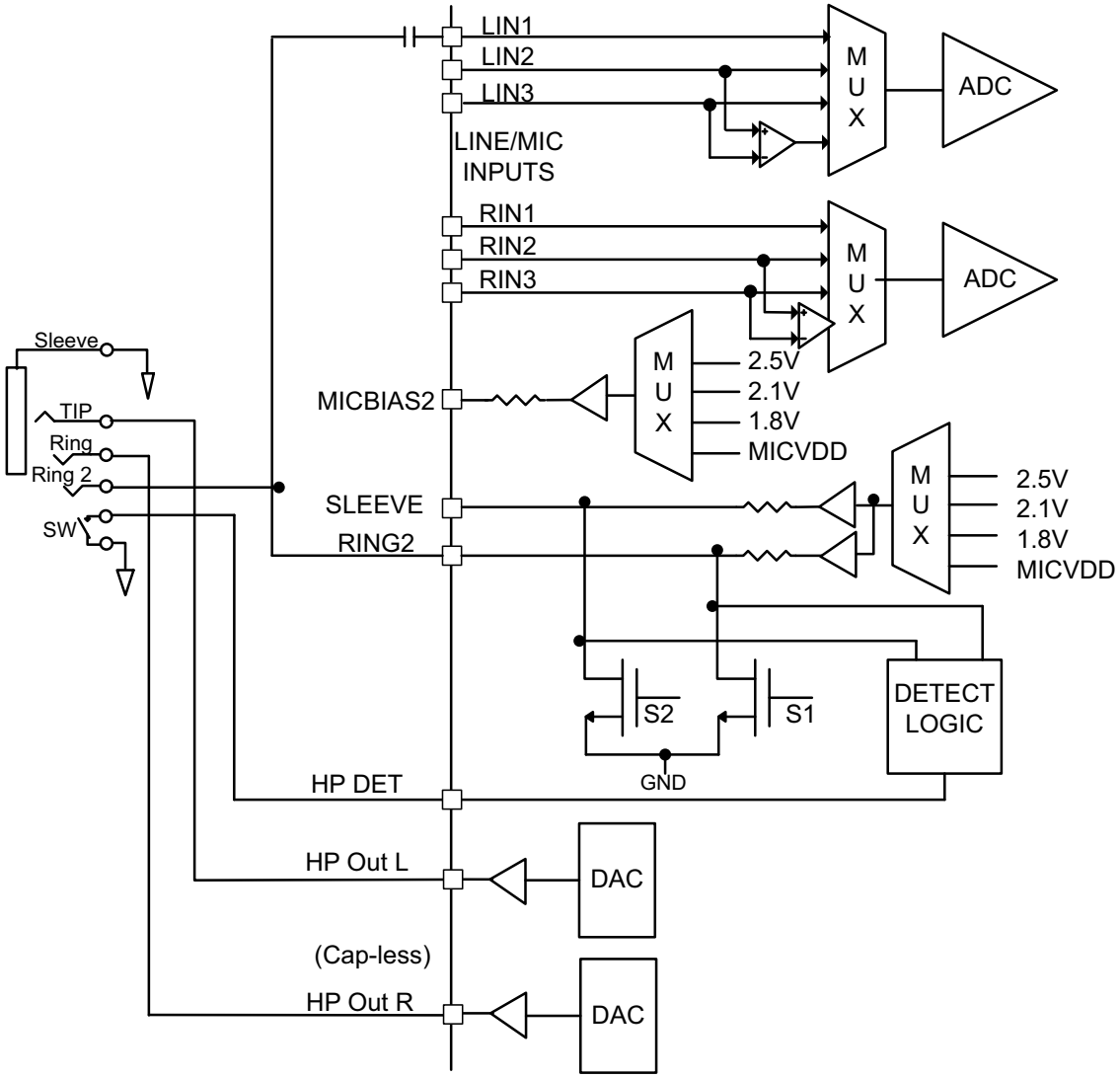


Figure 40. Pin Connection Diagram for 3 Terminal with isolated switch

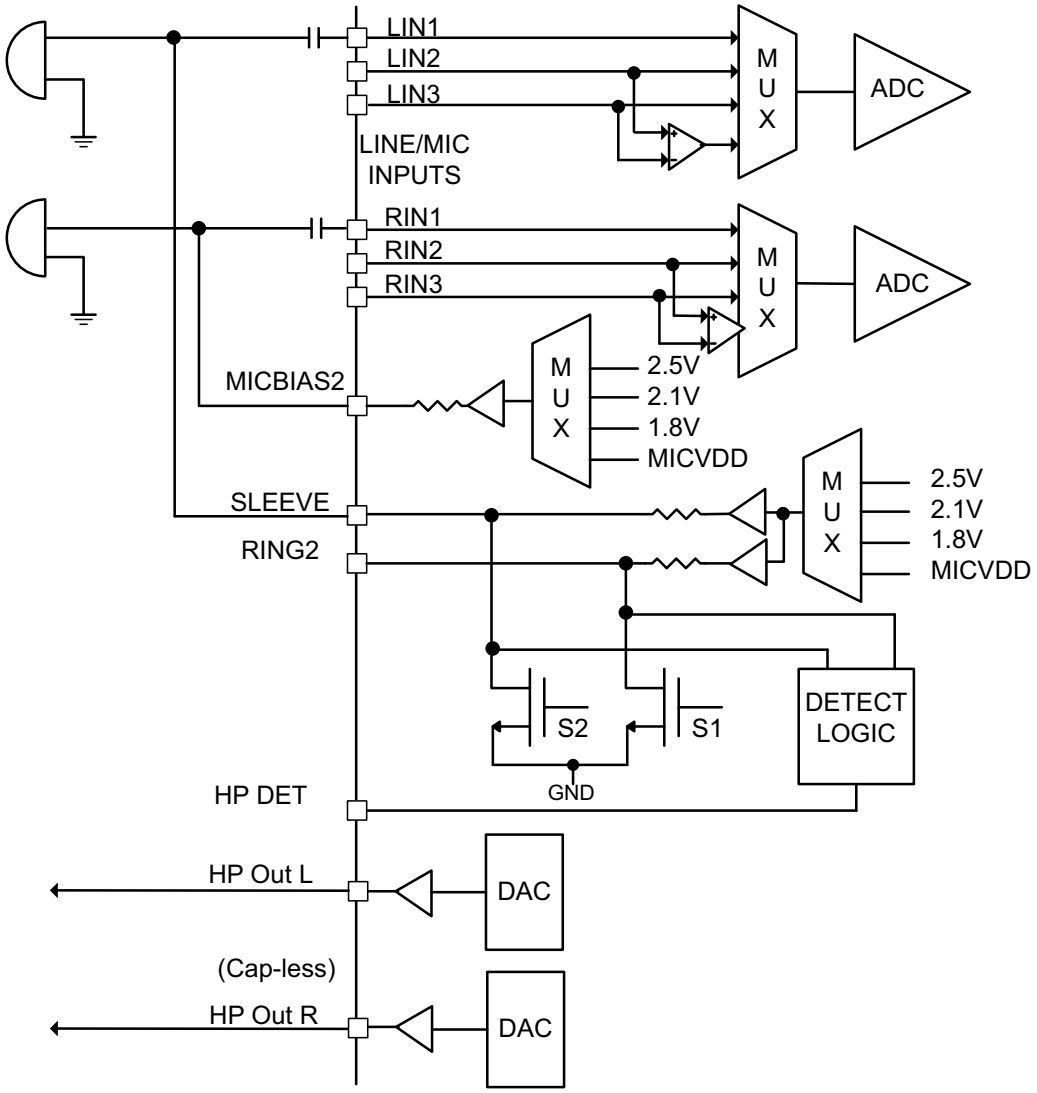


Figure 41. Pin Connection Diagram using internal Mlc's

8.2.3. Headset Type Detection and Microphone Selection Process

The process by which the headset type is detected is a follows:

- Headphone Detection and Headset Detection are enabled
- Headphone/Headset Plug insertion is detected and de-bounced
- If plug insertion is detected then the Headset Detection process is started
- The microphone is detected on either RING2 or SLEEVE
- The MICBIAS is enabled onto the microphone detected pin and the other pin is connected to GND.
- The Analog Input MUX is set to select the input that is connected to the microphone.

The process can be set to be automatic or controlled manually.

8.2.4. Headphone/Headset Control Registers

8.2.4.1 Headphone/Headset Detection Control Register 1

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 1-1h HSDCTL1	7	HPJKTYP	RW	0	Ring2/Sleeve ground connection for 3-terminal plug. 0 = Mode 0, normal operation 1 = Mode 1, Ring2 remains off for 3-terminal plug
	6	CONDETPWD	RW	1	Connection Detection Powerdown 0 = GHS connection detection analog circuitry on 1 = GHS connection detection analog circuitry off
	5:4	DETCYC[1:0]	RW	10b	Number of consecutive matching Cycles for detection 00 = 1 01 = 2 10 = 3(default) 11 = 4
	3	HPDLYBYP	RW	0	Headphone plug insertion detect delay bypass 0 = Headphone plug detect delay enabled 1 = Headphone plug detect delay bypassed
	2	HSDETPOL	RW	0	Polarity for headset detect trigger 0 = headset detection triggered on low to high transition of HP_DET pin. 1 = headset detection triggered on high to low transition of HP_DET pin
	1	HPID_EN	RW	0	Headphone Plug Insertion Detect Enable 0 = Plug Insertion detect disabled 1 = Plug Insertion detect enabled
	0	GBLHS_EN	RW	0	OMTP, CTIA Headset Detect Enable 0 = OMTP, CTIA Headset support disabled 1 = OMTP, CTIA headset support enabled

Table 163. HSDCTL1 Register

8.2.4.2 Headphone/Headset Detection Control Register 2

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 2-2h HSDCTL2	7:6	FMICBIAS1[1:0]	RW	00b	Force MICBIAS1 Drive to the headset jack when MB1MODE is set to 1 00 = Off 01 = Force Mic Bias on Ring2 10 = Force Mic Bias on Sleeve 11 = Invalid (Force Mic Bias on both Ring2 and Sleeve)
	5	MB1MODE	RW	0	MICBIAS1 MODE 1 = MICBIAS1 is manually configured 0 = MICBIAS1 is automatically configured by the headset detection circuit
	4	FORCETRG	RW	0	Force Detection - “0” to “1” transition forces detection. Bit is reset to “0” after detection process ends.
	3	SWMODE	RW	0	Ring 2/Sleeve/MICBIAS1 Switch Control 0 = Switching is manual. 1 = Switching is automatic
	2	GHSHIZ	RW	0	0 = sleeve and rin2 switches enabled 1 = force sleeve and ring2 switches Hi-Z
	1:0	FPLUGTYPE[1:0]	RW	11	Force Plug Type when SWMODE= 0 AND GHSHIZ = 0 00 = 4 terminal plug with mic on Ring2 (OMTP) 01 = 4 terminal plug with mic on sleeve (CTIA) 10 = Reserved (3 terminal plug) 11 = 3 terminal plug (headphone only)

Table 164. HSDCTL2 Register

8.2.4.3 Headphone/Headset Detection Status Register

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 3-3h HSDSTAT	7	RSVD	R	0	Reserved
	6:5	MBIAS1DRV[1:0]	R	00	Status of MICBIAS1 00 = Off 01 = MICBIAS1 active on Ring2 10 =MICBIAS1 active on Sleeve 11 = Invalid (MICBIAS1 active on Ring2 and Sleeve)
	4	RSVD	R	0	Reserved
	3	HSDETSTAT	R	0	Headset Detect Status - Presence of a plug in the headset jack as reported to the detection state machine.0 = Nothing plugged in1 = Plug inserted in jack
	2:1	PLUGTYPE[1:0]	R	11	Detected Headset Type 00 = OMTP 01 = CTIA 10 = Headphones (detect cycle not run) 11 = Headphones
	0	HSDETDONE	R	0	Headset Detect Done 0 = Headset detection not started/in process 1 = Headset detection completed

Table 165. HSDSTAT Register

8.2.4.4 Headset Detection Delay Register

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 4-4h HSDELAY	7:3	RSVD	R	0	Reserved
	2:0	T_STABLE[2:0]	RW	010b	Delay for plug insertion detect 000 = 64ms 001 = 128ms 010 = 256ms(default) 011 = 512ms 100 = 1s 101 = 2s 110 = 4s 111 = 8s

Table 166. HSDELAY Register

Note: Assumes correct time base settings

8.2.5. Lanyard Switch ("Turbo Button") Support

Many headsets that implement a 4-pin plug will provide a push-button switch. The switch may connected in parallel or in series with the microphone signal. If the switch is connected in series then the microphone input connection will temporarily be open circuit (high-impedance). If the switch is connected in parallel the switch will temporarily short the microphone input to ground. The switch is typically used to support call answer, call hang-up, pause/resume, track advance or other functions. This switch is commonly known as a lanyard switch or "turbo button.

The Lanyard switch detection requirements are:

- Support for a single switch function
- Lanyard switch support can be enabled or disabled. When disabled the circuitry associated with the function should be powered down.
- The Lanyard switch button press detection is only enabled if a headset is detected.
- The detection of a button press generated an interrupt
- The button press detection should be de-bounced to prevent false detections.
- Support for short and long button press detection should be provided.

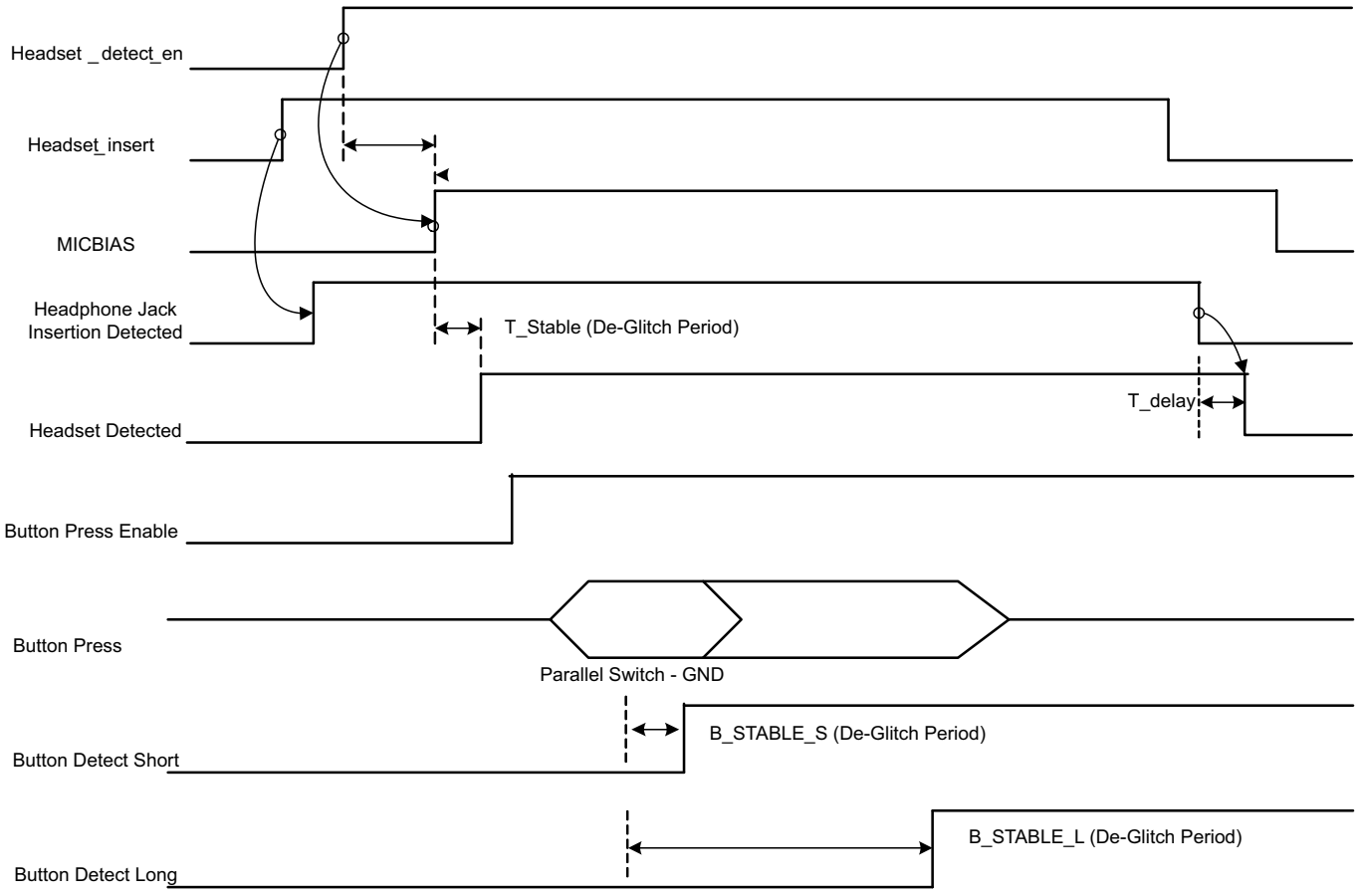


Figure 42. Lanyard Button Push Detect Diagram

8.2.6. Lanyard Button Support Registers

Register Address	Bit	Label	Type	Default	Description
Page 1, Reg 5-5h BUTCTL	7	BPUSHSTAT	R	0	Button Push Status 0 = short 1 = long
	6	BPUSHDET	RW	0	Button Push Detected - Cleared by writing a zero to this register. 0 = Button push not detected 1 = Button push detected
	5	BPUSHEN	RW	0	Button Push Detect Enable 0 = Button push detect disabled 1 = Button Push Detect Enabled
	4:3	B_STABLE_L[1:0]	RW	0	Delay for button push detection long 00 = 500ms 01 = 1s 10 = 1.5s 11 = 2.0s
	2:0	B_STABLE_S[2:0]	RW	000b	Delay for button push detection short 000 = 0 (OFF) 001 = 50ms 010 = 100ms 011 = 150ms 100 = 200ms 101 = 250ms 110 = 300ms 111 = 350ms

Table 167. BUTCTL Register

Note: Assumes correct timebase settings

9. CHARACTERISTICS

9.1. Audio Fidelity

DAC SNR: >102dB, A-Weighted, 3.3V/4.75V
ADC SNR: >95dB, A-Weighted, 3.3V/4.75V

9.2. Electrical Specifications

9.2.1. Absolute Maximum Ratings:

Voltage on any pin relative to Ground	Vss - 0.3V TO Vdd + 0.3V
Operating Temperature	0 ^{o}C TO 70 ^{o}C
Storage Temperature	-55 ^{o}C TO +125 ^{o}C
Soldering Temperature	260 ^{o}C
MICBias Output Current	3mA
Amplifier Maximum Supply Voltage	6 Volts = PVDD
Audio Maximum Supply Voltage	3 Volts = AVDD/CPVDD
Digital I/O Maximum Supply Voltage	3.6 Volts = DVDD_IO
Digital Core Maximum Supply Voltage	2.0 Volts = DVDD

Table 168. Absolute Maximum Ratings

9.3. Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Power Supplies				
DVDD_Core	1.4		2.0	V
DVDD_IO	1.6	3.3	3.5	
AVDD/CPVDD	1.7	1.9	2.0	
PVDD	3.0	3.7	5.5	V
Ambient Temperature	0	25	70	^{o}C
Tj			150	^{o}C

Table 169. Recommended Operating Conditions

*Note: **ESD:** The TSCS454xx codec is an ESD (Electrostatic discharge) sensitive device. Even though the TSCS454xx family implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.*

9.4. Characteristics

Test Conditions

Unless stated otherwise, DVDD_CORE=DVDD_IO=1.6V, AVDD=1.7V, PVDD=3.6V, TA=+25C, 997Hz signal, fs=48KHz, Input Gain=0dB, 24-bit audio

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Analog Inputs (L_{IN1}, L_{IN2}, L_{IN3}, R_{IN1}, R_{IN2}, R_{IN3})						
Full Scale Input Voltage	V_{FSIV}	$L/R_{IN1,2,3}$ Single Ended		0.5 -6		Vrms dBV
		$L/R_{IN1,2,3}$ Differential Mic		0.5 -6		Vrms dBV
Input Impedance				50		KΩ
Input Capacitance				10		pF
Analog Input Boost Amplifier						
Programmable Gain Min				0.0		dB
Programmable Gain Max				30.0		dB
Programmable Gain Step Size				10.0		dB
Analog Input PGA						
Programmable Gain Min				-17.25		dB
Programmable Gain Max				30.0		dB
Programmable Gain Step Size		Guaranteed Monotonic		0.75		dB
Digital Volume Control Amplifier						
Programmable Gain Min				-97		dB
Programmable Gain Max				30.0		dB
Programmable Gain Step Size		Guaranteed Monotonic		0.5		dB
Mute Attenuation				-999		dB
Analog Inputs (L_{IN1}/R_{IN1}, L_{IN2}/R_{IN2} Differential) to ADC						
Signal To Noise Ratio	SNR	A-weighted 20-20KHz	85	90		dB
Total Harmonic Distortion + Noise	THD+N	-1dBFS input		-80 0.01		dB %
Analog Inputs (L_{IN1}, L_{IN2}, L_{IN3}, R_{IN1}, R_{IN2}, R_{IN3} Single Ended) to ADC						
Signal To Noise Ratio	SNR	A-weighted 20-20KHz	85	90		dB
Total Harmonic Distortion + Noise	THD+N	-1dBFS input		-80 0.01		dB %
ADC channel Separation		997Hz full scale signal		70		dB
Channel Matching		997Hz signal			2	%
DAC to Line-Out (with 10K / 50pF load)						
Signal to Noise Ratio[1]	SNR	A-weighted		102		dB
Total Harmonic Distortion +Noise[2]	THD+N	997Hz full scale signal		-82		dB
Channel Separation		997Hz full scale signal		70		dB
Mute attenuation				-999		dB
Headphone Outputs (HPL, HPR)						

Table 170. Test conditions characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Full Scale Output Level	V_{FSOV}	RL = 10KΩ		1.0		Vrms
		R_L = 16Ω		0.8		Vrms
Output Power	P_O	997Hz full scale signal, R_L = 16Ω		40		mW (avg)
Signal to Noise Ratio	SNR	A-weighted, R_L = 16Ω		102		dB
Total Harmonic Distortion +Noise	THD+N	R_L = 16Ω, -3dBFS		-72		dB
		R_L = 16Ω, -6dBFS		-78		dB
		R_L = 32Ω, -3dBFS		-75		dB
		R_L = 32Ω, -6dBFS		-80		dB
Earpiece Output (SUB+, SUB-)						
Full Scale Output Level	V_{FSOV}	RL = 10KΩ		1.0		Vrms
		R_L = 16Ω		0.8		Vrms
Output Power	P_O	997Hz full scale signal, R_L = 16Ω		40		mW (avg)
Signal to Noise Ratio	SNR	A-weighted, R_L = 16Ω		102		dB
Total Harmonic Distortion +Noise	THD+N	R_L = 16Ω, -3dBFS		-72		dB
		R_L = 16Ω, -6dBFS		-78		dB
		R_L = 32Ω, -3dBFS		-75		dB
		R_L = 32Ω, -6dBFS		-80		dB
Analog Voltage Reference Levels						
Charge Pump Output	V-		-5%	-AVDD +100mV	+5%	V
Microphone Bias (MICBIAS1, MICBIAS2)						
Bias Voltage	$V_{MICBIAS}$		-	2.5	-	V
BIAS current Source					3	mA
Power Supply Rejection Ratio	$PSRR_{MICBIAS}$	3.3V<PVDD<5.5V		80		dB
		3.0V<PVDD<3.3v		40		dB
Digital Input/Output						
ADC/DAC BCLK input rate	Fmax			30		MHz
I2S BCLK/LRCLK ratio			32		1022	clocks/frame
Input High Level	V_{IH}		0.7x DVDD_IO			V
Input LOW Level	V_{IL}				0.3xDVDD_IO	V
Output High Level	V_{OH}	I_{OH}=-1mA	0.9x DVDD_IO			V
Output LOW Level	V_{OL}	I_{OL}=1mA		0.1xDVDD_IO		V
Input Capacitance				5		pF
Input Leakage			-0.9		0.9	uA
ESD / Latchup						

Table 170. Test conditions characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IEC1000-4-2			1			Level
JESD22-A114-B			2			Class
JESD22-C101			4			Class

Table 170. Test conditions characteristics

1.Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
2.THD+N ratio as defined in AES17 and outlined in AES6id,non-weighted, swept over 20 Hz to 20 kHz bandwidth.

9.4.1. SNR at Sample Rates other than 48KHz

Sample Rate (kHz)	DAC SNR (dB ratio)	ADC SNR (dB ratio)	Notes
48 kHz based rates			
96	102	90	ADC SNR is a design target. Typical is listed as 90
48	102	90	ADC SNR is a design target. Typical is listed as 90
24	96	90	SDM at 1/2 rate. ADC SNR is a design target. Typical is listed as 90
12	96	90	SDM at 1/2 rate. ADC SNR is a design target. Typical is listed as 90
44.1 kHz based rates			
88.2	102	90	ADC SNR is a design target. Typical is listed as 90
44.1	102	90	ADC SNR is a design target. Typical is listed as 90
22.05	96	90	SDM at 1/2 rate. ADC SNR is a design target. Typical is listed as 90
11.025	96	90	SDM at 1/2 rate. ADC SNR is a design target. Typical is listed as 90
32 kHz based rates			
64	101	90	ADC SNR is a design target. Typical is listed as 90
32	101	90	ADC SNR is a design target. Typical is listed as 90
16	89	90	SDM at 1/2 rate. ADC SNR is a design target. Typical is listed as 90
8	88	90	SDM at 1/2 rate. ADC SNR is a design target. Typical is listed as 90

Table 171. SNR Sample Ra

9.5. PLL Section DC Electrical Characteristics

Unless stated otherwise, DVDD_Core=1.8V -0.1V/+0.2V, Ambient Temp -10C to +80C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	DVDD_CORE		1.7	1.8	2.0	V
Supply Current	$I_{DVDD\_CORE(PLL)}$	No Load, VDD=1.9V		11	15	mA
Input High Level	V_{IH}		0.7x DVDD_CORE			V
Input LOW Level	V_{IL}				0.3xDVDD_CORE	V
Output High Level	V_{OH}	I_{OH}=-2mA	0.8x DVDD_CORE			V
Output LOW Level	V_{OL}	I_{OL}=2mA			0.2xDVDD_CORE	V
Input Capacitance	C_{IN}			5		pF
Load Capacitance, X1 and X2	C_L		TBD	TBD	TBD	pF
Internal Pull-Down Resistor	R_{PD}	All clock outputs	75	250		kΩ
Internal Pull-Up Resistor	R_{PU}	All pins with pull-up or pull-down		50		kΩ

Table 172. PLL Section DC Characteristics

9.6. PLL Section AC Timing Specs

Unless stated otherwise, DVDD_Core=1.8V -0.1V/+0.2V, Ambient Temp -10C to +80C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Frequency	f_{IN}		TBD	TBD	TBD	MHz
Output Rise Time	t_{OR}	20% to 80%[1]	1.1	2.2	3.3	ns
Output Fall Time	t_{OF}	80% to 20%[1]	1.1	2.2	3.3	ns
Output Impedance	R_O	VO=VDD/2	33	46	68	W
Output Clock Duty Cycle		VDD/2, 19.2MHz[1]	45	50	55	%
		VDD/2[1]	45	50	55	%
Frequency Synthesis Error		All Outputs		0		ppm
Cycle to cycle Jitter (all outputs)				250	300	ps
Long Term Jitter (all outputs)		n=1000			750	ps
Power Up Time	t_{PU}	From minimum VDD to outputs stable		1.5	4	ms
Output Enable Time					20	ns
Output Disable Time					20	ns

Table 173. PLL Section AC Characteristics

1.Measured with a 5pF load.

9.7. Typical Power Consumption

Mode	AVDD (V)	PVDD (V)	DVDD_IO DVDD_CORE (V)	I_{AVDD} (mA)	I_{PVDD} (mA)	I_{DVDD_IO} (mA)	I_{DVDD_CORE} (mA)	P_{TOTAL} (mW)	Notes
Playback to Headphone only	1.7	3.0	1.7	TBD	TBD	TBD	TBD	4	Full scale 1Vrms/10Kohm, does not include PLL/clock buffer section. fs=48kHz, stereo.
Record only	1.7	3.0	1.7	TBD	TBD	TBD	TBD	TBD	Full scale 500mVrms; does not include PLL/clock buffer section. fs=48kHz, stereo.

Table 174. Typical Power Consumption

9.8. Low Power Mode Power Consumption

Mode	AVDD (V)	PVDD (V)	DVDD_IO DVDD_CORE (V)	I_{AVDD} (mA)	I_{PVDD} (mA)	I_{DVDD_IO} (mA)	I_{DVDD_CORE} (mA)	P_{TOTAL} (mW)	Notes
Record only	1.7	3.0	1.7					TBD	Full scale 500mVrms; does not include PLL/clock buffer section. fs=48kHz, stereo.
Record only	1.7	3.0	1.7					TBD	Full scale 500mVrms; does not include PLL/clock buffer section. fs=8kHz, stereo.

Table 175. Low power mode power consumption

Low Power Settings
1) DAC/ADC modulators set to half rate
2) Constant Output Power function disabled
3) All unused functions disabled (for example, Input PGA, Input mux, and ADC disabled for playback tests)
6) PLL block power consumption not included

10. REGISTER MAP SUMMARY

Register (D15:9)	Name	Remarks	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
Page 0	Reset/Control/Device Setup/PLL/Clocking/ASRC										
R0 (00h)	PAGESEL	Page Select	PAGESEL[7:0]								00h
R1 (01h)	RESET	RESET	RESET[7:0]								77h
R2 (02h)	IRQEN	IRQ Mask	RSVD	THRMINTEN	HBPINTEN	HSDINTEN	HPDINTEN	RSVD	GPIO3INTEN	GPIO2INTEN	00h
R3 (03h)	IRQMASK	IRQ Mask	RSVD	THRMIM	HBPIM	HSDIM	HPDIM	RSVD	GPIO3IM	GPIO2IM	00h
R4 (04h)	IRQSTAT	IRQ Status	RSVD	THRMINT	HBPINT	HSDINT	HPDINT	RSVD	GPIO3INT	GPIO2INT	00
R6(06h)	DEVADD0	Device Address 0	DEV_ADD0[6:0]							RSVD	68h
R8(08h)	DEVID	Device ID 0	DEV_ID[7:0]								40h
R9(09h)	DEVREV	Device Revision	MAJ_REV[3:0]				MIN_REV[3:0]				10h
R10(0Ah)	PLLSTAT	PLL Status	RSVD						PLL2LK	PLL1LK	00h
R11(0Bh)	PLL1CTL	PLL1 Control	VCCI_PLL1[1:0]		RZ_PLL1[2:0]			CP_PLL1[2:0]			93h
R12(0Ch)	PLL1RDIV	PIL1 Ref Divider	REFDIV_PLL1[7:0]								19h
R13(0Dh)	PLL1ODIV	PLL1 Output Divider	OUTDIV_PLL1[7:0]								03h
R14(0Eh)	PLL1FDIVL	PLL1 FBDBK Divider Low	FBDIVL_PLL1[7:0]								80h
R15(0Fh)	PLL1FDIVH	PLL1 FBDBK Divider High	RSVD				FBDIVH_PLL1[3:0]				01h
R16(10h)	PLL2CTL	PLL2 Control	VCCI_PLL2[1:0]		RZ_PLL2[2:0]			CP_PLL2[2:0]			9B
R17(11h)h	PLL2RDIV	PIL2 Ref Divider	REFDIV_PLL2[7:0]								19h
R18(12h)	PLL2ODIV	PLL2 Output Divider	OUTDIV_PLL2[7:0]								05h
R19(13h)	PLL2FDIVL	PLL2 FBDBK Divider Low	FBDIVL_PLL2[7:0]								4Ch
R20(14h)	PLL1FDIVH	PLL2 FBDBK Divider High	RSVD				FBDIVH_PLL2[3:0]				02h
R21(15h)	PLLCTL	PLL Control	PU_PLL2	PU_PLL1	PLL2CLKEN	PLL1CLKEN	BCLKSEL		PLLISEL		00h
R22(16h)	ISRC	Internal Sample rate	RSVD					IBR	IBM[1:0]		12h
R24(18h)	SCLKCTL	System Clock Control	ASDM[1:0]		DSDM[1:0]		RSVD				A0h
R25(19h)	TMBASE	Time Base	TIMEBASE[7:0]								61h
R26(1Ah)	I2SP1CTL	I2S Port 1 Control	BCLK1STAT1	BCLK1P	PORT1MS	LRCLKP1	WL1[1:0]		FORMAT1[1:0]		0Ah
R27(1Bh)	I2SP2CTL	I2S Port 2 Control	BCLK2STAT2	BCLK2P	PORT2MS	LRCLKP2	WL2[1:0]		FORMAT2[1:0]		0Ah
R28(1Ch)	I2SP3CTL	I2S Port 3 Control	BCLK3STAT3	BCLK3P	PORT3MS	LRCLKP3	WL3[1:0]		FORMAT3[1:0]		0Ah
R29(1Dh)	I2S1MRATE	I2S Port 1 Sample Rate	I2S1MCLKHALF	I2S1MCLKDIV[1:0]		I2S1MBR[1:0]		RSVD	I2S1MBM[2:0]		12h
R30(1Eh)	I2S2MRATE	I2S Port 2 Sample Rate	I2S2MCLKHALF	I2S2MCLKDIV[1:0]		I2S2MBR[1:0]		RSVD	I2S2MBM[2:0]		12h
R31(1Fh)	I2S3MRATE	I2S Port 3 Sample Rate	I2S3MCLKHALF	I2S3MCLKDIV[1:0]		I2S3MBR[1:0]		RSVD	I2S3MBM[2:0]		12h
R32(20h)	I2SCMC	I2S Ports Clock Mode	RSVD		BCMP3[1:0]		BCMP2[1:0]		BCMP1[1:0]		12h
R33(21h)	MCLK2PINC	MCLK2 Pin Control	SLEWOUT[3:0]				RSVD	MCLK2IO	MCLK2OS[1:0]		81h
R34(22h)	I2SPINC0	PCM Pin Control 0	SDO3TRI	SDO2TRI	SDO1TRI	RSVD	RSVD	PCM3TRI	PCM2TRI	PCM1TRI	E0h
R35(23h)	I2SPINC1	PCM Pin Control 1	RSVD					SDO3PDD	SDO2PDD	SDO1PDD	00h
R36(24h)	I2SPINC2	PCM Pin Control 2	RSVD		LR3PDD	BC3PDD	LR2PDD	BC2PDD	LR1PDD	BC1PDD	00h
R37(25h)	GPIOCTL0	GPIO Control 0	GPIO3INTP	GPIO2INTP	GPIO3CFG	GPIO2CFG	GPIO3IO	GPIO2IO	GPIO1IO	GPIO0IO	00h
R38(26h)	GPIOCTL1	GPIO Control 1	GPIO3	GPIO2	GPIO1	GPIO0	GPIO3RD	GPIO2RD	GPIO1RD	GPIO0RD	00h
R40(28h)	ASRC	ASRC Control	ASRCOBW	ASRCIBW	ASRCOB						00h
R45(2Dh)	TDMCTL0	TDM Control 0	RSVD					TDMMD	SLSYNC	BDELAY	00h
R46(2Eh)	TDMCTL1	TDM Control 1	RSVD	TDMSO[2:0]		TDMDSS		RSVD	TDMSI[2:0]		21h
R47(2Fh)	PCMP2CTL0	PCM Port 2 Control 0	RSVD					PCMFLENP2	SLSYNCP2	BDELAYP2	00h
R48(30h)	PCMP2CTL1	PCM Port 2 Control 1	RSVD	PCMMOMP2	PCMSOP2	PCMDSSP2[1:0]		RSVD	PCMMIMP2	PCMSIP2	00h

Table 176. Register Map

Register (D15:9)	Name	Remarks	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R49(31h)	PCMP3CTL0	PCM Port 3 Control 0	RSVD					PCMFLENP3	SLSYNCP3	BDELAYP3	00h
R50(32h)	PCMP3CTL1	PCM Port 3 Control 1	RSVD	PCMMOMP3	PCMSOP3	PCMDSSP3[1:0]		RSVD	PCMMIMP3	PCMSIP3	00h
R51(33h)	PWRM0	Power Management 0	RSVD	INPROC3PU	INPROC2PU	INPROC1PU	INPROC0PU	MICB2PU	MICB1PU	MCLKPEN	00h
R52(34h)	PWRM1	Power Management 1	SUBPU	HPLPU	HPRPU	SPKLPU	SPKRPU	D2S2PU	D2S1PU	RSVD	00h
R53(35h)	PWRM2	Power Management 2	RSVD		I2S3OPU	I2S2OPU	I2S1OPU	I2S3IPU	I2S2IPU	I2S1IPU	00h
R54(36h)	PWRM3	Power Management 3	RSVD	BGSBUP	VGBAPU	LLINEPU	RLINEPU	RSVD			00h
R55(37h)	PWRM4	Power Management 4	RSVD			OPEARPU	OPHPLPU	OPHPRPU	OPSPKLPU	OPSPKRPU	00h
R56(38h)	I2SIDCTL	I2S Input Data Control			I2SI3DCTL		I2SI2DCTL		I2SI1DCTL		00h
R57(39h)	I2SODCTL	I2S Output Data Control			I2SO3DCTL		I2SO2DCTL		I2SO1DCTL		00h
R58(3Ah)	AUDIOMUX1		ASRCOMUX		I2S2MUX			I2S1MUX			
R59(3Bh)	AUDIOMUX2		ASRCOMUX		DACMUX			I2S3MUX			
R60(3Ch)	AUDIOMUX3		SUBMUX					CLSSDMUX			
Page 1	Capture/ADC/Input Processing										
R0 (00h)	PAGESEL	Page Select		PAGESEL[7:0]							00h
R1(01h)	HSDCTL1	Headphone/Headset Detection Control 1	HPJKTYPE	CONDETPWD	DETCYC[1:0]		HPDLYBYP	HSDETPOL	HPID_EN	GBLHS_EN	60h
R2(02h)	HSDCTL2	Headphone/Headset Detection Control 2	FMICBIAS1[1:0]		MB1MODE	FORCETRG	SWMODE	GHSHIZ	FPLUGTYPE[1:0]		03h
R3(03h)	HSDSTAT	Headphone/Headset Detection Status	RSVD	MBIAS1DRV[1:0]		RSVD	HSDETSTAT	PLUGTYPE[1:0]		HSDETDONE	06h
R4(04h)	HSDDELAY	Headphone/Headset Detection Delay	RSVD					T_STABLE[2:0]			02h
R5(05h)	BUTCTL	Button Control	BPUSHSTAT	BPUSHDET	BPUSHEN	B_STABLE_L[1:0]		B_STABLE_S[2:0]			00h
R6(06h)	CH0AIC	Ch0 Audio Input Control	INSELL[1:0]		MICBST0[1:0]		LADCIN[1:0]		INHPOR	IPCH0S	00h
R7(07h)	CH1AIC	CH1 Audio Input Control	INSELR[1:0]		MICBST1[1:0]		RADCIN[1:0]		RSVD	IPCH1S	00h
R8(08h)	CH2AIC	CJH2 Audio Input Control	RSVD		MICBST2[1:0]		RSVD				00h
R9(09h)	CH3AIC	CH3 Audio Input Control	RSVD		MICBST3[1:0]		RSVD				00h
R10(0Ah)	ICTL0	Input Control 0	IN1POL	IN0POL	INCH10SEL[1:0]		INMUTE1	INMUTE0	IN1HP	IN0HP	0Ch
R11(0Bh)	ICTL1	Input Control 1	IN3POL	IN2POL	INCH32SEL[1:0]		INMUTE3	INMUTE2	IN3HP	IN2HP	0Ch
R12(0Ch)	MICBIAS	Microphone Bias	MICBOV1[1:0]		MICBOV2[1:0]		RSVD		RSVD		00h
R13(0Dh)	PGACTL0	PGA Control 0	PGA0MUTE	PGA0ZC	PGA0VOL[5:0]						17h
R14(0Eh)	PGACTL1	PGA Control 1	PGA1MUTE	PGA1ZC	PGA1VOL[5:0]						17h
R15(0Fh)	PGACTL2	PGA Control 2	PGA2MUTE	RSVD	PGA2VOL[5:0]						17h
R16(10h)	PGACTL3	PGA Control 3	PGA3MUTE	RSVD	PGA3VOL[5:0]						17h
R17(11h)	PGAZ	PGA Zero Cross	RSVD						INHPOR	TOEN	00h
R18(12h)	ICH0VOL	In Channel 0 Volume	ICH0VOL[7:0]								BFh
R19(13h)	ICH1VOL	In Channel 1 Volume	ICH1VOL[7:0]								BFh
R20(14h)	ICH2VOL	In Channel 2 Volume	ICH2VOL[7:0]								BFh
R21(15h)	ICH3VOL	In Channel 3 Volume	ICH3VOL[7:0]								BFh
R22(16h)	ASRCIL VOL	ASRCI Left Volume	ASRCILVOL[7:0]								EFh
R23(17h)	ASRCR VOL	ASRCI Right Volume	ASRCIRVOL[7:0]								EFh
R24(18h)	ASRCOL VOL	ASRCO Left Volume	ASRCOLVOL[7:0]								EFh
R25(19h)	ASRCOR VOL	ASRCO Right Volume	ASRCORVOL[7:0]								EFh
R26 (1Ah)		RSVD	RSVD								
R27(1Bh)		RSVD	RSVD								BFh
R28(1Ch)	IVOLCTLU	Input Volume Control Update	RSVD				IFADE	INPVOLU	PGAVOLU	ASRCVOLU	08h
R29(1Dh)	ALCCTL0	ALC Control 0	ALCMODE	ALCREF[2:0]			ALCEN3	ALCEN2	ALCEN1	ALCEN0	40h
R30(1Eh)	ALCCTL1	ALC Control 1	RSVD	MAXGAIN[2:0]			ALCL[3:0]				7Bh
R31(1Fh)	ALCCTL2	ALC Control 2	ALCZC	MINGAIN[2:0]			HLD[3:0]				00h
R32(20h)	ALCCTL3	ALC Control 3	DCY[3:0]				ATK[3:0]				32h
R33(21h)	NGATE	Noise Gate	NGTH[4:0]					NGG[1:0]		NGAT	00h
R34(22h)	DMICCTL	D-Mic Control	DMIC2EN	DMIC1EN	RSVD	DMONO	DMDCLK[1:0]		DMRATE[1:0]		00h

Table 176. Register Map

Register (D15:9)	Name	Remarks	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R35-R255	RSVD	Reserved	Reserved								
Page 2	Playback Output Control										
R0(00h)	PAGESEL	Page Select		PAGESEL[7:0]							00h
R1(01h)	DACCTL	DAC Control	DACPOLR	DACPOLL	RSVD		DACMUTE	DACDEM	RSVD	ABYPASS	08h
R2(02h)	SPKRCTL	Speaker Control	SPKPOLR	SPKPOLL	RSVD		SPKMUTE	SPKDEM	RSVD		08h
R3(03h)	SUBCTL	SUB Control	SUBPOL	RSVD			SUBMUTE	SUBDEM	SUBMUX	SUBILIMDIS	08h
R4(04h)	DCCTL	DC Offset Control 1	SUBDCBYP	DACDCBYP	SPKDCVBYP	RSVD		DCCOEFSEL[2:0]			05h
R5(05h)	RSVD	Reserved	RSVD								00h
R6(06h)	OVOLCTLU	Output Volume Control Update	RSVD			OFADE	SUBVOLU	MVOLU	SPKVOLU	HPVOLU	08h
R7(07h)	MUTEC	Mute Control	ZDSTAT	RSVD	ZDLEN[1:0]		RSVD	AMUTE	RSVD		22h
R8(08h)	MVOLL	Master Volume Left	MVOL_L(7:0)								FFh
R9(09h)	MVOLR	Master Volume Right	MVOL_R(70)								FFh
R10(0Ah)	HPVOLL	HP Volume Left	RSVD	HPVOL_L(6:0)							77h
R11(0Bh)	HPLOLR	HP Volume Right	RSVD	HPVOL_R(6:0)							77h
R12(0Ch)	SPKVOLL	Speaker Volume Left	RSVD	SPKVOL_L(6:0)							6Fh
R13(0Dh)	SPKVOLR	Speaker Volume Right	RSVD	SPKVOL_R(6:0)							6Fh
R14(0Eh)	RSVD	Reserved	RSVD								00h
R15(0Fh)	RSVD	Reserved	RSVD								00h
R16(10h)	SUBVOL	SUB Volume	RSVD	SUBVOL(6:0)							6Fh
R17(11h)	COP0	Constant Output Power 0	COPATTEN	COPGAIN	HDELTAEN	COPTARGETt[4:0]					08h
R18(12h)	COP1	Constant Output Power 1	RSVD	HDCOMPMODE	AVGLENGTH[3:0]				MONRATE[1:0]		02h
R19 (13h)	COPSTAT	Constant Output Power Status	HDELTADET	UV	COPADJ[5:0						00h
R20 (14h)	PWM0	PWM Control 0	SCTO[1:0]		UVLO	ROUNDUP	BFDIS	BFORDER	NSSEL	QUANTSEL	D4h
R21 (15h)	PWM1	PWM Control 1	RSVD	DITHPOS[4:0]					DITHRNG	DITHDIS	00h
R22 (16h)	PWM2	PWM Control 2	DVALUE{5:0]						RSVD	PWMMODE	61h
R23(17h)	PWM3	PWM Control 3	PWMMUX[1:0]		CVALUE[5:0]						0Ah
R24(18h)	HPSW	Headphone Switch	RSVD					HPSWEN	HPSWPOL	TSDEN	00h
R25(19h)	THERMTS	Temp Sensor Control	TRIPHS	TRIPLS	TRIPSPLIT[1:0]		TRIPSHIFT[1:0]		TSPOLL[1:0]		09h
R26(1Ah)	THERMSPK1	Speaker Thermal Algorithm Control	FORCEPWD	INSTCUTMODE	INCRATIO[1:0]		INCSTEP[1:0]		DECSTEP[1:0]		81h
R27(1Bh)	THERMTS	Thermal Status	FPWDS	VOLSTAT[6:0]							08h
R28(1Ch)	SCSTAT	Short Circuit Status	RSVD			ESDF[1:0]		CPF	CLSDF[:1:0]		00h
R29(1Dh)	SDMON	Supply Monitoring	SDFORCE	RSVD		SDVALUE[4:0]					00h
R30-R255	RSVD	Reserved	Reserved								
Page 3	Speaker Output Processing										
R0(00h)	PAGESEL	Page Select		PAGESEL[7:0]							00h
R1(01h)	SPKEQFILT	SPK Eq Filter Control	EQ2EN	EQ2BE[2:0]			EQ1EN	EQ1BE{2:0]			00h
R2(02h)	SPKCRWDL	SPK Coeff Write Data L	WDATA_L[7:0]								00h
R3(03h)	SPKCRDWM	SPK Coeff Write Data M	WDATA_M[15:8]								00h
R4(04)	SPKCRWDH	SPK Coeff Write Data H	WDATA_H[23:16]								00h
R5(05h)	SPKCRRDL	SPK CoefF Read Data L	RDATA_L[7:0]								00h
R6(06h)	SPKCRRDM	SPKBCoefF Read Data M	RDATA_M[15:8]								00h
R7(07h)	SPKCRRDH	SPK CoefF Read Data H	RDATA_H[23:16]								00h
R8(08h)	SPKCRADD	SPK Coeff RAM Address	ADDRESS[7:0]								00h
R9(09h)	SPKCRS	SPK Coeff RAM Status	SPKCOEFR	RSVD							00h
R10(0Ah)	SPKMBCEN	SPK Multi-band Comp En	RSVD					MBCPEN3	SMBCPEN2	MBCPEN1	00h
R11(0Bh)	SPKMBCCTL	SPK Multi-band Comp CTL	RSVD		LVLMODE3	WINSEL3	LVLMODE2	WINSEL2	LVLMODE1	WINSEL1	00h
R12(0Ch)	SPKMBCMUG1	SPK Multi-band Compressor Make Up Gain Band 1	RSVD		PHASE	MUGAIN[4:0]					00h

Table 176. Register Map

Register (D15:9)	Name	Remarks	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R13(0Dh)	SPKMBCTHR1	SPK Multi-band Compressor Threshold Band 1	THRESH[7:0]								00h
R14(0Eh)	SPKMBCRAT1‘	SPK Multi-band Compressor Ratio Band 1	RSVD			RATIO1[4:0]					00h
R15(0Fh)	SPKMBCATK1L	SPK Multi-band Comp Attack time const Low Band 1	TCATKL[7:0]								00h
R16(10h)	SPKMBCATK1H	SPK Multi-band Comp Attack time const High Band 1	TCATKH1[7:0]								00h
R17(11h)	SPKMBCREL1L	SPK Multi-band Comp release time const Low Band 1	TCRELL[7:0]								00h
R18(12h)	SPKMBCREL1H	SPK Multi-band Comp release time const High Band 1	TCRELH[7:0]								00h
R19(13h)	SPKMBCMUG2	SPK Multi-band Compressor Make Up Gain Band 2	RSVD		PHASE	MUGAIN[4:0]					00h
R20(14h)	SPKMBCTHR2	SPK Multi-band Compressor Threshold Band 2	THRESH[7:0]								00h
R21(15h)	SPKMBCRAT2‘	SPK Multi-band Compressor Ratio Band 2	RSVD			RATIO1[4:0]					00h
R22(16h)	SPKMBCATK2L	SPK Multi-band Comp Attack time const Low Band 2	TCATKL[7:0]								00h
R23(17h)	SPKMBCATK2H	SPK Multi-band Comp Attack time const High Band 2	TCATKH1[7:0]								00h
R24(18h)	SPKMBCREL2L	SPK Multi-band Comp release time const Low Band 2	TCRELL[7:0]								00h
R25(19h)	SPKMBCREL32H	SPK Multi-band Comp release time const High Band 2	TCRELH[7:0]								00h
R26(1Ah)	SPKMBCMUG3	SPK Multi-band Compressor Make Up Gain Band 3	RSVD		PHASE	MUGAIN[4:0]					00h
R27(1Bh)	SPKMBCTHR3	SPK Multi-band Compressor Threshold Band 3	THRESH[7:0]								00h
R28(1Ch)	SPKMBCRAT3	SPK Multi-band Compressor Ratio Band 3	RSVD			RATIO1[4:0]					00h
R29(1Dh)	SPKMBCATK3L	SPK Multi-band Comp Attack time const Low Band 3	TCATKL[7:0]								00h
R30(11h)	SPKMBCATK3H	SPK Multi-band Comp Attack time const High Band 3	TCATKH1[7:0]								00h
R31(1Eh)	SPKMBCREL3L	SPK Multi-band Comp release time const Low Band 3	TCRELL[7:0]								00h
R32(20h)	SPKMBCREL3H	SPK Multi-band Comp release time const High Band 3	TCRELH[7:0]								00h
R33(21h)	SPKCLECTL	SPK Comp Limiter CTL	RSVD			LVLMODE	WINSEL	EXPEN	LIMIEN	COMPEN	00h
R34(22h)	SPKCLEMUG	SPK Compressor Make Up Gain	RSVD			MUGAIN[4:0]					00h
R35(23h)	SPKCOMPTHR	SPK Compressor Threshold	THRESH[7:0]								00h
R36(24h)	SPKCOMPRAT	SPK Compressor Ratio	RSVD			RATIO1[4:0]					00h
R37(25h)	SPKCOMPATKL	SPK Comp Attack time const Low	TCATKL[7:0]								00h
R38(26h)	SPKCOMATKH	SPK Comp Attack time const High	TCATKH1[7:0]								00h
R39(27h)	SPKCOMPRELL	SPK Comp release time const Low	TCRELL[7:0]								00h
R40(28h)	SPKCOMPRELH	SPK Comp release time const High	TCRELH[7:0]								00h
R41(29h)	SPKLIMTHR	SPK Limiter Threshold	THRESH[7:0]								00h
R42(2Ah)	SPKLIMTGT	SPK Limiter Target	TARGET[7:0]								00h
R43(2Bh)	SPKLIMATKL	SPK Limiter Attack time constant Low	TCATKLL[7:0]								00h
R44(2Ch)	SPKLIMATKH	SPK Limiter Attack time constant High	TCATKH[7:0]								00h

Table 176. Register Map

Register (D15:9)	Name	Remarks	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R45(2Dh)	SPKLIMRELL	SPK Limiter Release time constant Low	TCRELL[7:0]								00h
R46(2Eh)	SPKLIMRELH	SPK Limiter Release time constant High	TCRELH[7:0]								00h
R47(2Fh)	SPKEXPTHR	SPK Expander Threshold	THRESH[7:0]								00h
R48(30h)	SPKEXPRAT	SPK Expander Ratio	RATIO[7:0]								00h
R49(31h)	SPKEXPATKL	SPK Expander Attack time constant Low	TCATKL[7:0]								00h
R50(32h)	SPKEXPATKH	SPK Expander Attack time constant High	TCATKH[7:0]								00h
R51(33h)	SPKEXPRELL	SPK Expander Release time constant Low	TCRELL[7:0]								00h
R52(34h)	SPKEXPRELH	SPK Expander Release time constant High	TCRELH[7:0]								00h
R53(35h)	SPKFXCTL	SPK Effects Control	RSVD			3DEN	TBEN	TNLFBYP	BEEN	BNLFBYP	00h
R54-R255	RSVD	Reserved	RSVD								
Page 4	DAC/Headphone Output Processing										
R0(00h)	PAGESEL	Page Select		PAGESEL[7:0]							00h
R1(01h)	DACEQFILT	DAC Eq Filter Control	EQ2EN	EQ2BE[2:0]			EQ1EN	EQ1BE{2:0]			00h
R2(02h)	DACCRWDL	DAC Coeff Write Data L	WDATA_L[7:0]								00h
R3(03h)	DACCRWDM	DAC Coeff Write Data M	WDATA_M[15:8]								00h
R4(04)	DACCRWDH	DAC Coeff Write Data H	WDATA_H[23:16]								00h
R5(05h)	DACCRRDL	DAC CoefF Read Data L	RDATA_L[7:0]								00h
R6(06h)	DACCRRDM	DAC CoefF Read Data M	RDATA_M[15:8]								00h
R7(07h)	DACCRRDH	DAC CoefF Read Data H	RDATA_H[23:16]								00h
R8(08h)	DACCRADD	DAC Coeff RAM Address	ADDRESS[7:0]								00h
R9(09h)	DACCRS	DAC Coeff RAM Status	SPKCOEFR	RSVD							00h
R10(0Ah)	DACMBCEN	DAC Multi-band Comp En	RSVD					MBCPEN3	SMBCPEN2	MBCPEN1	00h
R11(0Bh)	DACMBCCTL	DAC Multi-band Comp CT2	RSVD		LVLMODE3	WINSEL3	LVLMODE2	WINSEL2	LVLMODE1	WINSEL1	00h
R12(0Ch)	DACMBCMUG 1	DAC Multi-band Compressor Make Up Gain Band 1	RSVD		PHASE	MUGAIN[4:0]					00h
R13(0Dh)	DACMBCTHR1	DAC Multi-band Compressor Threshold Band 1	THRESH[7:0]								00h
R14(0Eh)	DACMBCRAT1	DAC Multi-band Compressor Ratio Band 1	RSVD			RATIO1[4:0]					00h
R15(0Fh)	DACMBCATK1 L	DAC Multi-band Comp Attack time const Low Band 1	TCATKL[7:0]								00h
R16(10h)	DACMBCATK1 H	DAC Multi-band Comp Attack time const High Band 1	TCATKH1[7:0]								00h
R17(11h)	DACMBCREL1 L	DAC Multi-band Comp release time const Low Band 1	TCRELL[7:0]								00h
R18(12h)	DACMBCREL1 H	DAC Multi-band Comp release time const High Band 1	TCRELH[7:0]								00h
R19(13h)	DACMBCMUG 2	DAC Multi-band Compressor Make Up Gain Band 2	RSVD		PHASE	MUGAIN[4:0]					00h
R20(14h)	DACMBCTHR2	DAC Multi-band Compressor Threshold Band 2	THRESH[7:0]								00h
R21(15h)	DACMBCPAT2'	DAC Multi-band Compressor Ratio Band 2	RSVD			RATIO1[4:0]					00h
R22(16h)	DACMBCATK2 L	DAC Multi-band Comp Attack time const Low Band 2	TCATKL[7:0]								00h
R23(17h)	DACMBCATK2 H	DAC Multi-band Comp Attack time const High Band 2	TCATKH1[7:0]								00h
R24(18h)	DACMBCREL2 L	DAC Multi-band Comp release time const Low Band 2	TCRELL[7:0]								00h
R25(19h)	DACMBCREL3 H	DAC Multi-band Comp release time const High Band 2	TCRELH[7:0]								00h

Table 176. Register Map

Register (D15:9)	Name	Remarks	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R26(1Ah)	DACMBCMUG3	DAC Multi-band Compressor Make Up Gain Band 3	RSVD		PHASE	MUGAIN[4:0]					00h
R27(1Bh)	DACMBCTHR3	DAC Multi-band Compressor Threshold Band 3	THRESH[7:0]								00h
R28(1Ch)	DACMBCRAT3	DAC Multi-band Compressor Ratio Band 3	RSVD			RATIO1[4:0]					00h
R29(1Dh)	DACMBCATK3L	DAC Multi-band Comp Attack time const Low Band 3	TCATKL[7:0]								00h
R30(1Eh)	DACMBCATK3H	DAC Multi-band Comp Attack time const High Band 3	TCATKH1[7:0]								00h
R31(1Eh)	DACMBCREL3L	DAC Multi-band Comp release time const Low Band 3	TCRELL[7:0]								00h
R32(20h)	DACMBCREL3H	DAC Multi-band Comp release time const High Band 3	TCRELH[7:0]								00h
R33(21h)	DACCLECTL	DAC Comp Limiter CTL	RSVD			LVLMODE	WINSEL	EXPEN	LIMIEN	COMPEN	00h
R34(22h)	DACCLEMUG	DAC Compressor Make Up Gain	RSVD			MUGAIN[4:0]					00h
R35(23h)	DACCOMPTHR	DAC Compressor Threshold	THRESH[7:0]								00h
R36(24h)	DACCOMPRAT	DAC Compressor Ratio	RSVD			RATIO1[4:0]					00h
R37(25h)	DACCOMPATKL	DAC Comp Attack time const Low	TCATKL[7:0]								00h
R38(26h)	DACCOMPATKH	DAC Comp Attack time const High	TCATKH1[7:0]								00h
R39(27h)	DACCOMPRELL	DAC Comp release time const Low	TCRELL[7:0]								00h
R40(28h)	DACCMPRELH	DAC Comp release time const High	TCRELH[7:0]								00h
R41(29h)	DACLIMTHR	DAC Limiter Threshold	THRESH[7:0]								00h
R42(2Ah)	DACLIMTGT	DAC Limiter Target	TARGET[7:0]								00h
R43(2Bh)	DACLIMATKL	DAC Limiter Attack time constant Low	TCATKLL[7:0]								00h
R44(2Ch)	DACLIMATKH	DAC Limiter Attack time constant High	TCATKH[7:0]								00h
R45(2Dh)	DACLIMRELL	DAC Limiter Release time constant Low	TCRELL[7:0]								00h
R46(2Eh)	DACLIMRELH	DAC Limiter Release time constant High	TCRELH[7:0]								00h
R47(2Fh)	DACEXPTHR	DAC Expander Threshold	THRESH[7:0]								00h
R48(30h)	DACEXPRAT	DAC Expander Ratio	RATIO[7:0]								00h
R49(31h)	DACEXPATKL	DAC Expander Attack time constant Low	TCATKL[7:0]								00h
R50(32h)	DACEXPATKH	DAC Expander Attack time constant High	TCATKH[7:0]								00h
R51(34h)	DACEXPRELL	DAC Expander Release time constant Low	TCRELL[7:0]								00h
R52(34h)	DACEXPRELH	DAC Expander Release time constant High	TCRELH[7:0]								00h
R53(35h)	DACFXCTL	DAC Effects Control	RSVD			3DEN	TBEN	TNLFBYP	BEEN	BNLFBYP	00h
Page 5	SUB Output Processing										
R0(00h)	PAGESEL	Page Select		PAGESEL[7:0]							00h
R1(01h)	SUBEQFILT	SUB Eq Filter Control	EQ2EN	EQ2BE[2:0]			EQ1EN	EQ1BE{2:0]			00h
R2(02h)	SUBCRWDL	SUB Coeff Write Data L	WDATA_L[7:0]								00h
R3(03h)	SUBCRWDM	SUB Coeff Write Data M	WDATA_M[15:8]								00h
R4(04)	SUBCRWDH	SUB Coeff Write Data H	WDATA_H[23:16]								00h
R5(05h)	SUBCRRDL	SUB CoefF Read Data L	RDATA_L[7:0]								00h
R6(06h)	SUBCRRDM	SUB CoefF Read Data M	RDATA_M[15:8]								00h
R7(07h)	SUBCRRDH	SUB CoefF Read Data H	RDATA_H[23:16]								00h

Table 176. Register Map

Register (D15:9)	Name	Remarks	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R8(08h)	SUBCRADD	SUB Coeff RAM Address	ADDRESS[7:0]								00h
R9(09h)	SUBCRS	SUB Coeff RAM Status	SPKCOEFR	RSVD							00h
R10(0Ah)	SUBMBCEN	SUB Multi-band Comp En	RSVD					MBCPEN3	SMBCPEN2	MBCPEN1	00h
R11(0Bh)	SUBMBCCTL	SUB Multi-band Comp CTL	RSVD		LVLMODE3	WINSEL3	LVLMODE2	WINSEL2	LVLMODE1	WINSEL1	00h
R12(0Ch)	SUBMBCMUG 1	SUB Multi-band Compressor Make Up Gain Band 1	RSVD		PHASE	SUBMBCPG1[4:0]					00h
R13(0Dh)	SUBMBCTHR1	SUB Multi-band Compressor Threshold Band 1	THRESH[7:0]								00h
R14(0Eh)	SUBMBCRAT1'	SUB Multi-band Compressor Ratio Band 1	RSVD			RATIO1[4:0]					00h
R15(0Fh)	SUBMBCATK1 L	SUB Multi-band Comp Attack time const Low Band 1	TCATKL[7:0]								00h
R16(10h)	SUBMBCATK1 H	SUB Multi-band Comp Attack time const High Band 1	TCATKH1[7:0]								00h
R17(11h)	SUBMBCREL1 L	SUB Multi-band Comp release time const Low Band 1	TCRELL[7:0]								00h
R18(12h)	SUBMBCREL1 H	SUB Multi-band Comp release time const High Band 1	TCRELH[7:0]								00h
R19(13h)	SUBMBCUMG 2	SUB Multi-band Compressor Make Up Gain Band 2	RSVD		PHASE	MUGAIN[4:0]					00h
R20(14h)	SUBMBCTHR2	SUB Multi-band Compressor Threshold Band 2	THRESH[7:0]								00h
R21(15h)	SUBMBCRAT2'	SUB Multi-band Compressor Ratio Band 2	RSVD			RATIO1[4:0]					00h
R22(16h)	SUBMBCATK2 L	SUB Multi-band Comp Attack time const Low Band 2	TCATKL[7:0]								00h
R23(17h)	SUBMBCATK2 H	SUB Multi-band Comp Attack time const High Band 2	TCATKH1[7:0]								00h
R24(18h)	SUBMBCREL2 L	SUB Multi-band Comp release time const Low Band 2	TCRELL[7:0]								00h
R25(19h)	SUBMBCREL2 H	SUB Multi-band Comp release time const High Band 2	TCRELH[7:0]								00h
R26(1Ah)	SUBMBCMUG 3	SUB Multi-band Compressor Make Up Gain Band 3	RSVD		PHASE	MUGAIN[4:0]					00h
R27(1Bh)	SUBMBCTHR3	SUB Multi-band Compressor Threshold Band 3	THRESH[7:0]								00h
R28(1Ch)	SUBMBCRAT3	SUB Multi-band Compressor Ratio Band 3	RSVD			RATIO1[4:0]					00h
R29(1Dh)	SUBMBCATK3 L	SUB Multi-band Comp Attack time const Low Band 3	TCATKL[7:0]								00h
R30(1Eh)	SUBMBCATK3 H	SUB Multi-band Comp Attack time const High Band 3	TCATKH1[7:0]								00h
R31(1Eh)	SUBMBCREL3 L	SUB Multi-band Comp release time const Low Band 3	TCRELL[7:0]								00h
R32(20h)	SUBMBCREL3 H	SUB Multi-band Comp release time const High Band 3	TCRELH[7:0]								00h
R33(21h)	SUBCLECTL	SUB Comp Limiter CTL	RSVD			LVLMODE	WINSEL	EXPEN	LIMIEN	COMPEN	00h
R34(22h)	SUBCLEMUG	SUB Compressor Make Up Gain	RSVD			MUGAIN[4:0]					00h
R35(23h)	SUBCOMPTH R	SUB Compressor Threshold	THRESH[7:0]								00h
R36(24h)	SUBCOMPRAT	SUB Compressor Ratio	RSVD			RATIO1[4:0]					00h
R37(25h)	SUBCOMPATK L	SUB Comp Attack time const Low	TCATKL[7:0]								00h
R38(26h)	SUBCOMPATK H	SUB Comp Attack time const High	TCATKH1[7:0]								00h
R39(27h)	SUBCOMPREL L	SUB Comp release time const Low	TCRELL[7:0]								00h
R40(28h)	SUBCOMPREL H	SUB Comp release time const High	TCRELH[7:0]								00h

Table 176. Register Map

Register (D15:9)	Name	Remarks	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R41(29h)	SUBLIMTHR	SUB Limiter Threshold	THRESH[7:0]								00h
R42(2Ah)	SUBLIMTGT	SUB Limiter Target	TARGET[7:0]								00h
R43(2Bh)	SUBLIMATKL	SUB Limiter Attack time constant Low	TCATKLL[7:0]								00h
R44(2Ch)	SUBLIMATKH	SUB Limiter Attack time constant High	TCATKH[7:0]								00h
R45(2Dh)	SUBLIMRELL	SUB Limiter Release time constant Low	TCRELL[7:0]								00h
R46(2Eh)	SUBLIMRELH	SUB Limiter Release time constant High	TCRELH[7:0]								00h
R47(2Fh)	SUBEXPTH	SUB Expander Threshold	THRESH[7:0]								00h
R48(30h)	SUBSUBEXPRAT	SUB Expander Ratio	RATIO[7:0]								00h
R49(31h)	SUBEXPATKL	SUB Expander Attack time constant Low	TCATKL[7:0]								00h
R50(32h)	SUBEXPATKH	SUB Expander Attack time constant High	TCATKH[7:0]								00h
R51(33h)	SUBEXPRELL	SUB Expander Release time constant Low	TCRELL[7:0]								00h
R52(34h)	SUBEXPRELH	SUB Expander Release time constant High	TCRELH[7:0]								00h
R53(35h)	SUBFXCTL	SUB Effects Control	RSVD				TBEN	TNLFBYP	BEEN	BNLFBYP	00h
R534-R255	RSVD	Reserved	RSVD								00h
Page 10	Reserved For Future Use										
R1(01h)	ASRCCAPT	ASRC Input/Output Ratio	SEL								
R2(02h)	ASRCRATIO1		INT								
R3(03h)	ASRCRATIO2		FRACH								
R4(04h)	ASRCRATIO3		FRACM								
R5(05h)	ASRCRATIO4		FRACL								
R6(10h)	DTEST0		DTEST0								
R7(12h)	DTEST1		DTEST1								
R8(13h)	DTEST2										
R9(14h)	DTEST3										
R10(15h)	DTEST4										
R11(16h)	DTEST5		DTEST5								
R12(40h)	ATEST0		ATEST0								
R13(41h)	ATEST1		ATEST1								
R14(42h)	ATEST2		ATEST2								
R15(43h)	ATEST3		ATEST3								
R16(44h)	ATEST4		ATEST4								
R17(45h)	ATEST5		ATEST5								
R18(46h)	ATEST6		ATEST6								
R19(47h)	ATEST7										
R20(48h)	ATEST8		ATEST8								
R21(49h)	ATEST9		ATEST9								
R22(4Ah)	ATEST10		ATEST10								
R23(4Bh)	ATEST11		ATEST11								
R24(4Eh)	ATEST12		ATEST12								
R25(4Fh)	ATEST13		ATEST13								
R26(50h)	ATEST14		ATEST14								
R27(51h)	ATEST15		ATEST15								
R28(52h)	ATEST16		ATEST16								
R29(53h)	ATEST17										

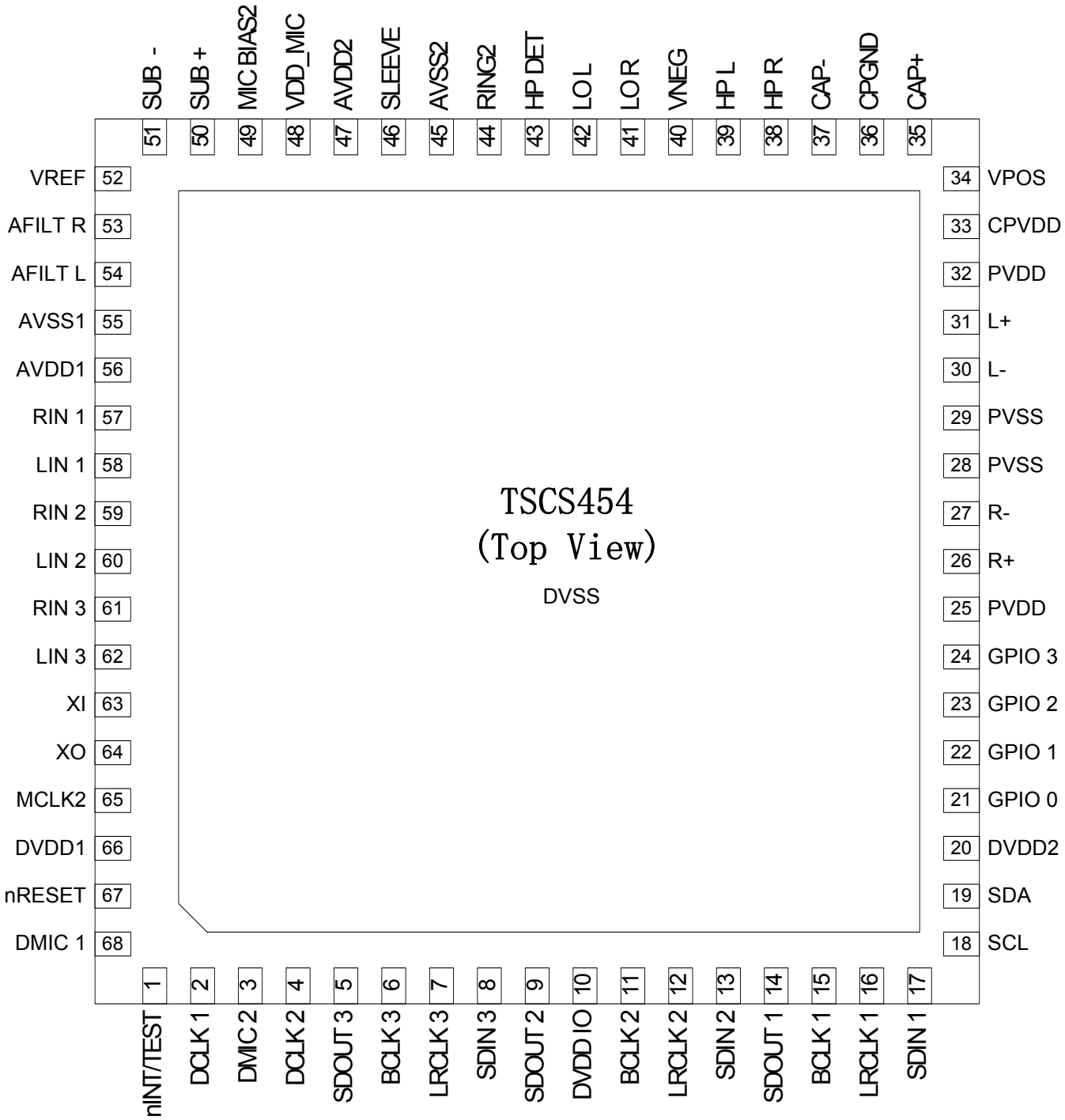
Table 176. Register Map

Register (D15:9)	Name	Remarks	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R30(54h)	ATEST18		ATEST18								
R31(55h)	ATEST19		ATEST19								
R32(56h)	ATEST20		ATEST20								
R33(57h)	ATEST21		ATEST21								
R34(58h)	ATEST22										
R35(59h)	ATEST23		ATEST23								
R36(5Ah)	ATEST24										
R37(5Bh)	ATEST25										
R38(5Ch)	ATEST26										
R39(5Dh)	ATEST27	ATEST27	ATEST27								
R40(5Eh)	ATEST28		ATEST28								
R41(5Fh)	ATEST29		ATEST29								
R42(60h)	ATEST30		ATEST30								
R43(61h)	ATEST31										
R44(62h)	ATEST32										
R45(63h)	ATEST33										
R46(64h)	ATEST34										
R47(80h)	BISTCTL										
R48(84h)	BIST1CFG0										
R49(89h)	BIST2CFG0										
R50(90h)	BIST1STAT		DONE	ACTIVE		RAM					
R51(94h)	BIST1FADDR0		ADDR0								
R52(95h)	BIST1FADDR1		ADDR1								
R53(98h)	BIST1FDATA0		BYTE0								
R54(99h)	BIST1FDATA1		BYTE1								
R55(9Ah)	BIST1FDATA2		BYTE2								
R56(9Bh)	BIST1FDATA3		BYTE3								
R57(A0h)	BIST2STAT		DONE	ACTIVE		RAM					
R58(A4h)	BIST2FADDR0		ADDR0								
R59(A5h)	BIST2FADDR1		ADDR1								
R60(A8h)	BIST2FDATA0		BYTE0								
A61(A9h)	BIST2FDATA1		BYTE1								
A61(AAh)	BIST2FDATA2		BYTE2								
A62(01h)	BONDOVER										
A63(02h)	FIPMUTE				FIPMUTE2			FIPMUTE1	FIPMUTE0		

Table 176. Register Map

11. PIN CONFIGURATION AND DESCRIPTION

11.1. 68-Pin QFN



11.2. PIN TABLE

11.2.1. POWER PIN

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down
PVDD1-3	BTL supply/Mic Bias Supply	I(Power)	-
PVSS1-3	BTL supply	I(Power)	-
DVDD_Core	Core logic+clocks	I(Power)	-
DVDD_IO	Interface (I2S, I2C, GPIO)	I(Power)	-
DVSS	Digital return	I(Power)	-
AVDD1-2	Analog core supply	I(Power)	-
AVDD_IO	Analog Power IO	I(Power)	-
AVSS1-2	Analog return	I(Power)	-
CPVDD	Charge pump supply	I(Power)	-
CPGND	Charge pump return	I(Power)	-
CAP+	Flying cap	I/O(Power)	-
(CAP-)1-2	Flying cap	I/O(Power)	-
V+	Positive Analog supply (Bypass cap)	O(Power)	-
(V-)	Negative Analog supply (Bypass cap)	O(Power)	-

Table 177. PowerPin

11.2.2. REFERENCE

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down
MICBIAS1	2.5V 1.5 mA microphone Bias Output 1	O(Analog)	None
MICBIAS2	2.5V 1.5 mA microphone Bias Output2	O(Analog)	None
AFILT1	ADC Input Filter cap	I(Analog)	None
AFILT2	ADC Input Filter cap	I(Analog)	None
VREF	VREF reference pin (bypass)	I(Analog)	None

Table 178. Referece Pin

11.2.3. ANALOG INPUT

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down
LIN1	Analog Audio Left Line/Mic Input 1	I(Analog)	None
RIN1	Analog Audio Right Line/Mic Input 1	I(Analog)	None
LIN2	Analog Audio Left Line/Mic Input 2	I(Analog)	None
RIN2	Analog Audio Right Line/Mic Input 2	I(Analog)	None
LIN3	Analog Audio Left Line/Mic Input 3	I(Analog)/	None
RIN3	Analog Audio Right Line/Mic Input 3	I(Analog)	None

Table 179. Analog Input Pin

11.2.4. ANALOG OUTPUT

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down
HPL	Audio Headphone Output Left - ground referenced	O(Analog)	None
HPR	Audio Headphone Output Right - ground referenced	O(Analog)	None
EAR+	BTL Subwoofer positive output	O(Analog)	None
EAR-	BTL Subwoofer negative output	O(Analog)	None
LINEOUTL	Audio Line Output Left - signal is a buffered version of Headphone Output Left	O(Analog)	None
LINEOUTR	Audio Line Output Right- signal is a buffered version of Headphone Output Right	O(Analog)	None
M_DET	Microphone Detect	I(Analog)	None

Table 180. Analog Output Pin

11.2.5. DATA and CONTROL

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down
BCLK1	I2S Bit Clock 1	I/O(Digital)	Pull-Down
LRCLK1	I2S Framing Clock 1	I/O(Digital)	Pull-Down
SDIN1	I2S Input Data 1	I(Digital)	Pull-Down
BCLK2	I2S Bit Clock 2	I/O(Digital)	Pull-Down
LRCLK2	I2S Framing Clock 2	I/O(Digital)	Pull-Down
SDIN2	I2S input Data 2	I(Digital)	Pull-Down
BCLK3	I2S Bit Clock 3	I/O(Digital)	Pull-Down
LRCLK3	I2S Framing Clock 3	I/O(Digital)	Pull-Down
SDIN3	I2S Input data 3	I(Digital)	Pull-Down
SDOUT1	I2S Output Data 1	O(Digital)	Pull-Down
SDOUT2	I2S Output Data 2	O(Digital)	Pull-Down
SDOUT3	I2S Output Data 3	O(Digital)	Pull-Down

Table 181. Data And Control Pin

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down
SCL	I2C shift clock for serial control port	I(Digital)	Pull-Up
SDA	I2C shift data for serial control port	I/O(Digital)	Pull-Up
DCLK1	Digital MIC Clock 1 clock output for digital MIC 1	ODigital)	Pull-Down
DCLK2	Digital MIC Clock 2 clock output for Digital MIC 2	O(Digital)	Pull-Down
DMIC1	Digital MIC Data Input 1 data input for Digital MIC 1	I(Digital)	Pull-Down
DMIC2	Digital MIC Data Input 2 data input for Digital MIC 2	I(Digital)	Pull-Down
GPIO0	General Purpose I/O	I/O(Digital)	Pull-Up
GPIO1	General Purpose I/O	I/O(Digital)	Pull-Up
GPIO2	General Purpose I/O	I/O(Digital)	Pull-Up
GPIO3	General Purpose I/O	I/O(Digital)	Pull-Up
BOOT	Boot Mode input 0 = boot from I2C 1 = Reserved	IDigital)	Pull-Down
nINT/nTEST	Interrupt /Test Pin (Input/Output) Open collector output driven low when an interrupt has been generated.	I/O(Digital)	Pull-Up
HP_DET	Headphone jack detection (Input)	I(Digital)	Pull-Up
M_DET	Microphone Detect		
nRESET	RESET (Input) The device is put into a low power state when this pin is driven low	IDigital)	Pull-Down

Table 181. Data And Control Pin

11.2.6. PLL SECTION

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down
XTAL_IN/MCLK	XTAL/MCLK1 (Input) Clock input connection to Crystal Oscillator or Digital Clock source	I(XTAL)	None
XTAL_OUT	XTA_OUTL (Input) Clock input connection to Crystal Oscillator	O(XTAL)	None
MCLKIO	MCLK (Output)/MCLK2 (Input) High frequency output clock	O(XTAL)	None

Table 182. PLL Pin

12. TSCS454XXPACKAGE INFORMATION

12.1. 68-Pin QFN Package Drawing

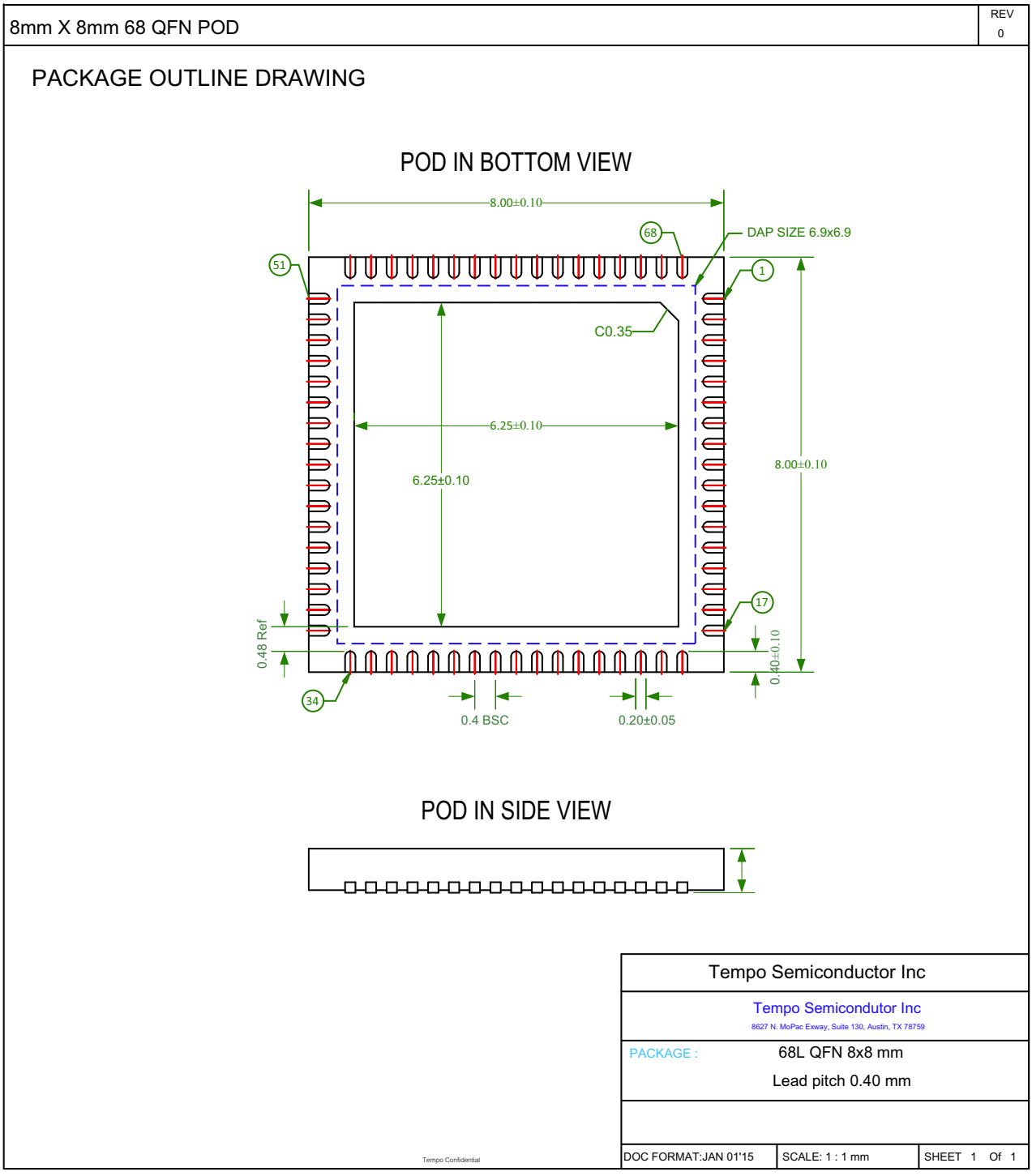


Figure 43. 68-Pin QFN Package Drawing

13. ORDERING INFORMATION

TSCS454XX1NTGXyyX	68 pin QFN package

yy is the silicon revision, Contact TSI Sales to get the current revision.

Add an 8 to the end of the part number for Tape And Reel delivery.

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