



# DATASHEET

## PORTABLE CONSUMER CODEC CLASS-H DIRECTCONNECT™ HEADPHONE AMPLIFIER

## TSDP11xx / TSDP10xx

### DESCRIPTION

The TSDP11xx and TSDP10xx devices are Class-H architecture Capless DirectConnect Ground-Referenced Output Headphone stereo amplifiers with GPIO shutdown control. The TSDP11xx provides independent left / right channel volume control, mute and fine parameter adjustment via the two-wire I2C compatible serial interface. Both provide high-quality audio fidelity with an SNR / DNR of up to 106dB, a THD+N as low as -85dB, an output power of up to 170mW per channel into 16Ω or up to 2Vrms into a 10KΩ. The differential inputs allow for flexible input configuration that maximizes noise rejection for best-in-class CMRR that exceeds the competition by up to 21dB.

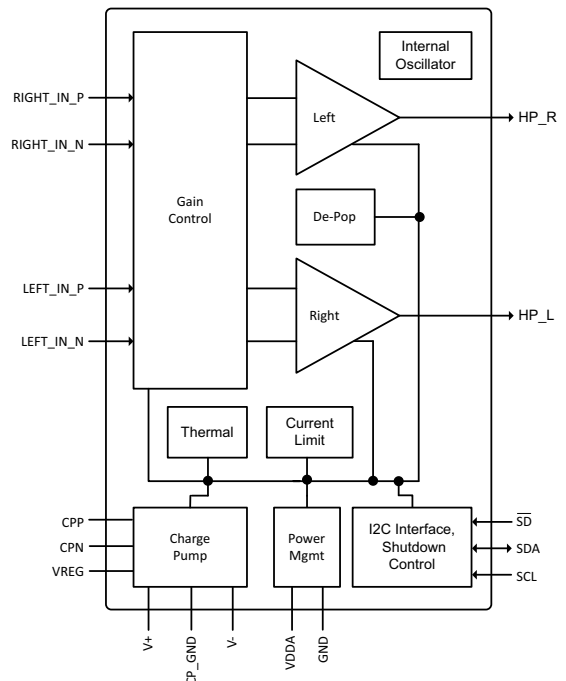
### TARGET APPLICATIONS

- **Gaming-Class Motherboards**
- **Tablet Computers**
- **Gaming-class Laptops**
- **Portable Gaming Platforms**
- **Digital Audio Streaming / Connected Audio Accessories**
- **Bluetooth™-enabled Headphones / Headsets / Docking Stations / Adapters**
- **Wi-Fi (Miracast, Chromecast, AirPlay 2®)-enabled Headphones / Headsets**
- **Lightning-enabled Headphones / Headsets / Docking Stations / Adapters**
- **Thunderbolt® I/II/III-enabled Headphones / Headsets / Docking Stations / Connectivity Expansion Hubs / Adapters**
- **HDMI™-enabled VR / AR / MR Headphones and Headsets**
- **MHL™-enabled VR / AR / MR Headphones and Headsets**
- **USB 1.1 / 2.0 / 3.0 / 3.1 Gen 1 / 3.1 Gen 2 / USB-C-enabled Headphones / Headsets / Docking Stations / Connectivity Expansion Hubs / Tablets / Mobile Phones / Tablet & Mobile Phone Cases / Portable Projectors**
- **Remote Controls / Gaming Controllers with Headphone Jacks**

### FEATURES

- **Class-H Capless DirectConnect Technology**
  - Eliminates Large Output DC Blocking Capacitors
  - Reduces Board Area
  - Reduces Component Height and Cost
  - Enables Full Bass Response Without Attenuation
  - Offers No Pop on Start-Up or Power-Down
  - Reduces Power consumption by as much as 45% at Typical Listening Levels compared to Class A/B solutions
  - < 1uA Shutdown Supply Current
  - < 1uA Shutdown Input Leakage Current
  - Up to 170mW Per Channel into 16Ω
  - Up to 106dB SNR / DNR (10KΩ)
  - Charge-pump allows for True Ground Centered Outputs
  - High Power Supply Rejection Ratio (>100 dB PSRR)
  - Differential Inputs for Maximum Noise Rejection Ratio (90 dB CMRR)
  - Optional register controlled High-Impedance Outputs When Disabled
  - Independent Left/Right Volume and Mute Control (TSDP11xx)
  - Power Supply Voltage Range: 2.5 V to 5.5 V
  - GPIO Control for Hardware Shutdown
  - Advanced Features Control via Register setting over I2C, including Low-Power Mode Support (TSDP11xx)
  - Compact 20-Pin, 4mm x 4mm QFN RoHS Package
  - Offerings in both Commercial and Industrial Temp Ranges offered in either Tray or Tape & Reel

### TSDP11XX BLOCK DIAGRAM



# TSDP1xx

## Class-H DirectConnect Headphone Amplifier

### 1. TSDP10XX FUNCTIONAL DIAGRAM

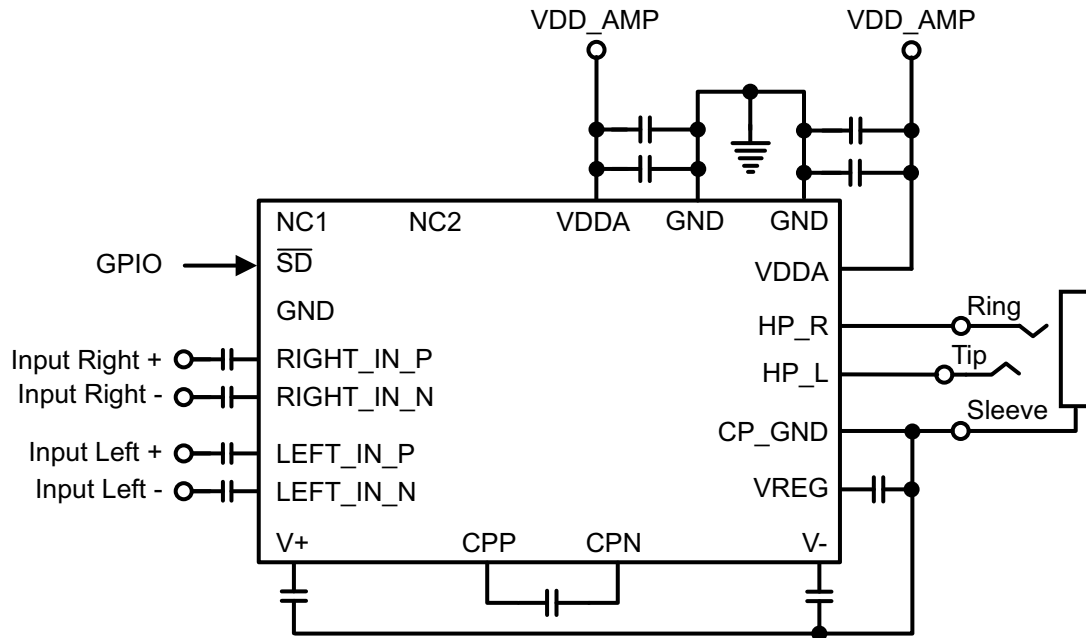


Figure 1. TSDP10xx Functional Diagram

### 2. TSDP11XX FUNCTIONAL DIAGRAM

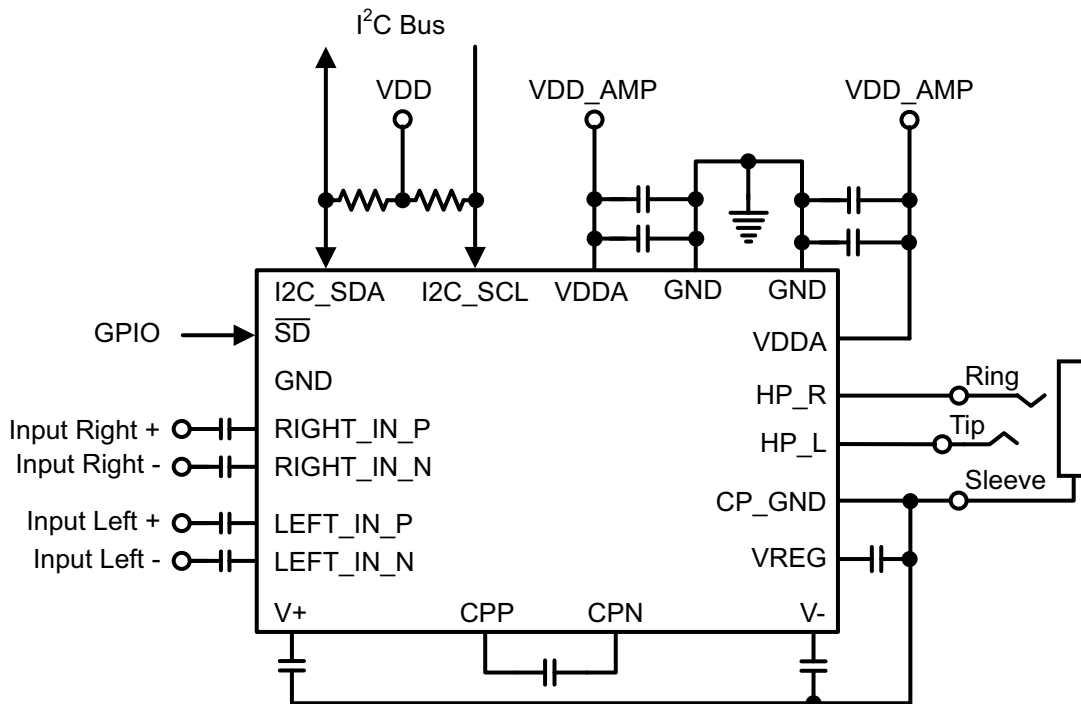


Figure 2. TSDP11xx Functional Diagram

# TSDP11xx / TSDP10xx

## Class-H DirectConnect Headphone Amplifier

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## Class-H DirectConnect Headphone Amplifier

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## TSDP11xx / TSDP10xx

### Class-H DirectConnect Headphone Amplifier

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#### 1. PRODUCT OVERVIEW

The TSDP11xx / TSDP10xx stereo Class-H Capless DirectConnect™ headphone amplifier is optimally designed for portable applications. The GPIO control allows the device to be put in a low power shutdown mode. The TSDP1xx is a high fidelity amplifier with SNR of 105dB. With a PSRR greater than 90dB, 21dB higher than any other solution on the market. The TSDP11xx / TSDP10xx can be connected directly to a battery without compromising the listening experience. The output noise of 5.6 $\mu$ Vrms (typical, *A-weighted*) provides a minimal noise background during periods of silence. Configurable differential inputs and high CMRR allow for maximum noise rejection in the noisy mobile environment. TSDP1xx is available in a 4x4mm QFN package. The TSDP1xx stereo headphone Capless DirectConnect™ architecture eliminates the large output coupling capacitors typically required for single-supply headphone drivers. The device consists of two 170mW Class-AB headphone drivers, supply controlled with Class-H charge-pump, shutdown control, and comprehensive click-and-pop suppression circuitry. The charge pump uses VREG to create a positive supply (V+) and inverts VREG to create a negative supply (V-). The headphone drivers operate from these bipolar supplies with their outputs biased around GND. The drivers have almost twice the supply range compared to other 3V/5V single-supply drivers, increasing the available output power. Additionally, by being biased around physical GND, the typical power-on click-and-pop are found in other non-ground center referenced output solutions on the market eliminated.

The benefit of this GND bias is that the driver outputs do not have the typical VDD/2 DC component. The large DC-blocking capacitors are unnecessary, thus improving low-end frequency response while conserving board space and system cost. Each channel, on the TSDP11x, has independent left/right, software controlled gain and mute, which makes it possible to optimize power savings and click-and-pop suppression in mixed-mode operation, mono/stereo click-and-pop suppression that eliminates audible transients on startup and shutdown. Additionally, the TSDP11xx / TSDP10xx family features thermal overload and short-circuit protection.

2. DETAILED BLOCK DIAGRAM

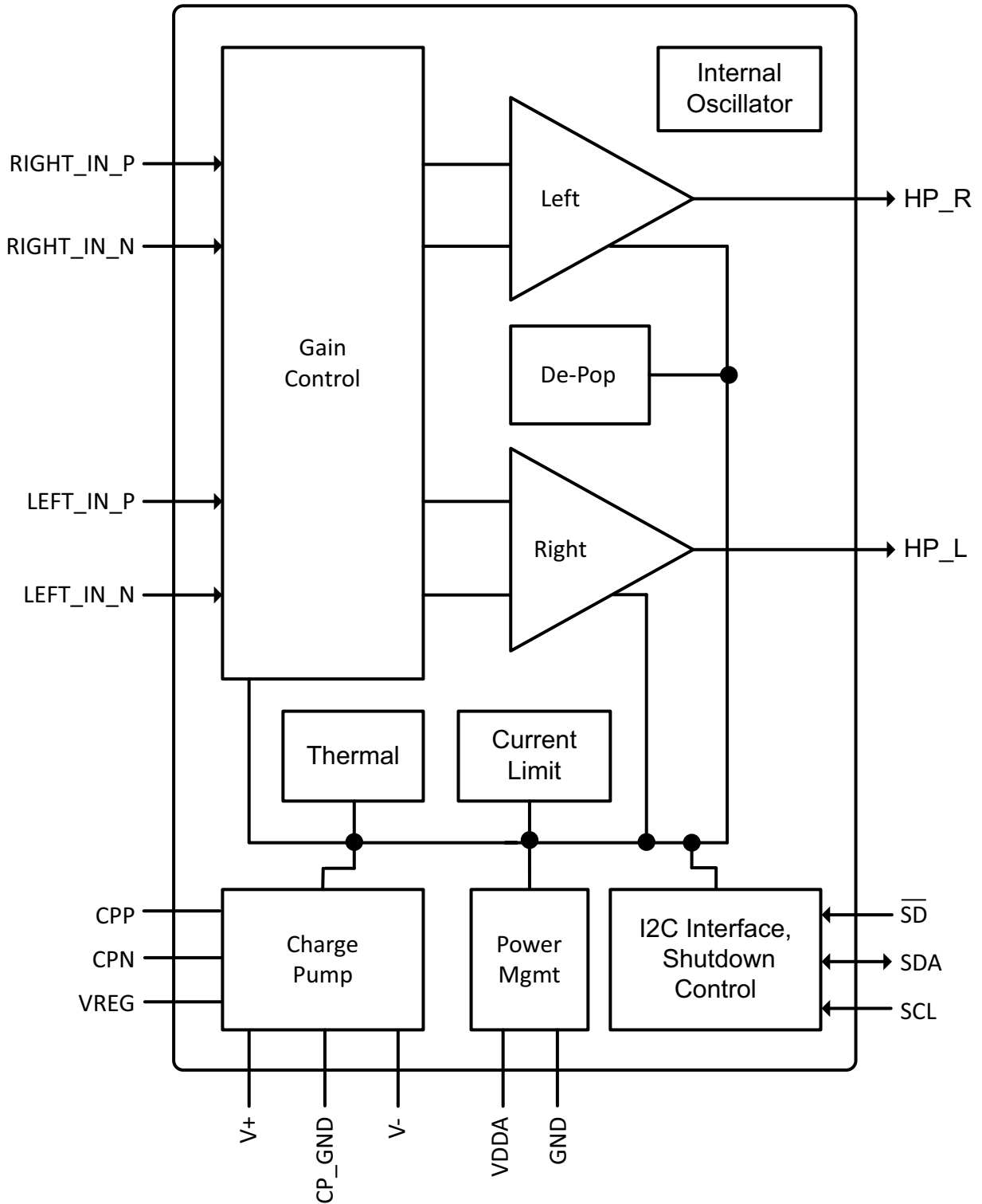


Figure 1. TSDP11xx Family Block Diagram

**3. FUNCTION DESCRIPTION**

**3.1. Internal Oscillator**

The TSDP11xx / TSDP10xx uses an internal oscillator to generate a master reference clock. This clock is used to run the charge pump, anti-pop circuitry monitor the chip temperature sensor and shutdown circuitry. The oscillator runs at 830kHz (typical).

The internal oscillator of the TSDP11xx can be varied with register control. The adjustment of frequency can be done with registers if needed.

*3.1.0.1. Oscillator Control1 Register*

| Register Address                  | Bit | Label              | Type | Default | Description  |
|-----------------------------------|-----|--------------------|------|---------|--|
| Reg 22<br>SELF_OSC_CTRL1<br>(15h) | 7:6 | SELFOSC_DIVCLK_SEL | RW   | 0h      | Selects the initial divider from the SELFOSC input clock to be used for the chopping clock & APOPCLOCK setting |
|                                   | 5:4 | SELFOSC_VCHP_SEL   | RW   | 0h      | Selects the divider from the selfosc input clock to be used for the Charge Pump clock setting                  |
|                                   | 3:0 | SELFOSC_FREQ_SEL   | RW   | 5h      | Selects the desired output frequency setting   |

**Table 1. SELF\_OSC\_CTRL1 Register**

*3.1.0.2. Oscillator Control2 Register*

| Register Address                  | Bit | Label                | Type | Default | Description  |
|-----------------------------------|-----|----------------------|------|---------|--|
| Reg 23<br>SELF_OSC_CTRL2<br>(16h) | 7:5 | RESERVED             | RO   | 0h      | Reserved   |
|                                   | 4   | SELFOSC_PWD          | RW   | 0h      | Powers down (i.e. when high) the self oscillator circuitry                           |
|                                   | 3   | SELFOSC_RSTB         | RW   | 1h      | resets (i.e. when low) the dflops in the divider circuitry                           |
|                                   | 2   | SELFOSC_CHPRCLK_PWDB | RW   | 0h      | Powers down (i.e. when low) the chopping clock output                                |
|                                   | 1   | SELFOSC_APOPCLK_PWDB | RW   | 1h      | Powers down (i.e. when low) the antipop clock output (i.e. also used for tempsensor) |
|                                   | 0   | SELFOSC_APOPCLK_SEL  | RW   | 0h      | Selects the desired output frequency for the apopclock setting                       |

**Table 2. SELF\_OSC\_CTRL2 Register**

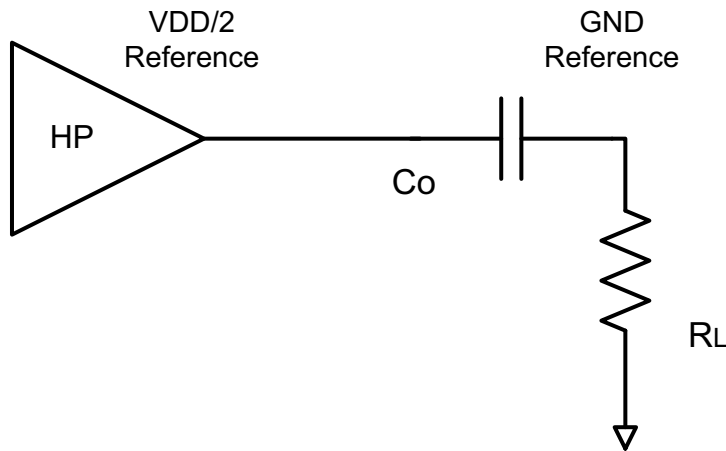
## 4. AUDIO INPUTS

The TSDP11xx / TSDP10xx provides differential audio analog inputs

### 4.0.1. Headphone Amplifiers

Single-supply headphone drivers traditionally have their outputs biased about a half the nominal DC voltage for maximum dynamic range. In other words, to block the DC bias, large capacitors are needed to couple the signal to the headphone driver. Without these capacitors, wasted large DC current will unnecessarily flow to the headphone speaker, and possibly damage both headphone driver and/or speaker.

Single-supply headphone amplifiers typically require dc-blocking capacitors. The capacitors are required because most headphone amplifiers have a dc bias on the outputs pin. If the dc bias is not removed, the output signal is severely clipped, and large amounts of dc current rush through the headphones, potentially damaging them. The functional diagram shown above illustrates the conventional headphone amplifier connection to the headphone jack and output signal. DC blocking capacitors are typically large in value to avoid attenuation of Bass (or low frequency) content. The headphone speakers (typical resistive values of 16Ω or 32Ω) combine with the dc blocking capacitors to form a high-pass filter.



**Figure 2. Conventional, Single-Supply Rail, Headphone Amplifier Connection**

### 4.1. DirectConnect Headphone Amplifiers

The Capless DirectConnect™ architecture uses charge pump to create an internal negative supply. This allows the outputs of the TSDP11xx / TSDP10xx to be centered around GND. In addition, the creation of the negative internal supply doubles the dynamic range while operating from a single supply. With the ground (GND) reference, there is no need for the large DC-blocking capacitors. Instead of requiring two large highly linear capacitors, the TSDP11xx / TSDP10xx requires only four, inexpensive small-value capacitors. This reduces board space, lowers the total solution BOM cost, and improves power consumption all while improving the frequency response of the headphone driver.

The HP\_R/HP\_L pins can drive a 16Ω, 32Ω headphone load or line output load up to 10KΩ without any external components. The signal volume of the headphone amplifier volume can be independently adjusted under software control by writing to HPVOL\_L and HPVOL\_R. Also setting the volume to 01100 will power down amp. The amplifier can be set to mute by enabling the mute register or setting the volume to 01110. The output remains at ground, so that no click noise is produced when muting or un-muting. Gains above 0dB run the risk of clipping large signals.

#### 4.1.1. Headphone Amplifiers

Single-supply headphone amplifiers typically require dc-blocking capacitors. The capacitors are required because most headphone amplifiers have a dc bias on the outputs pin. If the dc bias is not removed, the output signal is severely



## TSDP11xx / TSDP10xx

### Class-H DirectConnect Headphone Amplifier

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#### 4.1.2. Volume Control

The TSDP1xx features two independent controls for left/right volume ranging from +6dB to -22dB and mute. Changes in volume are walked automatically to the new target volume using an advanced pop suppression circuitry which eliminates unwanted audio pops and clicks at the output.

Channel volume can be controlled across a gain and attenuation range of -22dB to +6dB (each step is linear and has about a -22.98dB gain difference). The level of attenuation is specified by 5-bit code 'VOL\_x', where 'x' is L, or R. The value 01110" indicates mute; other values describe the number of 1.0dB steps above -22dB.

##### 4.1.2.1. Volume Control Register

| Register Address          | Bit | Label              | Type | Default | Description   |
|---------------------------|-----|--------------------|------|---------|---|
| Reg 19<br>HDPH_CTRL2(12h) | 7   | RESERVED           | RW   | 0       | Reserved  |
|                           | 6   | HP_DISCHOP_ANTIPOP | RW   | 1       | Disables the chopping for antipop when high. Only turns chopping at power up/down (i.e. code 1) on when both D2A_DISCHOP_ANTIPOP low and D2A_DISCHOP_AMP is high.                                       |
|                           | 5   | HP_DISCHOP_AMP     | RW   | 1       | Will enable chopping always when low and disable chopping when high.  |
|                           | 4:0 | HP_CNT_TARGET_L    | RW   | 10      | Sets the left channel final target gain for the anti-pop ramping circuitry (01100b==> pwd,01110==> mute,01111==> -22.8919dB, 11100b==> 0dB, 11000b ==> +2dB, 10101b ==> +4dB, 10011b ==> +6dB)          |
| Reg 20<br>HDPH_CTRL3(13h) | 7   | RESERVED           | RW   | 0       | Reserved  |
|                           | 6   | RESERVED           | RW   | 0       | Reserved  |
|                           | 5   | RESERVED           | RW   | 0       | Reserved  |
|                           | 4:0 | HP_CNT_TARGET_R    | RW   | 10      | Sets the right channel final target gain for the anti-pop ramping circuitry (01100b ==> pwd, 01110b ==> mute, 01111b ==> -22.8919dB, 11100b ==> 0dB, 11000b ==> +2dB, 10101b ==> +4dB, 10011b ==> +6dB) |

Table 3. HDPH\_CTRL2 and HDPH\_CTRL3 Register

#### 4.1.3. Current Limiter

Advanced short-circuit protection protects amplifier outputs from shorting conditions

## TSDP11xx / TSDP10xx

### Class-H DirectConnect Headphone Amplifier

To avoid damage to the outputs if a short circuit condition should occur, the headphone amplifier implements a current limiter protection circuits. The headphone output amplifier will detect the load current and will limit the output current if it exceeds the selected current limited and limit its output if in an over current state.

#### 4.1.3.1. HDPH\_CTRL1 Register

| Register Address          | Bit | Label    | Type | Default | Description  |
|---------------------------|-----|----------|------|---------|--|
| Reg 18<br>HDPH_CTRL1(11h) | 7:6 | HP_ILIM  | RW   | 3h      | Sets the current output limit for the headphones (i.e. 00b ==> powerdown, 01b ==> ~ 100mA, 10b ==> ~150mA, 11b ==> ~200mA) |
|                           | 5   | HPL_PWD  | RW   | 0h      | Left Headphone power down  |
|                           | 4   | HPR_PWD  | RW   | 0h      | Right Headphone power down   |
|                           | 3   | RESERVED | RW   | 0h      | Reserved.  |
|                           | 2   | RESERVED | RW   | 0h      | Reserved.  |
|                           | 1   | HPL_MUTE | RW   | 0h      | Left Headphone mute (sets ampfiier to unity gain with postive differential input set to GNDA)                              |
|                           | 0   | HPR_MUTE | RW   | 0h      | Right Headphone mute (sets ampfiier to unity gain with postive differential input set to GNDA)                             |

Table 4. HDPH\_CTRL1 Register

#### 4.1.4. Anti-pop Circuit

Advanced anti-pop circuit prevents amplifier outputs from creating audible pop conditions.

##### 4.1.4.1. Click-and-Pop

Due to the nature of power management and audio path configurability there are many situations which could introduce undesirable sounds. While it is not possible to prevent undesirable sounds in every situation, it is still possible to prevent them under most situations. In order to ensure the highest likely the user hearing a pop, the headphone should be fully powered down prior to removal of VDD.

| State Change       | Description                   | Desired (dBV Awt) |
|--------------------|-------------------------------|-------------------|
| Application of VDD | Headphone Output 10K-16Ω load | -65               |
| Application of VDD | Headphone Output 32-16Ω load  | -65               |
| Removal of VDD     | Headphone Output 10K-16Ω load | -65               |
| Removal of VDD     | Headphone Output 32-16Ω load  | -65               |

Table 5. State Change Description

4.1.4.2. *Anti Pop Control Register*

| Register Address          | Bit | Label              | Type | Default | Description   |
|---------------------------|-----|--------------------|------|---------|---|
| Reg 21<br>HDPH_CTRL4(14h) | 7   | RESERVED           | RW   | 0h      | Reserved  |
|                           | 6   | RESERVED           | RW   | 0h      | Reserved  |
|                           | 5   | RESERVED           | RW   | 1h      | Reserved  |
|                           | 4   | HP_OUTGND_REG      | RW   | 0h      | Register used to control the headphone output grounding switch when d2a_hp_outgnd_ovrd is set high  |
|                           | 3   | HP_OUTGND_OVRD     | RW   | 0h      | Over rides (i.e. when high) the antipop ramping control of the headphone output grounding switch with value from "d2a_hp_outgnd_reg"  |
|                           | 2   | RESERVED           | RW   | 0h      | Reserved  |
|                           | 1   | RESERVED           | RW   | 0h      | Reserved  |
|                           | 0   | HP_CONNECT_GND_VAG | RW   | 1h      | Turns on switches (i.e. when high) at the differential inputs to reference inputs to ground (i.e. DC blocking caps cause inputs to need reference). This was mainly added incase we needed to tristate inputs for Global Headset functionality. |

**Table 6. HDPH\_CTRL4 Register**

**4.1.5. Short-Circuit Protection**

The right channel and left channel audio outputs have independent current limit detection circuits with common register control settings. The current limit can be set to ~100mA, ~150mA, ~200mA, or the protection circuit can be disabled. The current limiting allows limiting the power delivered to the load without disabling the amplifiers. The lowest setting allows limiting the power delivered to the load to just above 1Vrms into a 16Ω load while still protecting against a short circuit event. The highest setting protects against a short circuit event while still delivering the maximum power into a 16Ω load.

**4.2. Charge Pump**

**4.2.1. Class-H Charge Pump**

The TSDP1xx features an 830kHz switching low-noise charge pump architecture. The architecture features controlled switching that minimizes noise generated by turn-on and turn-off transients. The switching frequency is well beyond the audio range, and does not interfere with the audio signals. By controlling the clocking of the switches, the impulse current noise caused by the parasitic bond wire and trace inductance is minimized or completely eliminated. Although not typically required, additional high-frequency noise attenuation can be achieved by increasing the size of the capacitor at V- to CP\_GND, V+ to CP\_GND as well as a fly cap between CPP and CPN. The TSDP1xx class-H amplifier employs a Class-AB output stage with power-supply voltages that are adjusted based on the output signal level. The output stage senses the output voltage level and adjusts the charge pump supply voltage dynamically. As indicated in the figure below, the adjustment can be made on a cycle by cycle basis. Thus when the music level is small, the charge pump supply voltage is correspondingly decreased; and when the music level is high, the charge pump voltage is increased.

## TSDP11xx / TSDP10xx

### Class-H DirectConnect Headphone Amplifier

For typical listening level, this feature can lower the power used in playback mode by almost 45% thus extending battery life by several hours or alternatively the designer could save BOM cost and board space by using smaller battery.

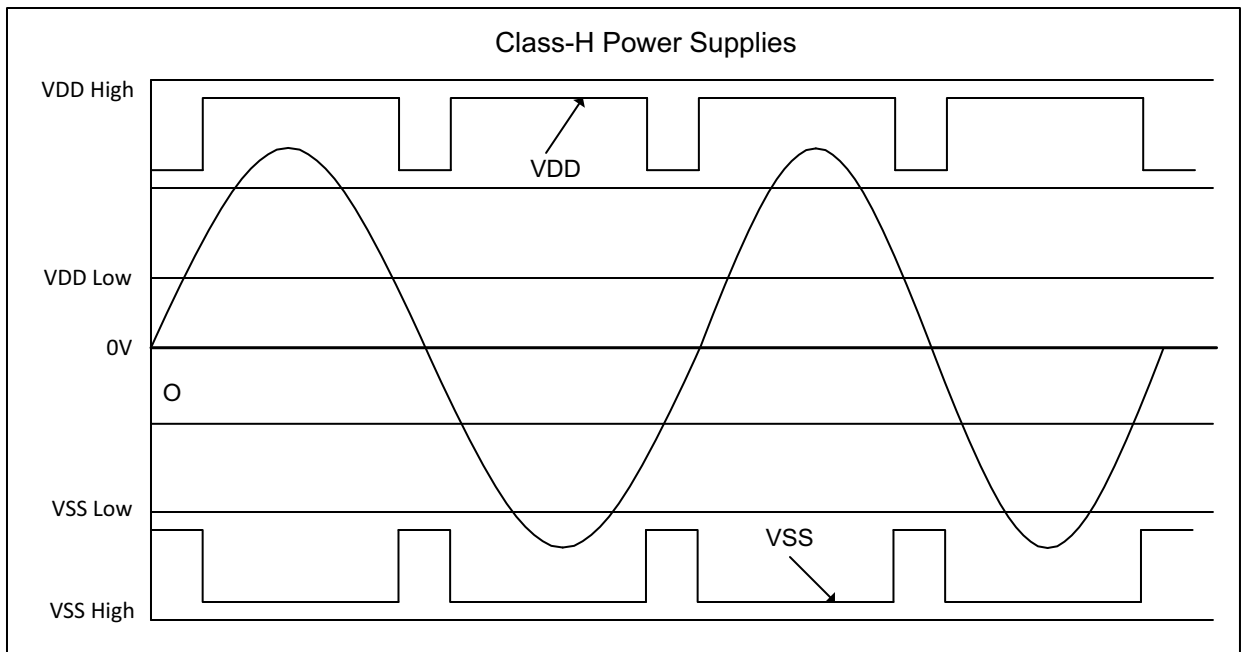


Figure 3. Class-H Charge Pump Operation

#### 4.2.2. Charge Pump Capacitors

The VREG\_CP output (i.e. pin14) should have a 10uF capacitor to ensure both stability and reduced ripple on the LDO output while supplying power to create the class H output supplies. The charge pump outputs V+ (pin 12), V- (pin 9) are the class H output supplies providing power to the headphone amplifiers and should each be decoupled to ground with 5uF capacitors. The generated supply voltage across these capacitors will change dependent on the combination of the two headphone output signal levels. A 5uF capacitance should also be placed across the CPP (pin 13) and CPN (pin 10) nodes. This capacitor helps create the positive (V+) and negative (V-) supply voltages via charge sharing. Providing a 10uF to the VDDA (pin 15) will help to reduce instantaneous demands from the power supply when providing power to the LDO. It should be noted that using a 0.1uF ceramic capacitor in parallel with the larger Tantalum capacitors at all supply pins can help to reduce unwanted high frequency noise on the supplies at the pins.

#### 4.2.3. Short-Circuit Protection

The Charge Pump also has short circuit detection circuitry which will disable the Charge Pump if a short circuit causes too large a current demand. The Charge Pump will be disabled for 511 charge pump clock cycles and then re-enabled for 63 charge pump clock cycles to see if the short circuit event has been removed. This algorithm will continue until the short circuit event has been removed.

| Register Address                | Bit | Label        | Type | Default | Description  |
|---------------------------------|-----|--------------|------|---------|--|
| Reg14<br>CP_SCUR_CTRL1<br>(0Dh) | 7:4 | 0]           | RO   | 0       | Reserved.  |
|                                 | 3   | RESERVED     | RW   | 1       | resets (i.e. when low) the flop used to latch the output of the comparator detecting Charge Pump Short Circuit event and resets the LSFR used to time the short circuit event checking |
|                                 | 2   | VCHP_SC_PWD  | RW   | 0       | Powers down the Charge Pump Short Circuit block  |
|                                 | 1   | VCHP_SC_BYPS | RW   | 0       | Bypasses the Short Circuit Event and forces Charge Pump to keep running  |
|                                 | 0   | RESERVED     | RW   | 0       | Reserved   |

Table 7. CP\_SCUR\_CTRL1 Register

### 4.3. Modes of Operation

HiZ is enabled, when the headphone amplifiers are powered down, by writing logic 1 in register 14 (i.e. HDPH\_CTRL4), bit 3 and ensuring that register 14 bits 4 and 0 are set to logic 0. Place logic 0 in register 14, bit 3 and logic 1 in register 14 bit 0 to disable the HiZ state of the outputs. The HiZ state puts the headphone outputs into a state of high impedance. Use this configuration when the outputs of the TSDP1xx share traces with other devices whose outputs may be active.

### 4.4. Jack Detection and Configuration Algorithm

The  $\overline{SD}$  pin of the TSDP1xx can be utilized to effect a Jack Detection and power up the chip when a plug is inserted into the Jack. The Jack pin connected to the  $\overline{SD}$  pin should be default ground prior to inserting the plug and pulled to VDDA when the plug is inserted into the JACK.

### 4.5. Thermal Shutdown

There are 2 trip points, “high” and “low”. The “high” trip point should always be set to a higher value than the “low” trip point. If the temperature of the chip increases above the “high” trip point, the headphone outputs will be powered down which will cause the output volumes to be decreased from the current volume toward mute and then the amplifiers will be powered down. The amplifiers will not be powered back up until the temperature on the chip has reduced to the “low” trip point. When the temperature drops below the “low” trip point, the amplifiers will be allowed to power back up and ramp back to the original volume setting. With proper settings on the clock division multiplexers, the “high” and “low” trip points are polled every ~1.5msec or ~3msec.

#### 4.5.1. Thermal Shutdown Registers

The temperature sensor circuit is configured and monitored using the Temp Sensor Control/Status Register

4.5.1.1. *Temp Sensor Control/Status*

| Register Address   | Bit | Label        | Type | Default | Description  |
|--|-----|--------------|------|---------|--|
| Reg 28-<br>TEMP_SENSE_CTRL1(1Bh)<br>Temp Sensor Control/Status | 7:5 | HI_TEMP_SEL  | RW   | 3       | Temp sensor block hi trip points ( 000b==>110C, 001b==>125C, 010b==>140C, 011b==>155C, 100b==>170C, 101b==>185C, 110b==>200C,111b==>215C)  |
|  | 4:2 | LO_TEMP_SEL  | RW   | 2       | Temp sensor block low trip points ( 000b==>110C, 001b==>125C, 010b==>140C, 011b==>155C, 100b==>170C, 101b==>185C, 110b==>200C,111b==>215C) |
|  | 1:0 | VBG_TRIM_SEL | RW   | 1       | Adjusts the VBG voltage in the Tempsensor by 8mV increments (i.e. 00 ==> 1.215V, , 01b ==> 1.223V, 10b ==> 1.2318V, 11b ==> 1.24V)         |

**Table 8. TEMP\_SENSE\_CTRL1 Register**

**4.5.2. Headphone Thermal Shutdown Control Register**

The thermal shutdown algorithm is configured using the Speaker Thermal Algorithm Control Register

4.5.2.1. *Speaker Thermal Control Register*

| Register Address  | Bit | Label          | Type | Default | Description                                      |
|---|-----|----------------|------|---------|--|
| Reg 29<br>TEMP_SENSE_CTRL2(1Ch)<br>Speaker Thermal Shutdown Control | 7:3 | RESERVED       | RO   | 0       | Reserved   |
|   | 2   | RESERVED       | RW   | 0       | Reserved   |
|   | 1   | TEMPSENSE_PWD  | RW   | 0       | Temp sensor power down 1b=power down             |
|   | 0   | TEMPSENSE_RSTB | RW   | 1       | Temp sensor reset = 0b, reset the tempense logic |

**Table 9. TEMP\_SENSE\_CTRL2 Register**

**4.6. Asynchronous I2C**

**4.6.1. I<sup>2</sup>C, 2-Wire Control Interface**

The TSDP11xx / TSDP10xx device includes a 2-Wire I<sup>2</sup>C compatible interface for communicating with an external controller. This interface supports communication to external micro-controller or other I<sup>2</sup>C compatible peripheral chips. The I<sup>2</sup>C interface supports normal (100kH) and fast mode (400kHz) operation.

## TSDP11xx / TSDP10xx

### Class-H DirectConnect Headphone Amplifier

#### 4.6.2. Device Address, ID, Revision Registers

##### 4.6.2.1. TSDP11xx Device Address Register 0

| Register Address      | Bit | Label         | Type | Default | Description                 |
|-----------------------|-----|---------------|------|---------|-----------------------------|
| Reg 1<br>DEVADD0(00h) | 7:1 | DEV_ADD0[6:0] | RW   | 68      | Register I2C Device Address |
|                       | 0   | RSVD          | R    | 0       | Reserved                    |

Table 10. TSDP11x DEVADD0 Register

##### 4.6.2.2. TSDP11xx Device Identification Register

| Register Address    | Bit | Label       | Type | Default   | Description  |
|---------------------|-----|-------------|------|-----------|--|
| Reg 2<br>DEVID(01h) | 7:0 | DEV_ID[7:0] | R    | 01000xxxb | 8-bit device identification number. The least significant three bits reflect the state of the Bond-Out pins. |

Table 11. TSDP11x DEVID Register

##### 4.6.2.3. TSDP11xx Device Revision Register

| Register Address     | Bit | Label        | Type | Default | Description   |
|----------------------|-----|--------------|------|---------|---|
| Reg 3<br>DEVREV(02h) | 7:4 | MAJ_REV[3:0] | R    | 0001    | 4-bit major revision number (all layer)<br>currently = 1 (1st release)<br>MMMM.mmmm currently = 1.0 |
|                      | 3:0 | MIN_REV[3:0] | R    | 0000    | 4-bit minor revision number (metal revision)<br>currently = 0 (no revisions-initial release)        |

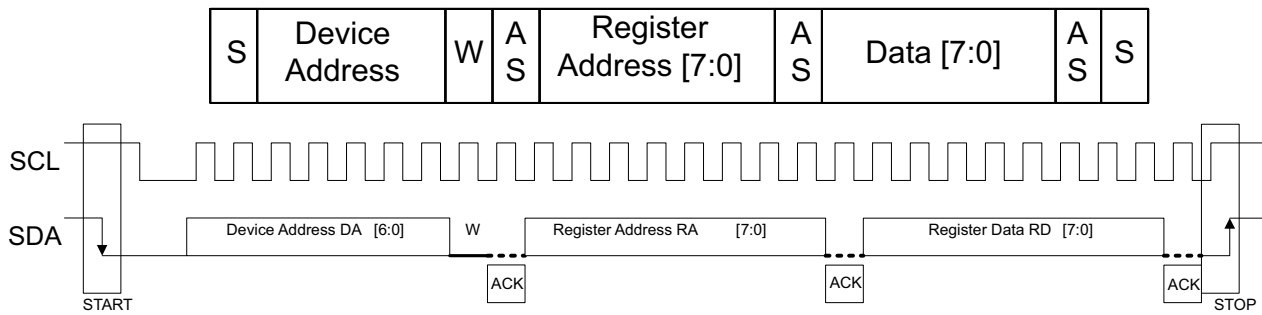
Table 12. TSDP11x DEVREV Register

#### 4.6.3. TSDP11x Register Write Cycle

The controller indicates the start of data transfer with a high to low transition on SDA while SCL remains high, signalling that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the TSDP11x and the R/W bit is '0', indicating a write, then the TSDP11xx responds by pulling SDA low on the next clock pulse (ACK); otherwise, the TSDP11xx returns to the idle condition to wait for a new start condition and valid address.

Once the TSDP11xx has acknowledged a correct device address, the controller sends the TSDP11xx register address. The TSDP11xx acknowledges the register address by pulling SDA low for one clock pulse (ACK). The controller then sends a byte of data (B7 to B0), and the TSDP11xx acknowledges again by pulling SDA low.

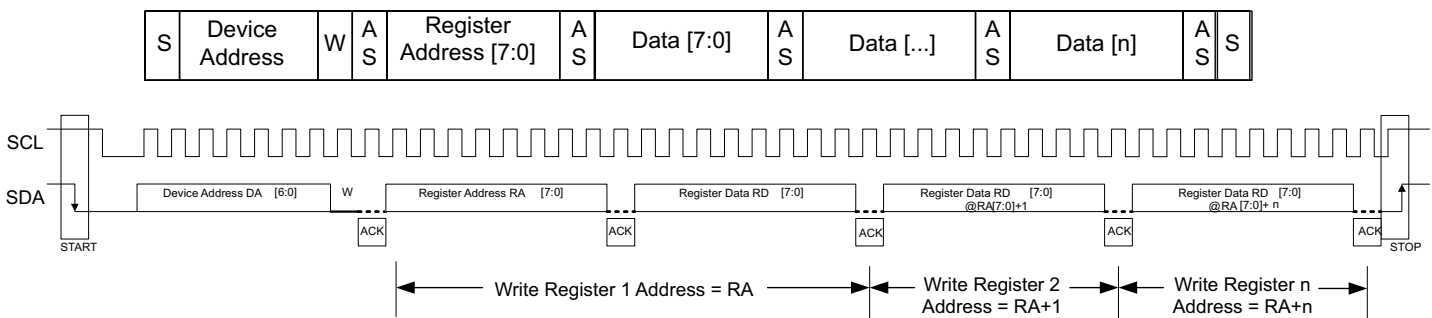
When there is a low to high transition on SDA while SCL is high, the transfer is complete. After receiving a complete address and data sequence the TSDP11xx returns to the idle state. If a start or stop condition is detected out of sequence, the device returns to the idle condition.



**Figure 4. TSDP11xx Page Register Write - 2 Wire Serial Control Interface**

**4.6.4. TSDP11xx Register Burst Write Cycle**

The controller may write more than one register within a single write cycle. To write additional registers, the controller will not generate a stop or start (repeated start) command after receiving the acknowledge for the second byte of information (register address and data). Instead the controller will continue to send bytes of data. After each byte of data is received, the register address is incremented.



**Figure 5. TSDP11xx Page Register Burst Write Cycle**

**4.6.5. TSDP11xx Register Read Cycle**

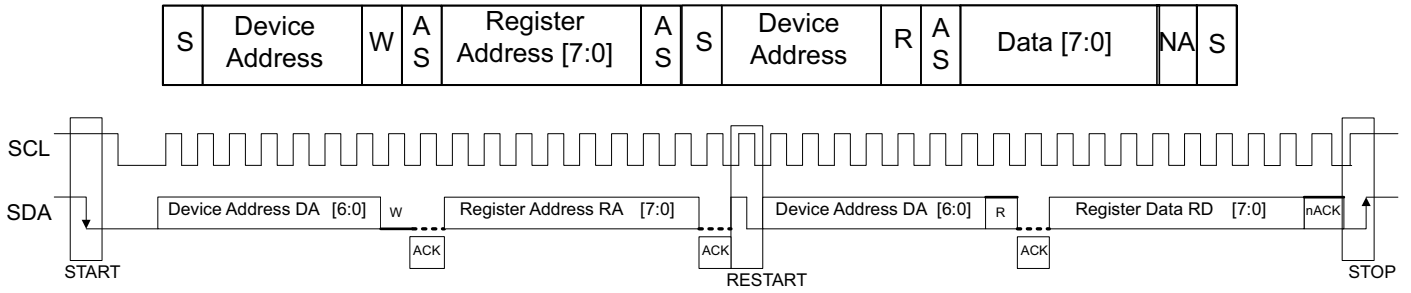
The controller indicates the start of data transfer with a high to low transition on SDA while SCL remains high, signalling that a device address and data will follow. If the device address received matches the address of the TSDP11xx and the R/W bit is '0', indicating a write, then the TSDP11xx responds by pulling SDA low on the next clock pulse (ACK); otherwise, the TSDP11xx returns to the idle condition to wait for a new start condition and valid address.

Once the TSDP11xx has acknowledged a correct address, the controller sends a restart command (high to low transition on SDA while SCL remains high). The controller then re-sends the devices address with the R/W bit set to '1' to indicate a read cycle. The TSDP11xx acknowledges by pulling SDA low for one clock pulse. The controller then receives a byte of register data (B7 to B0).

For a single byte transfer, the host controller will not acknowledge (high on data line) the data byte and generate a low to high transition on SDA while SCL is high, completing the transfer. If a start or stop condition is detected out of sequence, the device returns to the idle condition.



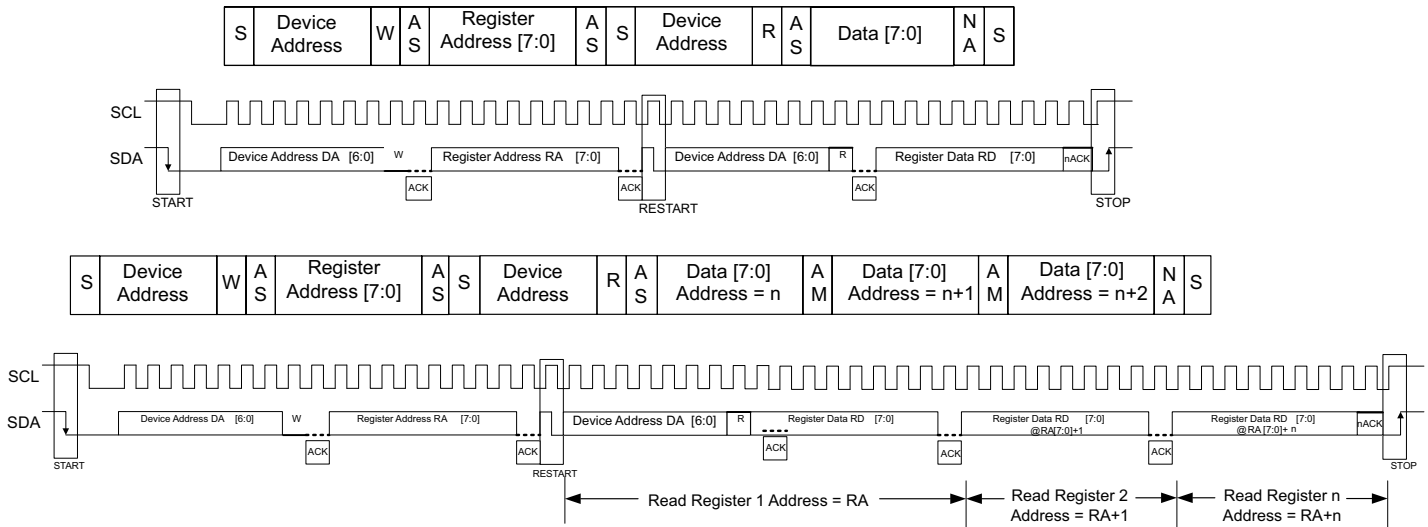
**TSDP11xx / TSDP10xx**  
**Class-H DirectConnect Headphone Amplifier**



**Figure 6. TSDP11xx Page Register Single Byte Read Cycle**

**4.6.6. TSDP11xx Page Register Burst Read Cycle**

The controller may read more than one register within a single read cycle. To read additional registers, the controller will not generate a stop or start (repeated start) command after sending the acknowledge for the byte of data. Instead the controller will continue to provide clocks and acknowledge after each byte of received data. The TSDP11xx will automatically increment the internal register address after each register has had its data successfully read (ACK from host) but will not increment the register address if the data is not received correctly by the host (nACK from host) or if the bus cycle is terminated unexpectedly. By automatically incrementing the internal register address after each byte is read, all the internal registers of the TSDP11xx may be read in a single read cycle.



**Figure 7. TSDP11xx Page Register Burst Multi-byte Read Cycle**

## 5. TSDP11XX REGISTERS

### 5.1. TSDP11xx STATUS0 Register

| Register Address      | Bit | Label           | Type | Default | Description  |
|-----------------------|-----|-----------------|------|---------|--|
| Reg 4<br>STATUS0(03h) | 7   | VREG_CP_SC_DET  | RO   | 0h      | Short Circuit Detected on LDO output when high (Requires VREG_CP_sc_rstb in Reg8(07h) to be toggled) |
|                       | 6   | VDDA_BELOW_3P1V | RO   | 0h      | Detects VDDA supply level for 2.5V operation (i.e. trip ~3.1V)                                       |
|                       | 5   | SUPPLY_OSC      | RO   | 0h      | Detects VDDA supply level for 3.3 to 5V operation (i.e. trip ~4.16V)                                 |
|                       | 4   | RESERVED        | RO   | 0h      | Reserved   |
|                       | 3   | RESERVED        | RO   | 0h      | Reserved   |
|                       | 2   | TEMP_OVERHEAT   | RO   | 0h      | Temp sensor statemachine overheat output.  |
|                       | 1   | OVERHEAT_HIGH   | RO   | 0h      | Temp sensor high overheat indicator.   |
|                       | 0   | OVERHEAT_LOW    | RO   | 0h      | Temp sensor low overheat indicator.  |

Table 13. TSDP11xx STATUS0 Register

### 5.2. TSDP11xx STATUS1 Register

| Register Address      | Bit | Label       | Type | Default | Description  |
|-----------------------|-----|-------------|------|---------|--|
| Reg 5<br>STATUS1(04h) | 7:2 | RESERVED    | RO   | 0h      | Reserved   |
|                       | 1   | SD          | RO   | 0h      | Input signal Shutdown from Pin.  |
|                       | 0   | VCHP_SC_DET | RO   | 0h      | Short Circuit Detected on Charge Pump VPOS or VNEG output when high (Will automatically reset) |

Table 14. TSDP11xx STATUS1 Register

**5.3. TSDP11xx CP\_CTRL1 Register**

| Register Address       | Bit | Label              | Type | Default | Description                 |
|------------------------|-----|--------------------|------|---------|-----------------------------|
| Reg 6<br>CP_CTRL1(05h) | 7   | DELAY_MODE         | RW   | 0h      | Reserved                    |
|                        | 6   | MODE_DELAY_BYPS    | RW   | 1h      | Reserved                    |
|                        | 5:3 | VCHP_CLKSEL        | RW   | 1h      | Reserved                    |
|                        | 2   | VCHP_HIZ_VPOS_OVRD | RW   | 0h      | Reserved                    |
|                        | 1   | VCHP_HIZ           | RW   | 0h      | Reserved                    |
|                        | 0   | VCHP_PWD           | RW   | 0h      | Powers down the Charge Pump |

Table 15. TSDP11xx CP\_CTRL1 Register

**5.4. TSDP11xx CP\_CTRL2 Register**

| Register Address       | Bit | Label       | Type | Default | Description  |
|------------------------|-----|-------------|------|---------|--|
| Reg 7<br>CP_CTRL2(06h) | 7:4 | RESERVED    | RO   | 0h      | Reserved   |
|                        | 3   | AB_OVR_MODE | RW   | 0h      | When "d2a_ab_ovr_en" is high, this bit will select the mode of operation (i.e. 0==> Split Mode, 1 ==> Invert Mode) |
|                        | 2   | AB_OVR_EN   | RW   |         | Enables the over riding of the automatic Class H operation when high   |
|                        | 1:0 | DROP_SEL    | RW   | 0h      | Timing options for delaying the change from Invert to Split  |

Table 16. TSDP11xx CP\_CTRL2 Register

**5.5. TSDP11xx VREG\_CP\_CTRL Register**

| Register Address           | Bit | Label           | Type | Default | Description   |
|----------------------------|-----|-----------------|------|---------|---|
| Reg 8<br>VREG_CP_CTRL(07h) | 7   | RESERVED        | RO   | 0h      | Reserved  |
|                            | 6:5 | VREG_CP_SEL     | RW   | 2h      | Selects the output voltage setting for the LDO (i.e. 00b => 2.395V, 01b ==> 2.592V, 10b ==> 2.793V, 11b ==> 3.076V) |
|                            | 4   | VREG_CP_SC_RSTB | RW   | 1h      | Resets the Short Circuit detection latched output   |
|                            | 3   | RESERVED        | RW   | 0h      | Reserved  |
|                            | 2   | RESERVED        | RW   | 0h      | Reserved  |
|                            | 1   | RESERVED        | RW   | 0h      | Reserved  |
|                            | 0   | VREG_CP_PWD     | RW   | 0h      | Powers down the LDO output and pulls the LDO output to ground.  |

Table 17. TSDP11xx VREG\_CP\_CTRL Register

**5.6. TSDP11xx VDDA\_SENSE\_CTRL Register**

| Register Address              | Bit | Label        | Type | Default | Description                    |
|-------------------------------|-----|--------------|------|---------|--------------------------------|
| Reg 9<br>VDDA_SENSE_CTRL(08h) | 7   | RESERVED     | RO   | 0h      | Reserved                       |
|                               | 6   | RESERVED     | RW   | 1h      | Reserved                       |
|                               | 5   | RESERVED     | RW   | 0h      | Reserved                       |
|                               | 4   | RESERVED     | RW   | 0h      | Reserved                       |
|                               | 3   | VDDSENSE_PWD | RW   | 0h      | Powers down the Vddsense block |
|                               | 2   | RESERVED     | RW   | 1h      | Reserved                       |
|                               | 1:0 | RESERVED     | RW   | 0h      | Reserved                       |

Table 18. TSDP11xx VDDA\_SENSE\_CTRL Register

**5.7. TSDP11xx BIASG\_CTRL2 Register**

| Register Address           | Bit | Label    | Type | Default | Description  |
|----------------------------|-----|----------|------|---------|--|
| Reg 25<br>BIASG_CTRL2(18h) | 7:1 | RESERVED | RO   | 0h      | Reserved   |
|                            | 0   | POR      | RW   | 0h      | This signal is Ored with the POR output to generate "a2d_por_5v" |

Table 19. TSDP11xx BIASG\_CTRL2 Register

**5.8. TSDP11xx REF\_SUP\_CTRL Register**

| Register Address            | Bit | Label            | Type | Default | Description                                      |
|-----------------------------|-----|------------------|------|---------|--|
| Reg 26<br>REF_SUP_CTRL(19h) | 7:4 | RESERVED         | RO   | 0h      | Reserved   |
|                             | 3   | REFSUPPLYDET_PWD | RW   | 0h      | Powers down the refs supply detection amplifier. |
|                             | 2   | RESERVED         | RW   | 0h      | Reserved   |
|                             | 1   | RESERVED         | RW   | 0h      | Reserved   |
|                             | 0   | RESERVED         | RW   | 0h      | Reserved   |

Table 20. TSDP11xx REF\_SUP\_CTRL Register

**5.9. TSDP11xx PAD\_CTRL Register**

| Register Address        | Bit | Label              | Type | Default | Description   |
|-------------------------|-----|--------------------|------|---------|---|
| Reg 30<br>PAD_CTRL(1Dh) | 7   | SD_B_PUB           | RW   | 1h      | SD pin pull up resistor, 1 is off                   |
|                         | 6   | SD_B_PD            | RW   | 1h      | SD pin pull down resistor, 1 is on                  |
|                         | 5   | I2C_DATA_PUB       | RW   | 0h      | I2C data pin pull up resistor, 0 is on              |
|                         | 4   | I2C_DATA_PD        | RW   | 0h      | I2C data pin pull down resistor, 0 is off           |
|                         | 3   | I2C_CLK_PUB        | RW   | 0h      | I2C clock pin pull up resistor, 0 is on             |
|                         | 2   | I2C_CLK_PD         | RW   | 0h      | I2C clock pin pull down resistor, 0 is off          |
|                         | 1   | CLK_DEGLITCH_BYPS  | RW   | 0h      | Bypasses the deglitch circuitry in the I2C CLK pad  |
|                         | 0   | DATA_DEGLITCH_BYPS | RW   | 0h      | Bypasses the deglitch circuitry in the I2C DATA pad |

Table 21. TSDP11xx PAD\_CTRL Register

**5.10. TSDP11xx SHUTDOWN Register**

| Register Address        | Bit | Label       | Type | Default | Description                  |
|-------------------------|-----|-------------|------|---------|------------------------------|
| Reg 31<br>SHUTDOWN(1Eh) | 7:1 | RESERVED    | RO   | 0h      | Reserved                     |
|                         | 0   | SHOUTDOWN_B | RW   | 1h      | Software Controlled Shutdown |

Table 22. TSDP11xx SHUTDOWN Register

# TSDP11xx / TSDP10xx

## Class-H DirectConnect Headphone Amplifier

### 5.11. TSDP11xx Register Map

#### 5.11.1. TSDP11xx Register Map Summary Table

| Register | Name                     | Remarks          | Bit[7]                 | Bit[6]                          | Bit[5]                     | Bit[4]                    | Bit[3]                   | Bit[2]                          | Bit[1]                     | Bit[0]                  | Default |
|----------|--------------------------|------------------|------------------------|---------------------------------|----------------------------|---------------------------|--------------------------|---------------------------------|----------------------------|-------------------------|---------|
| R1 (00h) | DEVADD0                  | Device Address 0 | DEV_ADD0[6:0]          |                                 |                            |                           |                          |                                 |                            | RSVD                    | D0h     |
| R2 (01h) | DEVID                    | Device ID        | DEV_ADD1[6:0]          |                                 |                            |                           |                          |                                 |                            |                         | 40h     |
| R3 (02h) | DEVREV                   | Device Revision  | MAJ_REV[3:0]           |                                 |                            |                           | MIN_REV[3:0]             |                                 |                            |                         | 10h     |
| R4 (03h) | STATUS                   | Status           | VREG_C<br>P_SC_D<br>ET | VDDA_BEL<br>OW_3P1V             | SUPPLY_<br>OSC             |                           |                          | TEMP_OV<br>ERHEAT               | OVERHE<br>AT_HIG<br>H      | OVERHE<br>AT_LOW        | 00h     |
| R5 (04h) | STATUS                   | Status           |                        |                                 |                            |                           |                          |                                 | SD                         | VCHIP_S<br>C_DET        | 00h     |
| R6 (05h) | CP_CTRL<br>1L            | Control          | DELAY<br>MODE          | MODE_DE<br>LAY_BYPA<br>S        | VCHP_CLKSEL                |                           |                          | VCHP_HI<br>Z_VPOS_<br>OVRD<br>J | VCHP_H<br>IZ               | VCHP_P<br>WD            | 48h     |
| R7(06h)  | CP_CTRL<br>2             | Control          |                        |                                 |                            |                           | AB_OVE<br>R_MOD<br>E     | AB_OVER<br>_EN                  | DROP_SEL                   |                         | 0h      |
| R8 0(7h) | VREG_CP<br>_CTRL         | REG<br>Control   |                        | VREG_CP_<br>SEL                 | VREG_C<br>P_SEL            | VREG_C<br>P_RSTB          | VREG_C<br>P_HAL<br>FCUR  | VREG_CP<br>_GNDshr<br>T         | VREG_C<br>P_BYPA<br>S      | VREG_C<br>P_PWD         | 50h     |
| R9(08h)  | VDAA_SE<br>NSE_CTR<br>L  | SENSE<br>Control |                        | VDDSENS<br>E_VREG_C<br>P_SEL_OV | VDDSEN<br>SE_MOD<br>E_OVRD | VDDSEN<br>SE_HALF<br>CUR  | VDDSEN<br>SE_PWD         | VDDSENS<br>E_RSTB               | VDD_TRP_SEL                |                         | 44      |
| R10(09h) | CLSH_SE<br>NSE_CTR<br>L1 |                  | RESERVED               |                                 |                            |                           | REFN_S<br>EL_PWD         | REFP_SE<br>L_PWD                | HPSENS<br>E_HALF<br>CUR    | HPSENS<br>E_PWD         | 0h      |
| R11(OAh) | CLSH_SE<br>NSE_CTR<br>L2 |                  | HP_REFNS_SEL           |                                 | HP_REFNI_SEL               |                           | HP_REFPS_SEL             |                                 | HP_REFPI_SEL               |                         | 0h      |
| R12(0Bh) | HI_CUR_C<br>TRL1         |                  |                        |                                 | SW1_SW<br>4_KILL_E<br>N    | SW_INVE<br>RT_KILL_<br>EN | SW1_W<br>EAK_ST<br>RONGB | STARTUP<br>_ONESH<br>T_RSTB     | STARTU<br>P_CNT_<br>64_32B | STARTU<br>P_SW_E<br>N   | 37h     |
| R13(0Ch) | HI_CUR_C<br>TRL2         |                  |                        |                                 |                            |                           | SW_REFNS_SEL             |                                 | SW_REFPI_SEL               |                         | 0h      |
| R14(0Dh) | CP_SCUR<br>_CTRL1        |                  |                        |                                 |                            |                           | VCHP_S<br>C_RSTB         | VCHP_SC<br>_PWD                 | VCHP_S<br>C_BYPS           | VCHP_S<br>C_HALF<br>CUR | 08h     |
| R15(0Eh) | CP_SCUR<br>_CTRL2        |                  | SC_REFPI_SEL           |                                 | SC_REFPS_SEL               |                           | SC_REFNI_SEL             |                                 | SC_REFNS_SEL               |                         | 80h     |
| R16(0Fh) | CP_REG_<br>CTRL1         |                  |                        |                                 |                            |                           | CLKREG<br>_RSTB          | CLKREG_<br>PWD                  | CLKREG<br>_BYPS            | CLKREG<br>_HALFC<br>UR  | 08h     |
| R17(10h) | CP_REG_<br>CTRL2         |                  |                        |                                 | CLKREG_REFP_SEL            |                           | CLKREG_REFNI_SE<br>L     |                                 | CLKREG_REFNS_S<br>EL       |                         | 0h      |

# TSDP11xx / TSDP10xx

## Class-H DirectConnect Headphone Amplifier

| Register | Name            | Remarks           | Bit[7]                | Bit[6]               | Bit[5]            | Bit[4]          | Bit[3]           | Bit[2]              | Bit[1]               | Bit[0]             | Default |
|----------|-----------------|-------------------|-----------------------|----------------------|-------------------|-----------------|------------------|---------------------|----------------------|--------------------|---------|
| R18(11h) | HDPH_CTL1       |                   | HP_ILIM               |                      | HPL_PWD           | HPR_PWD         | HP_PWD_OVRD      | HP_ANTIP_OP_BYPASS  | HPL_MUTE             | HPR_MUTE           | C0h     |
| R19(12h) | HDPH_CTL2       |                   | BST_HP_GAIN           | HP_DISCH_OP_ANTIP_OP | HP_DISCH_OPAMP    | HP_CNT_TARGET_L |                  |                     |                      |                    | 70h     |
| R20(13h) | HDPH_CTL3       |                   |                       | REDUCE_HP_IBAT       | HP_D3             | HP_CNT_TARGET_R |                  |                     |                      |                    | 10h     |
| R21(14h) | HDPH_CTL4       |                   | HP_ANTIP_POP_CNT_LOAD | HP_ANTIP_OP_CNT_HOLD | HP_ANTIP_POP_RSTB | HP_OUT_GND_REG  | HPOUT_GND_OVRD   | HP_AMP_N_GND_REG    | HP_AMP_IN_GND_OVRD   | HP_CONNECT_GND_VAG | 21h     |
| R22(15h) | SELFOSC_CTRL1   |                   | SELFOSC_DIVCLK_SEL    |                      | SELFOSC_VCHP_SEL  |                 | SELFOSC_FERQ_SEL |                     |                      |                    | 05h     |
| R23(16h) | SELFOSC_CTRL2   |                   |                       |                      |                   | SELFOSC_PWD     | SELFOSC_RSTB     | SELFOSC_CHPCLK_PWDB | SELFOSC_AOPCLK_PWD_B | SELFOSC_AOPCLK_SEL | 0Ah     |
| R24(17h) | BIASG_CTL1      |                   | IBIAS_NONDAC          |                      |                   |                 | IBIAS_SEL        |                     | IBIAS_REF_CORE_PWD   | IBIAS_GEN_MUX      | 0h      |
| R25(18h) | BIASG_CTL2      |                   |                       |                      |                   |                 |                  |                     |                      | POR                | 0h      |
| R26(19h) | REF_SUPPLY_CTRL |                   |                       |                      |                   |                 | REFSUPPLY_PWD    | SUPOVR_VAL          | SUPOVR_EN            | INVERT_SUPPLY_OSC  | 0h      |
| R27(1Ah) | BANGAP_CTRL     |                   |                       |                      |                   |                 |                  | BGCORE_BYPS         |                      | BGCORE_IBIAS_MUX   | 0h      |
| R28(1Bh) | TEMPSENSE_CTL1  | TEMPATURE Control | HI_TEMP_SEL           |                      |                   | IO_TEMP_SEL     |                  |                     | VBG_TRIM_SEL         |                    | 69h     |
| R29(1Ch) | TEMPSENSE_CTL2  |                   |                       |                      |                   |                 |                  | TS_TEST_MODE        | TEMPSENSE_PWD        | TEMPSENSE_RSTB     | 01h     |
| R30(1Dh) | PAD_CTRL        |                   | SD_B_PUB              | SD_B_PD              | I2C_DATA_PUB      | I2C_DATA_PD     | I2C_CLK_PUB      | I2C_CLK_PD          | CLK_DEGLITCH_BYPS    | DATA DEGLITCH_BYPS | C0h     |
| R31(1Eh) | SHUTDOWN        |                   |                       |                      |                   |                 |                  |                     |                      | SHUTDOWN_B         | 01h     |
| R32(1Fh) | SPARE2          |                   | TST                   |                      |                   |                 |                  |                     |                      |                    | 0h      |
| R33(1Gh) | SPARE2          |                   | TST                   |                      |                   |                 |                  |                     |                      |                    | 0h      |

**Table 23. TSDP11xx Register Map**

**Notes:**

- 1 Registers not described in this map should be considered "reserved".

6. PIN CONFIGURATION AND DESCRIPTION

6.1. TSDP10xx 20-Pin QFN

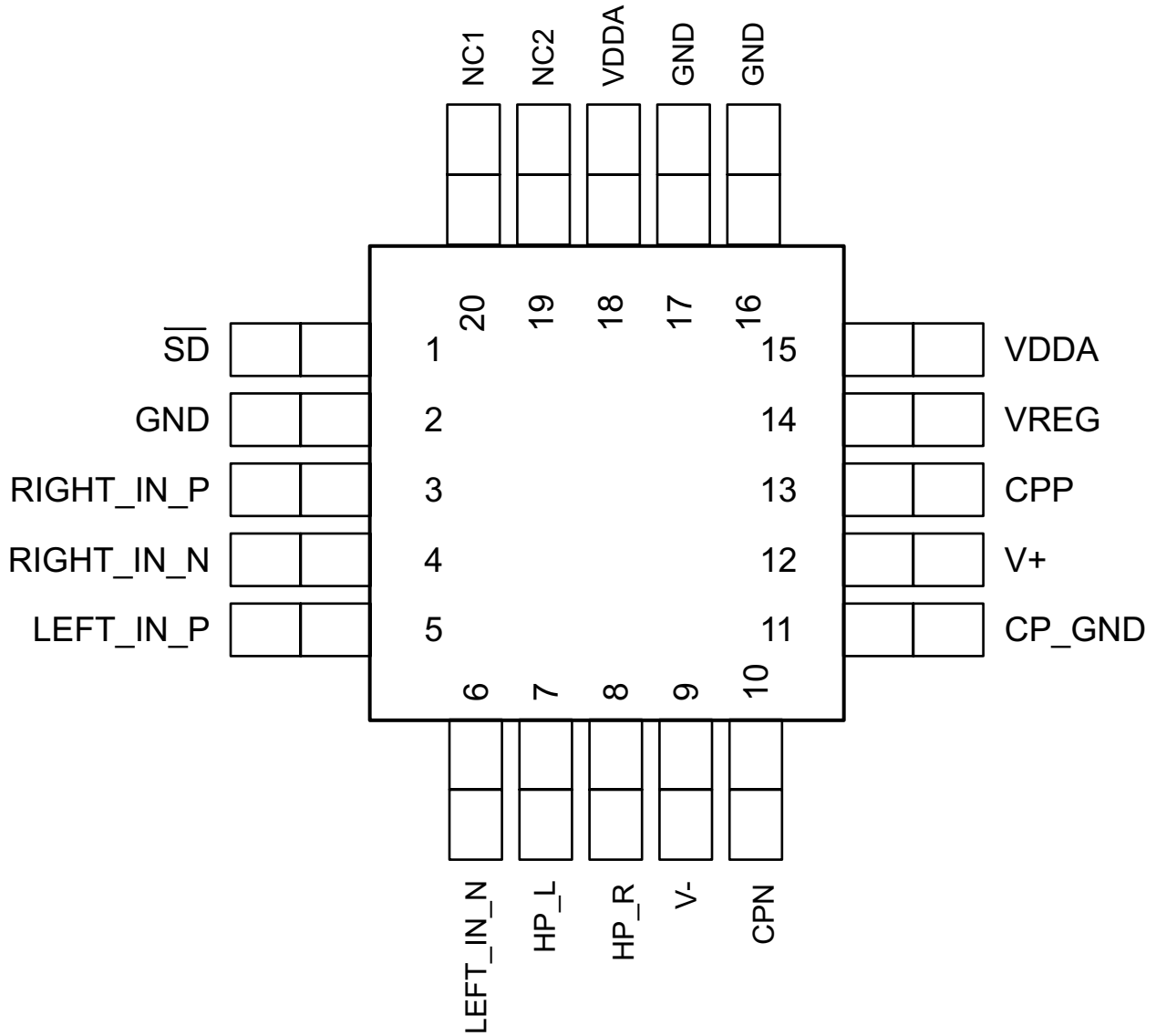


Figure 8. TSDP10xx 20-Pin QFN Pinout



6.2. TSDP11xx 20-Pin QFN

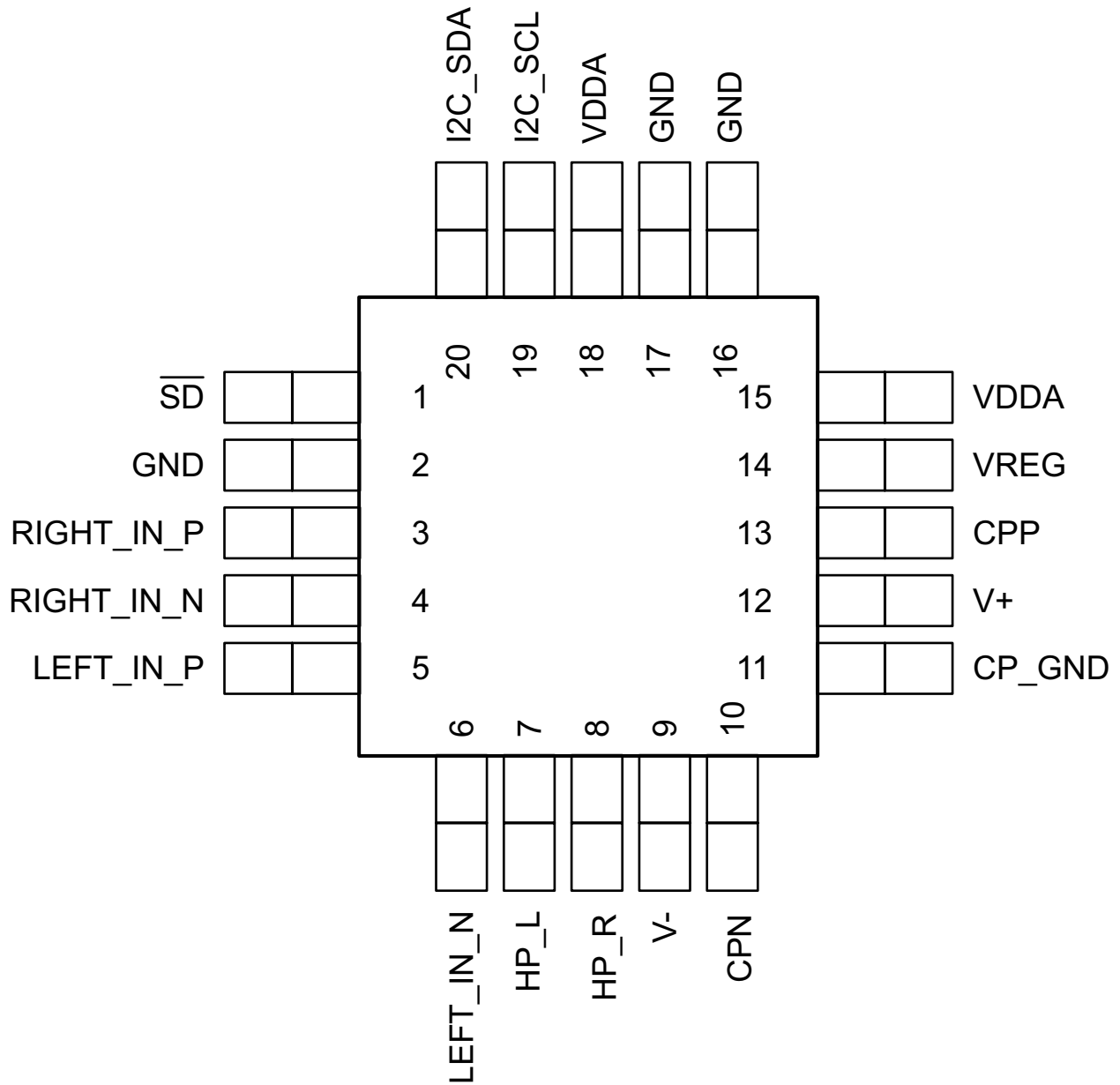


Figure 9. TSDP11xx 20-Pin QFN Pinout

### 6.3. Pin Description Tables for TSDP1xx Family of Devices

#### 6.3.1. Power Pins

| Pin Name | Pin Function                        | I/O        | Internal Pull-up<br>Pull-down | Pin<br>locations |
|----------|-------------------------------------|------------|-------------------------------|------------------|
| VDDA     | Positive supply                     | I(Power)   | -                             | 15, 18           |
| GND      | Ground supply                       | I(Power)   | -                             | 2,16,17          |
| V+       | Charge pump positive supply         | I(Power)   | -                             | 12               |
| V-       | Charge pump negative supply         | I(Power)   | -                             | 9                |
| CPP      | Charge pump positive fly cap        | I/O(Power) | -                             | 13               |
| CPN      | Charge pump negative fly cap        | I/O(Power) | -                             | 10               |
| VREG     | Regulator positive power output     | I/O(Power) |                               | 14               |
| CP_GND   | Charge pump output ground reference | I(Power)   | -                             | 11               |

Table 24. Power Pins

#### 6.3.2. Analog Input

| Pin Name   | Pin Function               | I/O       | Internal Pull-up<br>Pull-down | Pin<br>locations |
|------------|----------------------------|-----------|-------------------------------|------------------|
| LEFT_IN_P  | Left Audio Positive Input  | I(Analog) | None                          | 5                |
| LEFT_IN_N  | Left Audio Negative Input  | I(Analog) | None                          | 6                |
| RIGHT_IN_P | Right Audio Positive Input | I(Analog) | None                          | 3                |
| RIGHT_IN_N | Right Audio Negative Input | I(Analog) | None                          | 4                |

Table 25. Analog Input Pins

#### 6.3.3. Analog Output

| Pin Name | Pin Function                                     | I/O       | Internal Pull-up<br>Pull-down | Pin<br>locations |
|----------|--|-----------|-------------------------------|------------------|
| HP_L     | Audio Headphone Output Left - ground referenced  | O(Analog) | None                          | 7                |
| HP_R     | Audio Headphone Output Right - ground referenced | O(Analog) | None                          | 8                |

Table 26. Analog Output Pins

#### 6.3.4. TSDP11xx Serial Data and Shutdown Control

| Pin Name        | Pin Function   | I/O          | Internal Pull-up<br>Pull-down | Pin<br>locations |
|-----------------|--|--------------|-------------------------------|------------------|
| I2C_SCL         | I <sup>2</sup> C shift clock for serial control port | I(Digital)   | Pull-Up                       | 19               |
| I2C_SDA         | I <sup>2</sup> C shift data for serial control port  | I/O(Digital) | Pull-Up                       | 20               |
| $\overline{SD}$ | Shutdown Control for chip                            | I(Digital)   | Pull-Down                     | 1                |

Table 27. TSDP11xx Data and Control Pins

## TSDP11xx / TSDP10xx

### Class-H DirectConnect Headphone Amplifier

#### 6.3.5. TSDP10xx No Connects & Shutdown Control

| Pin Name               | Pin Function                     | I/O        | Internal Pull-up<br>Pull-down | Pin<br>locations |
|------------------------|----------------------------------|------------|-------------------------------|------------------|
| NC1                    | No Connect 1                     |            | Pull-Up                       | 19               |
| NC2                    | No Connect 2                     |            | Pull-Up                       | 20               |
| $\overline{\text{SD}}$ | <b>Shutdown Control</b> for chip | I(Digital) | Pull-Down                     | 1                |

Table 28. TSDP10x Data and Control Pins

## TSDP11xx / TSDP10xx

### Class-H DirectConnect Headphone Amplifier

#### 6.4. TSDP11xx Pin Function

| Pin | Name            | Input/Output Power | Description & Layout Recommendations  |
|-----|-----------------|--------------------|---|
| 1   | $\overline{SD}$ | I (DIG)            | Shutdown. $\overline{SD}$ is active low. $\overline{SD}$ turns the IC on and off. When $\overline{SD}$ is low, the device is in shutdown mode and the jack insertion detect circuitry is active. $\overline{SD}$ has to be high to turn on the device and run algorithm. Typically, $\overline{SD}$ is held low until the system gets an interrupt from the IC, indicating that a jack has been inserted. The system then pulls $\overline{SD}$ high.<br><br>0 = The IC is in shutdown mode<br>1 = The IC is active. The algorithm runs immediately after a load has been detected. |
| 2   | GND             | P (GND)            | Headphone Ground Reference. This need to be very clean ground for best results.   |
| 3   | RIGHT_IN_P      | I (ANA)            | Headphone Right Positive Differential Input   |
| 4   | RIGHT_IN_N      | I (ANA)            | Headphone Right Negative Differential Input   |
| 5   | LEFT_IN_P       | I (ANA)            | Headphone Left Positive Differential Input  |
| 6   | LEFT_IN_N       | I (ANA)            | Headphone Left Negative Differential Input  |
| 7   | HP_L            | O (ANA)            | Headphone Left Output   |
| 8   | HP_R            | O (ANA)            | Headphone Right Output  |
| 9   | V-              | P                  | Charge Pump Negative Power Output. Connect one side of 5 $\mu$ F capacitor to V_NEG and the other side to GND_CP.   |
| 10  | CPN             | P                  | Charge Pump Negative Fly Cap. Connect one side of 5 $\mu$ F capacitor to FCAP_1 (pin 13) and the other side to FCAP_2 (pin 10) with wide traces.  |
| 11  | CP_GND          | P (GND)            | Charge Pump Output Ground Reference   |
| 12  | V+              | P                  | Charge Pump Positive Power Output. Connect one side of 5 $\mu$ F capacitor to V+ and the other side to CP_GND (pin 11).   |
| 13  | CPP             | P                  | Charge Pump Positive Fly Cap. Connect one side of 5 $\mu$ F capacitor to CPN (pin 10) and the other side to CPP (pin 13) with wide traces.  |
| 14  | VREG            | P                  | Regulator Positive Power Output. Connect 10uF cap to GND (pin 16)   |
| 15  | VDDA            | P (VDD)            | Regulator Input Positive Power. Connect 10uF cap to GND (pin 16)  |
| 16  | GND             | P (GND)            | Regulator Input Ground Reference  |
| 17  | GND             | P (GND)            | Clean Analog Ground   |
| 18  | VDDA            | P (VDD)            | Clean Analog Power—Battery or regulated supply. A separate 1 $\mu$ F decoupling cap must be connected directly from VDDA (pin18) to GND (pin 17).   |
| 19  | I2C_SCL         | I (DIG)            | I2C Serial Clock Input For Register Read/Write  |
| 20  | I2C_SDA         | I/O (DIG)          | Serial Data I/O. Register Interface   |

Table 29. TSDP11xx Pin Function

## 6.5. TSDP10xx Pin Function

| Pin | Name            | Input/Output Power | Description & Layout Recommendations   |
|-----|-----------------|--------------------|--|
| 1   | $\overline{SD}$ | I (DIG)            | Shutdown. $\overline{SD}$ is active low. $\overline{SD}$ turns the IC on and off. When $\overline{SD}$ is low, the device is in shutdown mode and the jack insertion detect circuitry is active. $\overline{SD}$ has to be high to turn on the device and run algorithm. Typically, $\overline{SD}$ is held low until the system gets an interrupt from the IC, indicating that a jack has been inserted. The system then pulls $\overline{SD}$ high.<br><br>0 = The IC is in shutdown mode 1 = The IC is active. The algorithm runs immediately after a load has been detected. |
| 2   | GND             | P (GND)            | Headphone Ground Reference. This need to be very clean ground for best results.  |
| 3   | RIGHT_IN_P      | I (ANA)            | Headphone Right Positive Differential Input  |
| 4   | RIGHT_IN_N      | I (ANA)            | Headphone Right Negative Differential Input  |
| 5   | LEFT_IN_P       | I (ANA)            | Headphone Left Positive Differential Input   |
| 6   | LEFT_IN_N       | I (ANA)            | Headphone Left Negative Differential Input   |
| 7   | HP_L            | O (ANA)            | Headphone Left Output  |
| 8   | HP_R            | O (ANA)            | Headphone Right Output   |
| 9   | V-              | P                  | Charge Pump Negative Power Output. Connect one side of 5 $\mu$ F capacitor to V_NEG and the other side to GND_CP.  |
| 10  | CPN             | P                  | Charge Pump Negative Fly Cap. Connect one side of 5 $\mu$ F capacitor to FCAP_1 (pin 13) and the other side to FCAP_2 (pin 10) with wide traces.   |
| 11  | CP_GND          | P (GND)            | Charge Pump Output Ground Reference  |
| 12  | V+              | P                  | Charge Pump Positive Power Output. Connect one side of 5 $\mu$ F capacitor to V+ and the other side to CP_GND (pin 11).  |
| 13  | CPP             | P                  | Charge Pump Positive Fly Cap. Connect one side of 5 $\mu$ F capacitor to CPN (pin 10) and the other side to CPP (pin 13) with wide traces.   |
| 14  | VREG            | P                  | Regulator Positive Power Output. Connect 10uF cap to GND (pin 16)  |
| 15  | VDDA            | P (VDD)            | Regulator Input Positive Power. Connect 10uF cap to GND (pin 16)   |
| 16  | GND             | P (GND)            | Regulator Input Ground Reference   |
| 17  | GND             | P (GND)            | Clean Analog Ground  |
| 18  | VDDA            | P (VDD)            | Clean Analog Power—Battery or regulated supply. A separate 1 $\mu$ F decoupling cap must be connected directly from VDDA (pin18) to GND (pin 17).  |
| 19  | NC1             |                    | No Connect. Pins already have internal pull-ups.   |
| 20  | NC2             |                    | No Connect. Pins already have internal pull-ups.   |

Table 30. TSDP10xx Pin Function

## TSDP11xx / TSDP10xx

### Class-H DirectConnect Headphone Amplifier

#### 6.6. ELECTRICAL CHARACTERISTICS

$V_{DD}=5V$ ,  $T_A=25C$ ,  $GND=0$ ,  $R_L = 16\Omega$  (unless otherwise noted)

| Parameters                       | Symbol    | Conditions                | Min | Typ          | Max | Units   |
|----------------------------------|-----------|---------------------------|-----|--------------|-----|---------|
| Supply Voltage Range             | $V_{DD}$  |                           | 2.5 |              | 5.5 | V       |
| TSDP10x Quiescent Supply Current |           | One channel enabled       |     | 11           | 11  | mA      |
|                                  |           | Two channels enabled      |     | 22           | 22  |         |
| TSDP11x Quiescent Supply Current |           | One channel enabled       |     | 11*          | 11  | mA      |
|                                  |           | Two channels enabled      |     | 22*          | 22  |         |
| Shutdown Supply Current          |           |                           |     | >1           |     | $\mu A$ |
| Shutdown Threshold               |           | $V_{IH}$                  |     | 0.7 x<br>VDD |     | V       |
|                                  |           | $V_{IL}$                  |     | 0.3 x<br>VDD |     |         |
| Shutdown Input Leakage Current   |           |                           |     | >1           |     | $\mu A$ |
| Shutdown to full Operation       |           | No click-and-pop start-up |     | 30           |     | ms      |
| <b>CHARGE PUMP</b>               |           |                           |     |              |     |         |
| Oscillator Frequency             | $F_{osc}$ |                           |     | 830          | 970 | kHz     |
| <b>AMPLIFIERS</b>                |           |                           |     |              |     |         |
| Input Offset Voltage             | $V_{os}$  |                           |     | 0.1          |     | $\mu V$ |
| DC Power supply rejection ratio  | PSSR      |                           |     | -90          |     | dB      |
| Power supply rejection ratio     | CMRR      |                           |     | -101         |     | dB      |
| Output Power                     | $P_{OUT}$ | $R_L=16\Omega$            |     | 143          |     | mW      |
|                                  |           | $R_L=32\Omega$            |     | 93           |     |         |
|                                  |           | $R_L=10K\Omega$           |     | 0.395        |     |         |

Table 31. Electrical Characteristics

#### 6.7. OPERATING CHARACTERISTICS

$V_{DD}=5V$ ,  $T_A=25C$ ,  $GND=0$ ,  $R_L = 16\Omega$  (unless otherwise noted)

| Parameter                         | Symbol | Conditions                          | Min | Typ   | Max | Units      |
|-----------------------------------|--------|-------------------------------------|-----|-------|-----|------------|
| Signal-to-Noise Ratio             | SNR    | A-weighted; 0dB gain                |     | 104   |     | dB         |
| Total Harmonic Distortion + Noise | THD+N  | $R_L = 32\Omega$ , $P_{OUT} = 25mW$ |     | 0.008 |     | %          |
|                                   |        | $R_L = 16\Omega$ , $P_{OUT} = 50mW$ |     | 0.008 |     |            |
| Slew Rate                         | SR     |                                     |     | 0.95  |     | V/ $\mu s$ |
| Maximum Capacitive Load           | $C_L$  | No sustained oscillations           |     | 300   |     | pF         |
| Crosstalk                         |        |                                     |     | 90    |     | dB         |

Table 32. Operating Characteristics

## 7. CHARACTERISTICS

### 7.1. Audio Fidelity

SNR: > -105dB, A-Weighted, 5.0V

### 7.2. Electrical Specifications

#### 7.2.1. Absolute Maximum Ratings:

|                                       |                          |
|---------------------------------------|--------------------------|
| Voltage on any pin relative to Ground | Vss - 0.3V TO Vdd + 0.5V |
| Industrial Temperature                | -40 °C TO 85 °C          |
| Storage Temperature                   | -65 °C TO +150 °C        |
| Soldering Temperature                 | 260 °C                   |
| Headphone Output Current              | 230mA                    |
| Maximum Supply Voltage                | 5.5 Volts = VDD          |

**Table 33. Absolute Maximum Ratings**

### 7.3. Recommended Operating Conditions

| Parameter              | Min | Typ | Max | Unit |
|------------------------|-----|-----|-----|------|
| Power Supplies         |     |     |     |      |
| VDD                    | 2.5 | 5.0 | 5.5 | V    |
| Industrial Temperature | -40 | 25  | 85  | °C   |
| T <sub>j</sub>         |     |     | 150 | °C   |

**Table 34. Recommended Operating Conditions**

*Note: **ESD:** The TSDP11xx / TSDP10xx is an ESD (Electrostatic discharge) sensitive device. Even though the TSDP11xx / TSDP10xx family implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.*

**TSDP11xx / TSDP10xx**  
**Class-H DirectConnect Headphone Amplifier**

**7.4. Characteristics**

Test Conditions:

Unless stated otherwise, VDD=5.0V, TA=+25C, 997Hz signal, Input Signal=0.44VRMS,

| Parameter   | Symbol            | Test Conditions                               | Min             | Typ  | Max             | Unit        |
|---|-------------------|---|-----------------|------|-----------------|-------------|
| <b>Analog Inputs (L<sub>INP</sub>, L<sub>INN</sub>, R<sub>INP</sub>, R<sub>INN</sub>)</b> |                   |   |                 |      |                 |             |
| Full Scale Input Voltage  | V <sub>FSIV</sub> | L/R <sub>INx</sub> Differential Mic           |                 | 1.00 | .               | Vrms<br>dBV |
| Input Impedance   |                   |   |                 | 50   |                 | KΩ          |
| Input Capacitance   |                   |   |                 | 10   |                 | pF          |
| <b>Volume Control</b>   |                   |   |                 |      |                 |             |
| Programmable Gain Min   |                   |   |                 | 0    |                 | dB          |
| Programmable Gain Max   |                   |   |                 | 6    |                 | dB          |
| Programmable Gain Step Size   |                   |   |                 | 2    |                 | dB          |
| <b>Headphone Outputs (HPL, HPR)</b>   |                   |   |                 |      |                 |             |
| Full Scale Output Level   | V <sub>FSOV</sub> | R <sub>L</sub> = 10KΩ                         |                 | 2.0  |                 | Vrms        |
|   |                   | R <sub>L</sub> = 16Ω                          |                 | 1.6  |                 | Vrms        |
| Output Power  | P <sub>O</sub>    | 997Hz full scale signal, R <sub>L</sub> = 16Ω |                 | 167  |                 | mW<br>(avg) |
| Signal to Noise Ratio   | SNR               | A-weighted, R <sub>L</sub> = 16Ω              |                 | -105 |                 | dB          |
| Total Harmonic Distortion +Noise  | THD+N             | R <sub>L</sub> = 16Ω, -3dBFS                  |                 | -72  |                 | dB          |
|   |                   | R <sub>L</sub> = 16Ω, -6dBFS                  |                 | -78  |                 | dB          |
|   |                   | R <sub>L</sub> = 32Ω, -3dBFS                  |                 | -75  |                 | dB          |
|   |                   | R <sub>L</sub> = 32Ω, -6dBFS                  |                 | -80  |                 | dB          |
| <b>Digital Input/Output</b>   |                   |   |                 |      |                 |             |
| Input Capacitance   |                   |   |                 | 5    |                 | pF          |
| Input Leakage   |                   |   | -0.9            |      | 0.9             | uA          |
| <b>DC Characteristics for SD</b>  |                   |   |                 |      |                 |             |
| Input High Level  | VIH               |   | 0.7x<br>DVDD_IO |      |                 | V           |
| Input LOW Level   | VIL               |   |                 |      | 0.3x<br>DVDD_IO | V           |
| <b>DC Characteristics for SCL and SDA</b>   |                   |   |                 |      |                 |             |
| Input High Level  | VIH               |   | 0.7x<br>DVDD_IO |      |                 | V           |
| Input LOW Level   | VIL               |   |                 |      | 0.3x<br>DVDD_IO | V           |
| Output Low Level  | VOL               | IOL = 1mA                                     |                 |      | 0.1xDVDD_IO     | V           |
| <b>ESD / Latchup</b>  |                   |   |                 |      |                 |             |
| IEC1000-4-2   |                   |   | 1               |      |                 | Level       |
| JESD22-A114-B   |                   |   | 2               |      |                 | Class       |
| JESD22-C101   |                   |   | 4               |      |                 | Class       |

**Table 35. Characteristics**



## **7.5. Low Power Mode Power Consumption**

*Note: The TSDP11xx can support lower power modes via I2C register writes. Please contact [support@temposemi.com](mailto:support@temposemi.com) to get the specific configuration settings that are optimized for your target load, voltage rail and maximum acceptable THD+N performance.*

## TSDP11xx / TSDP10xx

### Class-H DirectConnect Headphone Amplifier

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#### 8. ORDERING GUIDE

|                   |  |
|-------------------|--|
| TSDP10XX1NBGXZBX  | Commercial Temp (0C to 70C), Fixed Function, Tray          |
| TSDP11XX1NBGXZBX  | Commercial Temp (0C to 70C), I2C Control, Tray             |
| TSDP10XX1NBGIZBX  | Industrial Temp (-40C to 85C), Fixed Function, Tray        |
| TSDP11XX1NBGIZBX  | Industrial Temp (-40C to 85C), I2C Control, Tray           |
| TSDP10XX1NBGXZBX8 | Commercial Temp (0C to 70C), Fixed Function, Tape & Reel   |
| TSDP11XX1NBGXZBX8 | Commercial Temp (0C to 70C), I2C Control, Tape & Reel      |
| TSDP10XX1NBGIZBX8 | Industrial Temp (-40C to 85C), Fixed Function, Tape & Reel |
| TSDP11XX1NBGIZBX8 | Industrial Temp (-40C to 85C), I2C Control, Tape & Reel    |

**Table 36. Part Number Table**