Tempo Semiconductor, Inc.

Data Sheet

OCTAL PDM TO 24-BIT TDM CONVERTER

TSDP18xx

GENERAL DESCRIPTION

The TSDP18xx is an ultra low-power, high-performance, 8 channel PDM to Linear PCM converter. It supports Digital MEMS Microphone (DMIC) sampling rates from 8kHz up to 384kHz enabling support for Ultrasonic capable DMICs.

TSDP18xx supports outputting up to 2 channels using the I2S or Left-Justified (LJ) formats as well as up to 8 channels using the Time-Division Multiplexed (TDM) format. The device enables a wide variety of configurations enabling 32-bit, 24-bit or 16-bit word lengths, clock polarity inversion, and more to maximize compatibility with most any DSP, Audio Processor, Codec or SOC.

The supplied DMIC sources are driven by a configurable PDM clock ranging from 256kHz up to 6.144MHz, while the digital audio output port operates in slave mode via supplied SCLK signal ranging from 256kHz up to 49.152MHz and LRCLK / FRMCLK signals.

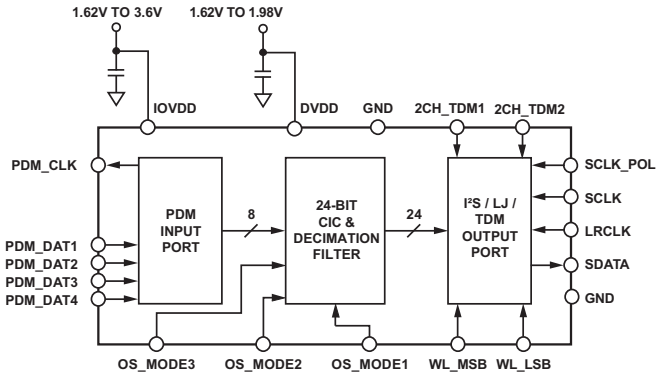
There is a wide range of support for SCLK to LRCLK / FMCLK ratios ranging from 32Fs to 512Fs.

Configuration of the FIR and decimation filter coefficients are based on combination of SCLK to LRCLK / FRMCLK ratio and the three OS_MODE pins which impact the Oversampling Mode, supporting 8x to 256x.

APPLICATIONS

- **1~8 Channel Digital Microphone Arrays including:**
  - Smart Speakers / Smart Screens
  - Voice Assistance Enabled Devices
  - Audio / Video Conferencing Systems
  - Augmented / Virtual Reality Systems
  - Multi-Mic Beam Forming Applications
  - Far Field Voice Pickup Applications
  - Multichannel Audio Recording Applications
- **DSD to PCM Conversion**

BLOCK DIAGRAM



FEATURES

- **High-Fidelity Octal PDM to Linear PCM Converter**
  - 24-bit internal processing with up to 32-bit output words
  - Internal processing takes place at the DMIC clock rate
  - > 142dB SNR / DNR / THD+N Level (20Hz ~ 20kHz)
  - Output Fs supports 8kHz up to 384kHz
  - Configurable DMIC fixed output clock, based on Fs of supplied LRCLK and specified oversampling mode
  - Support for wide range of SLCK to LRCLK / FRMCLK ratios: 32x, 48x, 64x, 96x, 128x, 192x, 256x, 384x, and 512x with automatic detection of SCLK
  - Configurable downsampling rates ranging from 8 to 256 depending on configuration of OS_MODE3, OS_MODE_2, & OS_MODE1 pins as well as SCLK to LRCLK / FRMCLK ratio
- **Configurable I2S / LJ / TDM Output Format Engine**
  - Supports either 2 Channel I2S or LJ output format or TDM format capable of supporting from 2 up to 8 channels of up 32-bit words
  - Supports configurable word lengths of 32-bits, 24-bits, or 16-bits
  - Supports SLCK polarity inversion
  - Supports FRMCLK widths from clock width to word-width
  - Supports I2S using two mono, single-edge clocked PDM DMICs or I2S using two mono DMICs or a stereo, double-edge clocked DMIC
- **Ultra low-power standby and operation**
  - Ultra-low standby (< 1uA) power consumption (when SCLK signal is stopped)
  - Single 1.8V (+/-5%) supply for both IOVDD and DVDD
  - IOVDD can also operate at 3.3V (+/-5%)
  - 2.68mA operating current for 8 Channel TDM mode, Fs = 48kHz, SLCK = 256Fs, IOVdd = 1.8V
- **3x3mm, 20-lead, 0.4mm pitch QFN**
- **Available in both Commercial (0C to 70C) and Industrial Temperature (-40C to 85C) Grades**

1.0 Features & Description

The TSDP18xx is the solution of choice for applications that are employing 1 to 8 DMICs that must undergo 1-bit PDM to Linear PCM conversion. The TSDP18xx supports a wide number of data delivery formats ranging from I2S to LJ to TDM for 1 to 2 channel operation or up to 8 channels (TDM).

The TSDP18xx ensures a long product life cycle by supporting the widest range of DMIC decimated sampling frequencies in the market, ranging from 8kHz up to 384kHz. The device also maximizes the dynamic range of most any 4th or 5th order DMICs used, while decreasing BOM cost, simplifying board layout, reducing pin count and reducing power consumption.

Fs is determined by the supplied LRCLK and SCLK signals as the digital audio output port only operates in slave mode.

Based on one of the following valid SCLK to LRCLK ratios (32x, 48x, 64x, 96x, 128x, 192x, 256x, 384x or 512x), as well as the settings of OS_MODE3, OS_MODE2, OS_MODE1 pins, the TSDP18xx automatically determines the oversampling rate, as well as the correct FIR decimation filter coefficients to be applied.

Valid input SCLK frequencies for the supported sampling frequencies range from 256kHz up to a maximum of 49.152MHz.

The device automatically powers down to use less than 1uA in standby mode and resets when the SCLK signal is removed.

The TSDP18xx comes in a tiny 3x3mm, 20-lead, 0.4mm pitch QFN and requires a single 1.8V rail for both the IOVDD and DVDD supplies. IOVDD can also support 3.3V (+/-5%).

1.1 Configuring I2S, LJ & TDM Operation

The 2CH_TDM1 and 2CH_TDM2 pins enables the designer to be able to select between either 2 channel I2S, using a double-edge clocked stereo PDM source, or two mono single-edged clocked PDM sources. Support for Left-Justified 2 channel output using a double-edged clocked stereo PDM source or up to 8 channel TDM output (again using 4 stereo double-edge clocked PDM sources) is also possible. Please refer to Table 1 below for configuration of these two pins. Note: When in 2 channel mode, the *maximum* SCLK to LRCLK ratio is 256. When in TDM mode, the SCLK to LRCLK ratio must be at least enough to support the number of desired channels at the specified bit width. Support for an odd number of words is possible, however, please note that unused channel / data frames may contain invalid data.

	2CH_TDM1	2CH_TDM2
I2S Mode 0, 1 Channel Output Mode, Double-Edged Clocking on PDM Sources	0	0
I2S Mode 1, 2 Channel Output Mode, Single-Edged Clocking on PDM Sources	0	1
Left-Justified, 2 Channel Output Mode, Double-Edged Clocking on PDM Source	1	0
TDM, up to 8 Channel Output Mode, Double-Edged Clocking on PDM Source	1	1

Table 1. Configuring the PCM Output Format using the 2CH_TDM1 and 2CH_TDM2 Pins

1.2 Configuring SCLK Polarity

If the SCLK_POL pin is held HIGH, the SCLK polarity is inverted from standard I2S or LJ modes, whereby the data is transmitted on the rising edge of SCLK. If the SCLK_POL pin is held LOW, data is transmitted on the falling edge of SCLK.

1.3 Configuring the PCM Word Width

Configuration of the WL_MSB and WL_LSB pins configures the TSDP18xx PCM word length. In order to ensure valid output data and formatting, ensure that an appropriate SCLK to LRCLK ratio is made available to the TSDP18xx in conjunction with an appropriate word length configuration of 32-bits, 24-bits or 16-bits as configured by the WL_MSB and WL_LSB pins as shown in Table 2, regardless of the settings of 2CH_TDM or I2S_LJ pins. For configurations where the PCM Word Length is < 32-bits, the rest of the data out to the 32-bit max word length is zero padded.

	WL_MSB	WL_MSB
PCM Word Length = 32-bits	0	0
PCM Word Length = 24-bits	0	1
Reserved	1	0
PCM Word Length = 16-bits	1	1

Table 2. PCM Word Length Configuration using WL_MSB and WL_LSB Pins

1.4 Configuring the OS_MODE [3:1] pins

The OS_MODE3, OS_MODE2, OS_MODE1 pins configures the TSDP18xx FIR Decimation value for a Typical Fs range as shown below in Table 3. In order to ensure valid output data, the designer must ensure that an valid SCLK to LRCLK ratio is made available to the TSDP18xx. Furthermore, given the supplied SCLK to LRCLK ratio, an appropriate word length configuration of 32-bits, 24-bits or 16-bits as configured by the WL_MSB and WL_LSB pins as shown in Table 2 should be made, regardless of the settings of 2CH_TDM or I2S_LJ pins.

OS_ MODE3	OS_ MODE2	OS_ MODE1	Oversample Rate	Bandwidth at -1dB (Normalized)	Typical Fs Range (kHz)	Valid SCLK / LRCLK Ratios for Corresponding OS_MODE Pin Selection
0	0	0	N/A	N/A	N/A	Reserved
0	0	1	N/A	N/A	N/A	Reserved
0	1	0	8	0.1189	256 to 384	32, 48, 64, 96, 128
0	1	1	16	0.2268	128 to 192	32, 48, 64, 96, 128, 192, 256
1	0	0	32	0.4536	64 to 96	32, 64, 96, 128, 192, 256, 384, 512
1	0	1	48	0.4536	48 to 64	48, 96
1	0	1	64	0.4536	32 to 48	64, 128, 192, 256, 384, 512
1	1	0	96	0.4536	24 to 32	96, 192
1	1	0	128	0.4536	16 to 24	128, 256, 384, 512
1	1	1	192	0.4536	8 to 16	192, 384
1	1	1	256	0.4536	8 to 12	256, 512

Table 3. Configuring the Oversampling Mode using OS_MODE3, OS_MODE2, OS_MODE1 Pins

2.0 Device Characteristics

DVDD_IO = 1.8 V, T_A = 25°C, PDM BCLK Output = 3.072 MHz, LRCLK Input = 48 kHz, TDM format, OS Rate = 64x unless otherwise noted. The PDM audio stream used in the below table was generated by the APx525 PDM Module, with a 5th order noise shaper. Measurements are without A-Weighting or AES-17 filter unless otherwise noted. Due to the fact that the SNR / DNR / THD+N Level (20Hz ~ 20kHz) performance of the TSDP18xx greatly exceeds that of the APx525 PDM Module as well as any available DMIC available on the market today. Please refer to the SNR / DNR / THD+N Level footnote and corresponding performance plots Figure 17, Figure 18 and Figure 19 as to how this measurement was captured.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Digital Input/Output						
Input High Level	V_{IH}		0.7x DVDD_IO			V
Input Low Level	V_{IL}				0.3x DVDD_IO	V
Output High Level	V_{OH}	I_{OH} = -1mA	0.9x DVDD_IO			V
Output Low Level	V_{OL}	I_{OH} = 1mA		0.1x DVDD_IO		V
Input Capacitance				5		pF
Input Leakage, High	I_{IH}	PDM_DAT, SCLK and LRCLK	-0.9		0.9	uA
Input Leakage, Low	I_{IL}	PDM_DAT, SCLK and LRCLK	-0.9		0.9	uA
SDATA Drive Strength				4.5		mA
PDM_CLK Drive Strength				9		mA
Internal Pull-Up Resistor	R_{PU} / R_{PD}	All Digital I/O pins with pull-up or pull-down		50		kΩ
ESD / Latchup						
IEC1000-4-2			1			Level
JESD22-A114-B			2			Class
JESD22-C101			4			Class
Performance						
SNR		20Hz to 20kHz, Ref to 0dB	125.9		126.4	dB
SNR / DNR / THD+N Level[1]		20Hz to 20kHz	141.9		142.4	dB
SNR, A-Weighted		20Hz to 20kHz, Ref to 0dB	130.6		131.5	dB
THD+N Level		20Hz to 20kHz	123		125	dBFS
THD+N Ratio, A-Weighted		20Hz to 20kHz, -60dBFS input	70.3		70.5	dBFS
Oversampling Rate		Depends on OS_MODE Settings	8		256	
Filter Ripple		DC to 0.437 output Fs	-0.15		+0.01	dBFS
Bandwidth		Rolloff at -1dB		0.4536		Fs
Stop-Band				0.566		Fs
Stop-Band Attenuation			79			dB
Gain		PDM to PCM		0		dB
Bit Width		Internal			24	Bits
Bit Width		Output	16		32	Bits
Interchannel Phase				0		Degrees

Table 4. TSDP18xx Device Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Timing						
Minimum dV/dt	dV/dt_{MIN}	0.5x DVDD level must be achieved in at least in 5ms or less	0.18	0.36		V/ms
Start Up	T_{SU}	From 0.9x DVDD and valid SCLK is presented to TSDP18xx to valid PDM_CLK signal is output from TSDP18xx		3		LRCK Cycles
Clocking						
PDM_CLK Output Range	F_{PDM_CLK}	Depends on OS_MODE Settings	0.256		6.144	MHz
LRCLK Input Range	F_{LRCLK}	Depends on OS_MODE Settings	8		384	kHz
SCLK Input Range	F_{SCLK}	Depends on OS_MODE Settings	0.256	3.072	49.152	MHz
SCLK / LRCLK Ratio		Depends on OS_MODE Settings	32		512	

Table 4. TSDP18xx Device Characteristics

1.The > 142dB SNR / DNR / THD+N Level performance number was generated using a generated PDM data source. Please refer to Figure 17, Figure 18, and Figure 19 and the associated Figure text descriptions to learn more about how the PDM data source was generated and also how these measurements were taken.

OS_MODE [3:1]	Decimation Factor	Group (Fixed) Delay	Typical Fs
010	8	4.5 Samples	384kHz
011	16	9.75 Samples	192kHz
1xx	32+	18.375 Samples	< = 96kHz

Table 5. TSDP18xx Group (Fixed) Delay

3.0 Typical Performance Characteristics (from APx525)

DVDD_IO = 1.8 V, T_A = 25°C, PDM BCLK Output = 3.072 MHz, LRCLK Input = 48 kHz, TDM format, OS Rate = 64x unless otherwise noted. PDM Generator is APx525 PDM Module, 5th order noise shaper, without A-Weighting or AES-17 filter unless otherwise noted.

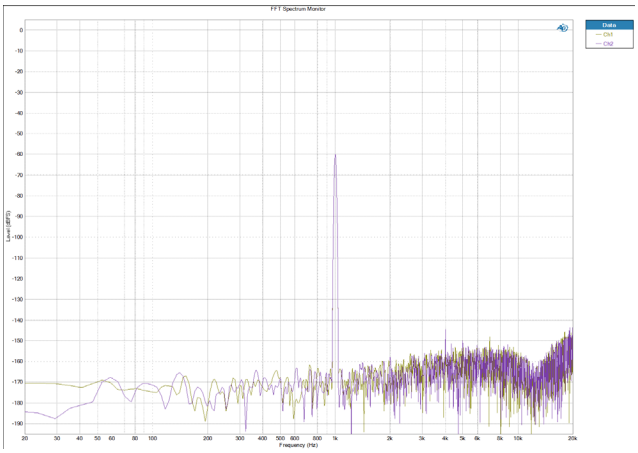


Figure 1. FFT, Fs = 48kHz, -60dBFS Input

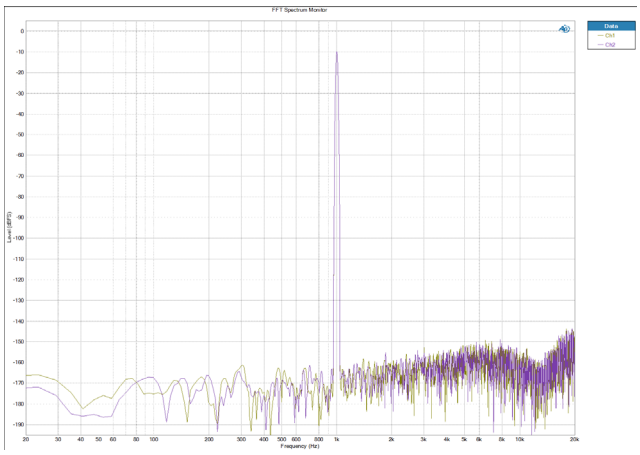


Figure 2. FFT, Fs = 48kHz, -10dBFS Input

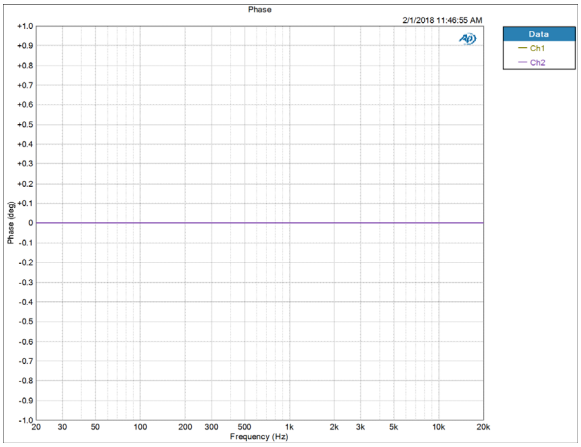


Figure 3. Filter Phase Response, Fs = 48kHz, -10dBFS

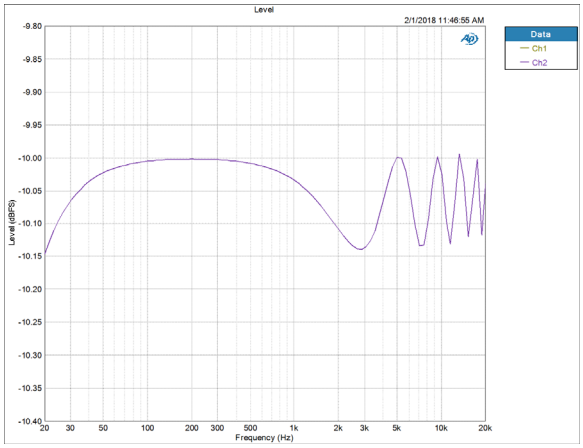


Figure 4. Filter Ripple, Fs = 48kHz, -10dBFS Input

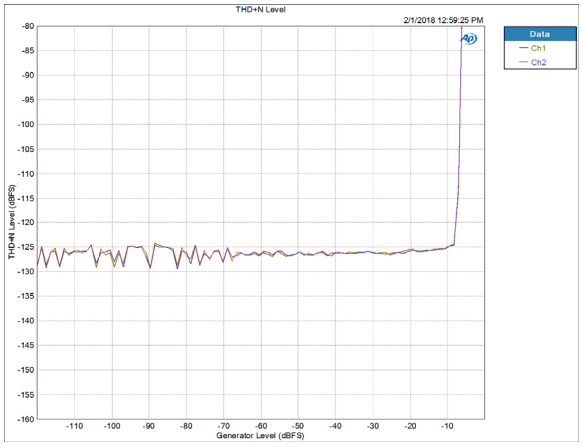


Figure 5. THD+N vs Level, Fs = 48kHz, -120 to 0dBFS

Figure Note: Please note that the reason THD+N vs. Level plot shows a spike in THD+N starting around -7dBFS is due to the fact that the Noise Shaper of the 5th 5th Order PDM Generator module in the APx525 goes unstable above -7dBFS and is not a reflection of the performance of the TSDP18xx.

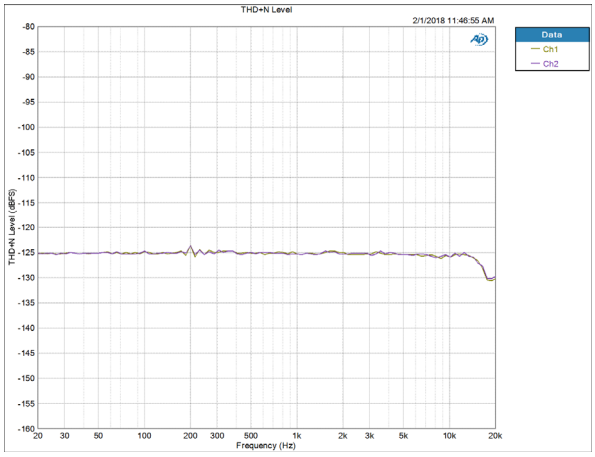


Figure 6. THD+N vs. Frequency, Fs = 48kHz, -10dBFS

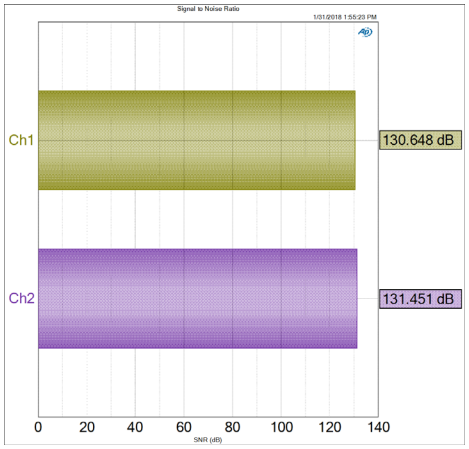


Figure 7. SNR, A-Weighted, Fs = 48kHz, Ref to 0dB

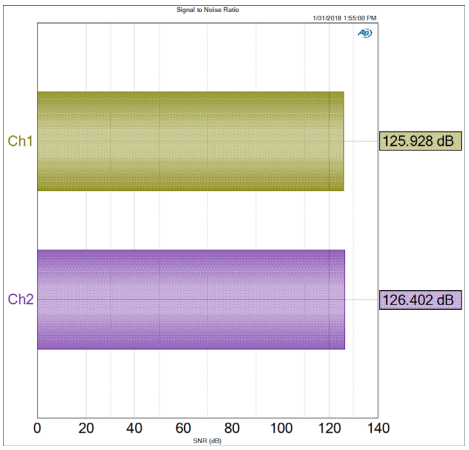


Figure 8. SNR, Unweighted, Fs = 48kHz, Ref to 0dB

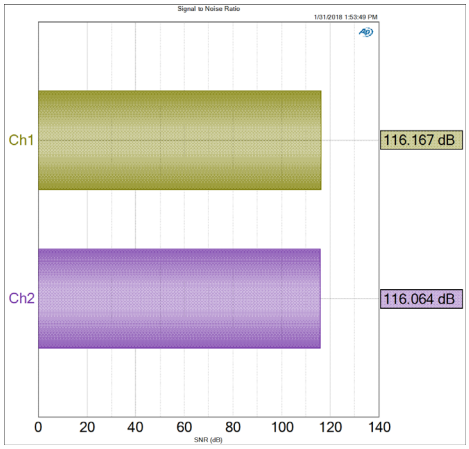


Figure 9. SNR, Unweighted, Fs = 48kHz, -10dBFS Input

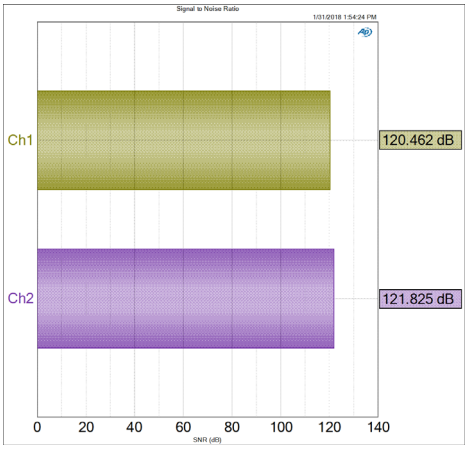


Figure 10. SNR, A-Weighted, Fs = 48kHz, -10dBFS Input

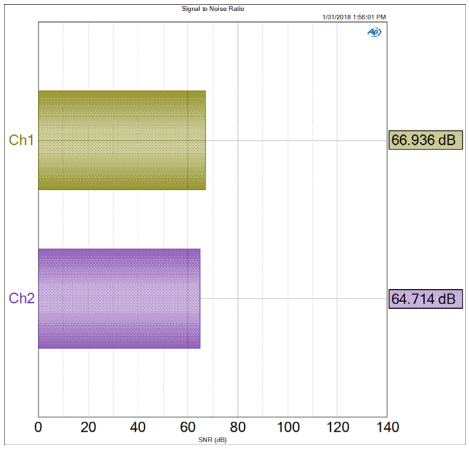


Figure 11. SNR, Unweighted, Fs = 48kHz, -60dBFS Input

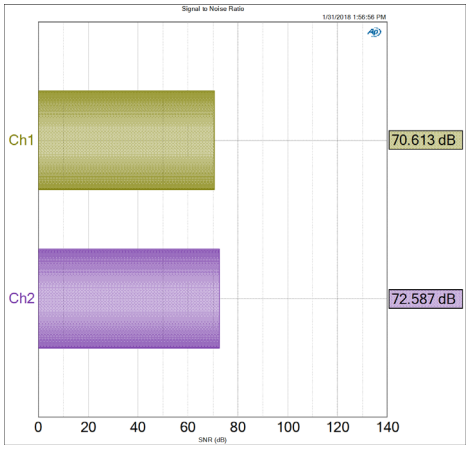


Figure 12. SNR, A-Weighted, Fs = 48kHz, -60dBFS Input

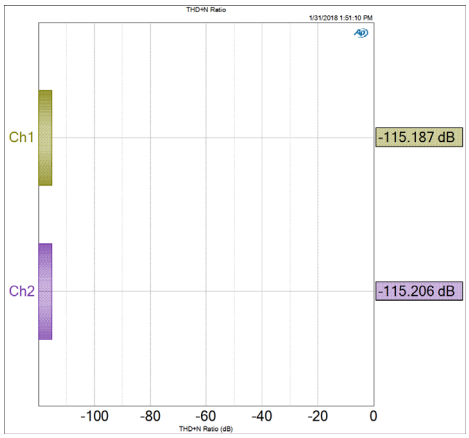


Figure 13. THD+N, Unweighted, Fs = 48kHz, -10dBFS Input

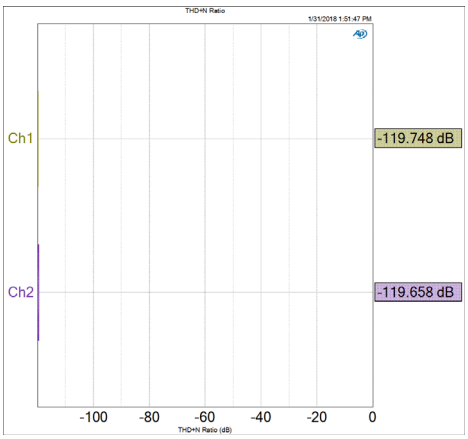


Figure 14. THD+N, A-Weighted, Fs = 48kHz, -10dBFS Input

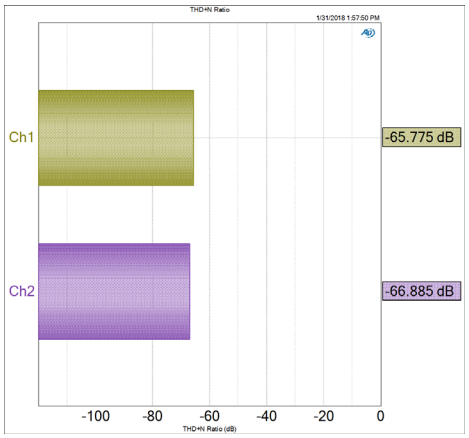


Figure 15. THD+N, Unweighted, Fs = 48kHz, -60dBFS Input

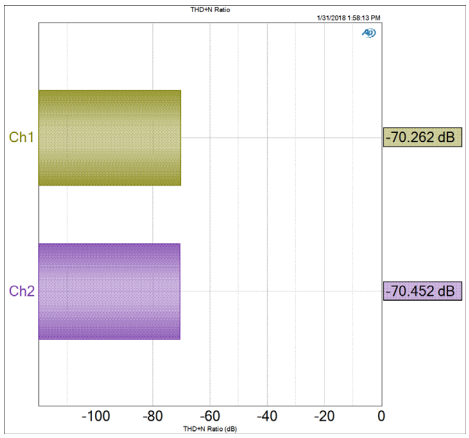


Figure 16. THD+N, A-Weighted, Fs = 48kHz, -60dBFS Input

3.1 Typical Performance Characteristics (from Generated PDM Source)

DVDD_IO = 1.8 V, T_A = 25°C, PDM BCLK Output = 3.072 MHz, LRCLK Input = 48 kHz, I2S format, OS Rate = 64x. The PDM signal was generated from a 286-bit repeating digital signal, with a 10.745kHz fundamental. It was generated by taking a 5th order modulator module of a 3072 / 286kHz input. This 286-bit repeating generated output file was then used as the signal source (as shown in Figure 17) sent from the APx525 into the TSDP18xx, with the Linear PCM I2S formatted output sent back into the APx525, with an AES-17 20kHz brick wall filter applied, but no A-Weighting.

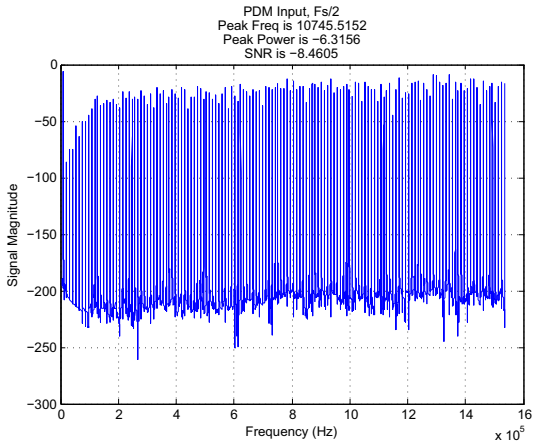


Figure 17. 286-bit repeating PDM Source carrying a 10.745kHz sine wave

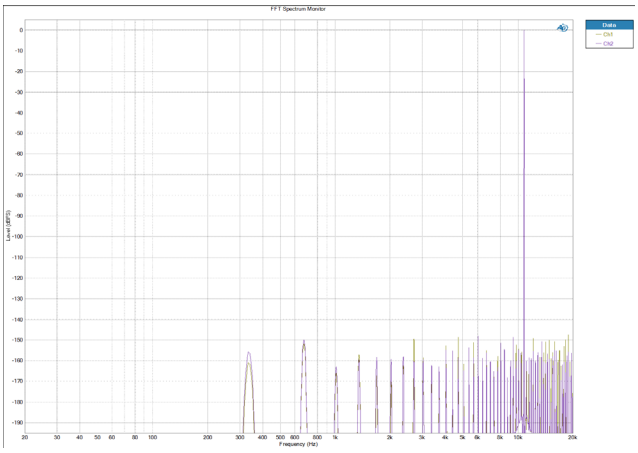


Figure 18. FFT, Fs = 48kHz, 0dBFS, 10.745kHz sine wave, Converted Linear PCM I2S Output from TSDP18xx

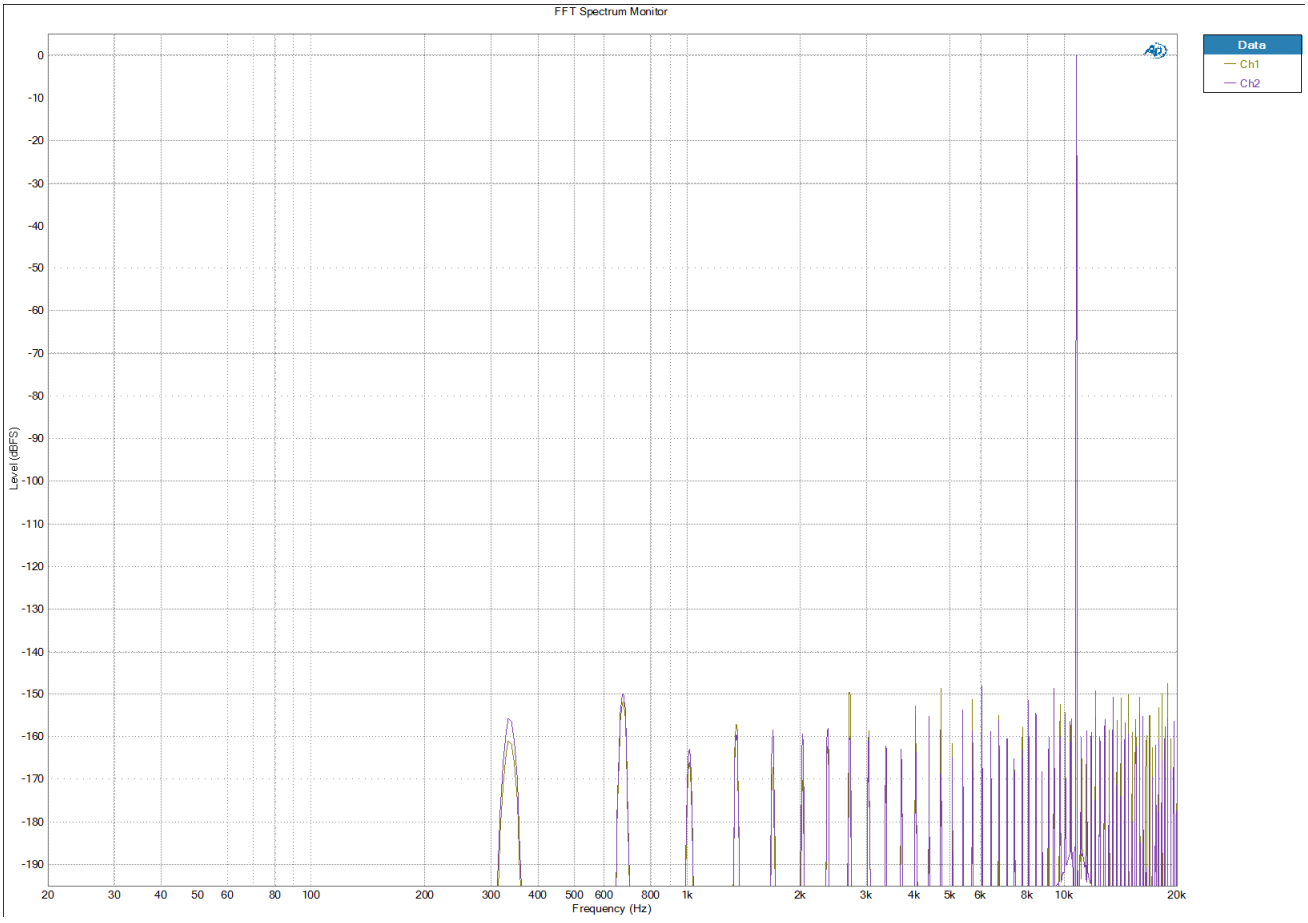


Figure 19. Zoom In of Figure 18

4.0 QFN Package Lead Configuration and Function Descriptions

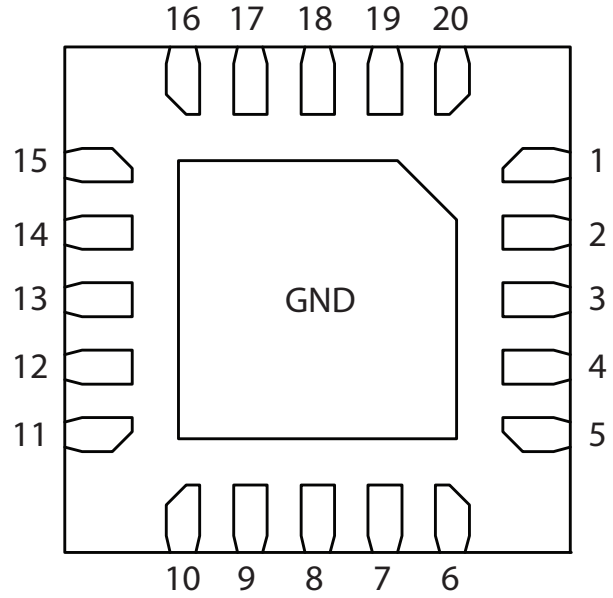
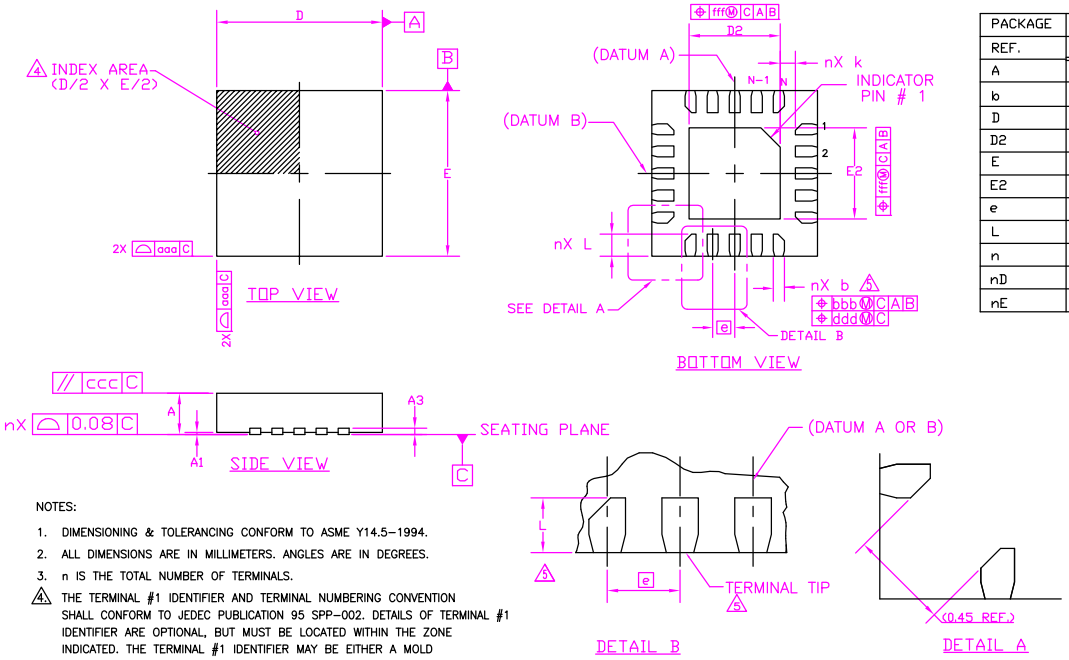


Figure 20. TSDP18xx QFN Package Lead Configuration

Lead Count	Signal Name	Type	Description
1	SCLK_POL	Input	If HIGH, the SCLK polarity is inverted from standard I2S, LJ or TDM modes, whereby the data is transmitted on the rising edge of SCLK and sampled on the falling edge of SCLK.
2	2CH_TDM2	Input	2CH_TDM2 input pin used to configure the output PCM mode. Refer to Table 1. Note: If the output format is 2-Channel, then the maximum SCLK to LRCLK ratio supported is 256.
3	GND	Ground	Ground
4	2CH_TDM1	Input	2CH_TDM1 input pin used to configure the output PCM mode. Refer to Table 1. Note: If the output format is 2-Channel, then the maximum SCLK to LRCLK ratio supported is 256.
5	GND	Ground	Ground
6	OS_MODE2	Input	Input pin used to configure the oversampling mode. Refer to Table 3.
7	OS_MODE3	Input	Input pin used to configure the oversampling mode. Refer to the Table 3.
8	OS_MODE1	Input	Input pin used to configure the oversampling mode. Refer to Table 3.
9	PDM_DATA4	Input	PDM Data Input for stereo or mono DMICs
10	PDM_DATA3	Input	PDM Data Input for stereo or mono DMICs
11	PDM_DATA2	Input	PDM Data Input for stereo or mono DMICs
12	IOVDD	Supply	IO Supply
13	PDM_DAT1	Input	PDM Data Input for stereo or mono DMICs
14	PDM_CLK	Output	PDM Clock Output for all DMICs
15	WL_LSB	Input	LSB in the Word Length configuration. Refer to Table 2.
16	WL_MSB	Input	MSB in the Word Length configuration. Refer to Table 2.
17	SCLK	Input	Serial Bit Clock for I2S/TDM
18	SDATA	Output	Serial Data Output for High Fs I2S/TDM
19	DVDD	Supply	Core Supply
20	LRCLK	Input	Left/Right Clock for I2S/Frame Sync for TDM

Table 6. QFN Package Lead Function Descriptions

5.0 QFN Package Mechanical Specifications



PACKAGE	20L 3X3 - 0.4		
REF.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.15	0.20	0.25
D		3.00 BSC.	
D2	1.55	1.65	1.75
E		3.00 BSC.	
E2	1.55	1.65	1.75
e		0.40 BSC.	
L	0.30	0.40	0.50
n		20	
nD		5	
nE		5	

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A1	0	0.02	0.05	
A3		0.203 REF.		
k	0.20	–	–	
TOLERANCES OF FORM AND POSITION				
aaa		0.10		
bbb		0.07		
ccc		0.10		
ddd		0.05		

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. n IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC PUBLICATION 95 SPP-002. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. nD AND nE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. DETAIL A; AS REQUIRED TO MAINTAIN MINIMUM SPACING BETWEEN LEADS.
9. DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OR CUTTING BURR

Figure 21. 3mm x 3mm, 20-lead, 0.4mm pitch QFN Package Mechanical Drawing (Note: Drawing Not to Scale)

6.0 Audio Data Formats

6.1 Audio Input Format

6.1.1 Double-Edge Clocked PDM Input Timing

The PDM_CLK signals to the DMIC are provided at an Fs determined by OS_MODE1, 2, 3 pins, provided valid LRCLK and SCLK signals are made available. For I2S Mode 1, Left-Justified and TDM modes, the TSDP18xx supports the industry standard double clock-edge latching as shown in Figure 22 and corresponding Table 7

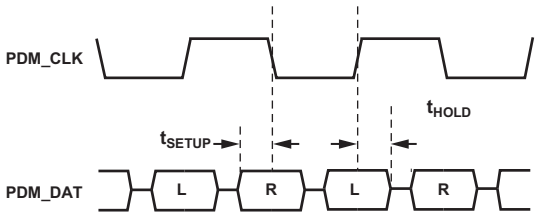


Figure 22. Doubled-edged Clocked PDM Timing Diagram

Parameter	t_{MIN}	t_{MAX}	Unit
Data Setup Time, t_{SETUP}	7		ns
Data Setup Time, t_{HOLD}	4		ns

Table 7. Double-Edge Clocked PDM Input Timing

Please note that the Right Channel PDM data is latched into the TSDP18xx on the falling edge of the PDM_CLK while the Left Channel of the PDM data is latched into the TSDP18xx on the rising edge of the PDM_CLK. Please note that this mode is only applicable to 3 out of the 4 possible PCM output modes (I^2S Mode 1, LJ and TDM). I^2S Mode 2 employs the singled-edge clocked PDM timing as shown below in Figure 23.

6.1.2 Single-Edge Clocked PDM Input Timing

When the 2CH_TDM1 and 2CH_TDM2 pins are configured for I2S Mode 2, the PDM_CLK signals to the DMIC are provided at an Fs determined by OS_MODE1, 2, 3 pins, provided valid LRCLK and SCLK signals are made available. The TSDP18xx also supports the lesser used industry standard single clock-edge latching as shown in Figure 23 and corresponding Table 8:

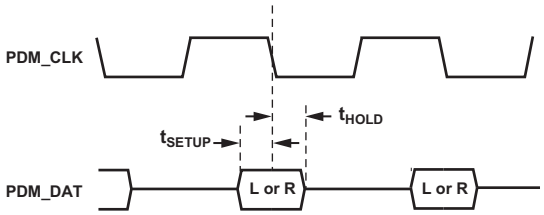


Figure 23. Single-Edged Clocked PDM Timing Diagram

Parameter	t_{MIN}	t_{MAX}	Unit
Data Setup Time, t_{SETUP}	7		ns
Data Setup Time, t_{HOLD}	4		ns

Table 8. Single-Edge Clocked PDM Input Timing

When the single edge PDM clock mode is selected, the left channel will be taken from PDM-DAT2 and the right channel from PDM_DAT1.

6.2 Audio Output Formats

For the Digital Audio Output, the TSDP18xx supports 3 standard audio interface formats, with a broad level of configuration via pin strappings, which enhances compatibility to meet the needs of most any audio DSP or SOC.

6.2.1 Left Justified Audio Output

The TSDP18xx Left Justified mode is conformant with the standard specification as shown in Figure 24. In particular, the MSB is available on the first rising edge of SCLK following a LRCLK transition. The other bits are then transmitted in order. The LRCLK signal is high when left channel data is present and low when right channel data is present. In the below figure, the SCLK_POL pin is LOW, showing standard polarity of the SCLK signal for the LJ format. When in this mode, the maximum SCLK to LRCLK ratio is 128.

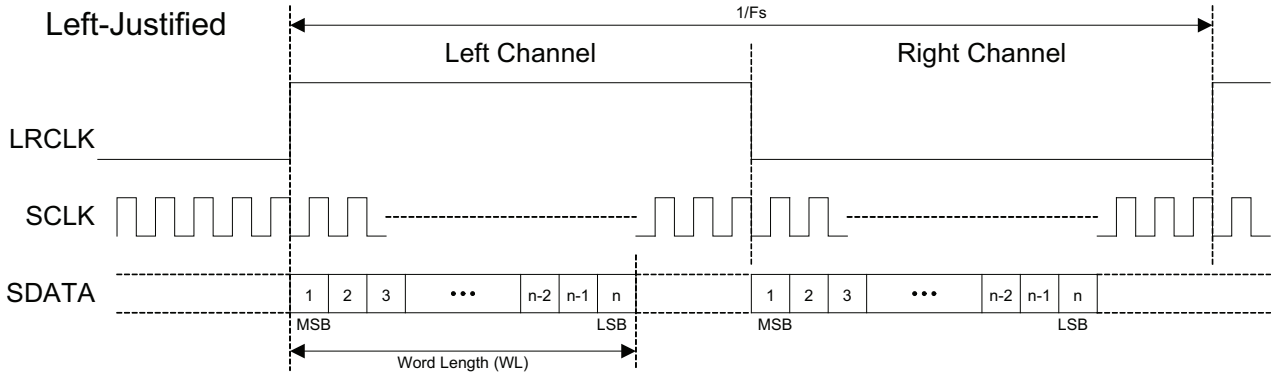


Figure 24. Left-Justified Audio Interface (assuming n-bit word lengths)

6.2.2 I²S Format Audio Output

The TSDP18xx I²S mode is conformant with the standard specification as shown in Figure 25. In particular, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. In the below figure, the SCLK_POL pin is LOW, showing standard polarity of the SCLK signal for the I²S format. When in this mode, the maximum SCLK to LRCLK ratio is 128.

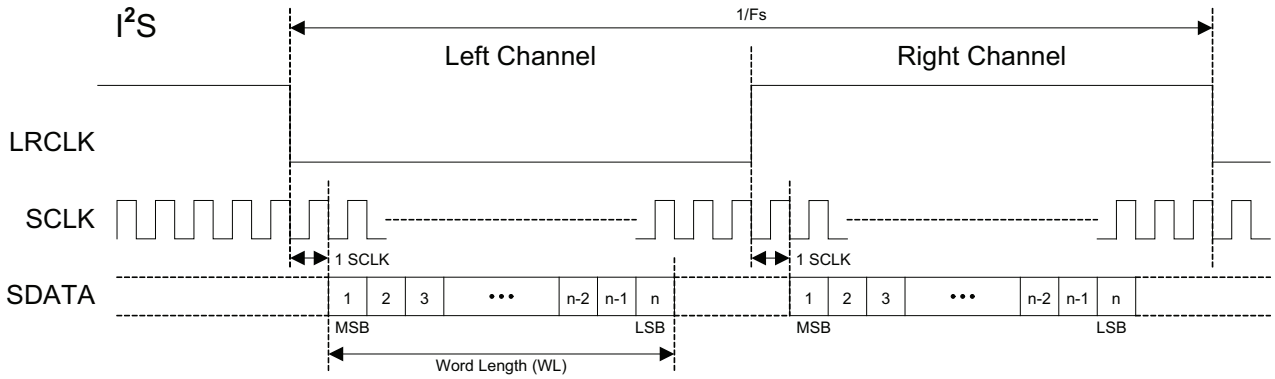


Figure 25. I²S Justified Audio Interface (assuming n-bit word length)

6.2.3 TDM Format Audio Output

TDM is a mechanism for transmitting or receiving multiple channels of audio information over a single data connection. When the TSDP18xx is in TDM mode, the SDOUT pin is used to output TDM data.

TDM data is transferred MSB first and the SCLK to FMCLK (serial bit clock / frame clock) ratio can be any supported rate from 32Fs up to 512Fs, provided that SCLK < 49.152MHz and the word-length set by WL_MSB and WL_LSB does not exceed the total number of SCLKs available to clock out the total number of data bits desired. The digital audio output port supports up to eight, 32-bit, 24-bit or 16-bit time slots (MSB justified within a slot).

The audio data is left-justified within the time slot by padding the unused bits with zeros, when the word length is < 32-bits. Valid audio data word lengths are 32, 24, or 16 bits.

Either short or word-length frame syncs can be accepted.

If SCLK_POL is LOW, data is transmitted on the rising edge of SCLK, otherwise, data is transmited on the falling edge of SCLK.

The FMCLK is one serial bit clock in length for a short frame sync pulse. The FMCLK is one slot wide for a long frame sync pulse for the frame clcok. This setting is configured by the FM_LGTH pin.

6.2.3.1 SCLK, LRCK, Word Length & PCM Word Slot Availability

For certainly applications where there may be an uneven number of DMICs (7, 5, 3 or 1) and/or the PCM output word widths of 24-bits has been set, the following data points of how the TSDP18xx operates should help to clarify any questions the designer may have:

After a maximum of 8 slots have been output from the TSDP18xx when in TDM mode or 2 slots when in I2S or LJ mode, the device just continues to clock out zeros.

If the slot count is not an integer value, as indicated in Table 9 below by the numbers with an "*" next to them, the device will automatically sync back up once all SCLKs have taken place within that TDM frame.

A valid configuration for 5 DMICs with a 24-bit word length is one that offers a 128 SCLK to LRCLK ratio. In this case, you have 5 24-bit word slots plus 8 extra cycles, however, please note that the data found in the extra 8 cycles may be undefined.

Ignoring the right frame data when in I2S or LJ mode, or all other word slots other than the first in TDM mode can support systems that have less than 2 DMICs.

Using multiple TSDP18xx devices, each with their own TDM bus can support systems that have more then 8 DMICs.

	Valid PCM Word Slots in TDM Mode SCLK to LRCLK Ratio								
Word Length	**512**	**384**	**256**	**192**	**128**	**96**	**64**	**48**	**32**
32	**8**	**8**	**8**	**6**	**4**	**3**	**2**	**N/A**	**N/A**
24	**8**	**8**	**8**	**8**	**5***	**4**	**2***	**2**	**N/A**
16	**8**	**8**	**8**	**8**	**8**	**6**	**4**	**3**	**2**

Table 9. TDM Mode PCM Word Slot Availability based on SCLK to LRCLK Ratio and Word Length

6.2.4 Standard SCLK Polarity, TDM Audio Output

In TDM mode, the MSB is available on the first rising edge of SCLK following a FMCLK transition. The other bits up to the LSB are then transmitted in order. The frame sync pulse must be present for at least one SCLK cycle, or may be continue for up to the duration of a word length, as shown by the dashed line in Figure 26.

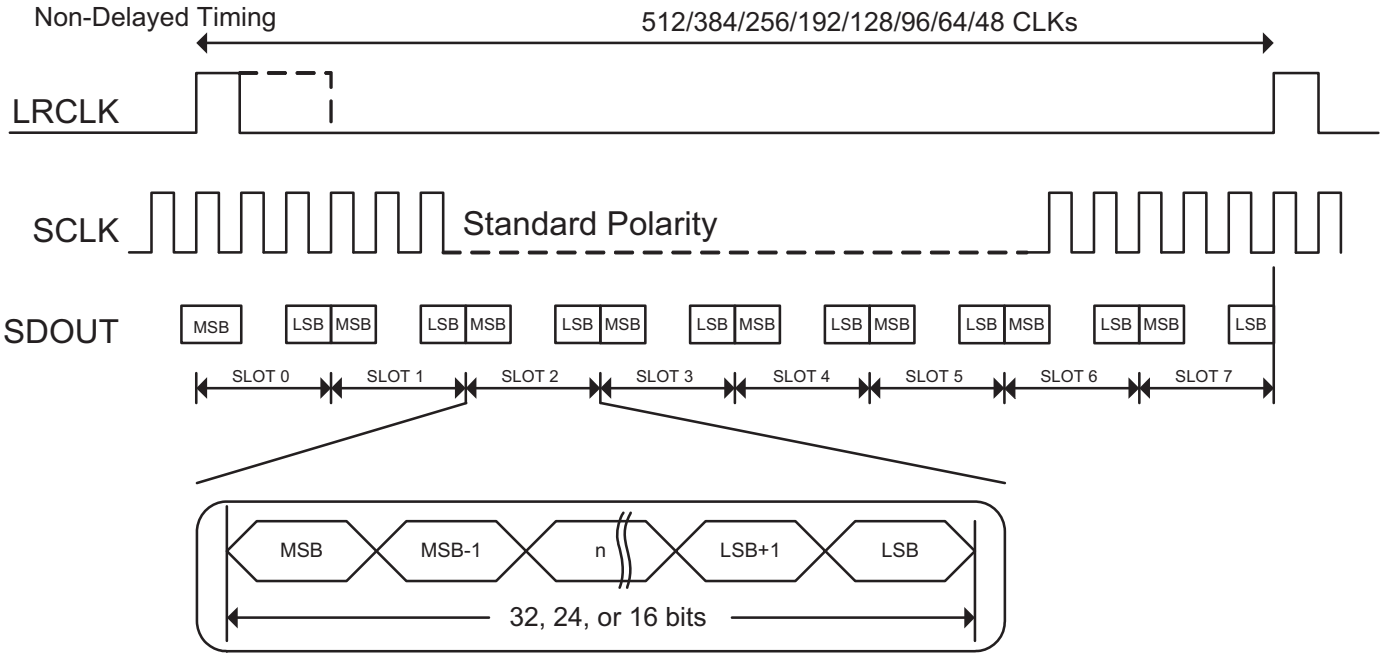


Figure 26. TDM Audio Output (Standard Polarity)

6.2.5 Inverted SCLK Polarity, TDM Audio Output

In TDM mode, the MSB is available on the first falling edge of BCLK following a FMCLK transition. The other bits up to the LSB are then transmitted in order.The frame sync pulse must be present for at least one SCLK cycle, or may be continue for up to the duration of a word length, as shown by the dashed line in Figure 7.

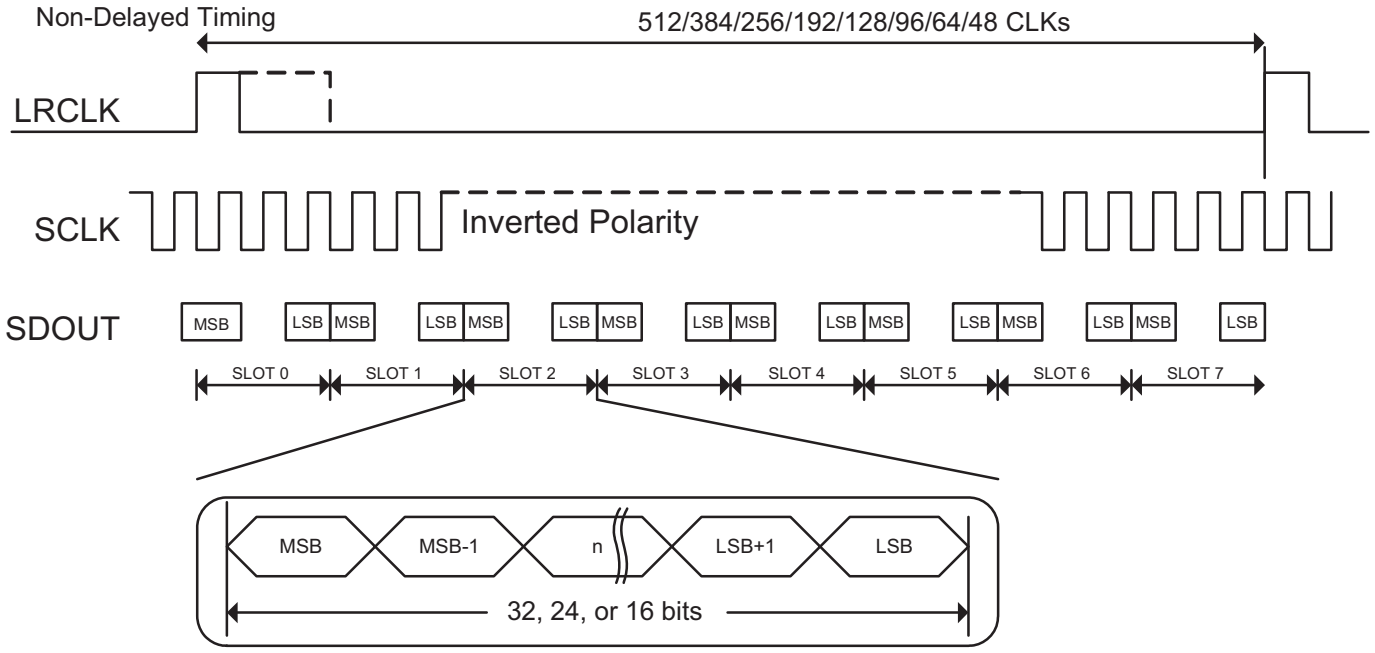


Figure 27. TDM Audio Output (Inverted Polarity)

7.0 Ordering Information

TSDP1808X1NEGXZAX8	Commercial Temp (0C ~ 70C), 3x3mm, 20-lead, 0.4mm pitch QFN package, Tape & Reel
TSDP1808X1NEGIZAX8	Industrial Temp (-40C ~ 85C), 3x3mm, 20-lead, 0.4mm pitch QFN package, Tape & Reel
TSDP18xx Eval Board	TSDP18xx Evaluation Board using 20-lead QFN, Commercial Temp
TSDP1808X1NEGXZAX	Commercial Temp (0C ~ 70C), 3x3mm, 20-lead, 0.4mm pitch QFN package, Tray
TSDP1808X1NEGIZAX	Industrial Temp (-40C ~ 85C), 3x3mm, 20-lead, 0.4mm pitch QFN package, Tray

Please contact sales@temposemi.com for more information on lead times.