TSL2740

ALS and Proximity Light-to-Digital Sensor

General Description

The TSL2740 device features advanced proximity measurement and digital ambient light sensing (ALS). The proximity detection feature provides object detection (e.g. mobile device screen to user's ear) by photodiode detection of reflected IR energy. Detect/release events are interrupt driven, and occur when proximity result crosses upper and/or lower threshold settings. The proximity engine features offset adjustment registers to compensate for unwanted IR energy reflection at the sensor. Proximity results are further improved by automatic ambient light subtraction. The ALS sensor features 2 output channels, a visible channel and an IR channel. The visible channel has a photodiode with a UV and IR blocking filter whereas the IR channel has a photodiode with an IR pass filter. Each channel has a dedicated data converter producing a 16-bit output. This architecture allows applications to accurately measure ambient light which enables devices to calculate illuminance to control a display backlight.

Ordering Information and *Content Guide* appear at end of datasheet.

Key Benefits & Features

The benefits and features of TSL2740, ALS and Proximity Light-to-Digital Sensor are listed below:

Figure 1:
Added Value of Using TSL2740

| Benefits	Features
• Single device integrated optical solution	• 2.0mm x 2.0mm x 0.5mm • Power management features • I^{2}C fast mode interface compatible
• Accurate ambient light sensing	• Photopic ambient light sense (ALS) • UV / IR blocking filter • Programmable gain and integration time
• Reduced power consumption	• 1.8V power supply with 1.8V I^{2}C bus
• Compensates for unwanted IR system crosstalk reflection • Compensates for unwanted ambient light photodiode current	• Programmable proximity offset adjustment register • Proximity automatic ambient light subtraction

Applications

The TSL2740 applications include:

- Ambient light sensing
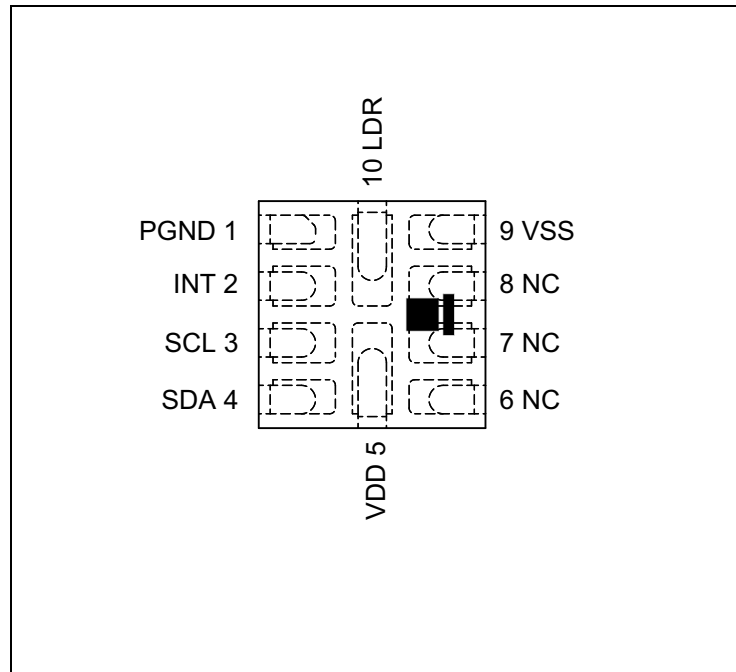- Display backlight control

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of TSL2740
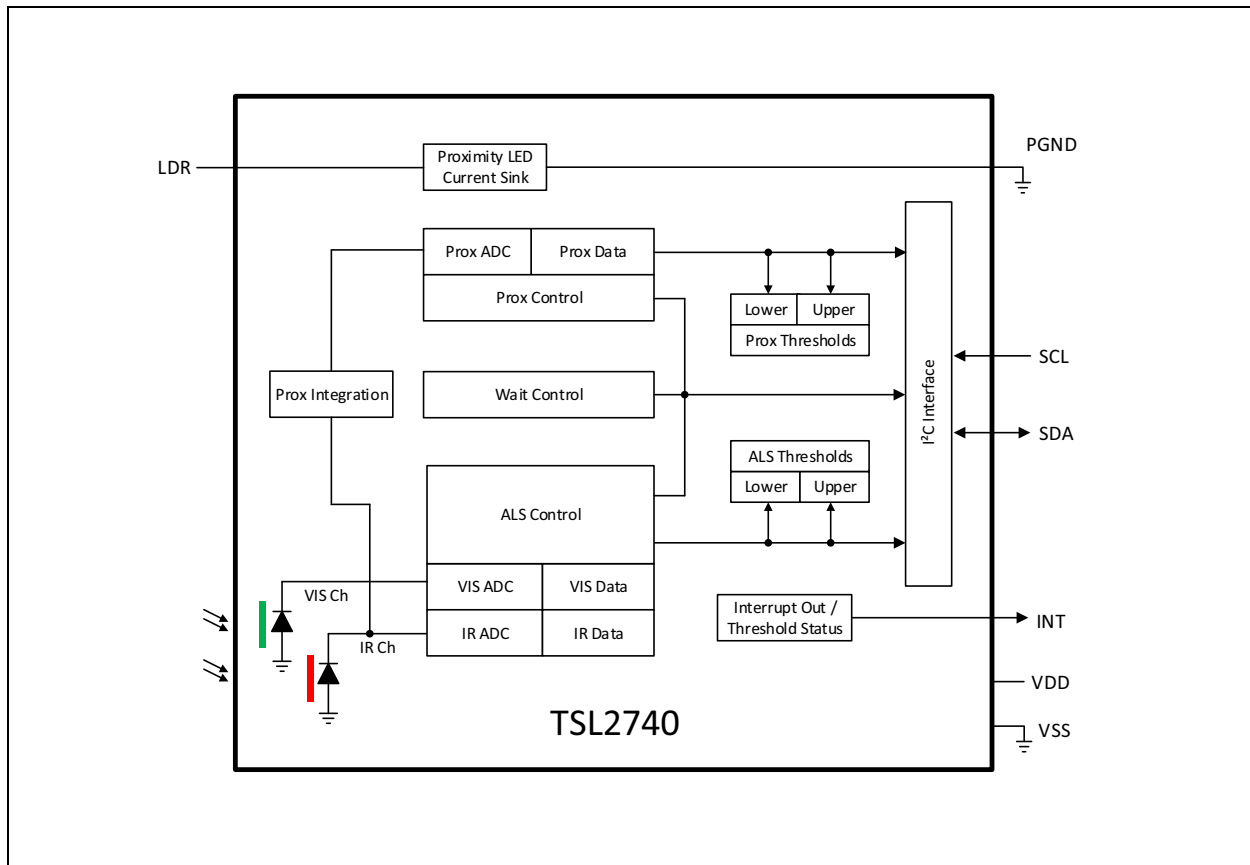
Pin Assignment

Figure 3:
Pin Diagram of TSL2740

Figure 4:
Pin Description of TSL2740 (10-Pin QFN)

Pin Number	Pin Name	Description
1	PGND	Power ground
2	INT	Interrupt. Open drain output (active low)
3	SCL	I²C serial clock input terminal
4	SDA	I²C serial data I/O terminal
5	VDD	Supply voltage
6	NC	No connection
7	NC	No connection
8	NC	No connection
9	VSS	Ground. All voltages are referenced to VSS
10	LDR	LED drive. Current sink for LED

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
V_{DD}	Supply voltage	-0.3	2.2	V	All voltages are with respect to GND
V_{IO}	Digital I/O terminal voltage	-0.3	3.6	V	INT, SCL and SDA
I_{out}	Output terminal current	-1	20	mA	INT and SDA
T_{strg}	Storage temperature range	-40	85	°C	
I_{SCR}	Input current (latch up immunity) JEDEC JESD78D	± 100		mA	Class II
ESD_{HBM}	Electrostatic discharge HBM JS-001-2014	± 2000		V	
ESD_{CDM}	Electrostatic discharge CDM JEDEC JESD22-C101F	± 500		V	

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Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply voltage	1.7	1.8	2.0	V
	Supply voltage accuracy, V_{DD} total error including transients	-3		3	%
T_A	Operating free-air temperature [1]	-30		85	°C

Note(s):

1. While the device is operational across the temperature range, performance will vary with temperature. Specifications are stated at 25°C unless otherwise noted.

Figure 7:
Operating Characteristics, V_{DD} = 1.8V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{OSC}	Oscillator frequency			8.107		MHz
I_{DD}	Supply current	Active ALS State (PON=AEN=1) [1]	50	90	150	µA
		Idle State (PON=1,AEN=0) [2]		30	60	
		Sleep State [3]		0.7	5	
V_{OL}	INT, SDA output low voltage	6mA sink current			0.6	V
I_{LEAK}	Leakage current, INT, SCL and SDA		-5		5	µA
V_{IH}	SCL, SDA input high voltage [4]		1.26			V
V_{IL}	SCL, SDA input low voltage				0.54	V
T_{Active}	Time from power-on to ready to receive I²C commands			1.5		ms

Note(s):

1. This parameter indicates the supply current during periods of ALS integration. If Wait is enabled (WEN=1), the supply current is lower during the Wait period.
2. Idle state occurs when PON=1 and all functions are not enabled.
3. Sleep state occurs when PON = 0 and I²C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.
4. Digital pins: SDA, SCL, INT, are tolerant to a communication voltage up to 3.0V.

Typical Operating Characteristics

Figure 8:
ALS Operating Characteristics, V_{DD} = 1.8V, T_A = 25°C

Parameter	Conditions	Min	Typ	Max	Units
Integration time step size		2.68	2.78	2.90	ms
Number of integration steps [1]		1		256	steps
Dark ADC count value	E_e = 0 µW/ cm^2; AGAIN = 64x; ATIME = 100ms (0x23)	0	1	3	counts
R_e Irradiance responsivity Settings: AGAIN = 16x ATIME = 400ms	**Visible Channel**				
	White LED, 2700K	309	363	417	counts/ (µW/cm^2)
	IR Channel				
	λ_D = 950 nm LED		352		counts/ (µW/cm^2)
Gain scaling, relative to 1x gain setting	AGAIN = 4x		4		x
	AGAIN = 16x		16		
	AGAIN = 64x		67		
	AGAIN = 128x		140		
ADC noise	AGAIN = 16x		0.005		% full scale

Note(s):

1. Specified by design and characterization; not production tested.

Figure 9:
Proximity Characteristics, VDD = 1.8V, T$_A$ =25°C

Parameter	Conditions		Min	Typ	Max	Units
ADC conversion time step size				88		μs
ADC number of integration steps [1]			1		256	steps
ADC counts [1]			0		255	counts
Gain scaling, relative to 1x gain setting	PGAIN = 1 (2x)			2		x
	PGAIN = 2 (4x)			4		
	PGAIN = 3 (8x)			8		
LED pulse count [1]			1		64	pulses
LED pulse width	PPULSE_LEN = 0			4		μs
	PPULSE_LEN = 1			8		
	PPULSE_LEN = 2			16		
	PPULSE_LEN = 3			32		
LED drive current	I$_{SINK}$ (sink current) @ 1.6 V, LDR pin	PLDRIVE = 31 (192mA)		192		mA
		PLDRIVE = 16 (102mA)	91.8	102	112.2	
		PLDRIVE = 7 (48mA)		48		
		PLDRIVE = 3 (24mA)		24		
		PLDRIVE = 1 (12mA)		12		
		PLDRIVE = 0 (6mA)		6		

Note(s):

1. Specified by design and characterization; not production tested.
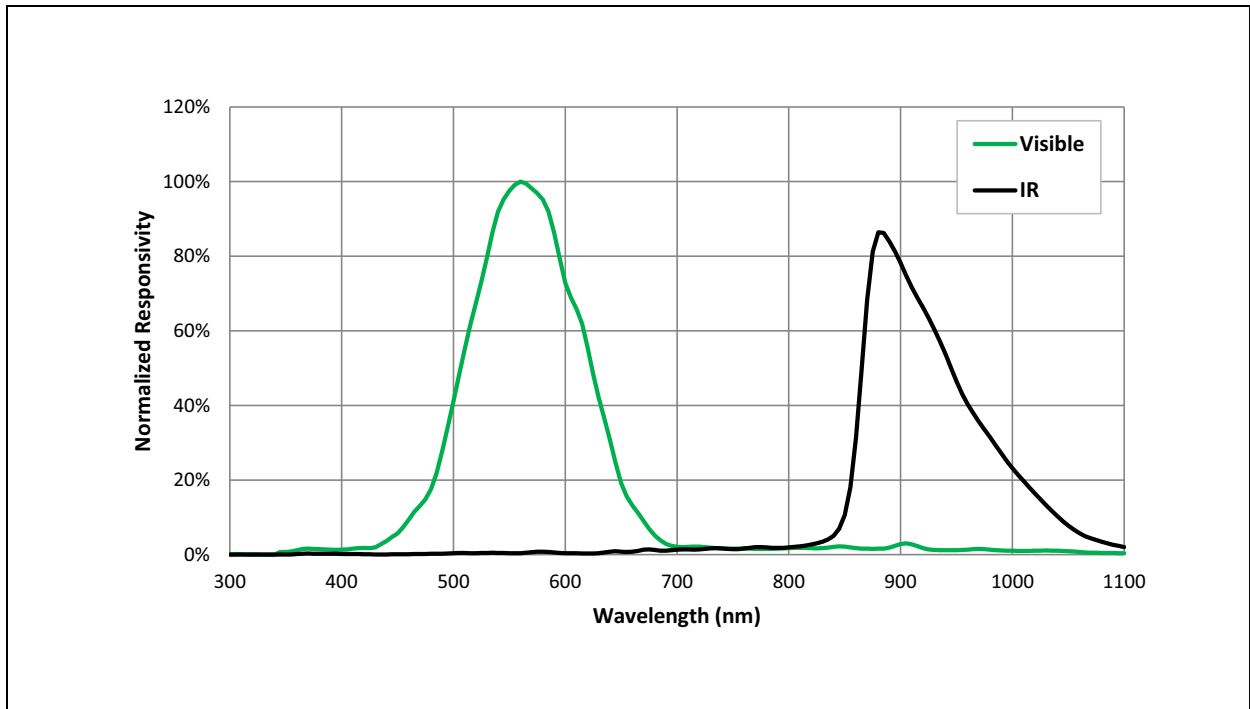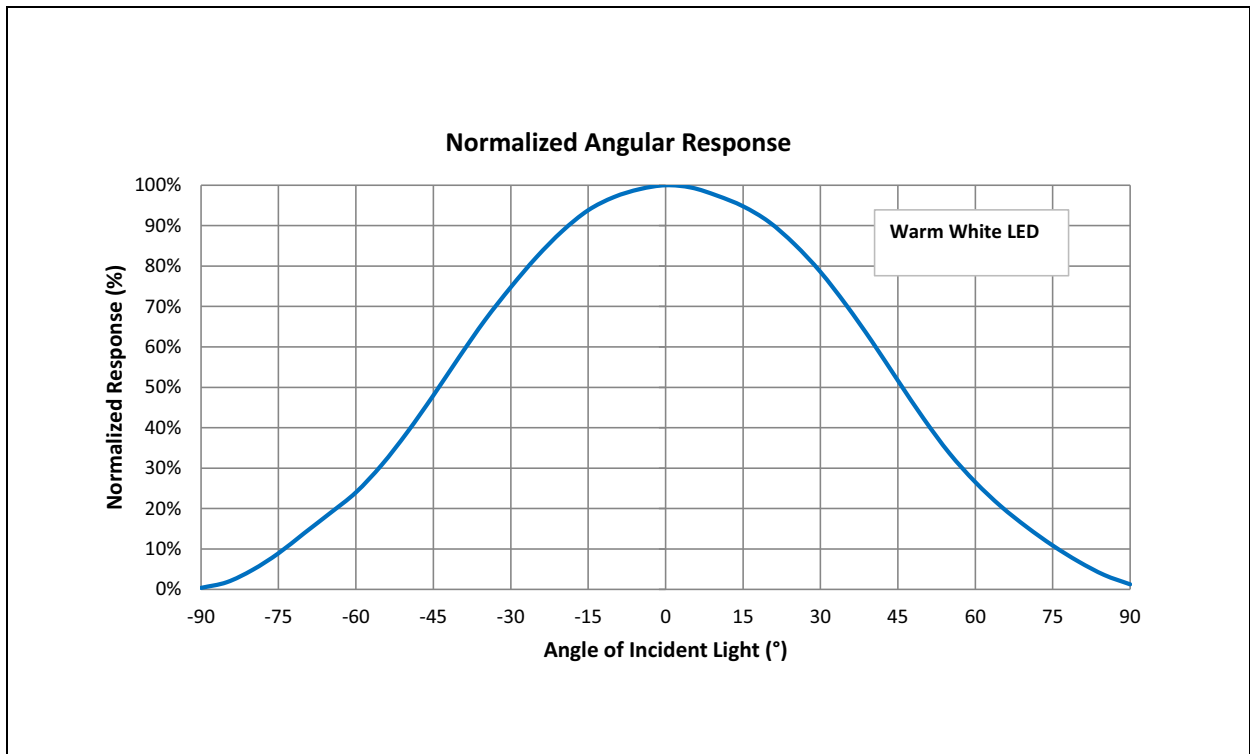
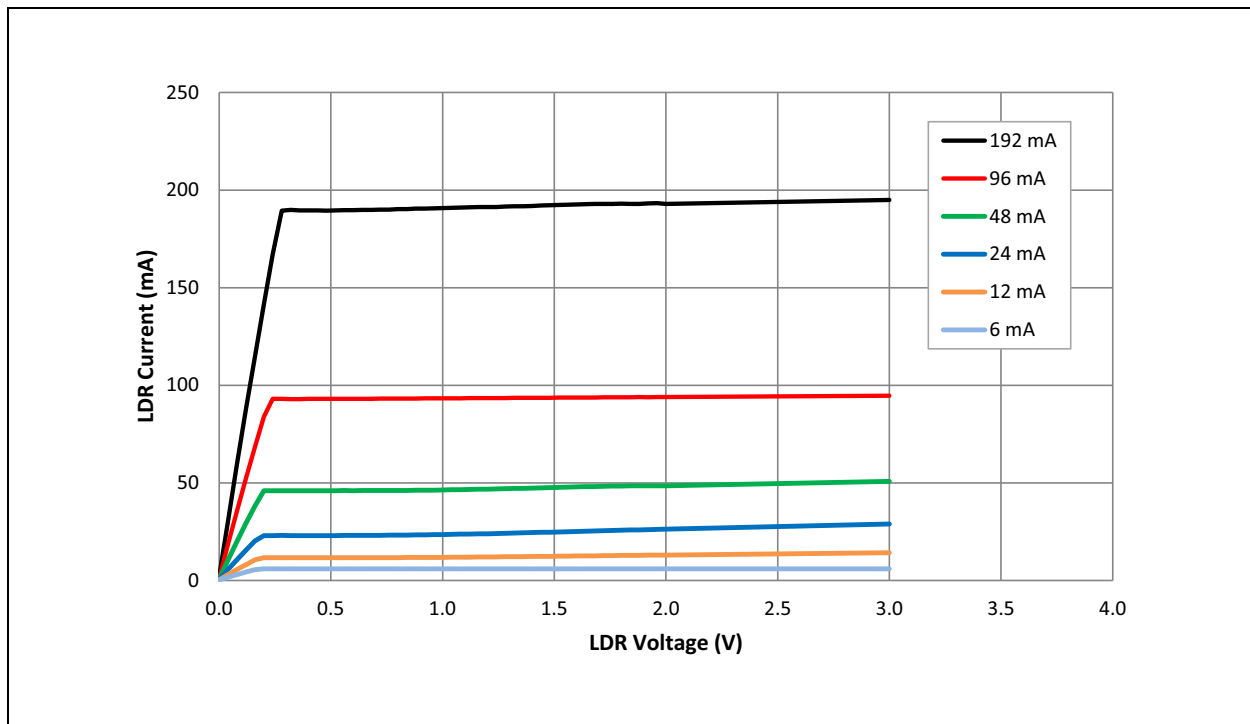**Figure 10:**
Spectral Responsivity

Figure 11:
ALS Responsivity vs Angular Displacement

Figure 12:
Typical LDR Current vs Voltage

Detailed Description

Proximity

Proximity results are affected by three fundamental factors: the IR LED emission, IR reception, and environmental factors, including target distance and surface reflectivity.

The IR reception signal path begins with IR detection from a photodiode and ends with the 8-bit proximity result in PDATA register. Signal from the photodiode is amplified, and offset adjusted to optimize performance. Offset correction or cross-talk compensation is accomplished by adjustment to the POFFSET register.

The analog circuitry of the device applies the offset value as a subtraction to the signal accumulation; therefore a positive offset value has the effect of decreasing the results.

Ambient Light Sensing

The ALS reception signal path begins as photodiodes receive filtered light and ends with the 16-bit results in the VISDATAL/H and IRDATAL/H registers. The visible channel's photodiode is filtered with a UV and IR filter to receive only visible light. The IR channel's photodiode is filtered to receive only IR. Signals from the photodiodes simultaneously accumulate for a period of time set by the value in ATIME before the results are available. Gain is adjustable from 1x to 128x to facilitate operation over a wide range of lighting conditions. Custom Lux equations can be created for specific applications and system designs.

I²C Characteristics

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and fast clock frequency modes with a chip address of 0x39. Read and Write transactions comply with the standard set by Philips (now NXP).

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP command and the I²C bus is released).

During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address + 1.

I²C Write Transaction

A Write transaction consists of a START, CHIP-ADDRESS$_{WRITE}$, REGISTER-ADDRESS, DATA BYTE(S), and STOP. Following each byte (9th clock pulse) the slave places an ACKNOWLEDGE/ NOT-ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

I²C Read Transaction

A Read transaction consists of a START, CHIP-ADDRESS$_{WRITE}$, REGISTER-ADDRESS, START, CHIP-ADDRESS$_{READ}$, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

Alternately, if the previous I²C transaction was a Read, the internal register address buffer is still valid, allowing the transaction to proceed without "re"-specifying the register address. In this case the transaction consists of a START, CHIP-ADDRESS$_{READ}$, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9th clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at:

www.i2c-bus.org/references/

Timing Diagrams

Figure 13:
I²C Timing
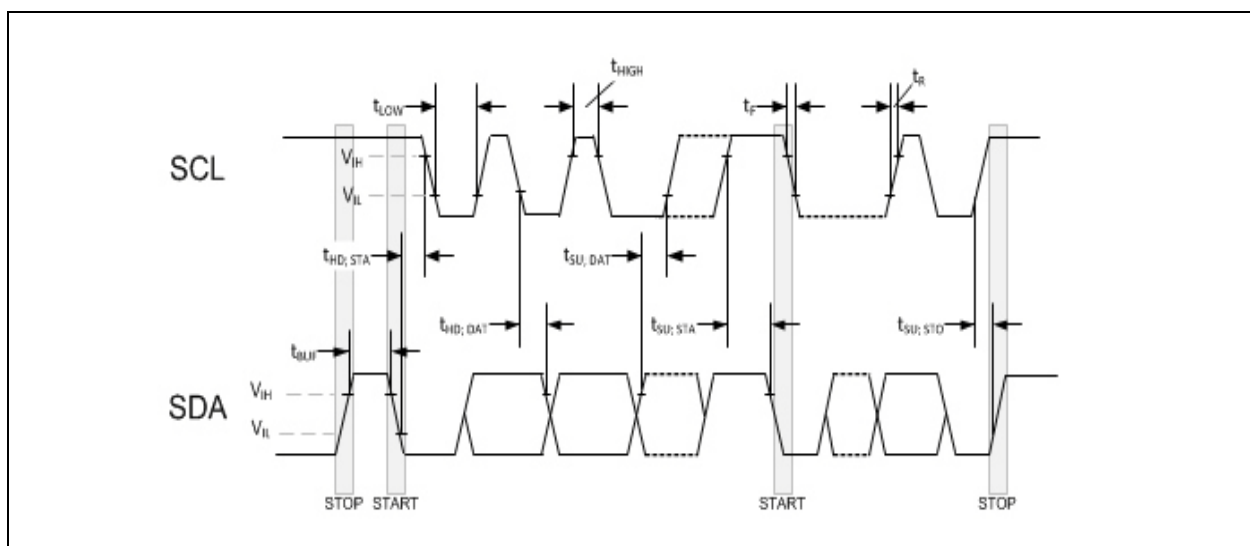
Principles of Operation

System State Machine

An internal state machine provides system control of the ALS, proximity detection, and power management features of the device. At power up, an internal power-on-reset initializes the device and puts it in a low power Sleep state. When a write on I^{2}C bus to the Enable register (0x80) PON bit is set, the device transitions to the Idle state. If PON is disabled, the device will return to the Sleep state to save power. Otherwise, the device will remain in the Idle state until the ALS function is enabled. Once enabled, the device will execute the ALS and Wait states in sequence. Upon completion, the device will automatically begin a new ALS-Wait cycle as long as PON and AEN remain enabled. If the ALS function generates an interrupt and the Sleep-After-Interrupt (SAI) feature is enabled, the device will transition to the Sleep state and remain in a low-power mode until an I^{2}C command is received clearing the interrupts in the STATUS register. See Interrupts for additional information.

Register Description

Figure 14:
Register Overview

Address	Register Name	R/W	Register Function	Reset Value
0x80	ENABLE	R/W	Enables states and functions	0x00
0x81	ATIME	R/W	ALS integration time	0x00
0x82	PRATE	R/W	Proximity sampling time	0x1F
0x83	WTIME	R/W	Wait time	0x00
0x84	AILTL	R/W	ALS interrupt low threshold low byte	0x00
0x85	AILTH	R/W	ALS interrupt low threshold high byte	0x00
0x86	AIHTL	R/W	ALS interrupt high threshold low byte	0x00
0x87	AIHTH	R/W	ALS interrupt high threshold high byte	0x00
0x88	PILT	R/W	Proximity interrupt low threshold	0x00
0x8A	PIHT	R/W	Proximity interrupt high threshold	0x00
0x8C	PERS	R/W	Interrupt persistence filters	0x00
0x8D	CFG0	R/W	Configuration register zero	0x80
0x8E	PCFG0	R/W	Proximity configuration register zero	0x4F
0x8F	PCFG1	R/W	Proximity configuration register one	0x80
0x90	CFG1	R/W	Configuration register one	0x00
0x91	REVID	R	Revision ID	0x21
0x92	ID	R	Device ID	0xE4
0x93	STATUS	R	Device status register	0x00
0x94	VISDATAL	R	Visible channel data low byte	0x00
0x95	VISDATAH	R	Visible channel data high byte	0x00
0x96	IRDATAL	R	IR channel data low byte	0x00
0x97	IRDATAH	R	IR channel data high byte	0x00
0x9C	PDATA	R	Proximity channel data	0x00
0x9E	REVID2	R	Auxiliary ID	0x01
0x9F	CFG2	R/W	Configuration register two	0x04
0xAB	CFG3	R/W	Configuration register three	0x0C
0xC0	POFFSETL	R/W	Proximity offset magnitude	0x00

Address	Register Name	R/W	Register Function	Reset Value
0xC1	POFFSETH	R/W	Proximity offset sign	0x00
0xD6	AZ_CONFIG	R/W	Autozero configuration	0x7F
0xD7	CALIB	R/W	Calibration start	0x00
0xD9	CALIBCFG	R/W	Calibration configuration	0x50
0xDC	CALIBSTAT	R/W	Calibration status	0x00
0xDD	INTENAB	R/W	Interrupt enables	0x00

Register Access:

- R = Read Only
- W = Write Only
- R/W = Read or Write
- SC = Self Clearing after access

Detailed Register Description

Enable Register (Address 0x80)

Figure 15:
Enable Register

Addr: 0x80				Enable
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	RESERVED	0000	RW	Reserved.
3	WEN	0	RW	This bit activates the wait feature. Active high.
2	PEN	0	RW	This bit activates the proximity detection. Active high.
1	AEN	0	RW	This bit actives the ALS function. Active high. *Set AEN=1 and PON=1 in the same command to ensure auto-zero function is run prior to the first measurement.
0	PON	0	RW	This field activates the internal oscillator and ADC channels. Active high.

Before activating AEN or PEN, preset each applicable operating mode registers and bits.

ATIME Register (Address 0x81)

Figure 16:
ATIME Register

Addr: 0x81				ATIME			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**			
7:0	ATIME	0x00	RW	ALS/Color value that specifies the integration time in 2.81ms intervals. 0x00 indicates 2.8ms. The maximum ALS value depends on the integration time. For every 2.81ms, the maximum value increases by 1024. This means that to be able to reach ALS full scale, the integration time has to be at least 64*2.8ms.			
				Value	**Integration Cycles**	**Integration Time**	**Maximum ALS Value**
				0x00	1	2.8ms	1023
				0x01	2	5.6ms	2047
				…	…	…	…
				0x3F	64	180ms	65535
				…	…	…	…
				0xFF	256	721ms	65535

The ATIME register controls the integration time of the ALS ADCs. The timer is implemented with a down counter with 0x00 as the terminal count. The timer is clocked at a 2.8ms nominal rate. Loading 0x00 will generate a 2.8ms integration time, loading 0x01 will generate a 5.6ms integration time, and so forth. The RC oscillator runs at 8MHz nominal rate. This gets divided by 11 to generate the integration clock of 727kHz. One count in ATIME (nominal 2.8ms) are 2.81ms. This is 2048 integration clock cycles: 125ns*11*8*256=2.81ms.

PRATE Register (Address 0x82)

Figure 17:
PRATE Register

Addr: 0x82				PRATE	
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:0	PRATE	0x1F	RW	This register defines the duration of 1 Prox Sample, which is (PRATE + 1)*88µs.	

WTIME Register (Address 0x83)

Figure 18:
WTIME Register

Addr: 0x83				WTIME			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**			
7:0	WTIME	0x00	RW	Value that specifies the wait time between ALS cycles in 2.81ms increments.			
				Value	**Increments**	**Wait Time**	
				0x00	1	2.8ms (33.8ms)	
				0x01	2	5.6ms (67.6ms)	
				…	…	…	
				0x3F	64	180ms (2.16s)	
				…	…	…	
				0xFF	256	721ms (8.65s)	

The wait timer is implemented using a down counter.
Wait time = (value +1) x 2.8ms. If WLONG is enabled then
Wait time = (value +1) x 2.8ms x 12.

AILTL Register (Address 0x84)

Figure 19:
AILTL Register

Addr: 0x84				AILTL
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AILTL	0x00	RW	This register sets the low byte of the LOW ALS threshold.

The Clear (C) channel is compared against low-going 16-bit threshold value set by AILTL and AILTH.

AILTH Register (Address 0x85)

Figure 20:
AILTH Register

Addr: 0x85				AILTH
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AILTH	0x00	RW	This register sets the high byte of the LOW ALS threshold.

The Clear (C) channel is compared against low-going 16-bit threshold value set by AILTL and AILTH.

The contents of the AILTH and AILTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the C channel is below the AILTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert.

When setting the 16-bit ALS threshold AILTL must be written first, immediately followed by AILTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

AIHTL Register (Address 0x86)

Figure 21:
AIHTL Register

Addr: 0x86				AIHTL
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AIHTL	0x00	RW	This register sets the low byte of the HIGH ALS threshold.

The Clear (C) channel is compared against high-going 16-bit threshold value set by AIHTL and AIHTH.

The contents of the AIHTH and AIHTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the C channel is above the AIHTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert. When setting the 16-bit ALS threshold AIHTL must be written first, immediately followed by AIHTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

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AIHTH Register (Address 0x87)

Figure 22:
AIHTH Register

Addr: 0x87				AIHTH
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AIHTH	0x00	RW	This register sets the high byte of the HIGH ALS threshold.

The Clear (C) channel is compared against high-going 16-bit threshold value set by AIHTL and AIHTH.
The contents of the AIHTH and AIHTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the C channel is above the AIHTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert.
When setting the 16-bit ALS threshold AIHTL must be written first, immediately follow by AIHTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

PILT Register (Address 0x88)

Figure 23:
PILT Register

Addr: 0x88				PILT
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PILT	0x00	RW	This register sets the Proximity ADC channel low threshold.

The proximity channel is compared against low-going 8-bit threshold value set by PILT.
If the value generated by the proximity channel is below the PILT threshold and the PPERS value is reached, the PINT bit is asserted. If PIEN is set, then the INT pin will also assert.

PIHT Register (Address 0x8A)

Figure 24:
PIHT Register

Addr: 0x8A				PIHT
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PIHT	0x00	RW	This register sets the proximity ADC channel high threshold.

The proximity channel is compared against high-going 8-bit threshold value set by PIHT.

If the value generated by the proximity channel is above the PIHT threshold and the PPERS value is reached, the PINT bit is asserted. If PIEN is set, then the INT pin will also assert.

PERS Register (Address 0x8C)

Figure 25:
PERS Register

Addr: 0x8C				PERS	
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:4	PPERS	0000	RW	This register sets the proximity persistence filter.	
				Value	**Interrupt**
				0	Every proximity cycle
				1	Any value outside PILT/PIHT thresholds
				2	2 consecutive proximity values out of range
				3	3 consecutive proximity values out of range
				…	….
				15	15 consecutive proximity values out of range

Addr: 0x8C				PERS	
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
3:0	APERS	0000	RW	This register sets the ALS persistence filter.	
				0	Every ALS cycle
				1	Any value outside ALS thresholds
				2	2 consecutive ALS values out of range
				3	3 consecutive ALS values out of range
				4	5 consecutive ALS values out of range
				5	10 consecutive ALS values out of range
				6	15 consecutive ALS values out of range
				7	20 consecutive ALS values out of range
				…	…
				13	50 consecutive ALS values out of range
				14	55 consecutive ALS values out of range
				15	60 consecutive ALS values out of range

The frequency of consecutive proximity channel results outside of threshold limits are counted; this count value is compared against the PPERS value. If the counter is equal to the PPERS value an interrupt is asserted. Any time a proximity channel result is inside the threshold values the counter is cleared. The frequency of consecutive clear channel results outside of threshold limits are counted; this count value is compared against the APEARS value. If the counter is equal to the APERS setting an interrupt is asserted. Any time a clear channel result is inside the threshold values the counter is cleared.

CFG0 Register (Address 0x8D)

Figure 26:
CFG0 Register

Addr: 0x8D				CFG0
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved	10000	RW	This field must be set to the default value.
2	WLONG	0	RW	When Wait Long is asserted the wait period as set by WTIME is increased by a factor of 12.
1:0	Reserved	00	RW	This field must be set to the default value.

The wait timer is implemented using a down counter.
Wait time = (value +1) x 2.8ms. If WLONG is enabled then
Wait time = (value +1) x 2.8ms x 12.

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PCFG0 Register (Address 0x8E)

Figure 27:
PCFG0 Register

Addr: 0x8E				PCFG0	
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:6	PPULSE_LEN	01	RW	Proximity pulse length. Default is 8µs.	
				Value	**Pulse Length**
				0	4µs
				1	8µs
				2	16µs
				3	32µs
5:0	PPULSE	001111	RW	Maximum number of pulses in a single proximity cycle. Default is 16 pulses.	
				Value	**Maximum Number of Pulses**
				0	1
				1	2
				2	3
				…	…
				63	64

PCFG1 Register (Address 0x8F)

Figure 28:
PCFG1 Register

Addr: 0x8F				PCFG1
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	PGAIN	10	RW	This field sets the gain of the proximity IR sensor. Default is 4x gain. **Value** / **Prox Gain**: 0 / 1x; 1 / 2x; 2 / 4x; 3 / 8x
5	Reserved	0	RW	Reserved.
4:0	PLDRIVE	00000	RW	This field sets the drive strength of the IR LED current. Default is 6mA. **Value** / **LED Current**: 0 / 6mA; 1 / 12mA; $i_{LED} = 6(PLDRIVE +1)$ mA; 30 / 186mA; 31 / 192mA

CFG1 Register (Address 0x90)

Figure 29:
CFG1 Register

Addr: 0x90				CFG1
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0000	RW	Reserved.
3	IR_TO_GREEN	0	RW	If set high, the IR (Proximity) photodiode is switched into the Green channel's data converter. GDATAL/H register will report IR content. Green photodiode is not connected.
2	Reserved	0	RW	Reserved.
1:0	AGAIN	00	RW	This field sets the gain of the ALS/Color sensor. Default is 1x gain. **Value** / **ALS/Color Gain** 0 / 1x 1 / 4x 2 / 16x 3 / 64x

REVID Register (Address 0x91)

Figure 30:
REVID Register

Addr: 0x91				REVID
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved	00100	RO	Reserved.
2:0	REV_ID	001	RO	Device revision number.

ID Register (Address 0x92)

Figure 31:
ID Register

Addr: 0x92		ID		
Bit	Bit Name	Default	Access	Bit Description
7:2	ID	111001	RO	Device type identification.
1:0	Reserved	00	RO	Reserved.

Status Register (Address 0x93)

Figure 32:
Status Register

Addr: 0x93		Status Register		
Bit	Bit Name	Default	Access	Bit Description
7	ASAT	0	R, SC	The Analog Saturation flag signals that the ALS/Color results may be unreliable due to saturation of the AFE.
6	PSAT	0	R, SC	The Proximity Saturation flag indicates that an ambient- or reflective-saturation event occurred during a previous proximity cycle.
5	PINT	0	R, SC	The Proximity Interrupt flag indicates that proximity results have exceeded thresholds and persistence settings.
4	AINT	0	R, SC	The ALS Interrupt flag indicates that ALS/Color results (clear channel) have exceeded thresholds and persistence settings.
3	CINT	0	R, SC	The Calibration Interrupt flag indicates that calibration has completed.
2	Reserved	0	R, SC	Reserved.
1	PSAT_REFLECTIVE	0	R, SC	The Reflective Proximity Saturation Interrupt flag signals that the AFE has saturated during the IR LED active portion of proximity integration.
0	PSAT_AMBIENT	0	R, SC	The Ambient Proximity Saturation Interrupt flag signals that the AFE has saturated during the IR LED inactive portion of proximity integration.

All flags in this register can be cleared by setting the bit high. Alternatively, if the CFG3.int_read_clear bit is set, then simply reading this register automatically clears all eight flags.

VISDATAL Register (Address 0x94)

Figure 33:
VISDATAL Register

Addr: 0x94			CDATAL	
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	VISDATAL	0x00	RO	This register contains the low byte of the 16-bit visible channel data.

VISDATAH Register (Address 0x95)

Figure 34:
VISDATAH Register

Addr: 0x95			VISDATAH	
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	VISDATAH	0x00	RO	This register contains the high byte of the 16-bit visible channel data.

IRDATAL Register (Address 0x96)

Figure 35:
IRDATAL Register

Addr: 0x96			RDATAL	
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	IRDATAL	0x00	RO	This register contains the low byte of the 16-bit IR channel data.

IRDATAH Register (Address 0x97)

Figure 36:
IRDATAH Register

Addr: 0x97			RDATAH	
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	IRDATAH	0x00	RO	This register contains the high byte of the 16-bit IR channel data.

PDATA Register (Address 0x9C)

Figure 37:
PDATA Register

Addr: 0x9C		PDATA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PDATA	0x00	RO	This register contains the 8-bit proximity channel data.

REVID2 Register (Address 0x9E)

Figure 38:
REVID2 Register

Addr: 0x9E		REVID2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0000	RO	Reserved.
3:0	REVID2	0001	RO	Package identification.

CFG2 Register (Address 0x9F)

Figure 39:
CFG2 Register

Addr: 0x9F		CFG2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	Reserved	000	RW	Reserved.
4	AGAINMAX	0	RW	This bit adjusts the overall ALS gain factor. See Figure 40 for recommended settings and corresponding overall ALS gain factor.
3	Reserved	0	RW	Reserved.
2	AGAINL	1	RW	This bit adjusts the overall ALS gain factor. See Figure 40 for recommended settings and corresponding overall ALS gain factor.
1:0	Reserved	00	RW	Reserved.

The ALS gain can be adjusted by setting the two AGAIN bits as well as the AGAINMAX and AGAINL bits which yields an overall range from ½ x to 128x.

Figure 40:
AGAIN Range

AGAIN[1]	AGAIN[0]	AGAINMAX	AGAINL	Overall ALS Gain
0	0	0	0	½
0	0	0	1	1
0	1	0	1	4
1	0	0	1	16
1	1	0	1	64
1	1	1	1	128

CFG3 Register (Address 0xAB)

Figure 41:
CFG3 Register

Addr: 0xAB				CFG3			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**			
7	INT_READ_CLEAR	0	RW	If the Interrupt-Clear-by-Read bit is set, then all flag bits in the STATUS register will be reset whenever the STATUS register is read over I²C.			
6:5	Reserved	10	RW	Reserved.			
4	SAI	0	RW	The Sleep After Interrupt bit is used to place the device into a low power mode upon an interrupt pin assertion.			
				PON	**SAI**	**INT**	**Oscillator**
				0	X	X	OFF
				1	0	X	ON
				1	1	1	ON
				1	1	0	OFF
3:0	Reserved	1100	RW	Reserved.			

The SAI bit sets the device operational mode following the completion of an ALS or proximity cycle. If AINT and AIEN are both set or if PINT and PIEN are both set, causing an interrupt on the INT pin, and the SAI bit is set, then the oscillator will deactivate. The Device will appear as if PON = 0, however, PON will read as 1. The device can only be reactivated (oscillator enabled) by clearing the interrupts in the STATUS register.

POFFSETL Register (Address 0xC0)

Figure 42:
POFFSETL Register

Addr: 0xC0		POFFSETL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	POFFSETL	0x00	RW	This register contains the magnitude portion of proximity offset adjust value.

Typically, optical and/or electrical crosstalk negatively influence proximity operation and results. The POFFSETL/POFFSETH registers provide a mechanism to remove system crosstalk from the proximity data. POFFSETL and POFFSETH contains the magnitude and sign of a value which adjusts PDATA is generated in the AFE. An offset value in the range of ± 255 is possible.

POFFSETH Register (Address 0xC1)

Figure 43:
POFFSETH Register

Addr: 0xC1		POFFSETH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	Reserved	0000000	RW	Reserved.
0	POFFSETH	0	RW	This register contains the sign portion of proximity offset adjust value.

Typically, optical and/or electrical crosstalk negatively influence proximity operation and results. The POFFSETL/POFFSETH registers provide a mechanism to remove system crosstalk from the proximity data. POFFSETL and POFFSETH contains the magnitude and sign of a value which adjusts PDATA is generated in the AFE. An offset value in the range of ± 255 is possible.

AZ_CONFIG Register (Address 0xD6)

Figure 44:
AZ_CONFIG Register

Addr: 0xD6		AZ_CONFIG		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7	Reserved	0	RW	Reserved.
6:0	AZ_NTH_ ITERATION	1111111	RW	Run autozero automatically before every nth ALS cycle (00h = never, n = every nth ALS cycle, and 7Fh = only before the first ALS cycle).

CALIB Register (Address 0xD7)

Figure 45:
CALIB Register

Addr: 0xD7		CALIB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Reserved	00	RO	Reserved.
5	ELECTRICAL_ CALIBRATION	0	RW	Selects proximity calibration type. 1=Electrical offset only. 0= Calibration compensates for electrical and optical crosstalk.
4:1	Reserved	0000	RW	Reserved.
0	START_OFFSET_ CALIB	0	RW	Set to 1 to start a calibration sequence.

Proximity response in systems with electrical and optical crosstalk may be improved by using the calibration feature. Optical crosstalk is caused when the photodiode receives a small portion of the LED IR which was unintentionally reflected by a surface other than the target. Electrical offset is caused by electrical disturbance in the sensor AFE, and also influences the proximity result. The calibration routine adjusts the value in POFFSET_L/H until the proximity result is as close to zero as possible without becoming zero.

Optical and electrical calibration function identically, except that during an electrical calibration the proximity photodiode is disconnected from the AFE.

Upon power-up, the device always automatically performs an electrical calibration. However, an electrical calibration can be initiated anytime by setting the ELECTRICAL_CALIBRATION and START_OFFSET_CALB bits.

To perform an optical (and electrical) calibration do not set the ELECTRICAL_CALIBRATION bit when setting the START_OFFSET_CALIB. The CINT flag will assert after calibration has finished.

Upon completion proximity offset registers are automatically loaded with calibration result.

CALIBCFG Register (Address 0xD9)

Figure 46:
CALIBCFG Register

Addr: 0xD9				CALIBCFG
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	BINSRCH_ TARGET	010	RW	Proximity Result Target.

Value	PDATA Target
0	0
1	1
2	3
3	7
4	15
5	31
6	63
7	127

Bit	Bit Name	Default	Access	Bit Description
4	Reserved	1	RW	Reserved.
3	AUTO_ OFFSET_ADJ	0	RW	The Proximity Auto Offset Adjust bit causes the value in POFFSETL register to be decremented if PDATA ever becomes zero.
2:0	PROX_AVG	000	RW	The Proximity Averaging field defines the number of ADC samples collected and averaged during a cycle which become the proximity result.

Value	Sample Size
0	Disable
1	2
2	4
3	8
4	16
5	32
6	64
7	128

The binary search target field is used by the calibration feature to set the baseline value for PDATA when no target is present. For example, calibration of a device in open air, with no target,

and BINSEARCH_TARGET setting of 4 causes the PDATA value will be approximately 15 counts. This feature is useful because it forces PDATA result to always be above zero.

The PROX_AVG field sets the number of ADC samples that are averaged to calculate the PDATA result.

CALIBSTAT Register (Address 0xDC)

Figure 47:
CALIBSTAT Register

Addr: 0xDC		CALIBSTAT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	Reserved	0000000	RW	Reserved.
0	CALIB_FINISHED	0	RW	This flag indicates that calibration has finished. It can be cleared by writing a 1 to CINT in the status register.

INTENAB Register (Address 0xDD)

Figure 48:
INTENAB Register

Addr: 0xDD		INTENAB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ASIEN	0	RW	ALS Saturation Interrupt Enable.
6	PSIEN	0	RW	Proximity Saturation Interrupt Enable.
5	PIEN	0	RW	Proximity Interrupt Enable.
4	AIEN	0	RW	ALS/Color Interrupt Enable.
3	CIEN	0	RW	Calibration Interrupt Enable.
2:0	Reserved	000	RW	Reserved.

Application Information

Schematic

Figure 49:
Typical Applications Circuit
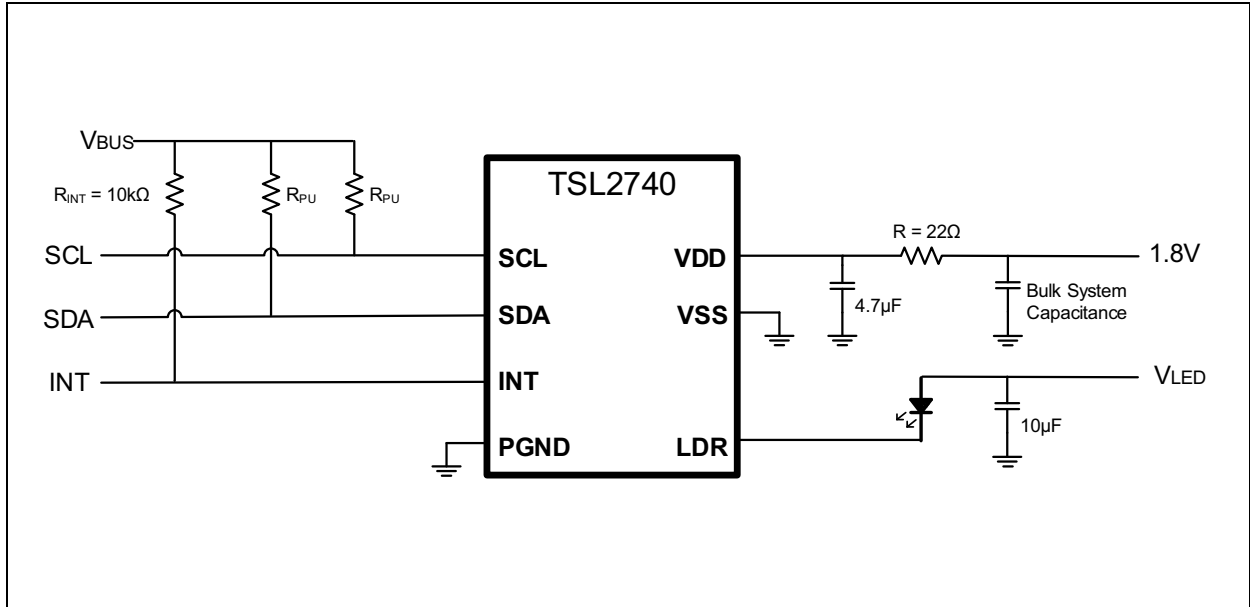
Note(s):

1. The value of the I²C pull up resistors RPU should be based on the 1.8V bus voltage, system bus speed and trace capacitance.

2. The bulk capacitor can affect the stability of a regulated supply output and should be chosen with the regulator characteristics in mind.

3. VSS and PGND should be connected to the same solid ground plane as close to the device as possible.

Package Drawings & Markings

Figure 50:
Package Drawing
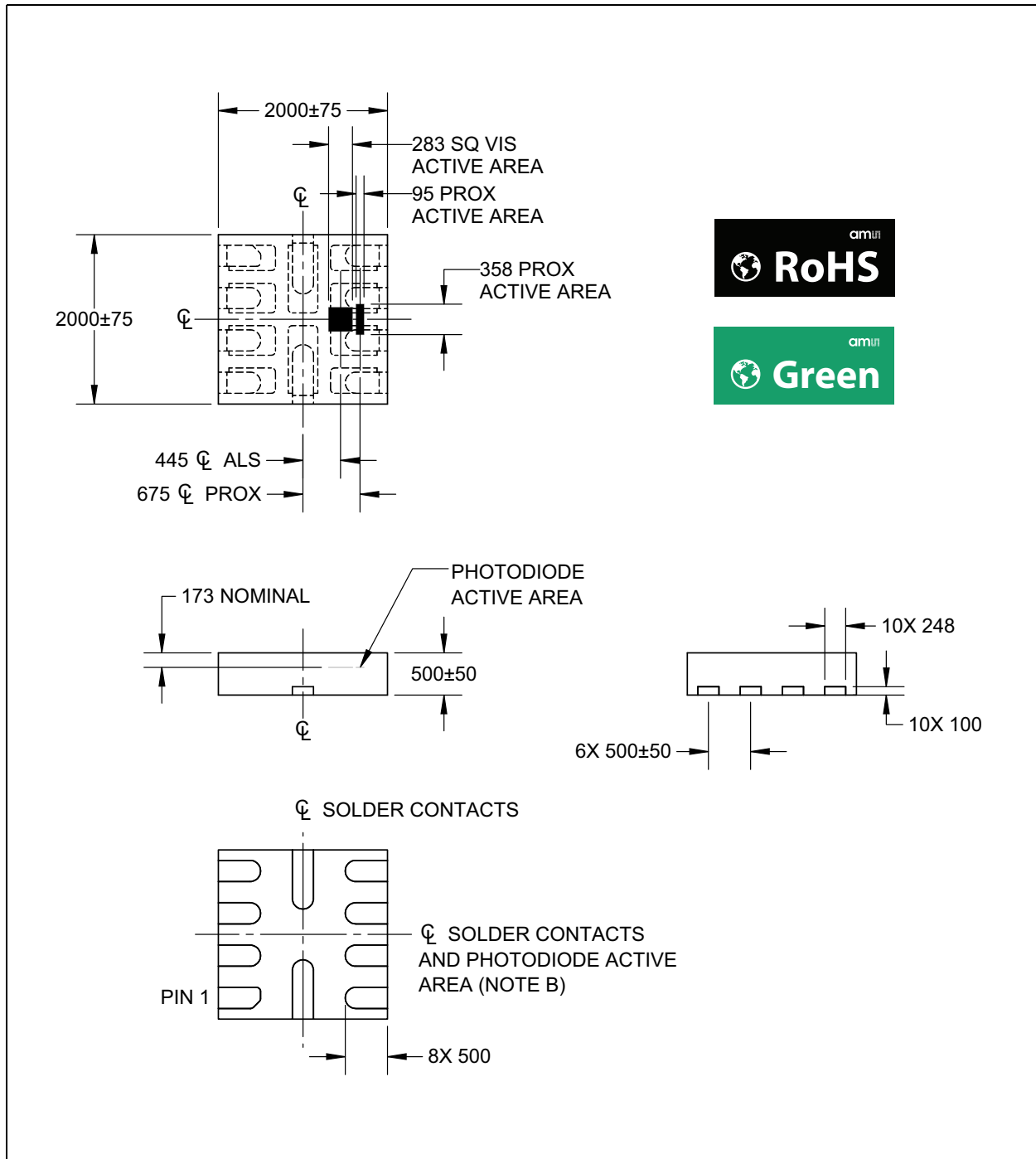
Note(s):

1. All linear dimensions are in micrometers. Dimension tolerance is ±20µm unless otherwise stated.

2. The die is centered vertically within the package within a tolerance of ±75µm.

3. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.

4. Contact finish is Copper Alloy A194 with pre-plated NiPdAu lead finish.

5. This package contains no lead (Pb).

6. This drawing is subject to change without notice.

Figure 51:
Recommended PCB Pad Layout
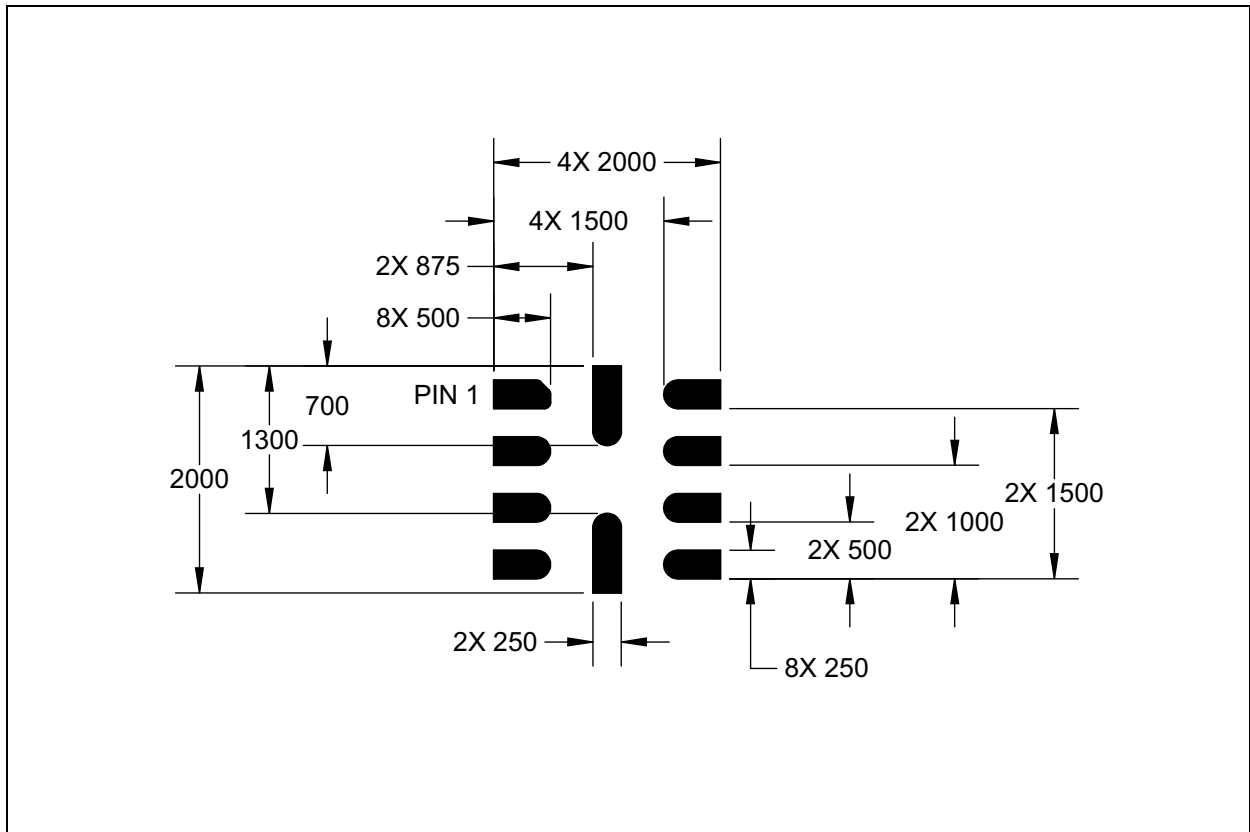
Note(s):

1. All dimensions are in micrometers.

2. Dimension tolerances are 50µm unless otherwise noted.

3. This drawing is subject to change without notice.

Tape & Reel Information

Figure 52:
Tape and Reel Information
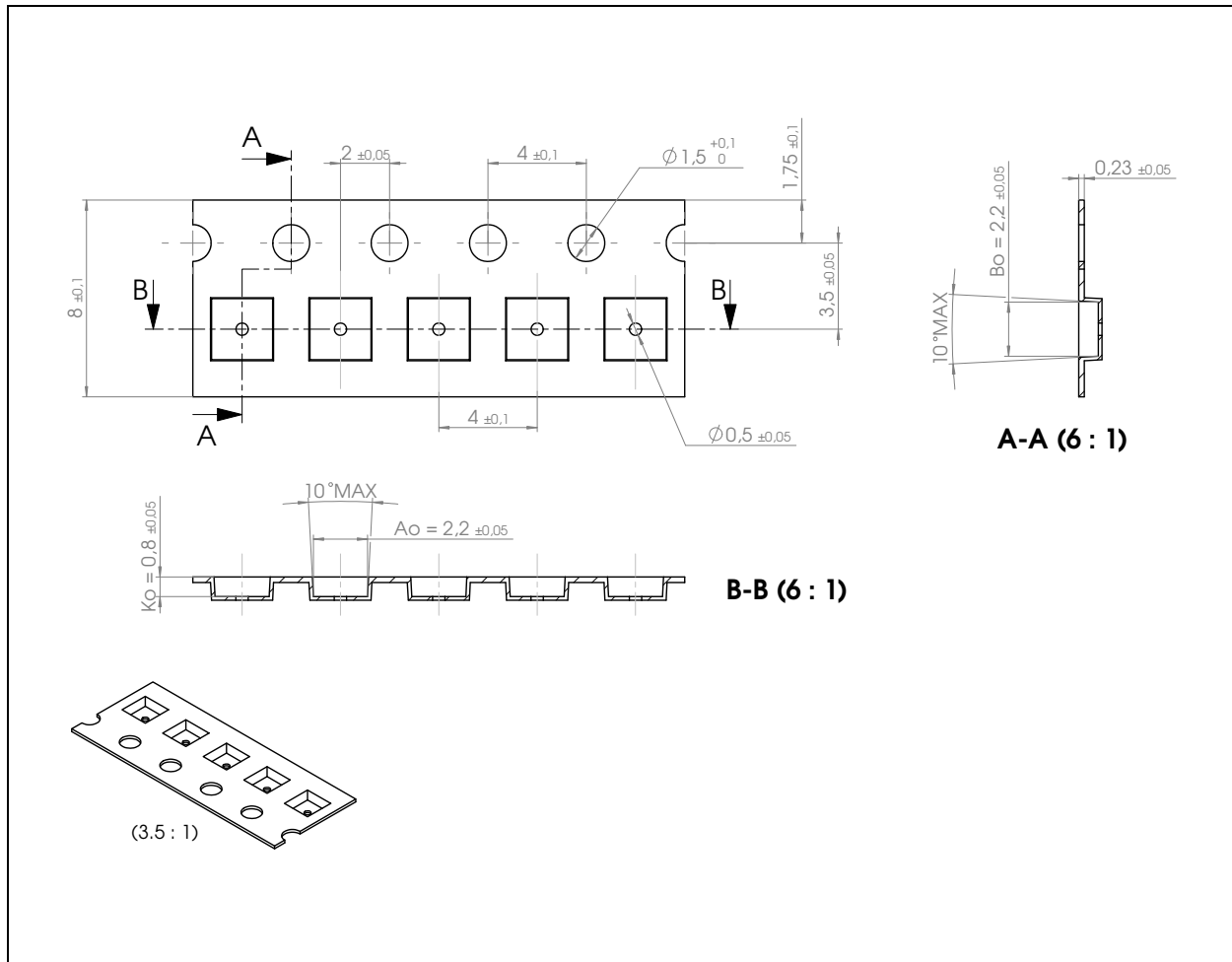
Note(s):

1. All linear dimensions are in millimeters.

2. For missing tolerances and dimensions, refer to EIA-481.

Soldering & Storage Information

The QFN package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 53:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5°C/s
Soak time	t_{SOAK}	2 to 3 minutes
Time above 217°C (T_1)	t_1	Max 60s
Time above 230°C (T_2)	t_2	Max 50s
Time above T_{peak} - 10°C (T_3)	t_3	Max 10s
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max - 5°C/s

Figure 54:
Solder Reflow Profile Graph
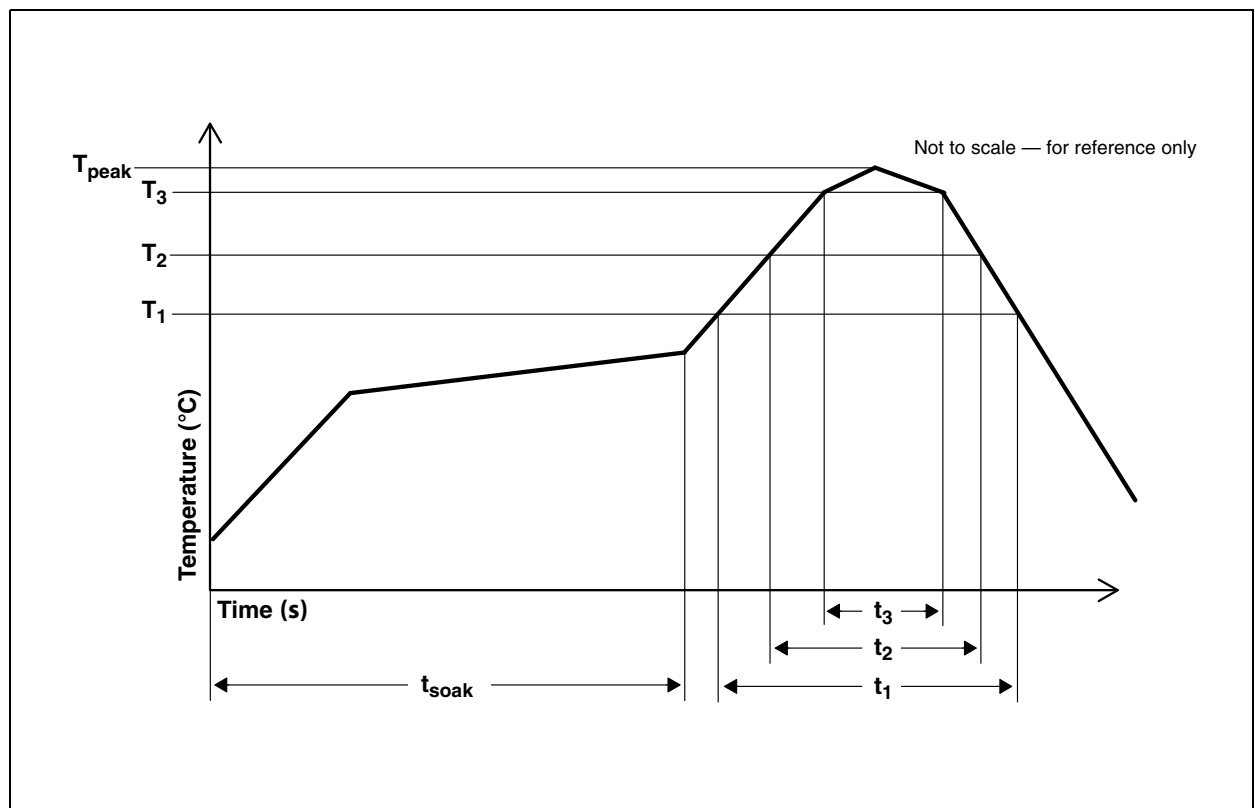
Storage Information

Moisture Sensitivity Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The QFN package has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Ordering & Contact Information

Ordering Code	I²C Bus	I²C Address	Delivery Form	Delivery Quantity
TSL27403	1.8V	39h	Tape and Reel	10000 pcs/reel
TSL27403M	1.8V	39h	Tape and Reel	1000 pcs/reel

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Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Revision Information

Changes from 0-05 (2017-Aug-28) to current revision 1-00 (2017-Nov-06)	Page
Updated Figure 8 and added note below	6
Updated Figure 9 and added note below	7
Updated Figure 14	13
Updated REVID Register	25
Updated REVID2 Register	28
Updated Figure 49	36

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.

2. Correction of typographical errors is not explicitly mentioned.

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Content Guide