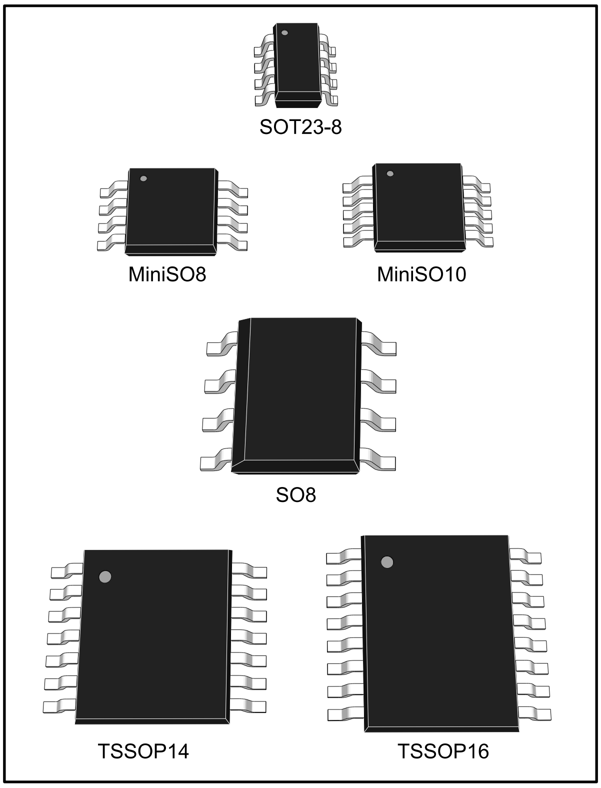
TSV639x, TSV639xA

Micropower (60 µA), wide bandwidth (2.4 MHz) CMOS op amps

Datasheet - production data



Features

- Rail-to-rail input and output
- Low-power consumption: 60 µA typ at 5 V
- Low supply voltage: 1.5 V - 5.5 V
- Gain bandwidth product: 2.4 MHz typ, stable for gain equal or above -3 or 4
- Low-power shutdown mode: 5 nA typ
- Low offset voltage: 800 µV max (A version)
- Low input bias current: 1 pA typ
- EMI hardened operational amplifiers
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40 °C to 125 °C

Applications

- Battery-powered applications
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation

Description

The TSV639x series of dual and quad operational amplifiers (op amps) offers low voltage operation and rail-to-rail input and output.

For applications configured with gain, the TSV639x series offers an excellent speed/power consumption ratio, 2.4 MHz gain bandwidth product while consuming only 60 µA at 5 V. The devices also feature an ultra-low input bias current and have a shutdown mode (TSV6393, TSV6395).

These features make the TSV639x family ideal for sensor interfaces, battery supplied and portable applications, as well as active filtering.

Table 1: Device summary

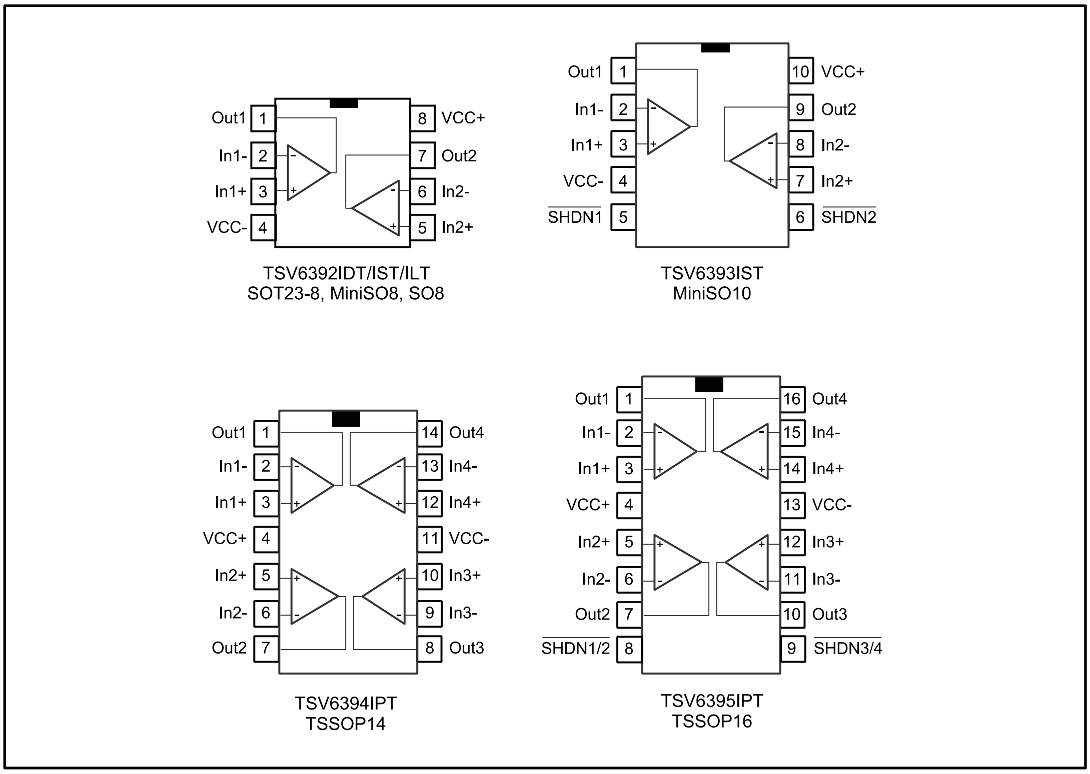
Reference	Dual version		Quad version	
	Without standby	With standby	Without standby	With standby
TSV639x	TSV6392	TSV6393	TSV6394	TSV6395
TSV639xA	TSV6392A	TSV6393A	TSV6394A	TSV6395A

This is information on a product in full production.

Contents

1 Package pin connections

Figure 1: Pin connections for each package (top view)



2 Absolute maximum ratings and operating conditions

Table 2: Absolute maximum ratings (AMR)

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		6	V
V_{id}	Differential input voltage (2)		$\pm V_{CC}$	
V_{in}	Input voltage (3)		$(V_{CC}^{-}) - 0.2$ to $(V_{CC}^{+}) + 0.2$	
I_{in}	Input current (4)		10	mA
$\overline{SHDN}$	Shutdown voltage (3)		$(V_{CC}^{-}) - 0.2$ to $(V_{CC}^{+}) + 0.2$	V
T_{stg}	Storage temperature		-65 to 150	°C
T_j	Maximum junction temperature		150	
R_{thja}	Thermal resistance junction to ambient (5)(6)	SOT23-8	105	°C/W
		MiniSO8	190	
		MiniSO10	113	
		SO8	125	
		TSSOP14	100	
		TSSOP16	95	
ESD	HBM: human body model (7)		4	kV
	MM: machine model (8)		300	V
	CDM: charged device model (9)		1.5	kV
	Latch-up immunity		200	mA

Notes:

(1) All voltage values, except the differential voltage are with respect to the network ground terminal.

(2) Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.

(3) $V_{CC} - V_{in}$ must not exceed 6 V, V_{in} must not exceed 6 V.

(4) The input current must be limited by a resistor in-series with the inputs.

(5) R_{th} are typical values.

(6) Short-circuits can cause excessive heating and destructive dissipation.

(7) Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.

(8) Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.

(9) Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

Table 3: Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.5 to 5.5	V
V_{icm}	Common-mode input voltage range	$(V_{CC}^{-}) - 0.1$ to $(V_{CC}^{+}) + 0.1$	
T_{oper}	Operating free-air temperature range	-40 to 125	°C

3 Electrical characteristics

Table 4: Electrical characteristics at VCC+ = 1.8 V with VCC- = 0 V, Vicm = VCC/2, Tamb = 25 °C, and RL connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSV639x			3	mV
		TSV639xA			0.8	
		TSV6393AIST (MiniSO10)			1	
		$T_{min} < T_{op} < T_{max}$, TSV639x			4.5	
		$T_{min} < T_{op} < T_{max}$, TSV639xA			2	
		$T_{min} < T_{op} < T_{max}$, TSV6393AIST			2.2	
DV_{io}	Input offset voltage drift			2		μV/°C
I_{io}	Input offset current, $V_{out} = V_{CC}/2$			1	10 (1)	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
I_{ib}	Input bias current, $V_{out} = V_{CC}/2$			1	10 (1)	
		$T_{min} < T_{op} < T_{max}$		1	100	
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 1.8 V, V_{out} = 0.9 V	53	74		dB
		$T_{min} < T_{op} < T_{max}$	51			
A_{vd}	Large signal voltage gain	R_L= 10 kΩ, V_{out} = 0.5 V to 1.3 V	85	95		
		$T_{min} < T_{op} < T_{max}$	80			
V_{OH}	High-level output voltage, $V_{OH} = V_{CC} - V_{out}$	R_L = 10 kΩ		5	35	mV
		R_L = 10 kΩ, $T_{min} < T_{op} < T_{max}$			50	
V_{OL}	Low-level output voltage	R_L = 10 kΩ		4	35	
		R_L = 10 kΩ, $T_{min} < T_{op} < T_{max}$			50	
I_{out}	I_{sink}	V_o = 1.8 V	6	12		mA
		$T_{min} < T_{op} < T_{max}$	4			
	I_{source}	V_o = 0 V	6	10		
		$T_{min} < T_{op} < T_{max}$	4			
I_{CC}	Supply current (per operator)	No load, $V_{out} = V_{CC}/2$	40	50	60	μA
		$T_{min} < T_{op} < T_{max}$			62	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF		2		MHz
Gain	Minimum gain for stability	Phase margin = 60 °, R_f = 10 kΩ, R_L = 10 kΩ, C_L = 20 pF		4		V/V
				-3		
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to 1.3 V		0.7		V/μs
e_n	Equivalent input noise voltage	f = 1 kHz		60		nV/√Hz
		f = 10 kHz		33		

Notes:

(1)Guaranteed by design.

Table 5: Shutdown characteristics VCC = 1.8 V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
I_{CC}	Supply current in shutdown mode (all operators)	$\overline{SHDN} = V_{CC}^-$		2.5	50	nA
		$T_{min} < T_{op} < 85$ °C			200	nA
		$T_{min} < T_{op} < 125$ °C			1.5	µA
t_{on}	Amplifier turn-on time	$R_L = 2$ kΩ, $V_{out} = (V_{CC}^-)$ to $(V_{CC}^-) + 0.2$ V		200		ns
t_{off}	Amplifier turn-off time	$R_L = 2$ kΩ, $V_{out} = (V_{CC}^+) - 0.5$ V to $(V_{CC}^+) - 0.7$ V		20		ns
V_{IH}	$\overline{SHDN}$ logic high		1.35			V
V_{IL}	$\overline{SHDN}$ logic low				0.6	V
I_{IH}	$\overline{SHDN}$ current high	$\overline{SHDN} = V_{CC}^+$		10		pA
I_{IL}	$\overline{SHDN}$ current low	$\overline{SHDN} = V_{CC}^-$		10		pA
I_{OLeak}	Output leakage in shutdown mode	$\overline{SHDN} = V_{CC}^-$		50		pA
		$T_{min} < T_{op} < 125$ °C		1		nA

Table 6: Electrical characteristics at VCC+ = 3.3 V, VCC- = 0 V, Vicm = VCC/2, Tamb = 25 °C, RL connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSV639x			3	mV
		TSV639xA			0.8	
		TSV6393AIST (MiniSO10)			1	
		$T_{min} < T_{op} < T_{max}$, TSV639x			4.5	
		$T_{min} < T_{op} < T_{max}$, TSV639xA			2	
		$T_{min} < T_{op} < T_{max}$, TSV6393AIST			2.2	
DV_{io}	Input offset voltage drift			2		μV/°C
I_{io}	Input offset current			1	10 [1]	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
I_{ib}	Input bias current			1	10 [1]	
		$T_{min} < T_{op} < T_{max}$		1	100	
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 3.3 V, V_{out} = 1.65 V	57	79		dB
		$T_{min} < T_{op} < T_{max}$	53			
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_{out} = 0.5 V to 2.8 V	88	98		
		$T_{min} < T_{op} < T_{max}$	83			
V_{OH}	High-level output voltage, $V_{OH} = V_{CC} - V_{out}$	R_L = 10 kΩ		6	35	mV
		R_L = 10 kΩ, $T_{mi.} < T_{op} < T_{max}$			50	
V_{OL}	Low-level output voltage	R_L = 10 kΩ		7	35	
		R_L = 10 kΩ, $T_{min} < T_{op} < T_{max}$			50	
I_{out}	I_{sink}	V_o = 3.3 V	23	45		mA
		$T_{min} < T_{op} < T_{max}$	20			
	I_{source}	V_o = 0 V	23	38		
		$T_{min} < T_{op} < T_{max}$	20			
I_{CC}	Supply current (per operator)	No load, V_{out} = 1.75 V	43	55	64	μA
		$T_{min} < T_{op} < T_{max}$			66	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF		2.2		MHz
Gain	Minimum gain for stability	Phase margin = 60 °, R_f = 10 kΩ, R_L = 10 kΩ, C_L = 20 pF		4		V/V
				-3		
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to 2.8 V		0.9		V/μs

Notes:

[1]Guaranteed by design.

Table 7: Electrical characteristics at VCC+ = 5 V with VCC- = 0 V, Vicm = VCC/2, Tamb = 25 °C, and RL connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltages	TSV639x			3	mV
		TSV639xA			0.8	
		TSV6393AIST (MiniSO10)			1	
		$T_{min} < T_{op} < T_{max}$, TSV639x			4.5	
		$T_{min} < T_{op} < T_{max}$, TSV639xA			2	
		$T_{min} < T_{op} < T_{max}$, TSV6393AIST			2.2	
DV_{io}	Input offset voltage drift			2		μV/°C
I_{io}	Input offset current, $V_{out} = V_{CC}/2$			1	10 (1)	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
I_{ib}	Input bias current, $V_{out} = V_{CC}/2$			1	10 (1)	
		$T_{min} < T_{op} < T_{max}$		1	100	
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 5 V, V_{out} = 2.5 V	60	80		dB
		$T_{min} < T_{op} < T_{max}$	55			
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$)	V_{CC} = 1.8 to 5 V	75	93		
		$T_{min} < T_{op} < T_{max}$	73			
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_{out} = 0.5 V to 4.5 V	89	98		
		$T_{min} < T_{op} < T_{max}$	84			
EMIRR	EMI rejection ratio, EMIRR = -20 log ($V_{RFpeak}/\Delta V_{io}$)	V_{RF} = 100 mV_{rms}, f = 400 MHz		61		
		V_{RF} = 100 mV_{rms}, f = 900 MHz		85		
		V_{RF} = 100 mV_{rms}, f = 1800 MHz		92		
		V_{RF} = 100 mV_{rms}, f = 2400 MHz		83		
V_{OH}	High-level output voltage, $V_{OH} = V_{CC} - V_{out}$	R_L = 10 kΩ		7	35	mV
		R_L = 10 kΩ, $T_{min} < T_{op} < T_{max}$			50	
V_{OL}	Low-level output voltage	R_L = 10 kΩ		6	35	
		R_L = 10 kΩ, $T_{min} < T_{op} < T_{max}$			50	
I_{out}	I_{sink}	V_o = 5 V	40	65		mA
		$T_{min} < T_{op} < T_{max}$	35			
	I_{source}	V_o = 0 V	40	72		
		$T_{min} < T_{op} < T_{max}$	35			
I_{CC}	Supply current (per operator)	No load, $V_{out} = V_{CC}/2$	50	60	69	μA
		$T_{min} < T_{op} < T_{max}$			72	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF		2.4		MHz
Gain	Minimum gain for stability	Phase margin = 60 °, R_f = 10 kΩ, R_L = 10 kΩ, C_L = 20 pF,		4		V/V
				-3		
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF		1.1		V/μs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
e_n	Equivalent input noise voltage	f = 1 kHz		60		nV/√Hz
		f = 10 kHz		33		
THD+N	Total harmonic distortion + noise	V_{CC} = 5 V, f_{in} = 1 kHz, A_{CL} = -10, R_L = 100 kΩ, V_{icm} = $V_{CC}/2$, BW = 22 kHz, V_{out} = 1 V_{rms}		0.015		%

Notes:

(1)Guaranteed by design.

Table 8: Shutdown characteristics at VCC = 5 V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
I_{CC}	Supply current in shutdown mode (all operators)	$\overline{SHDN}$ = V_{CC}^-		5	50	nA
		T_{min} < T_{op} < 85 °C			200	
		T_{min} < T_{op} < 125 °C			1.5	µA
t_{on}	Amplifier turn-on time	R_L = 2 kΩ, V_{out} = (V_{CC}^-) V to (V_{CC}^-) + 0.2 V		200		ns
t_{off}	Amplifier turn-off time	R_L = 2 kΩ, V_{out} = (V_{CC}^+) - 0.5 V to (V_{CC}^+) - 0.7 V		20		
V_{IH}	$\overline{SHDN}$ logic high		2			V
V_{IL}	$\overline{SHDN}$ logic low				0.8	V
I_{IH}	$\overline{SHDN}$ current high	$\overline{SHDN}$ = V_{CC}^+		10		pA
I_{IL}	$\overline{SHDN}$ current low	$\overline{SHDN}$ = V_{CC}^-		10		
I_{OLeak}	Output leakage in shutdown mode	$\overline{SHDN}$ = V_{CC}^-		50		
		T_{min} < T_{op} < 125 °C		1		nA

4 Electrical characteristic curves

Figure 2: Supply current vs. supply voltage at Vicm = VCC/2

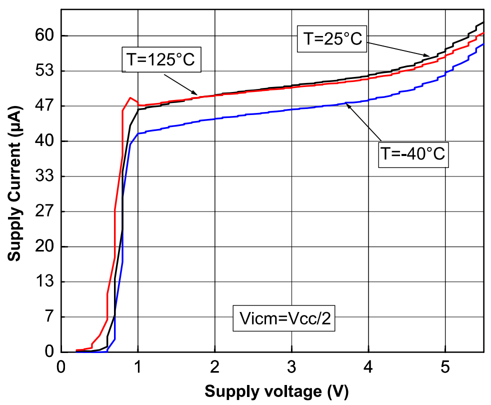


Figure 3: Output current vs. output voltage at VCC = 1.5 V

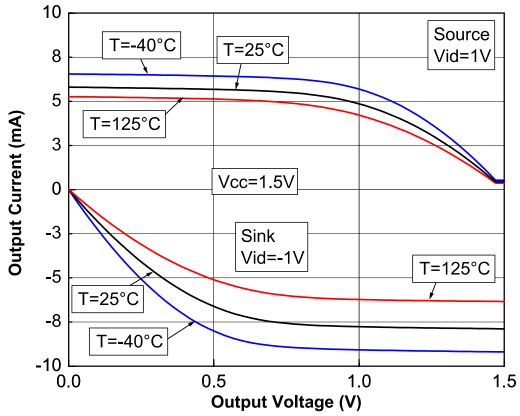


Figure 4: Output current vs. output voltage at VCC = 5 V

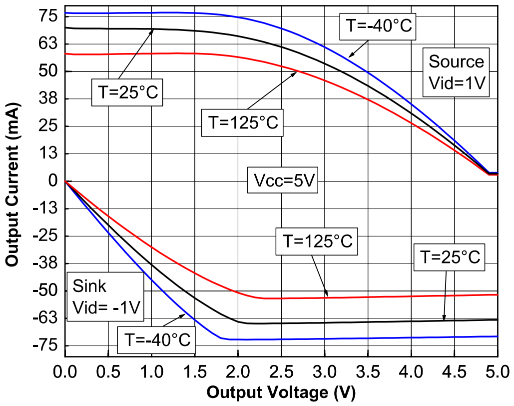


Figure 5: Closed loop response for gain = -10, at VCC = 1.5 V and VCC = 5 V

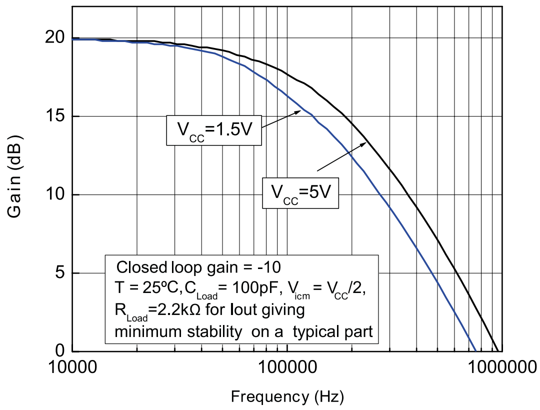


Figure 6: Closed loop response for gain = -3 at VCC = 1.5 V

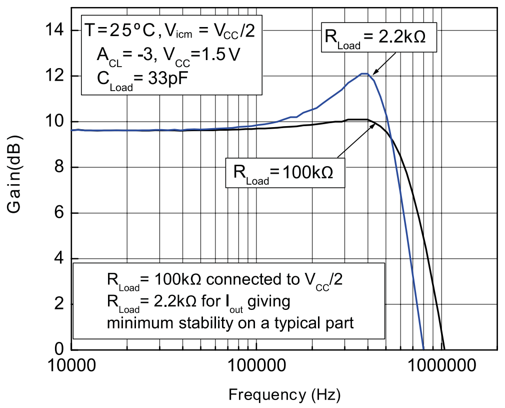


Figure 7: Closed loop response for gain = -3 at VCC = 5 V

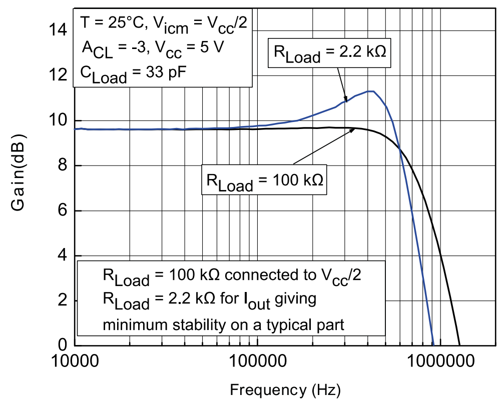


Figure 8: Positive slew rate vs. supply voltage in closed loop

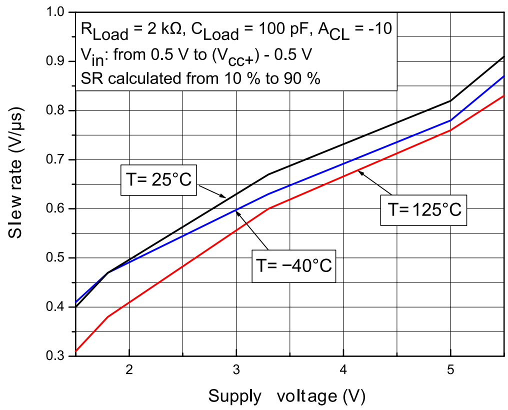


Figure 9: Negative slew rate vs. supply voltage in closed loop

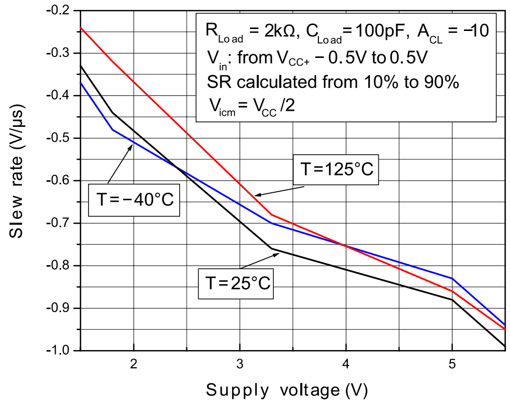


Figure 10: Slew rate vs. supply voltage in open loop

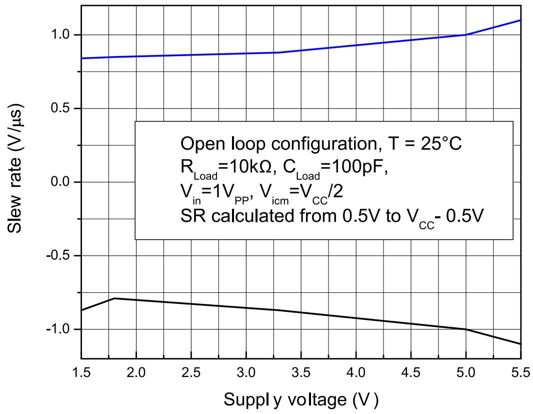


Figure 11: Slew rate timing in open loop

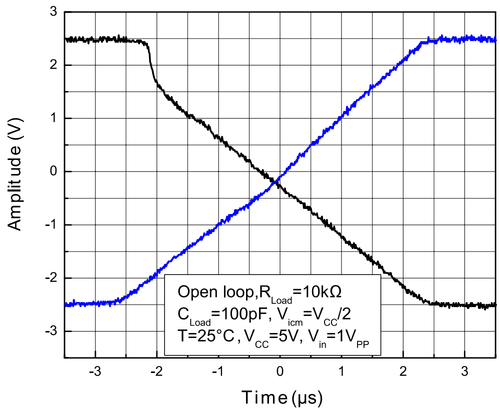


Figure 12: Slew rate timing in closed loop

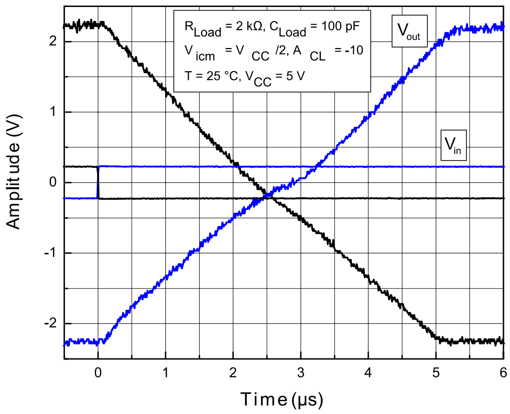


Figure 13: Noise vs. frequency

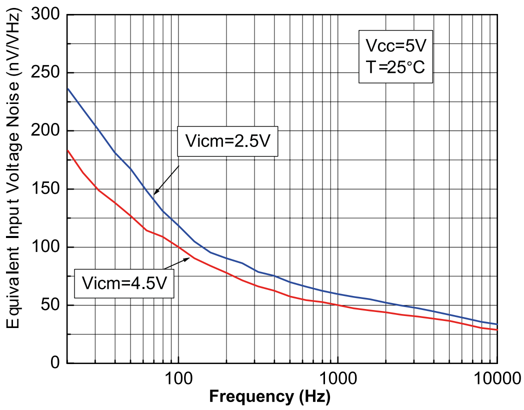


Figure 14: Distortion and noise vs. output voltage at VCC = 1.8 V

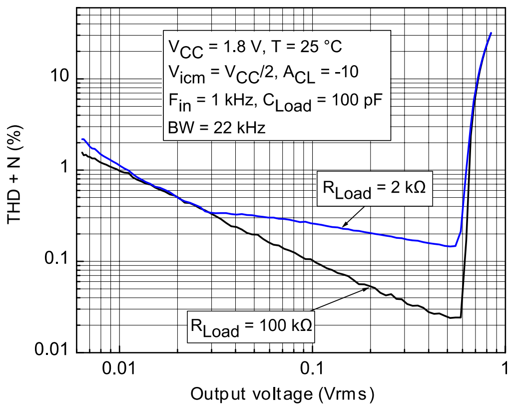


Figure 15: Distortion and noise vs. frequency at VCC = 1.8 V

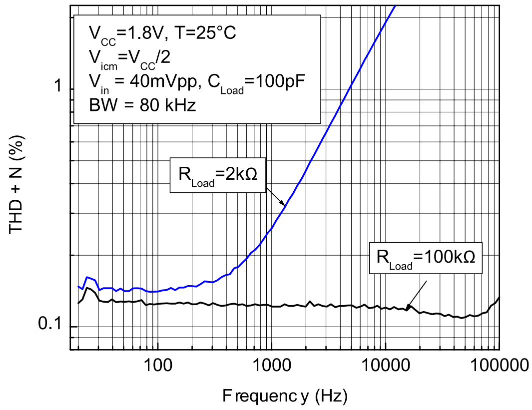


Figure 16: Distortion and noise vs. output voltage at VCC = 5 V

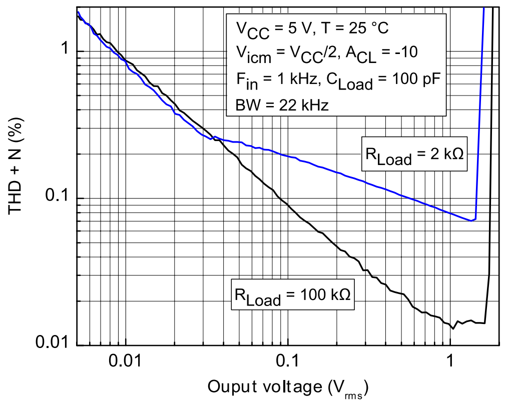


Figure 17: Distortion and noise vs. frequency at VCC = 5 V

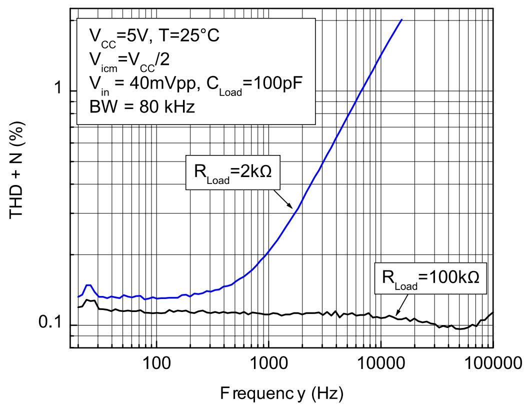
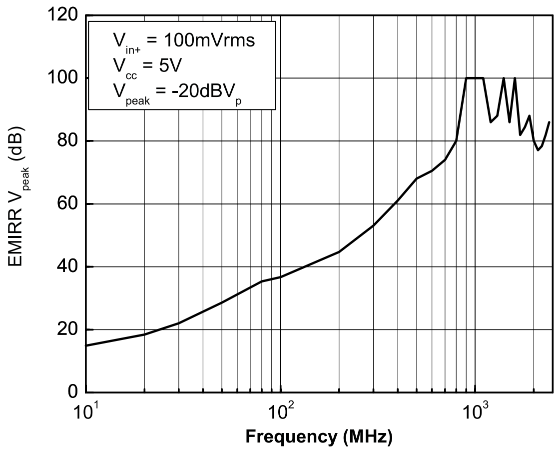


Figure 18: EMIRR vs. frequency at VCC = 5 V, T = 25 °C



5 Application information

5.1 Operating voltages

The TSV639x can operate from 1.5 to 5.5 V. Their parameters are fully specified for 1.8, 3.3 and 5 V power supplies. However, the parameters are very stable in the full V_{CC} range and several characterization curves show the TSV639x characteristics at 1.5 V. Additionally, the main specifications are guaranteed in extended temperature ranges from -40 °C to 125 °C.

5.2 Rail-to-rail input

The TSV639x are built with two complementary PMOS and NMOS input differential pairs. The devices have a rail-to-rail input, and the input common mode range is extended from (V_{CC}^{-}) - 0.1 V to (V_{CC}^{+}) + 0.1 V. The transition between the two pairs appears at (V_{CC}^{+}) - 0.7 V. In the transition region, the performance of CMR, SVR, V_{io} (*Figure 19* and *Figure 20*) and THD is slightly degraded.

Figure 19: Input offset voltage vs input common-mode at VCC = 1.5 V

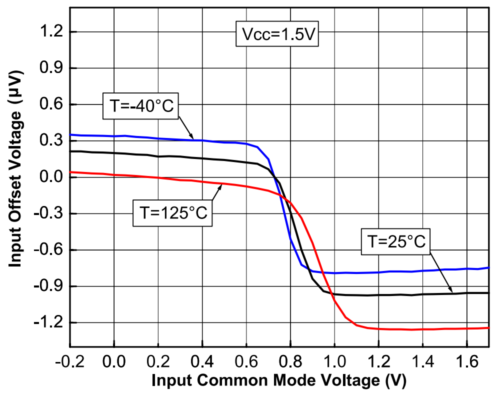
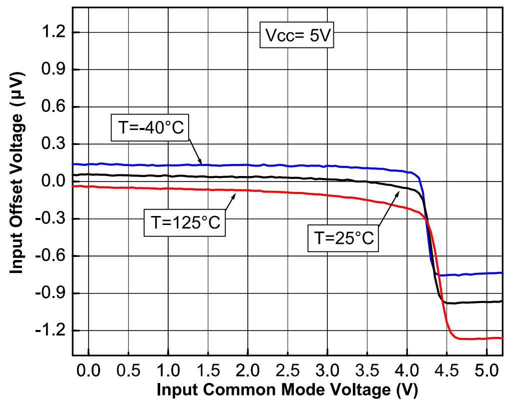


Figure 20: Input offset voltage vs input common-mode at VCC = 5 V



The devices are guaranteed without phase reversal.

5.3 Rail-to-rail output

The operational amplifiers' output levels can go close to the rails: 35 mV maximum above and below the rail when connected to a 10 kΩ resistive load to $V_{CC}/2$.

5.4 Shutdown function (TSV6393 - TSV6395)

The operational amplifiers are enabled when the $\overline{SHDN}$ pin is pulled high. To disable the amplifiers, the $\overline{SHDN}$ must be pulled down to V_{CC}^-. When in shutdown mode, the amplifiers' output is in a high impedance state. The $\overline{SHDN}$ pin must never be left floating but tied to V_{CC}^+ or V_{CC}^-.

The turn-on and turn-off times are calculated for an output variation of 200 mV (*Figure 21* and *Figure 22* show the test configurations).

Figure 21: Test configuration for turn-on time (Vout pulled down)

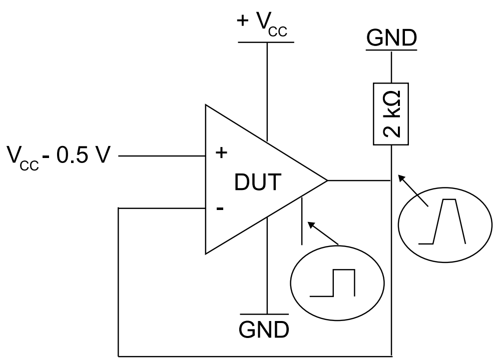


Figure 22: Test configuration for turn-off time (Vout pulled down)

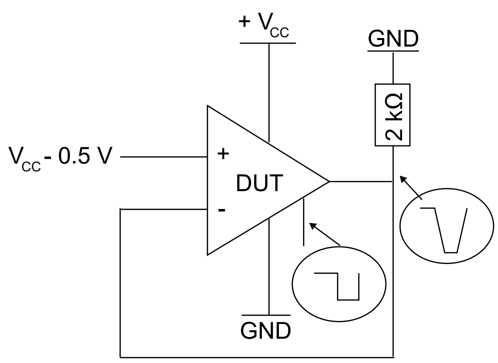


Figure 23: Turn-on time, VCC = 5 V, Vout pulled down, T = 25 °C

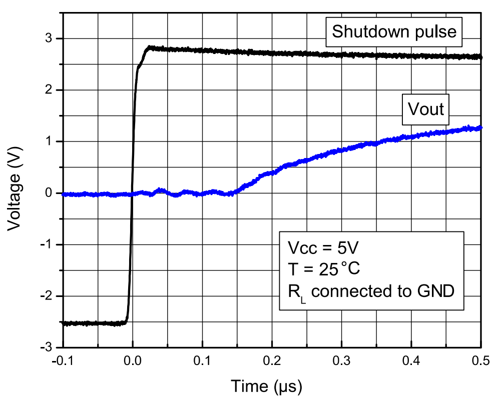
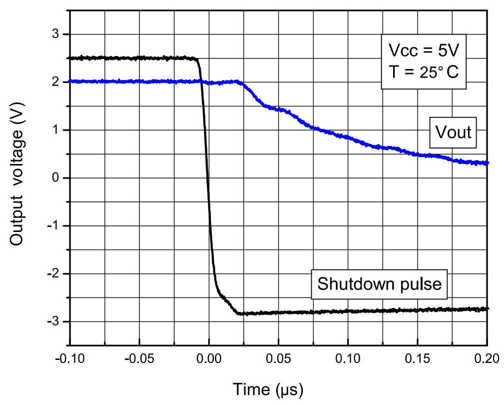


Figure 24: Turn-off time, VCC = 5 V, Vout pulled down, T = 25 °C



5.5 Optimization of DC and AC parameters

These devices use an innovative approach to reduce the spread of the main DC and AC parameters. An internal adjustment achieves a very narrow spread of the current consumption (60 µA typical, min/max at ±17 %). Parameters linked to the current consumption value, such as GBP, SR and A_{vd}, benefit from this narrow dispersion.

5.6 Driving resistive and capacitive loads

These products are micropower, low-voltage operational amplifiers optimized to drive rather large resistive loads, above 2 kΩ. For lower resistive loads, the THD level may significantly increase.

The amplifiers have a relatively low internal compensation capacitor, making them very fast while consuming very little. They are ideal when used in a non-inverting configuration or in an inverting configuration in the following conditions.

- IGainI ≥ 3 in an inverting configuration (C_L = 20 pF, R_L = 100 kΩ) or IgainI ≥ 10 (C_L = 100 pF, R_L = 100 kΩ)
- Gain ≥ 4 in a non-inverting configuration (C_L = 20 pF, R_L = 100 kΩ) or gain ≥ 11 (C_L = 100 pF, R_L= 100 kΩ)

As these operational amplifiers are not unity gain stable, for a low closed-loop gain, it is recommended to use the TSV63x (60 µA, 880 kHz) which is unity gain stable.

Table 9: Related products

Part #	Icc (µA) at 5 V	GBP (MHz)	SR (V/µs)	Minimum gain for stability (C_{Load} = 100 pF)
TSV62-2-3-4-5	29	0.42	0.14	1
TSV629-2-3-4-5	29	1.3	0.5	11
TSV63-2-3-4-5	60	0.88	0.34	1
TSV639-2-3-4-5	60	2.4	1.1	11

5.7 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

5.8 Macromodel

Two accurate macromodels (with or without shutdown feature) of the TSV639x are available on STMicroelectronics' web site at ***www.st.com***. This model is a trade-off between accuracy and complexity (that is, time simulation) of the TSV639x operational amplifiers. It emulates the nominal performances of a typical device within the specified operating conditions mentioned in the datasheet. It also helps to validate a design approach and to select the right operational amplifier, *but it does not replace on-board measurements*.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

6.1 SOT23-8 package information

Figure 25: SOT23-8 package outline

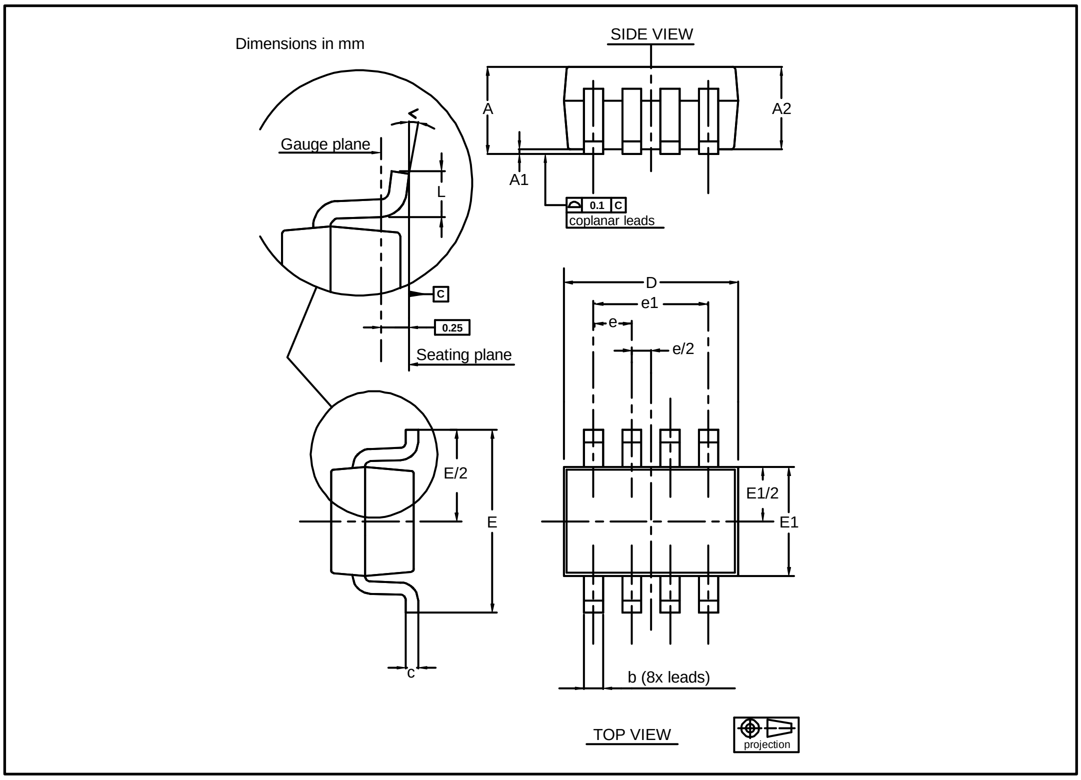


Table 10: SOT23-8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.45			0.057
A1			0.15			0.006
A2	0.90		1.30	0.035		0.051
b	0.22		0.38	0.009		0.015
c	0.08		0.22	0.003		0.009
D	2.80		3.00	0.110		0.118
E	2.60		3.00	0.102		0.118
E1	1.50		1.75	0.059		0.069
e		0.65			0.026	
e1		1.95			0.077	
L	0.30		0.60	0.012		0.024
<	0 °		8 °	0 °		8 °

6.2 MiniSO8 package information

Figure 26: MiniSO8 package outline

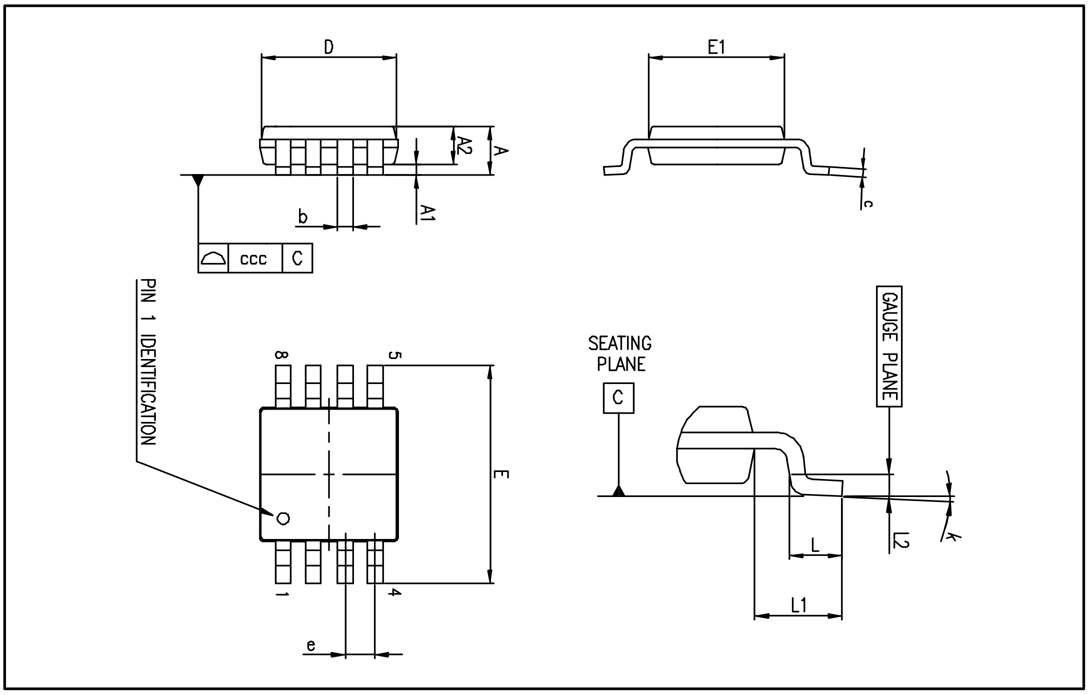


Table 11: MiniSO8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

6.3 MiniSO10 package information

Figure 27: MiniSO10 package outline

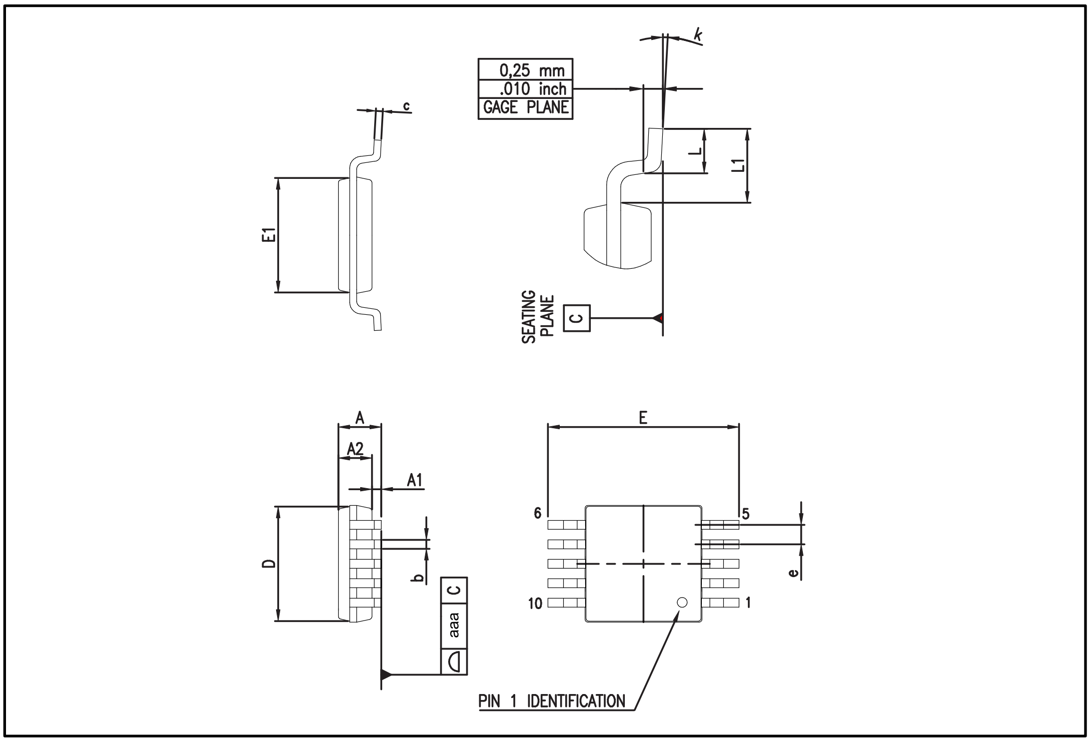


Table 12: MiniSO10 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.10			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.034	0.037
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.15	0.23	0.30	0.006	0.009	0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	0.114	0.118	0.122
e		0.50			0.020	
L	0.40	0.55	0.70	0.016	0.022	0.028
L1		0.95			0.037	
k	0 °	3 °	6 °	0 °	3 °	6 °
aaa			0.10			0.004

6.4 SO8 package information

Figure 28: SO8 package outline

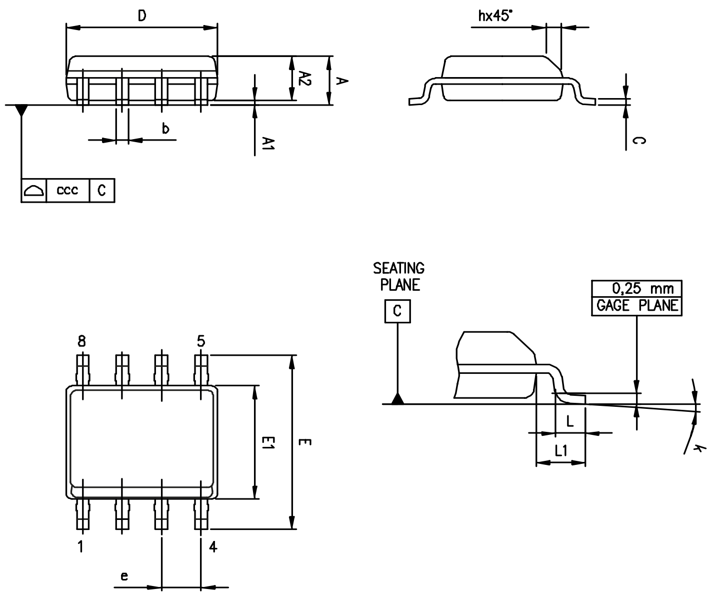


Table 13: SO8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004

6.5 TSSOP14 package information

Figure 29: TSSOP14 package outline

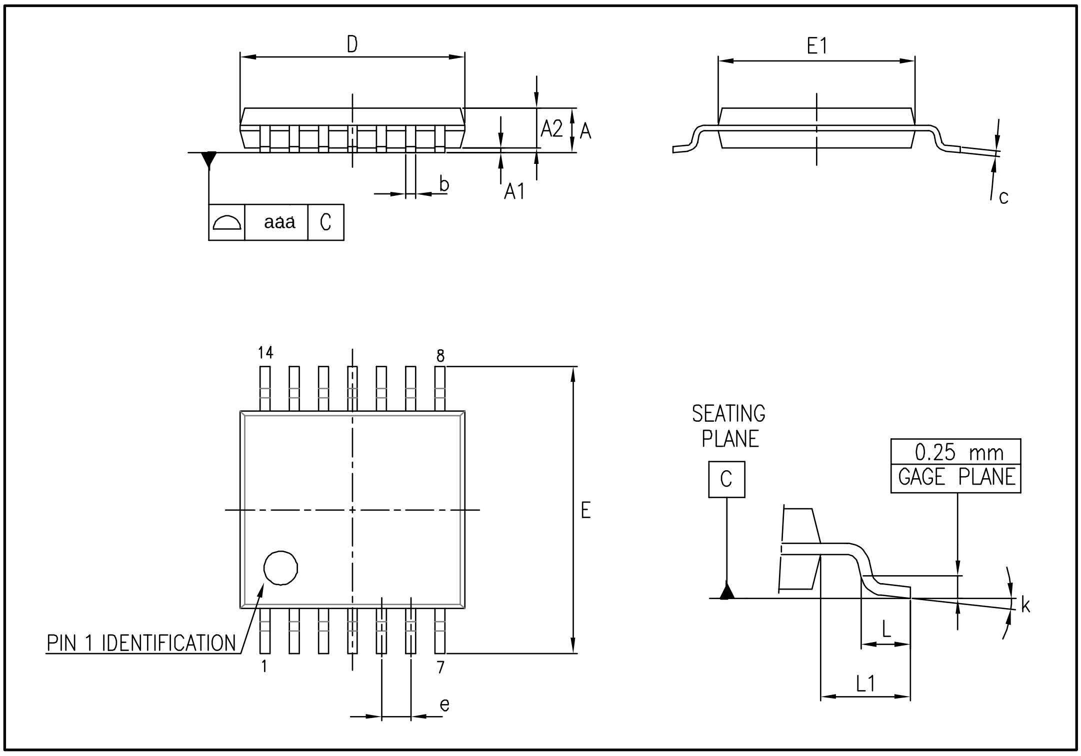


Table 14: TSSOP14 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.176
e		0.65			0.0256	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°		8°	0°		8°
aaa			0.10			0.004

6.6 TSSOP16 package information

Figure 30: TSSOP16 package outline

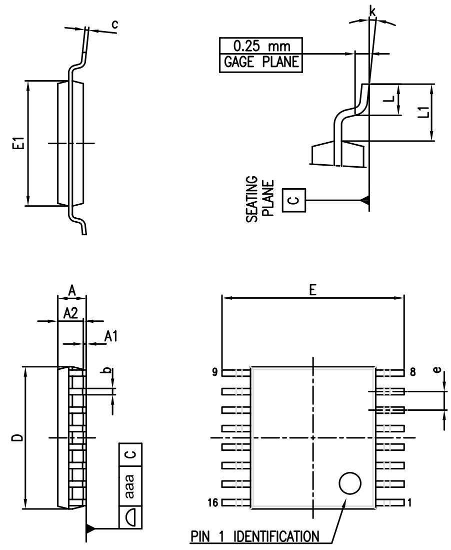


Table 15: TSSOP16 mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.026	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
aaa			0.10			0.004

7 Ordering information

Table 16: Order codes

Order code	Temperature range	Package	Packing	Marking
TSV6392IDT	-40 °C to 125 °C	SO8	Tape and reel	V6392I
TSV6392AIDT				V632AI
TSV6392IST		MiniSO8		K111
TSV6392AIST				K146
TSV6392ILT		SOT23-8		K111
TSV6393IST		MiniSO10		K111
TSV6393AIST				K145
TSV6394IPT		TSSOP14		V6394I
TSV6394AIPT				V6394AI
TSV6395IPT		TSSOP16		V6395I
TSV6395AIPT				V6395AI

8 Revision history

Table 17: Document revision history

Date	Revision	Changes
18-Jan-2010	1	Initial release
29-Feb-2016	2	Updated layout *Table 4*, *Table 6*, and *Table 7*: for V_{OH}, added $V_{OH} = V_{CC} - V_{out}$ to the parameter column; moved the values in the “min” column to the “max” column. *Table 10: "SOT23-8 mechanical data"*: added angle information to “Inches” columns. *Table 16: "Order codes"*: removed obsolete order codes TSV6392ID and TSV6392AID.