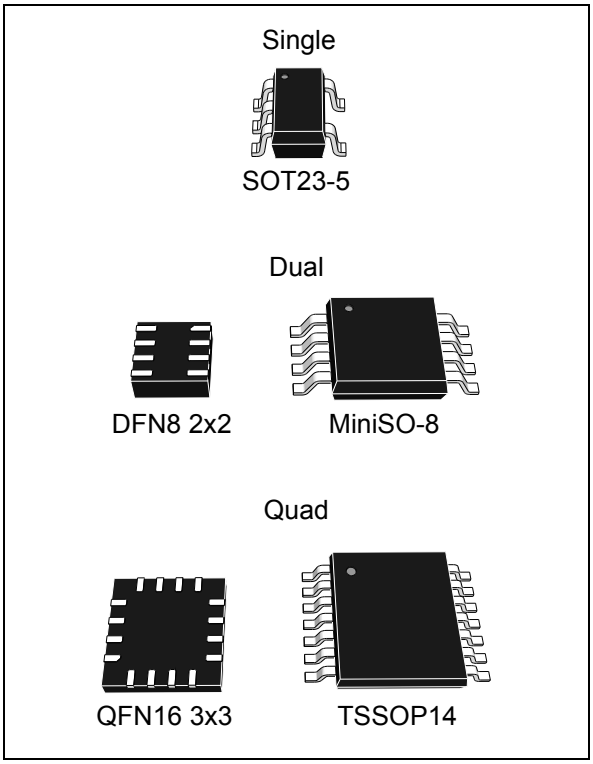
# TSX631, TSX632, TSX634, TSX631A, TSX632A, TSX634A

## Micropower (45 µA, 200 kHz) rail-to-rail 16 V CMOS operational amplifiers

**Datasheet - production data**




## Features

- Low power consumption: 60 µA max at 16 V
- Supply voltage: 3.3 V to 16 V
- Rail-to-rail input and output
- Gain bandwidth product: 200 kHz typ
- Low offset voltage:
  - 500 µV max for “A” version
  - 1 mV max for standard version
- Low input bias current: 1 pA typ
- Automotive qualification

### Benefits

- Power savings in power-conscious applications
- Easy interfacing with high impedance sensors

### Related products

- See TSX56x or TSX92x series for higher gain bandwidth products (900 kHz or 10 MHz)

## Applications

- Industrial signal conditioning
- Automotive signal conditioning
- Active filtering
- Medical instrumentation
- High impedance sensors

## Description

The TSX63x and TSX63xA series of operational amplifiers offer low voltage operation and rail-to-rail input and output. TSX631 is the single version, TSX632 the dual version and TSX634 the quad version, with pinouts compatible with industry standards.

The TSX63x and TSX63xA series offer a 200 kHz gain bandwidth product while consuming 60 µA maximum at 16 V.

The devices are housed in the tiniest industrial packages.

These features make the TSX63x and TSX63xA family ideal for sensor interfaces and industrial signal conditioning. The wide temperature range and high ESD tolerance ease the use in harsh automotive applications.

**Table 1. Device summary**

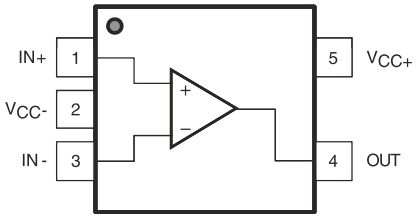
| Op-amp version | Standard $V_{io}$ | Enhanced $V_{io}$ |
|---|---|---|
| Single | TSX631 | TSX631A |
| Dual | TSX632 | TSX632A |
| Quad | TSX634 | TSX634A |

# Contents

# 1 Package pin connections

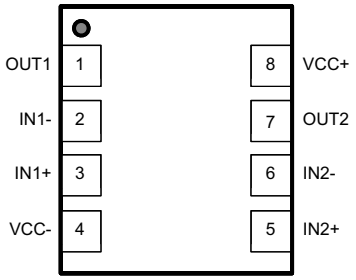
**Figure 1. Pin connections for each package (top view)**

**Single**

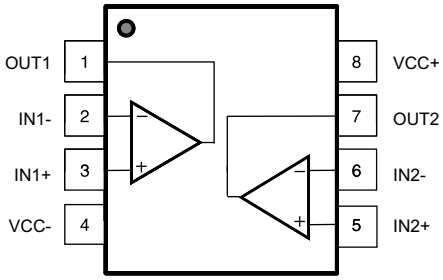



**SOT23-5 (TSX631)**

**Dual**

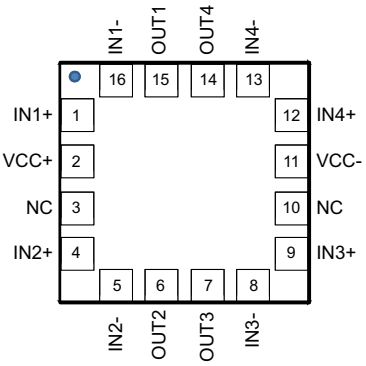



**DFN8 2x2 (TSX632)**

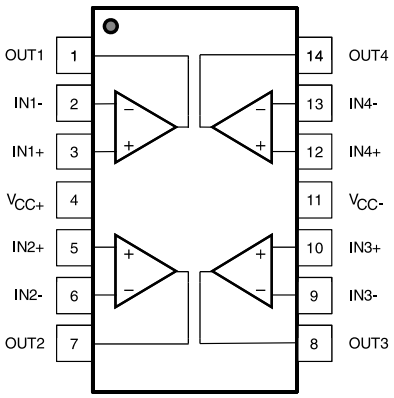



**Mini-SO8 (TSX632)**

**Quad**




**QFN16 3x3 (TSX634)**




**TSSOP14 (TSX634)**

# 2 Absolute maximum ratings and operating conditions

**Table 2. Absolute maximum ratings (AMR)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply voltage(1) | 18 | V |
| $V_{id}$ | Differential input voltage (2) | $\pm V_{CC}$ | |
| $V_{in}$ | Input voltage(3) | $V_{CC-}$ - 0.2 to $V_{CC+}$ + 0.2 | |
| $I_{in}$ | Input current(4) | 10 | mA |
| $T_{stg}$ | Storage temperature | -65 to +150 | °C |
| $R_{thja}$ | Thermal resistance junction to ambient(5)(6)<br>SOT23-5<br>DFN8 2x2<br>MiniSO-8<br>QFN16 3x3<br>TSSOP14 | <br>250<br>120<br>190<br>80<br>100 | °C/W |
| $R_{thjc}$ | Thermal resistance junction to case<br>DFN8 2x2<br>QFN16 3x3 | <br>33<br>30 | |
| $T_j$ | Maximum junction temperature | 160 | °C |
| ESD | HBM: human body model(7) | 4 | kV |
| | MM: machine model(8) | 200 | V |
| | CDM: charged device model(9) | 1.3 | kV |
| | Latch-up immunity | 200 | mA |

1. All voltage values, except the differential voltage are with respect to network ground terminal.
2. The differential voltage is the non-inverting input terminal with respect to the inverting input terminal. See *Section 4.5* for precautions of using the TSX631 with high differential input voltage.
3. $V_{CC}$-$V_{in}$ must not exceed 18 V, $V_{in}$ must not exceed 18 V.
4. Input current must be limited by a resistor in series with the inputs.
5. Short-circuits can cause excessive heating and destructive dissipation.
6. $R_{th}$ are typical values.
7. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
8. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
9. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

**Table 3. Operating conditions**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 3.3 to 16 | V |
| $V_{icm}$ | Common mode input voltage range | $V_{CC-}$ - 0.1 to $V_{CC+}$ + 0.1 | |
| $T_{oper}$ | Operating free air temperature range | -40 to +125 | °C |

# 3 Electrical characteristics

**Table 4. Electrical characteristics at $V_{CC+}$ = +3.3 V with $V_{CC-}$ = 0 V, $V_{icm}$ = $V_{CC}$/2, T = 25 ° C, and $R_L$= 10 kΩ connected to $V_{CC}$/2 (unless otherwise specified)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DC performance** | | | | | | |
| $V_{io}$ | Offset voltage | TSX63xA, T = 25 °C | | | 700 | µV |
| | | TSX63xA, -40°C < T < 125 °C | | | 1500 | |
| | | TSX63x, T = 25 °C | | | 1.6 | mV |
| | | TSX63x, -40°C < T < 125 °C | | | 2.4 | |
| $V_{io}$ | Offset voltage, high common mode ($V_{icm}$=$V_{CC}$, $R_L$ > 1 MΩ) | T = 25 °C | | | 4 | |
| | | -40°C < T < 125 °C | | | 5 | |
| $\Delta V_{io}/\Delta T$ | Input offset voltage drift | -40°C < T < 125 °C(1) | | 1 | 8 | µV/°C |
| $I_{io}$ | Input offset current ($V_{out}$ = $V_{CC}$/2) | T = 25 °C | | 1 | 100(2) | pA |
| | | -40°C < T < 125 °C | | | 200(2) | |
| $I_{ib}$ | Input bias current ($V_{out}$ = $V_{CC}$/2) | T = 25 °C | | 1 | 100(2) | |
| | | -40°C < T < 125 °C | | | 200(2) | |
| $R_{IN}$ | Input resistance | | | 1 | | TΩ |
| $C_{IN}$ | Input capacitance | | | 5 | | pF |
| CMR1 | Common mode rejection ratio CMR = 20 log ($\Delta V_{icm}/\Delta V_{io}$) ($V_{icm}$ = -0.1 V to $V_{CC}$-1.65 V, $V_{out}$ = $V_{CC}$/2, $R_L$ > 1 MΩs) | T = 25 °C | 65 | 79 | | dB |
| | | -40°C < T < 125 °C | 62 | | | |
| CMR2 | Common mode rejection ratio CMR = 20 log ($\Delta V_{icm}/\Delta V_{io}$) ($V_{icm}$ = -0.1 V to $V_{CC}$+0.1 V, $V_{out}$ = $V_{CC}$/2, $R_L$ > 1 MΩ) | T = 25 °C | 59 | 74 | | |
| | | -40°C < T < 125 °C | 55 | | | |
| $A_{vd}$ | Large signal voltage gain ($V_{out}$ = 0.5 V to ($V_{CC}$ - 0.5 V), $R_L$ > 1 MΩ) | T = 25 °C | 100 | 110 | | |
| | | -40°C < T < 125°C | 90 | | | |
| $V_{OH}$ | High level output voltage $V_{id}$ = +1 V, $V_{OH}$ = $V_{CC}$-$V_{out}$ | $R_L$ = 10 kΩ, T = 25 °C | | | 70 | mV |
| | | $R_L$ = 10 kΩ, -40 °C < T < 125 °C | | | 100 | |
| $V_{OL}$ | Low level output voltage $V_{id}$ = -1 V, | $R_L$ = 10 kΩ, T = 25 °C | | | 70 | |
| | | $R_L$ = 10 kΩ, -40°C < T < 125 °C | | | 100 | |
| $I_{out}$ | $I_{sink}$ ($V_{out}$ = $V_{CC}$) | T = 25 °C | 4.3 | 5.3 | | mA |
| | | -40°C < T < 125 °C | 2.5 | | | |
| | $I_{source}$ ($V_{out}$ = 0 V) | T = 25 °C | 3.3 | 4.3 | | |
| | | -40°C < T < 125 °C | 2.5 | | | |
| $I_{CC}$ | Supply current (per operator, $V_{out}$ = $V_{CC}$/2, $R_L$ > 1 MΩ) | T = 25 °C | | 45 | 60 | µA |
| | | -40°C < T < 125 °C | | | 60 | |

**Table 4. Electrical characteristics at $V_{CC+}$ = +3.3 V with $V_{CC-}$ = 0 V, $V_{icm}$ = $V_{CC}$/2, T = 25 ° C, and $R_L$= 10 kΩ connected to $V_{CC}$/2 (unless otherwise specified)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **AC performance** | | | | | | |
| GBP | Gain bandwidth product | $R_L$ = 100 kΩ, $C_L$ = 100 pF | 160 | 200 | | kHz |
| $F_u$ | Unity gain frequency | | | 160 | | |
| $\Phi_m$ | Phase margin | | | 55 | | degrees |
| $G_m$ | Gain margin | | | 9 | | dB |
| SR | Slew rate | $R_L$ = 100 kΩ, $C_L$ = 100 pF, $V_{out}$ = 0.5 V to $V_{CC}$ - 0.5V | | 0.12 | | V/µs |
| $\int e_n$ | Low-frequency peak-to-peak input noise | Bandwidth: f = 0.1 to 10 Hz | | 5 | | $\mu V_{pp}$ |
| $e_n$ | Equivalent input noise voltage | f = 1 kHz | | 60 | | $\frac{nV}{\sqrt{Hz}}$ |
| | | f = 10 kHz | | | | |
| THD+N | Total harmonic distortion + noise | Follower configuration, $f_{in}$ = 1 kHz, $R_L$ = 100 kΩ, $V_{icm}$ = 0.9V, BW = 22 kHz, $V_{out}$ = 1 $V_{pp}$ | | 0.005 | | % |

1. See *Chapter 4.3: Input offset voltage drift over temperature on page 18*
2. Guaranteed by design

**Table 5. Electrical characteristics at $V_{CC+}$ = +5 V with $V_{CC-}$ = 0 V, $V_{icm}$ = $V_{CC}$/2, T = 25 ° C, and $R_L$= 10 kΩ connected to $V_{CC}$/2 (unless otherwise specified)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DC performance** | | | | | | |
| $V_{io}$ | Offset voltage | TSX63xA, T = 25 °C | | | 700 | µV |
| | | TSX63xA, -40°C < T < 125 °C | | | 1500 | |
| | | TSX63x, T = 25 °C | | | 1.6 | mV |
| | | TSX63x, -40°C < T < 125 °C | | | 2.4 | |
| $V_{io}$ | Offset voltage, high common mode ($V_{icm}$=$V_{CC}$, $R_L$ > 1 MΩ) | T = 25 °C | | | 4 | |
| | | -40°C < T < 125 °C | | | 5 | |
| $\Delta V_{io}/\Delta T$ | Input offset voltage drift | -40°C < T < 125 °C(1) | | 1 | 8 | µV/°C |
| $\Delta V_{io}$ | Long term input offset voltage drift | T = 25 °C(2) | | 17 | | $\frac{nV}{\sqrt{month}}$ |
| $I_{io}$ | Input offset current ($V_{out}$ = $V_{CC}$/2) | T = 25 °C | | 1 | 100(3) | pA |
| | | -40°C < T < 125 °C | | | 200(3) | |
| $I_{ib}$ | Input bias current ($V_{out}$ = $V_{CC}$/2) | T = 25 °C | | 1 | 100(3) | |
| | | -40°C < T < 125 °C | | | 200(3) | |
| $R_{IN}$ | Input resistance | | | 1 | | TΩ |
| $C_{IN}$ | Input capacitance | | | 5 | | pF |
| CMR1 | Common mode rejection ratio CMR = 20 log ($\Delta V_{icm}/\Delta V_{io}$) ($V_{icm}$ = -0.1 V to $V_{CC}$-1.65 V, $V_{out}$ = $V_{CC}$/2, $R_L$ > 1 MΩ) | T = 25 °C | 65 | 79 | | dB |
| | | -40°C < T < 125 °C | 62 | | | |
| CMR2 | Common mode rejection ratio CMR = 20 log ($\Delta V_{icm}/\Delta V_{io}$) ($V_{icm}$ = -0.1 V to $V_{CC}$+0.1 V, $V_{out}$ = $V_{CC}$/2, $R_L$ > 1 MΩ) | T = 25 °C | 62 | 77 | | |
| | | -40°C < T < 125 °C | 58 | | | |
| $A_{vd}$ | Large signal voltage gain ($V_{out}$ = 0.5 V to ($V_{CC}$ - 0.5 V), $R_L$ > 1 MΩ) | T = 25 °C | 100 | 110 | | |
| | | -40°C < T < 125 °C | 90 | | | |
| $V_{OH}$ | High level output voltage $V_{id}$ = +1 V, $V_{OH}$ = $V_{CC}$-$V_{out}$ | $R_L$ = 10 kΩ, T=25 °C | | | 70 | mV |
| | | $R_L$ = 10 kΩ, -40°C < T < 125 °C | | | 100 | |
| $V_{OL}$ | Low level output voltage $V_{id}$ = -1 V, | $R_L$ = 10 kΩ, T = 25 °C | | | 70 | |
| | | $R_L$ = 10 kΩ, -40°C < T < 125 °C | | | 100 | |
| $I_{out}$ | $I_{sink}$ ($V_{out}$ = $V_{CC}$) | T = 25 °C | 11 | 14 | | mA |
| | | -40°C < T < 125 °C | 8 | | | |
| | $I_{source}$ ($V_{out}$ = 0 V) | T = 25 °C | 9 | 12 | | |
| | | -40°C < T < 125 °C | 7 | | | |
| $I_{CC}$ | Supply current (per operator, $V_{out}$ = $V_{CC}$/2, $R_L$ > 1 MΩ) | T = 25 °C | | 45 | 60 | µA |
| | | -40°C < T < 125 °C | | | 60 | |

**Table 5. Electrical characteristics at $V_{CC+}$ = +5 V with $V_{CC-}$ = 0 V, $V_{icm}$ = $V_{CC}$/2, T = 25 ° C, and $R_L$= 10 kΩ connected to $V_{CC}$/2 (unless otherwise specified)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **AC performance** | | | | | | |
| GBP | Gain bandwidth product | $R_L$ = 100 kΩ, $C_L$ = 100 pF | 160 | 200 | | kHz |
| $F_u$ | Unity gain frequency | | | 160 | | |
| $\Phi_m$ | Phase margin | | | 55 | | degrees |
| $G_m$ | Gain margin | | | 9 | | dB |
| SR | Slew rate | $R_L$ = 100 kΩ, $C_L$ = 100 pF, $V_{out}$ = 0.5 V to $V_{CC}$ - 0.5V | | 0.12 | | V/µs |
| $\int e_n$ | Low-frequency peak-to-peak input noise | Bandwidth: f = 0.1 to 10 Hz | | 5 | | $\mu V_{pp}$ |
| $e_n$ | Equivalent input noise voltage | f = 1 kHz | | 60 | | $\frac{nV}{\sqrt{Hz}}$ |
| | | f = 10 kHz | | | | |
| THD+N | Total harmonic distortion + noise | Follower configuration, $f_{in}$ = 1 kHz, $R_L$ = 100 kΩ, $V_{icm}$ = 2.5V, BW = 22 kHz, $V_{out}$ = 1 $V_{pp}$ | | 0.005 | | % |

1. See *Chapter 4.3: Input offset voltage drift over temperature on page 18*
2. Typical value is based on the Vio drift observed after 1000h at 125°C extrapolated to 25°C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration. See *Chapter 4.4: Long term input offset voltage drift on page 19*.
3. Guaranteed by design

**Table 6. Electrical characteristics at $V_{CC+}$ = +10 V with $V_{CC-}$ = 0 V, $V_{icm}$ = $V_{CC}$/2, T = 25 ° C, and $R_L$=10 kΩ connected to $V_{CC}$/2 (unless otherwise specified)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DC performance** | | | | | | |
| $V_{io}$ | Offset voltage | TSX63xA, T = 25 °C | | | 500 | µV |
| | | TSX63xA, -40°C < T < 125 °C | | | 1300 | |
| | | TSX63x, T = 25 °C | | | 1 | mV |
| | | TSX63x, -40°C < T < 125 °C | | | 1.8 | |
| $V_{io}$ | Offset voltage, high common mode ($V_{icm}$=$V_{CC}$, $R_L$ > 1 MΩ) | T = 25 °C | | | 4 | |
| | | -40°C < T < 125 °C | | | 5 | |
| $\Delta V_{io}/\Delta T$ | Input offset voltage drift | -40°C < T < 125 °C(1) | | 1 | 8 | µV/°C |
| $\Delta V_{io}$ | Long term input offset voltage drift | T = 25 °C(2) | | 180 | | $\frac{nV}{\sqrt{month}}$ |
| $I_{io}$ | Input offset current ($V_{out}$ = $V_{CC}$/2) | T = 25 °C | | 1 | 100(3) | pA |
| | | -40°C < T < 125 °C | | | 200(3) | |
| $I_{ib}$ | Input bias current ($V_{out}$ = $V_{CC}$/2) | T = 25 °C | | 1 | 100(3) | |
| | | -40°C < T < 125 °C | | | 200(3) | |
| $R_{IN}$ | Input resistance | | | 1 | | TΩ |
| $C_{IN}$ | Input capacitance | | | 5 | | pF |
| CMR1 | Common mode rejection ratio CMR = 20 log ($\Delta V_{icm}/\Delta V_{io}$) ($V_{icm}$ = -0.1 V to $V_{CC}$-1.65 V, $V_{out}$ = $V_{CC}$/2, $R_L$ > 1 MΩ) | T = 25 °C | 71 | 84 | | dB |
| | | -40°C < T < 125 °C | 68 | | | |
| CMR2 | Common mode rejection ratio CMR = 20 log ($\Delta V_{icm}/\Delta V_{io}$) ($V_{icm}$ = -0.1 V to $V_{CC}$+0.1 V, $V_{out}$ = $V_{CC}$/2, $R_L$ > 1 MΩ) | T = 25 °C | 69 | 82 | | |
| | | -40°C < T < 125 °C | 66 | | | |
| $A_{vd}$ | Large signal voltage gain ($V_{out}$ = 0.5 V to ($V_{CC}$ - 0.5 V), $R_L$ > 1 MΩ) | T = 25 °C | 100 | 110 | | |
| | | -40°C < T < 125 °C | 90 | | | |
| $V_{OH}$ | High level output voltage $V_{id}$ = +1 V, $V_{OH}$ = $V_{CC}$-$V_{out}$ | $R_L$ = 10 kΩ, T = 25 °C | | | 70 | mV |
| | | $R_L$ = 10 kΩ, -40°C < T < 125 °C | | | 100 | |
| $V_{OL}$ | Low level output voltage $V_{id}$ = -1 V, | $R_L$ = 10 kΩ, T = 25 °C | | | 70 | |
| | | $R_L$ = 10 kΩ, -40°C < T < 125 °C | | | 100 | |
| $I_{out}$ | $I_{sink}$ ($V_{out}$ = $V_{CC}$) | T = 25 °C | 35 | 51 | | mA |
| | | -40°C < T < 125 °C | 25 | | | |
| | $I_{source}$ ($V_{out}$ = 0 V) | T = 25 °C | 30 | 42 | | |
| | | -40°C < T < 125 °C | 20 | | | |
| $I_{CC}$ | Supply current (per operator, $V_{out}$ = $V_{CC}$/2, $R_L$ > 1 MΩ) | T = 25 °C | | 45 | 60 | µA |
| | | -40°C < T < 125 °C | | | 60 | |

**Table 6. Electrical characteristics at $V_{CC+}$ = +10 V with $V_{CC-}$ = 0 V, $V_{icm}$ = $V_{CC}$/2, T = 25 ° C, and $R_L$=10 kΩ connected to $V_{CC}$/2 (unless otherwise specified)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **AC performance** | | | | | | |
| GBP | Gain bandwidth product | $R_L$ = 100 kΩ, $C_L$ = 100 pF | 160 | 200 | | kHz |
| $F_u$ | Unity gain frequency | | | 160 | | |
| $\Phi_m$ | Phase margin | | | 55 | | degrees |
| $G_m$ | Gain margin | | | 9 | | dB |
| SR | Slew rate | $R_L$ = 100 kΩ, $C_L$ = 100 pF, $V_{out}$ = 0.5 V to $V_{CC}$ - 0.5V | | 0.12 | | V/µs |
| $\int e_n$ | Low-frequency peak-to-peak input noise | Bandwidth: f = 0.1 to 10 Hz | | 5 | | $\mu V_{pp}$ |
| $e_n$ | Equivalent input noise voltage | f = 1 kHz | | 60 | | $\frac{nV}{\sqrt{Hz}}$ |
| | | f = 10 kHz | | | | |
| THD+N | Total harmonic distortion + noise | Follower configuration, $f_{in}$ = 1 kHz, $R_L$ = 100 kΩ, $V_{icm}$ = 5 V, BW = 22 kHz, $V_{out}$ = 1 $V_{pp}$ | | 0.004 | | % |

1. See *Chapter 4.3: Input offset voltage drift over temperature on page 18*
2. Typical value is based on the Vio drift observed after 1000h at 125°C extrapolated to 25°C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration. See *Chapter 4.4: Long term input offset voltage drift on page 19*.
3. Guaranteed by design

**Table 7. Electrical characteristics at $V_{CC+}$ = +16 V with $V_{CC-}$ = 0 V, $V_{icm}$ = $V_{CC}$/2, T = 25 ° C, and $R_L$=10 kΩ connected to $V_{CC}$/2 (unless otherwise specified)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DC performance** | | | | | | |
| $V_{io}$ | Offset voltage | TSX63xA, T = 25 °C | | | 700 | µV |
| | | TSX63xA, -40°C < T < 125 °C | | | 1500 | |
| | | T = 25 °C | | | 1.6 | mV |
| | | -40°C < T < 125 °C | | | 2.4 | |
| $V_{io}$ | Offset voltage, high common-mode ($V_{icm}$=$V_{CC}$, $R_L$ > 1 MΩ) | T = 25°C | | | 4 | |
| | | -40°C < T < 125 °C | | | 5 | |
| $\Delta V_{io}/\Delta T$ | Input offset voltage drift | -40°C < T < 125 °C(1) | | 1 | 8 | µV/°C |
| $\Delta V_{io}$ | Long term input offset voltage drift | T = 25 °C(2) | | 3.4 | | $\frac{\mu V}{\sqrt{month}}$ |
| $I_{io}$ | Input offset current ($V_{out}$ = $V_{CC}$/2) | T = 25 °C | | 1 | 100(3) | pA |
| | | -40°C < T < 125 °C | | | 200(3) | |
| $I_{ib}$ | Input bias current ($V_{out}$ = $V_{CC}$/2) | T = 25 °C | | 1 | 100(3) | |
| | | -40°C < T < 125 °C | | | 200(3) | |
| $R_{IN}$ | Input resistance | | | 1 | | TΩ |
| $C_{IN}$ | Input capacitance | | | 5 | | pF |
| CMR1 | Common mode rejection ratio CMR = 20 log ($\Delta V_{icm}/\Delta V_{io}$) ($V_{icm}$ = -0.1 V to $V_{CC}$-1.65 V, $V_{out}$ = $V_{CC}$/2, $R_L$ > 1 MΩ) | T = 25 °C | 71 | 85 | | dB |
| | | -40°C < T < 125 °C | 68 | | | |
| CMR2 | Common mode rejection ratio CMR = 20 log ($\Delta V_{icm}/\Delta V_{io}$) ($V_{icm}$ = -0.1 V to $V_{CC}$+0.1 V, $V_{out}$ = $V_{CC}$/2, $R_L$ > 1 MΩ) | T = 25 °C | 69 | 83 | | |
| | | -40°C < T < 125 °C | 66 | | | |
| SVR | Common mode rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$) ($V_{CC}$ =3.3 V to 16 V, $V_{out}$ = $V_{icm}$ $V_{CC}$/2) | T = 25 °C | 73 | 87 | | |
| | | -40°C < T < 125 °C | 70 | | | |
| $A_{vd}$ | Large signal voltage gain ($V_{out}$ = 0.5 V to ($V_{CC}$ - 0.5 V), $R_L$ > 1 MΩ) | T = 25 °C | 100 | 110 | | |
| | | -40°C < T < 125 °C | 90 | | | |
| $V_{OH}$ | High level output voltage $V_{id}$ = +1 V, $V_{OH}$ = $V_{CC}$-$V_{out}$ | $R_L$ = 10 kΩ, T = 25 °C | | | 70 | mV |
| | | $R_L$ = 10 kΩ, -40°C < T < 125 °C | | | 100 | |
| $V_{OL}$ | Low level output voltage $V_{id}$ = -1 V, | $R_L$ = 10 kΩ, T = 25 °C | | | 70 | |
| | | $R_L$ = 10 kΩ, -40°C < T < 125 °C | | | 100 | |

**Table 7. Electrical characteristics at $V_{CC+}$ = +16 V with $V_{CC-}$ = 0 V, $V_{icm}$ = $V_{CC}$/2, T = 25 ° C, and $R_L$=10 kΩ connected to $V_{CC}$/2 (unless otherwise specified)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{out}$ | $I_{sink}$ | $V_{out}$ = $V_{CC}$, T = 25 °C | 40 | 92 | | mA |
| | | $V_{out}$ = $V_{CC}$, -40°C < T < 125 °C | 35 | | | |
| | $I_{source}$ | $V_{out}$ = 0 V, T = 25 °C | 30 | 90 | | |
| | | $V_{out}$ = 0 V, -40°C < T < 125 °C | 25 | | | |
| $I_{CC}$ | Supply current (per operator, $V_{out}$ = $V_{CC}$/2, $R_L$ > 1 MΩ) | T = 25 °C | | 45 | 60 | µA |
| | | -40°C < T < 125 °C | | | 60 | |
| **AC performance** | | | | | | |
| GBP | Gain bandwidth product | $R_L$ = 100 kΩ, $C_L$ = 100 pF | 160 | 200 | | kHz |
| $F_u$ | Unity gain frequency | | | 160 | | |
| $\Phi_m$ | Phase margin | | | 55 | | degrees |
| $G_m$ | Gain margin | | | 9 | | dB |
| SR | Slew rate | $R_L$ = 100 kΩ, $C_L$ = 100 pF, $V_{out}$ = 0.5 V to $V_{CC}$ - 0.5V | | 0.12 | | V/µs |
| $\int e_n$ | Low-frequency peak-to-peak input noise | Bandwidth: f = 0.1 to 10 Hz | | 5 | | $\mu V_{pp}$ |
| $e_n$ | Equivalent input noise voltage | f = 1 kHz | | 60 | | $\frac{nV}{\sqrt{Hz}}$ |
| | | f = 10 kHz | | | | |
| THD+N | Total harmonic distortion + noise | Follower configuration, $f_{in}$ = 1 kHz, $R_L$ = 100 kΩ, $V_{icm}$ = 8 V, BW = 22 kHz, $V_{out}$ = 1 $V_{pp}$ | | 0.004 | | % |

1. See *Chapter 4.3: Input offset voltage drift over temperature on page 18*
2. Typical value is based on the Vio drift observed after 1000h at 125°C extrapolated to 25°C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration. See *Chapter 4.4: Long term input offset voltage drift on page 19*.
3. Guaranteed by design

**Figure 2. Supply current vs. supply voltage at $V_{icm} = V_{CC}/2$**

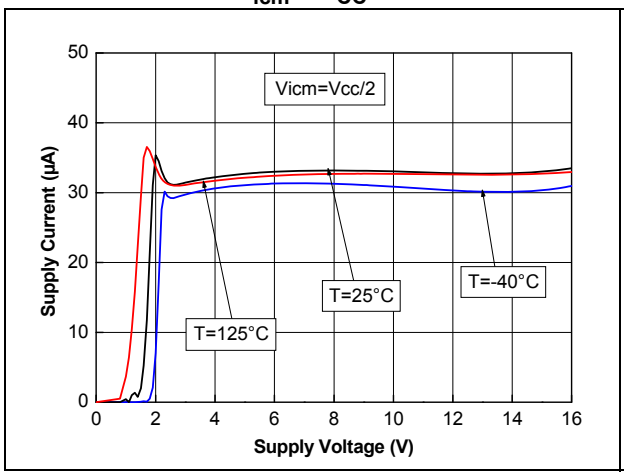



**Figure 3. Input offset voltage distribution at $V_{CC}$ = 16 V**

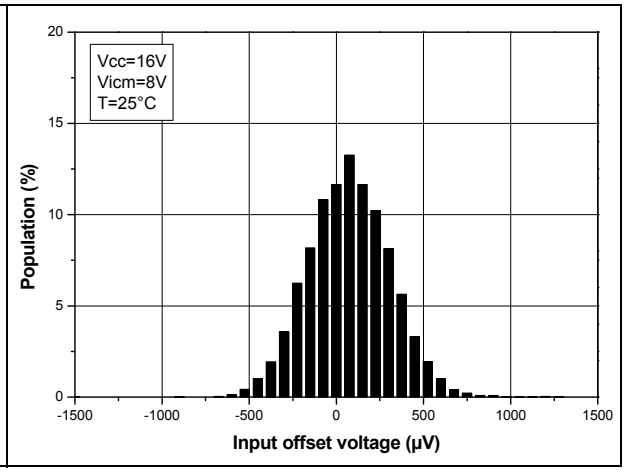



**Figure 4. Input offset voltage distribution at $V_{CC}$ = 10 V**

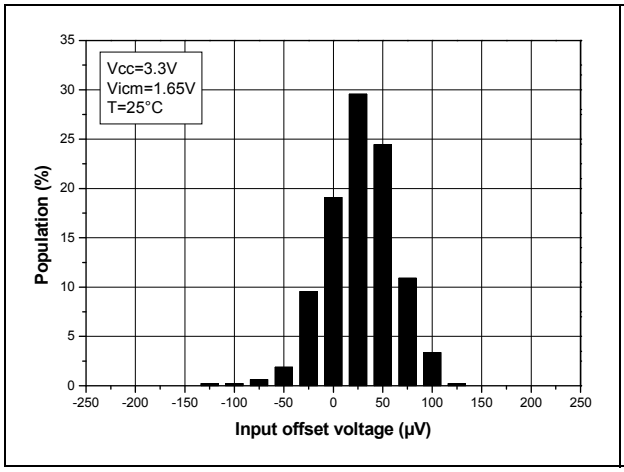



**Figure 5. Input offset voltage vs. temperature at $V_{CC}$=16 V**

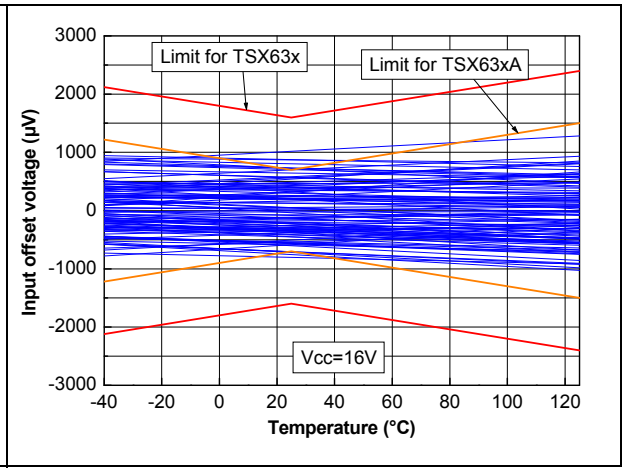



**Figure 6. Input offset voltage temperature coefficient distribution**

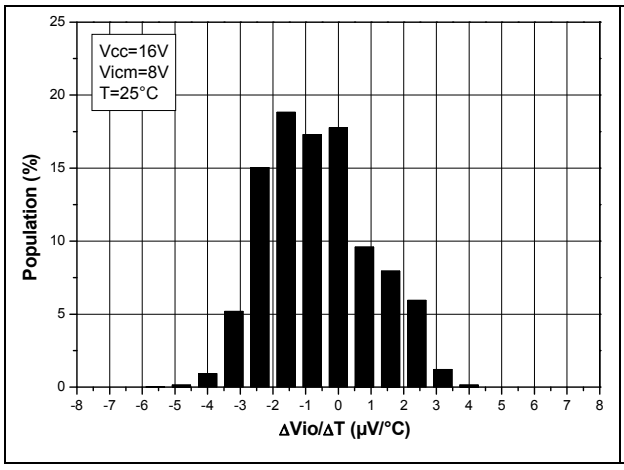



**Figure 7. Input offset voltage vs. input common mode voltage**

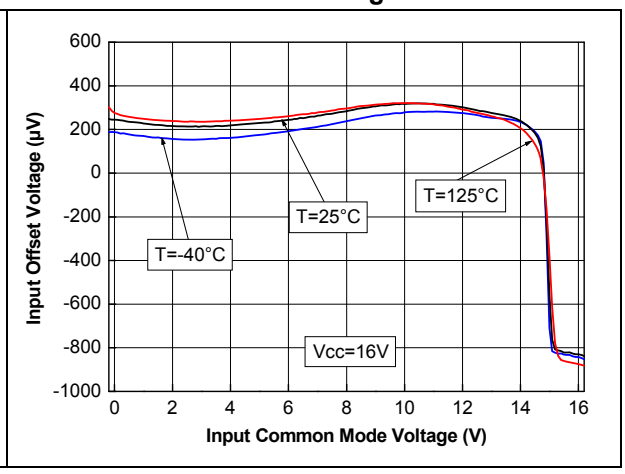


**Figure 8. Output current vs. output voltage at $V_{CC}$ = 3.3 V**

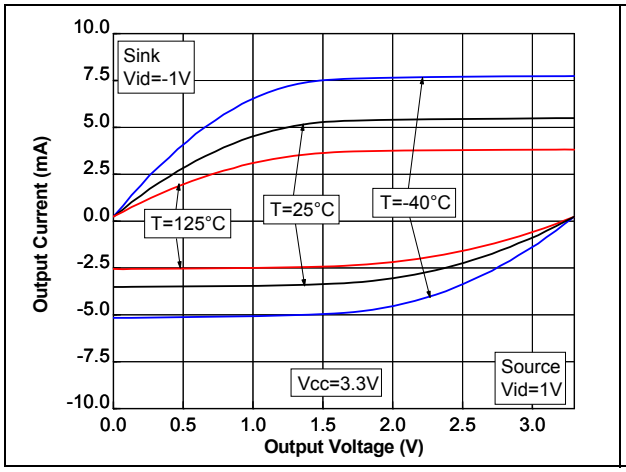



**Figure 9. Output current vs. output voltage at $V_{CC}$ = 16 V**

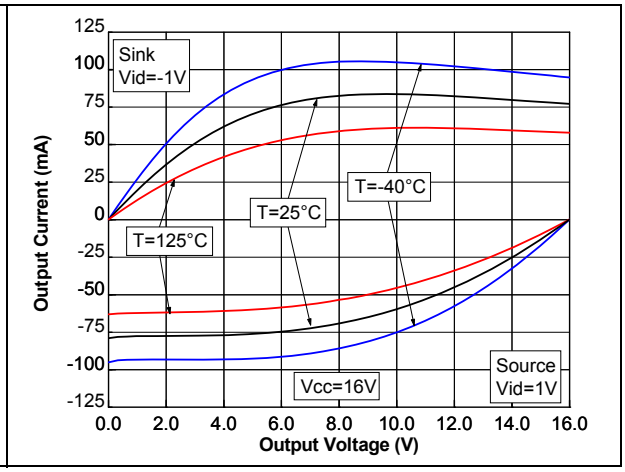



**Figure 10. Output low-rail linearity performance ($R_L$≥ 2 kΩ)**

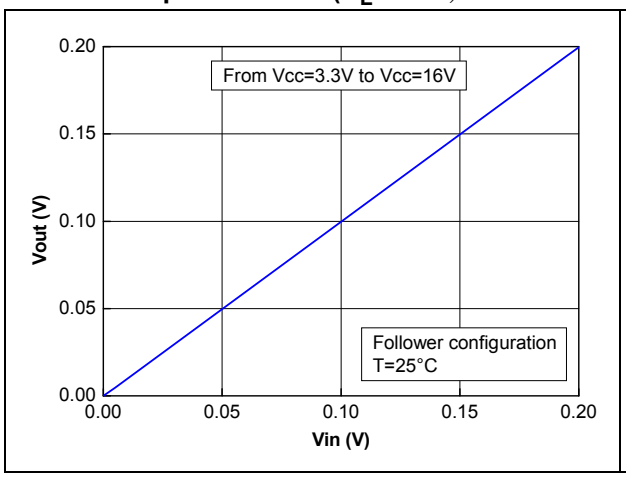



**Figure 11. Output high-rail linearity performance ($R_L$≥ 2kΩ)**

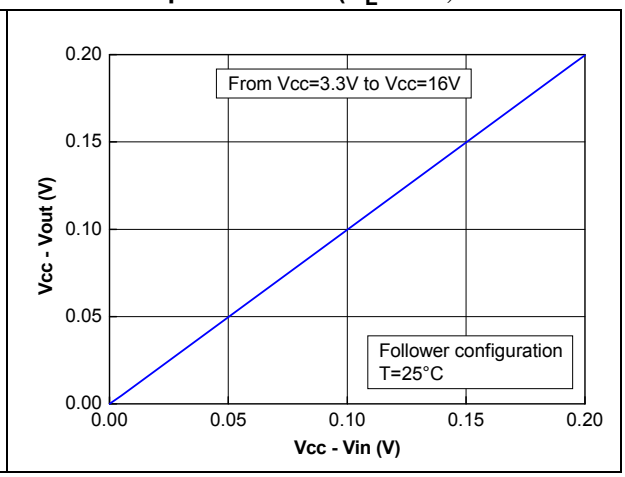



**Figure 12. Bode diagram at $V_{CC}$ = 3.3 V, $R_L$= 10 kΩ**

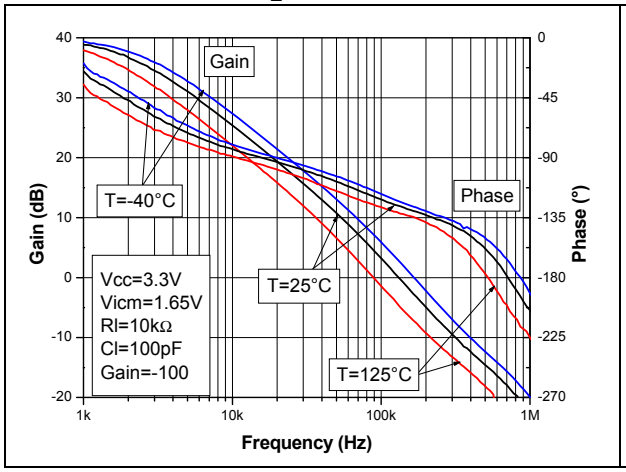



**Figure 13. Bode diagram at $V_{CC}$ = 3.3 V, $R_L$= 100 kΩ**

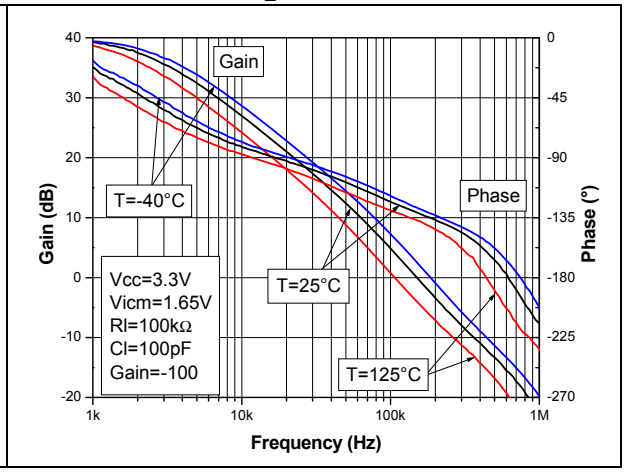


**Figure 14. Bode diagram at $V_{CC}$ = 16 V, $R_L$ = 10 kΩ**

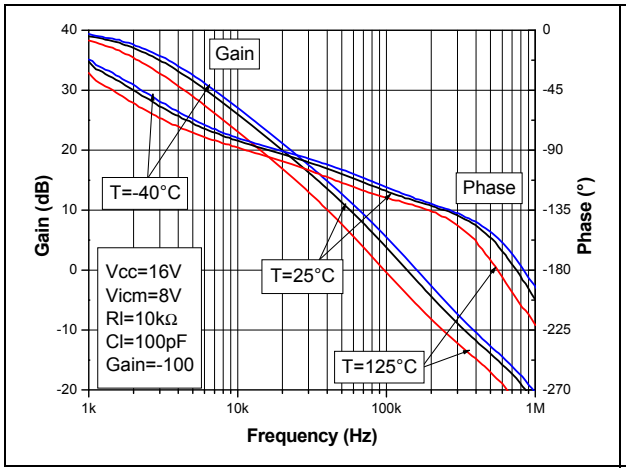



**Figure 15. Bode diagram at $V_{CC}$ = 16 V, $R_L$ = 100 kΩ**

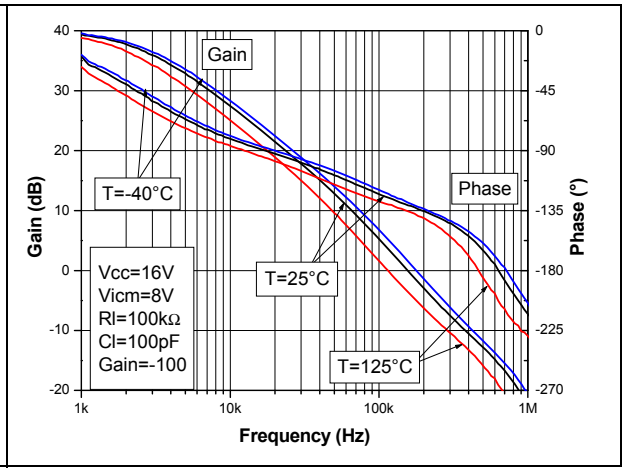



**Figure 16. Closed-loop gain vs. capacitive load**

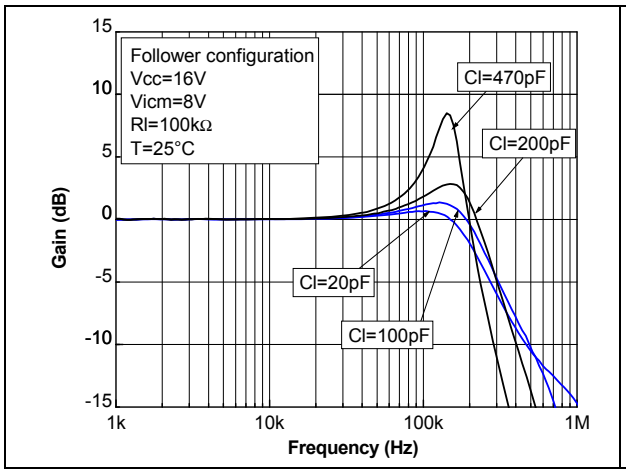



**Figure 17. In-series resistor ($R_{iso}$) vs. capacitive load**

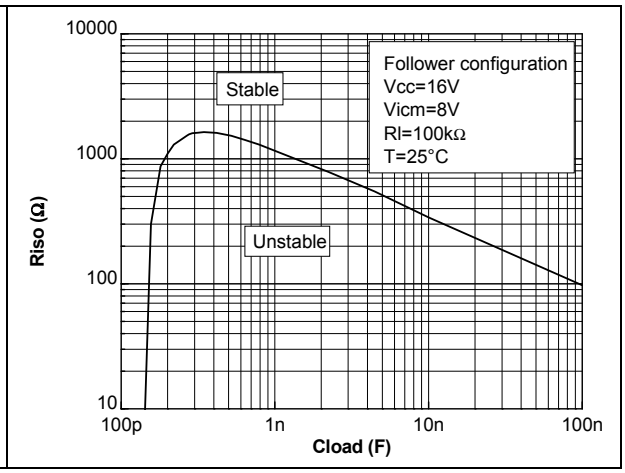



**Figure 18. Negative slew rate**

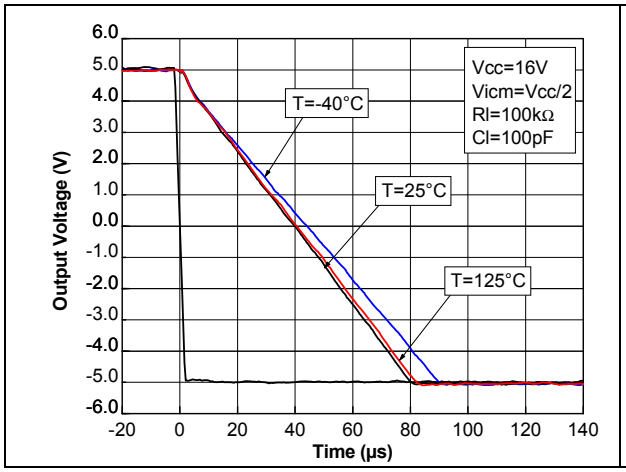



**Figure 19. Positive slew rate**

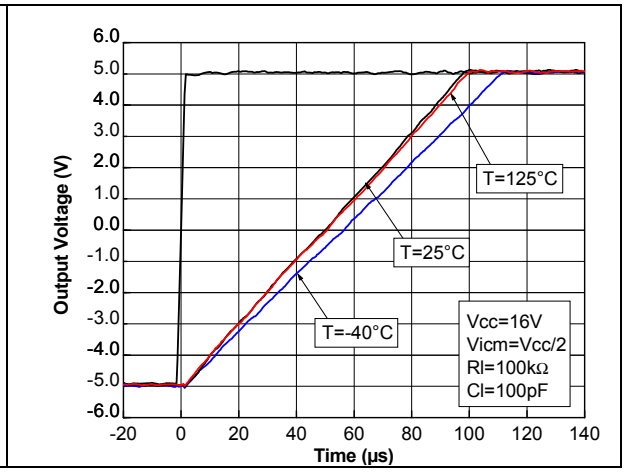


Figure 20. Slew rate vs. supply voltage

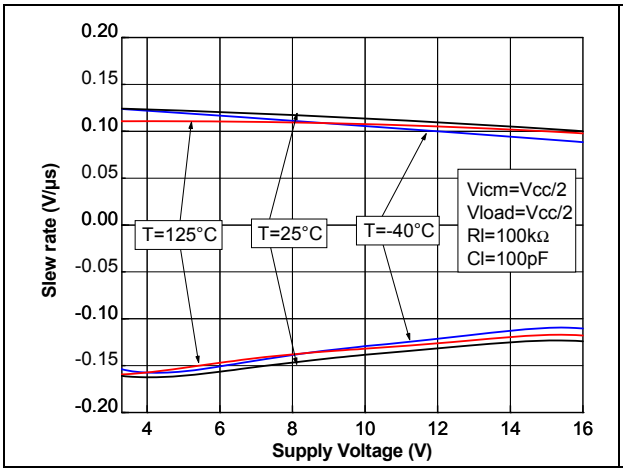



Figure 21. Small step response

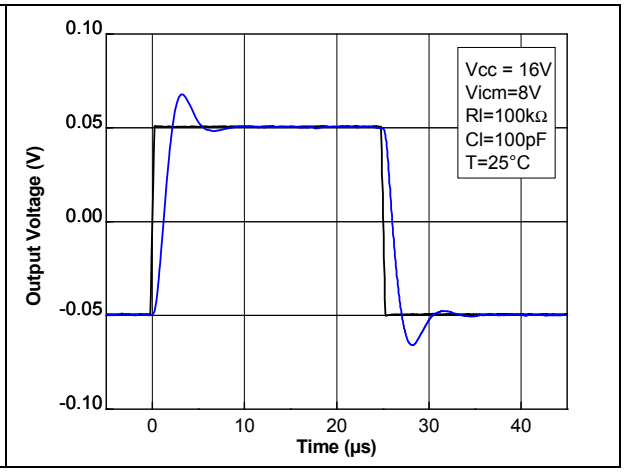



Figure 22. Noise vs. frequency at $V_{CC}$ = 16 V

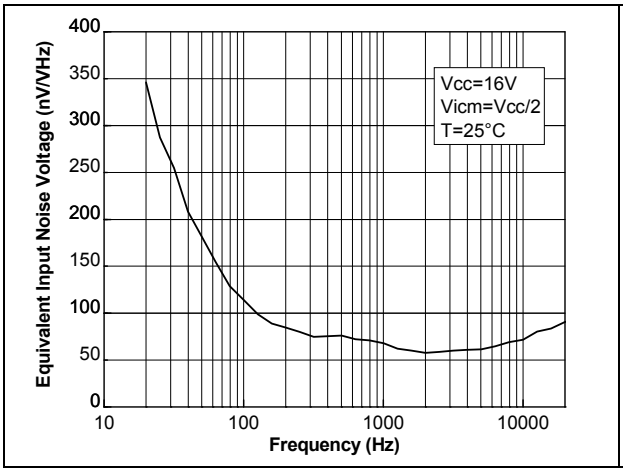



Figure 23. 0.1 Hz to 10 Hz noise at $V_{CC}$ = 16 V

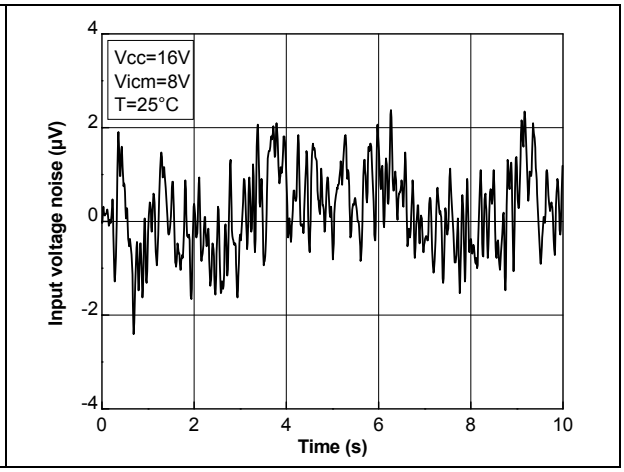



Figure 24. THD+N vs. frequency at $V_{CC}$ = 16 V

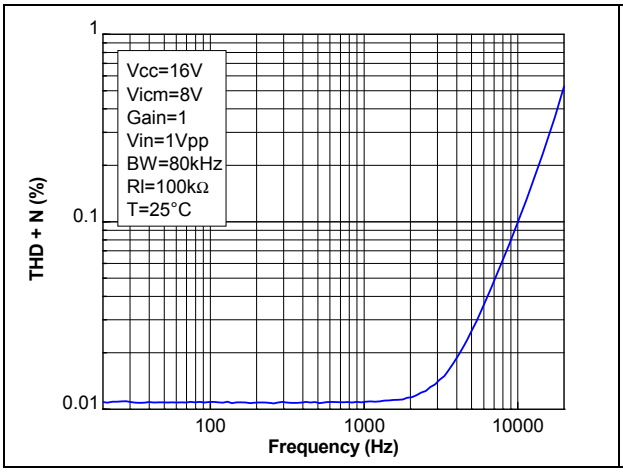



Figure 25. THD+N vs. output voltage at $V_{CC}$ = 16 V

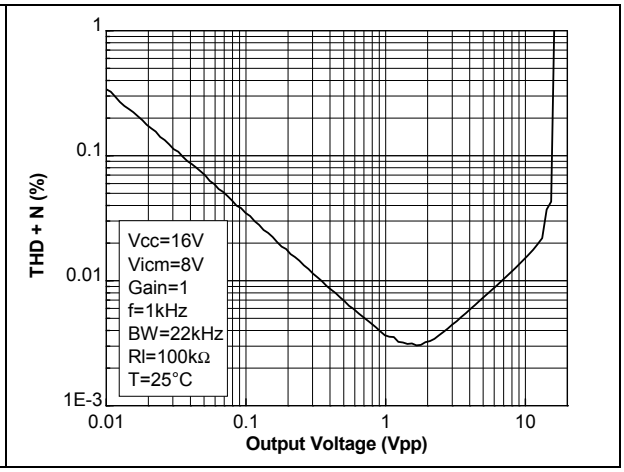


**Figure 26. Output impedance vs. frequency in closed loop configuration**

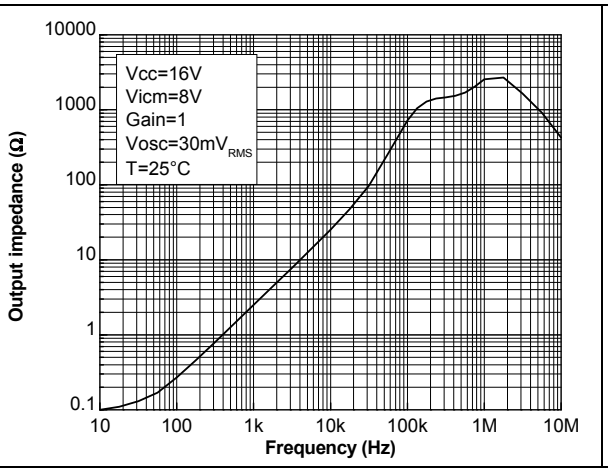
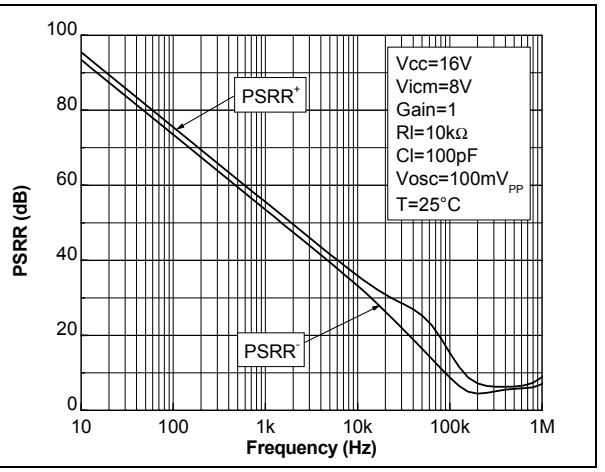



**Figure 27. PSRR vs. frequency**



# 4 Application information

## 4.1 Operating voltages

The amplifiers of the TSX63x and TSX63xA series can operate from 3.3 to 16 V. Their parameters are fully specified at 3.3, 5, 10 and 16 V power supplies. However, the parameters are very stable in the full $V_{CC}$ range. Additionally, the main specifications are guaranteed in extended temperature ranges from -40 ° C to +125 ° C.

## 4.2 Rail-to-rail input

The TSX63x and TSX63xA are built with two complementary PMOS and NMOS input differential pairs. The devices have a rail-to-rail input, and the input common mode range is extended from $V_{CC-}$- 0.1 V to $V_{CC+}$ + 0.1 V.

However, the performance of these devices is clearly optimized for the PMOS differential pairs (which means from $V_{CC-}$ - 0.1V to $V_{CC+}$ - 1.65V).

Beyond $V_{CC+}$ - 1.65 V, the op-amp is still functional but with a degraded performance as can be observed in the electrical characteristics section of this datasheet (mainly $V_{io}$).

These performances are suitable for a number of applications requiring rail-to-rail input and output.

The devices are guaranteed without phase reversal.

## 4.3 Input offset voltage drift over temperature

The maximum input voltage drift over the temperature variation is defined as the offset variation related to offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed using *Equation 1*.

**Equation 1**

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25°C)}{T - 25°C}\right|$$

with T = -40 °C and 125 °C.

The datasheet maximum value is guaranteed by a measurement on a representative sample size ensuring a $C_{pk}$ (process capability index) greater than 2.

## 4.4 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using *Equation 2*.

**Equation 2**

$$A_{FV} = e^{\beta \cdot (V_S - V_U)}$$

Where:

$A_{FV}$ is the voltage acceleration factor

$\beta$ is the voltage acceleration constant in 1/V, constant technology parameter ($\beta = 1$)

$V_S$ is the stress voltage used for the accelerated test

$V_U$ is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in *Equation 3*.

**Equation 3**

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S}\right)}$$

Where:

$A_{FT}$ is the temperature acceleration factor

$E_a$ is the activation energy of the technology based on the failure rate

k is the Boltzmann constant ($8.6173 \times 10^{-5}$ eV.K$^{-1}$)

$T_U$ is the temperature of the die when $V_U$ is used (K)

$T_S$ is the temperature of the die under temperature stress (K)

The final acceleration factor, $A_F$, is the multiplication of the voltage acceleration factor and the temperature acceleration factor (*Equation 4*).

**Equation 4**

$$A_F = A_{FT} \times A_{FV}$$

$A_F$ is calculated using the temperature and voltage defined in the mission profile of the product. The $A_F$ value can then be used in *Equation 5* to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

**Equation 5**

$$Months = A_F \times 1000\,h \times 12\,months / (24\,h \times 365.25\,days)$$

To evaluate the op-amp reliability, a follower stress condition is used where $V_{CC}$ is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules).

The $V_{io}$ drift (in µV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see *Equation 6*).

**Equation 6**

$$V_{CC} = \max V_{op} \text{ with } V_{icm} = V_{CC} / 2$$

The long term drift parameter ($\Delta V_{io}$), estimating the reliability performance of the product, is obtained using the ratio of the $V_{io}$ (input offset voltage value) drift over the square root of the calculated number of months (*Equation 7*).

**Equation 7**

$$\Delta V_{io} = \frac{V_{io}drift}{\sqrt{(months)}}$$

where $V_{io}$ drift is the measured drift value in the specified test conditions after 1000 h stress duration.

## 4.5 High values of input differential voltage

In closed loop configuration, which represents the typical use of an op-amp, the input differential voltage is low (close to $V_{io}$). However, some specific conditions can lead to higher input differential values, such as:

- operation in an output saturation state
- operation at speeds higher than the device bandwidth, with output voltage dynamics limited by slew rate.
- use of the amplifier in a comparator configuration, hence in open loop

Use of the TSX631 in comparator configuration, especially combined with high temperature and long duration can create a permanent drift of $V_{io}$.

All channels of the dual and quad versions of the TSX632 and TSX634 are virtually unaffected when used in comparator configuration.

## 4.6 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

## 4.7 Macromodel

Accurate macromodels of the TSX63x and TSX63xA are available on STMicroelectronics' web site at www.st.com. These models are a trade-off between accuracy and complexity (that is, time simulation) of the TSX63x and TSX63xA operational amplifiers. They emulate the nominal performances of a typical device within the specified operating conditions mentioned in the datasheet. They also help to validate a design approach and to select the right operational amplifier, *but they do not replace on-board measurements*.

# 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

## 5.1 SOT23-5 package information

**Figure 28. SOT23-5 package mechanical drawing**

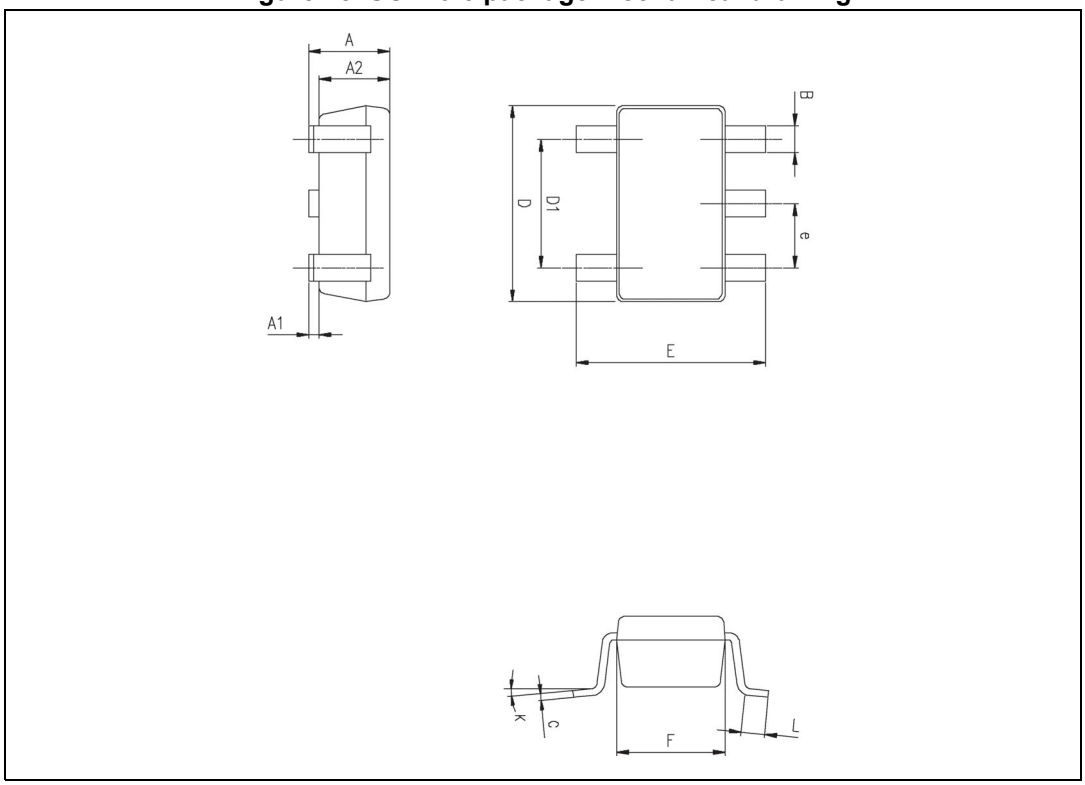



**Table 8. SOT23-5 package mechanical data**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.90 | 1.20 | 1.45 | 0.035 | 0.047 | 0.057 |
| A1 | | | 0.15 | | | 0.006 |
| A2 | 0.90 | 1.05 | 1.30 | 0.035 | 0.041 | 0.051 |
| B | 0.35 | 0.40 | 0.50 | 0.013 | 0.015 | 0.019 |
| C | 0.09 | 0.15 | 0.20 | 0.003 | 0.006 | 0.008 |
| D | 2.80 | 2.90 | 3.00 | 0.110 | 0.114 | 0.118 |
| D1 | | 1.90 | | | 0.075 | |
| e | | 0.95 | | | 0.037 | |
| E | 2.60 | 2.80 | 3.00 | 0.102 | 0.110 | 0.118 |
| F | 1.50 | 1.60 | 1.75 | 0.059 | 0.063 | 0.069 |
| L | 0.10 | 0.35 | 0.60 | 0.004 | 0.013 | 0.023 |
| K | 0 ° | | 10 ° | 0 ° | | 10 ° |

## 5.2 DFN8 2x2 package information

**Figure 29. DFN8 2x2 package mechanical drawing**

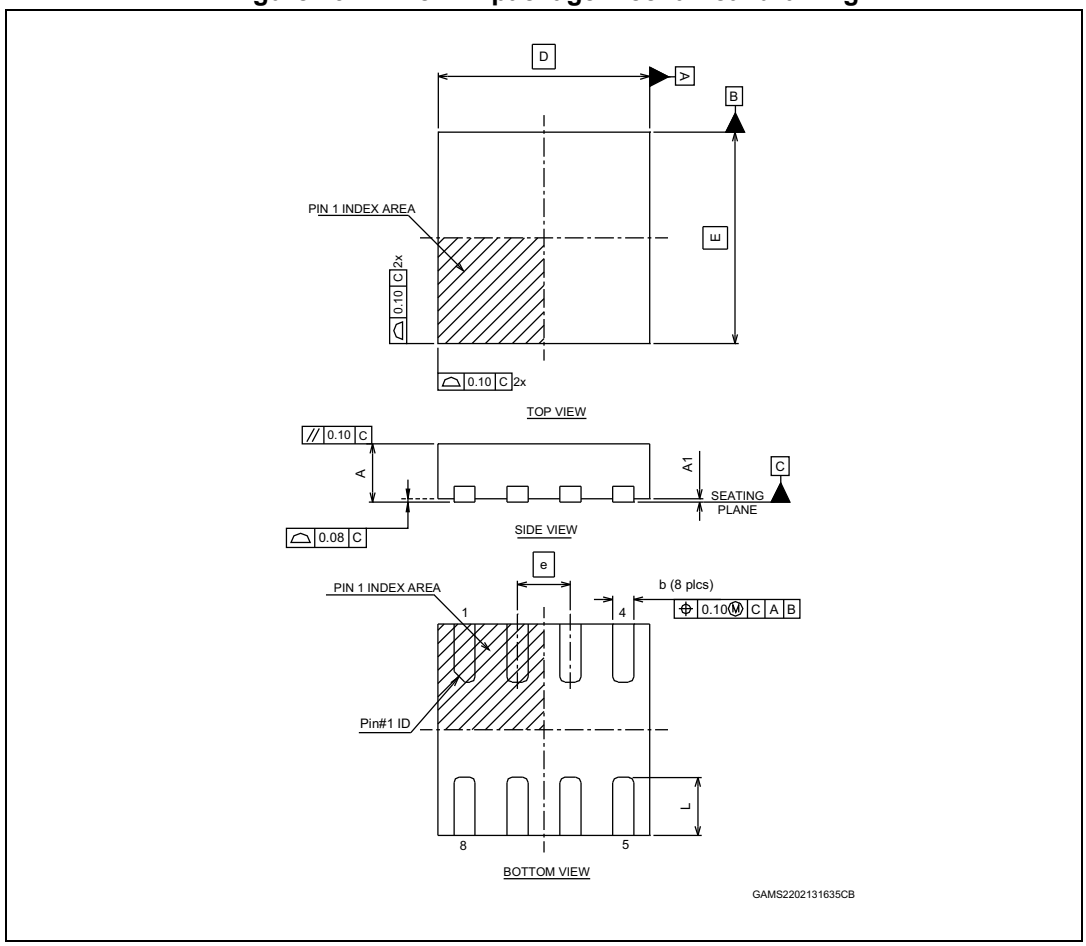



**Table 9. DFN8 2x2 package mechanical data**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.70 | 0.75 | 0.80 | 0.028 | 0.030 | 0.031 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D | | 2.00 | | | 0.079 | |
| E | | 2.00 | | | 0.079 | |
| e | | 0.50 | | | 0.020 | |
| L | 0.045 | 0.55 | 0.65 | 0.018 | 0.022 | 0.026 |
| N | 8 | | | 8 | | |

## 5.3 MiniSO-8 package information

Figure 30. MiniSO-8 package mechanical drawing

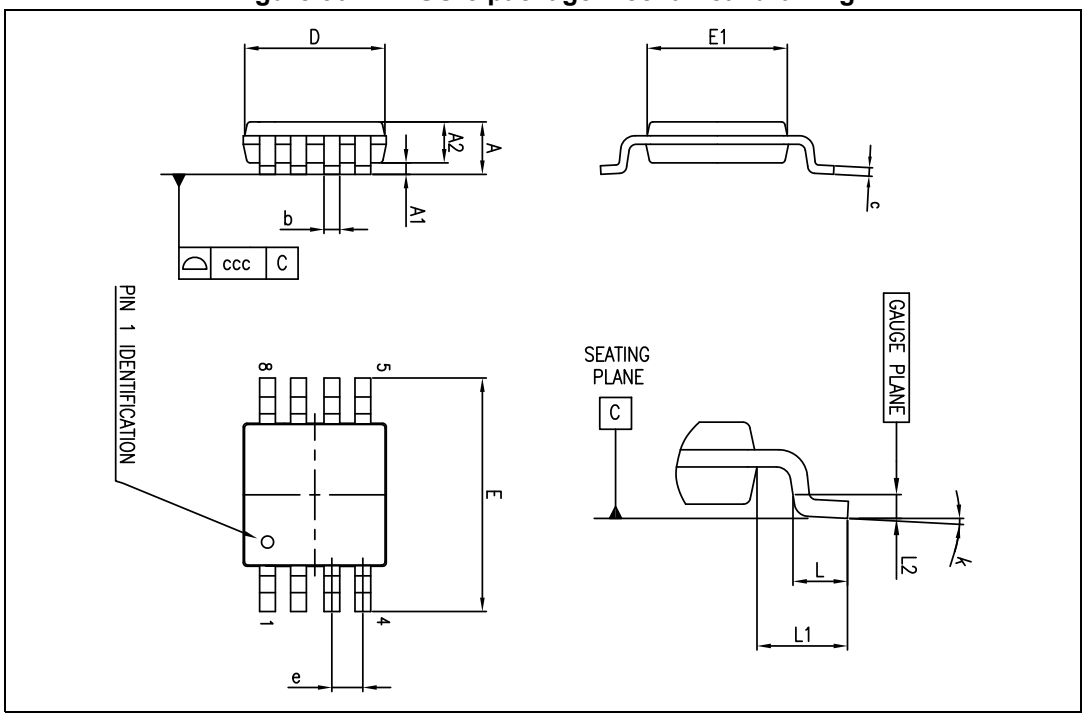



Table 10. MiniSO-8 package mechanical data

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 1.1 | | | 0.043 |
| A1 | 0 | | 0.15 | 0 | | 0.006 |
| A2 | 0.75 | 0.85 | 0.95 | 0.030 | 0.033 | 0.037 |
| b | 0.22 | | 0.40 | 0.009 | | 0.016 |
| c | 0.08 | | 0.23 | 0.003 | | 0.009 |
| D | 2.80 | 3.00 | 3.20 | 0.11 | 0.118 | 0.126 |
| E | 4.65 | 4.90 | 5.15 | 0.183 | 0.193 | 0.203 |
| E1 | 2.80 | 3.00 | 3.10 | 0.11 | 0.118 | 0.122 |
| e | | 0.65 | | | 0.026 | |
| L | 0.40 | 0.60 | 0.80 | 0.016 | 0.024 | 0.031 |
| L1 | | 0.95 | | | 0.037 | |
| L2 | | 0.25 | | | 0.010 | |
| k | 0 ° | | 8 ° | 0 ° | | 8 ° |
| ccc | | | 0.10 | | | 0.004 |

## 5.4 QFN16 3x3 package information

**Figure 31. QFN16 3x3 package mechanical drawing**

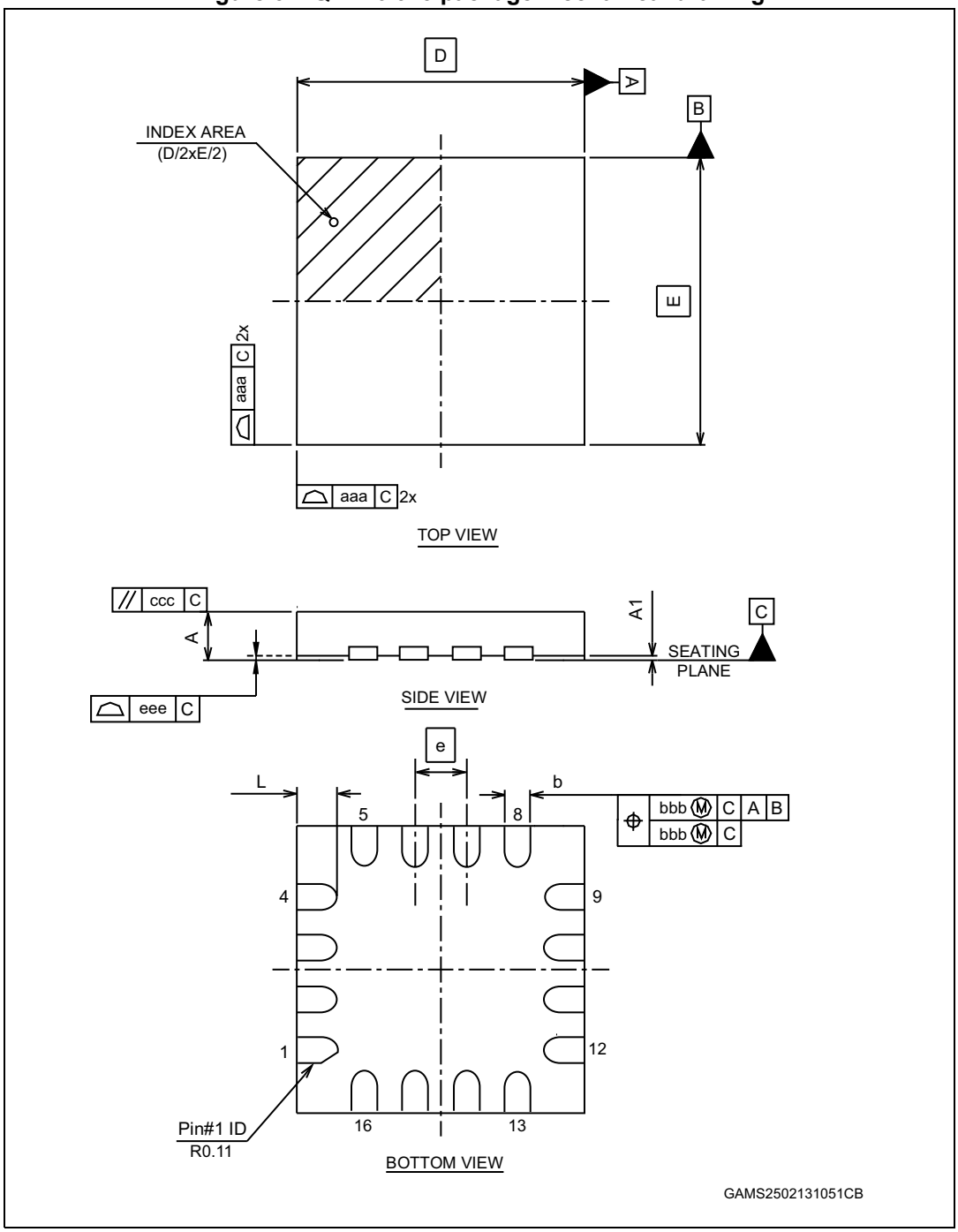


Table 11. QFN16 3x3 package mechanical data

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.50 | | 0.65 | 0.020 | | 0.026 |
| A1 | 0 | | 0.05 | 0 | | 0.002 |
| b | 0.18 | 0.25 | 0.30 | 0.007 | 0.010 | 0.012 |
| D | | 3.00 | | | 0.118 | |
| E | | 3.00 | | | 0.118 | |
| e | | 0.50 | | | 0.020 | |
| L | 0.30 | | 0.50 | 0.012 | | 0.020 |
| aaa | | | 0.15 | | | 0.006 |
| bbb | | | 0.10 | | | 0.004 |
| ccc | | | 0.10 | | | 0.004 |
| ddd | | | 0.05 | | | 0.002 |
| eee | | | 0.08 | | | 0.003 |

## 5.5 TSSOP14 package information

**Figure 32. TSSOP14 package mechanical drawing**

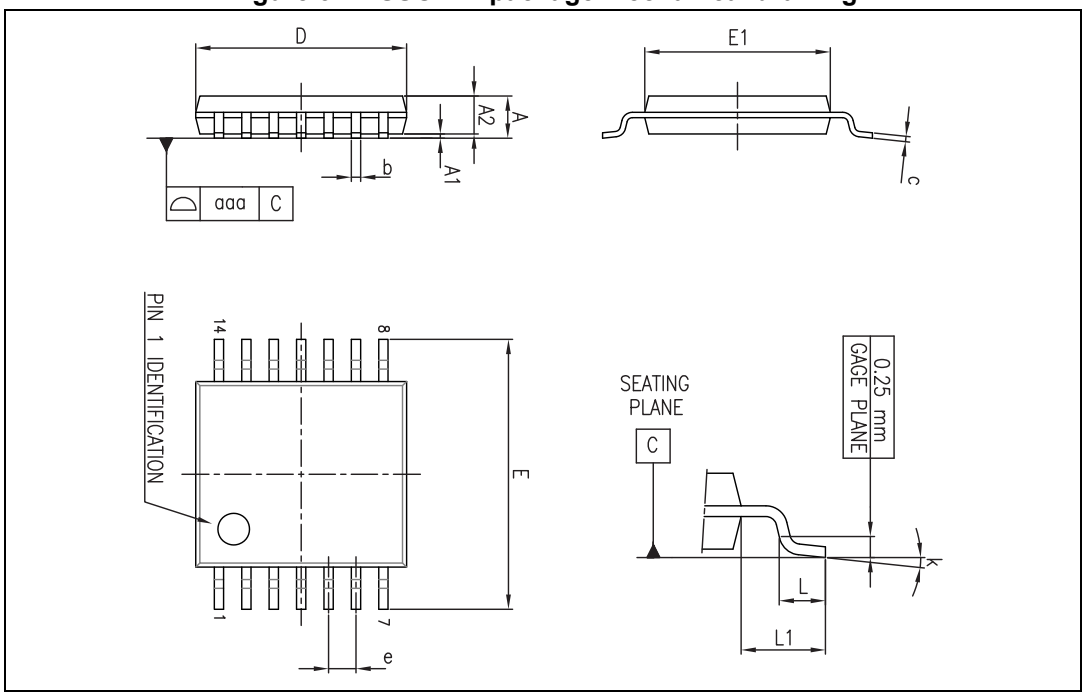



**Table 12. TSSOP14 package mechanical data**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 1.20 | | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.80 | 1.00 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | | 0.30 | 0.007 | | 0.012 |
| c | 0.09 | | 0.20 | 0.004 | | 0.0089 |
| D | 4.90 | 5.00 | 5.10 | 0.193 | 0.197 | 0.201 |
| E | 6.20 | 6.40 | 6.60 | 0.244 | 0.252 | 0.260 |
| E1 | 4.30 | 4.40 | 4.50 | 0.169 | 0.173 | 0.176 |
| e | | 0.65 | | | 0.0256 | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | | 1.00 | | | 0.039 | |
| k | 0 ° | | 8 ° | 0 ° | | 8 ° |
| aaa | | | 0.10 | | | 0.004 |

# 6 Ordering information

**Table 13. Order codes**

| Order code | Temperature range | No. of channels | Package | Packing | Marking |
|---|---|---|---|---|---|
| TSX631ILT | -40 to 125 °C | 1 | SOT23-5 | Tape and reel | K27 |
| TSX632IQ2T | | 2 | DFN8 2x2 | | K27 |
| TSX632IST | | 2 | MiniSO8 | | K27 |
| TSX634IQ4T | | 4 | QFN16 3x3 | | K27 |
| TSX634IPT | | 4 | TSSOP14 | | TSX634I |
| TSX631IYLT | -40 to 125 °C Automotive grade(1) | 1 | SOT23-5 | | K188 |
| TSX632IYST | | 2 | MiniSO8 | | K188 |
| TSX634IYPT | | 4 | TSSOP14 | | TSX634IY |
| TSX631AILT | -40 to 125 °C | 1 | SOT23-5 | | K189 |
| TSX632AIST | | 2 | MiniSO8 | | K189 |
| TSX634AIPT | | 4 | TSSOP14 | | TSX634AI |
| TSX631AIYLT | -40 to 125°C Automotive grade(1) | 1 | SOT23-5 | | K190 |
| TSX632AIYST | | 2 | MiniSO8 | | K190 |
| TSX634AIYPT | | 4 | TSSOP14 | | TSX634AIY |

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent are on-going.

# 7 Revision history

Table 14. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 26-Mar-2013 | 1 | Initial release |