TX53

Computer On Module

- Processor — Freescale i.MX537, 800 MHz
Freescale i.MX535, 1.2GHz
- RAM — 512MB/1GB DDR3 SDRAM
- ROM — 128MB NAND Flash
- RTC — DS1339 Real Time Clock
- Power supply — Single 3.1V to 5.5V
- Size — 31mm SO-DIMM
- Temp.-Range — -20°C..70°C (i.MX535 commercial)
-40°C..85°C (i.MX537 industrial)

Key Features

- 10/100Mbps Ethernet
- Two High Speed USB 2.0 ports
- LCD controller up to 1600 x 1200, 24bpp
- OpenGL ES 2.0 and OpenVG 1.1 hardware accelerators
- Multi-format HD 1080p video decoder and 720p video encoder hardware engine
- Two Camera Interfaces
- NEON SIMD media accelerator
- Unified 256KB L2 cache
- Vector Floating Point Unit
- Several interfaces:
3x UART, 2x SDIO, 2x SSI/AC97/I2S,
I2C, CSPI, Keypad, Ext. Memory I/F
- 3.3V I/O

i.MX537 only:

- IEEE1588 support
- Two CAN interfaces

LVDS Option only:

- Dual LVDS display port
- SATA

OS Support

- Windows Embedded Compact 7
- Linux

1.2 GHz Cortex A8

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TX53

Board highlights:

- Highly integrated
- Industrial temperature range (i.MX537 only)
- Standard TX-DIMM pinout
- as small as possible - only 31mm
- 3.3V I/O

The TX53 is a member of a module series, specially designed for Freescales i.MX multimedia processors. TX modules are complete computers, implemented on a board smaller than a credit card, and ready to be designed into your embedded system. TX modules includes a Freescale® i.MX processor, SDRAM and Flash memory. The integrated LCD-controller enables direct connection of an LCD screen. The TX53 is specifically targeted at embedded applications where size, high cpu-performance and cost are critical factors.

Computer on module

- Freescale® i.MX535, 1.2 GHz / i.MX537, 800 MHz
- 512 MByte/1GByte SDRAM (32bit) (up to 2GB on request)
- DDR3-800
- 128 MByte NAND Flash memory
- DIMM200-module (67,6mm x 31 mm x 3,6mm)
- Industrial i.MX537 / Commercial i.MX535
- Operating temperature range -20..70°C / -40°C..85°C

Processor

The i.MX53 family of processors represents Freescale's next generation of advanced multimedia and power-efficient implementation of the ARM Cortex™-A8 core. The i.MX53, prepares your end device for tomorrow's smart mobile technology today. The i.MX53 enables hours of full HD 1080p video playback and an amazing Adobe® Flash® 10.1 experience. With core processing speeds up to 1 GHz as well as a high level of integration, the i.MX53 enables a great user experience at a lower retail price point.

High Performance CPU : ARM Cortex-A8 up to 1GHz

- OpenGL® ES 2.0 and OpenVG™ 1.1 hardware accelerators
- Multi-format HD1080p video decoder and HD720p video encoder hardware engine
- Dual display capable with multiple display options including TFT LCD, LVDS, analog TV-formats (composite, component, RGB) and standard VGA
- Hardware accelerated image post-processing, display quality enhancement, and video and graphics combining
- Two simultaneous camera inputs with hardware pre-processing
- Dual USB 2.0 Controllers (HS OTG, HS Host) with integrated PHY
- Two additional High-Speed USB 2.0 controllers
- 10/100 Ethernet controller with IEEE1588 time-stamping
- Wide array of serial interfaces including SDIO, SPI, I2C, UART
- Security solution supporting High Assurance Boot, Cipher and random number generator accelerators, and Tamper Detection

Standard TX-DIMM pinout:

- 4-wire UARTs (x3)
- LCD
- I2C / PWM
- Serial Audio Interfaces (x2)
- 4-wire SD-Card/SDIO

High-Speed communication interfaces incl. onboard Ethernet PHY / on-chip USB PHY allows direct use of connectors/magnetics on the baseboard without the need for additional logic:

- 10/100 Mbps Ethernet
- 480 Mbps USB OTG (Host or Device)
- 480 Mbps USB Host

Additional interfaces like CAN, 2 UARTs and external memory interface are available on TX53 specific pins. Some interfaces are multiplexed with other functions.

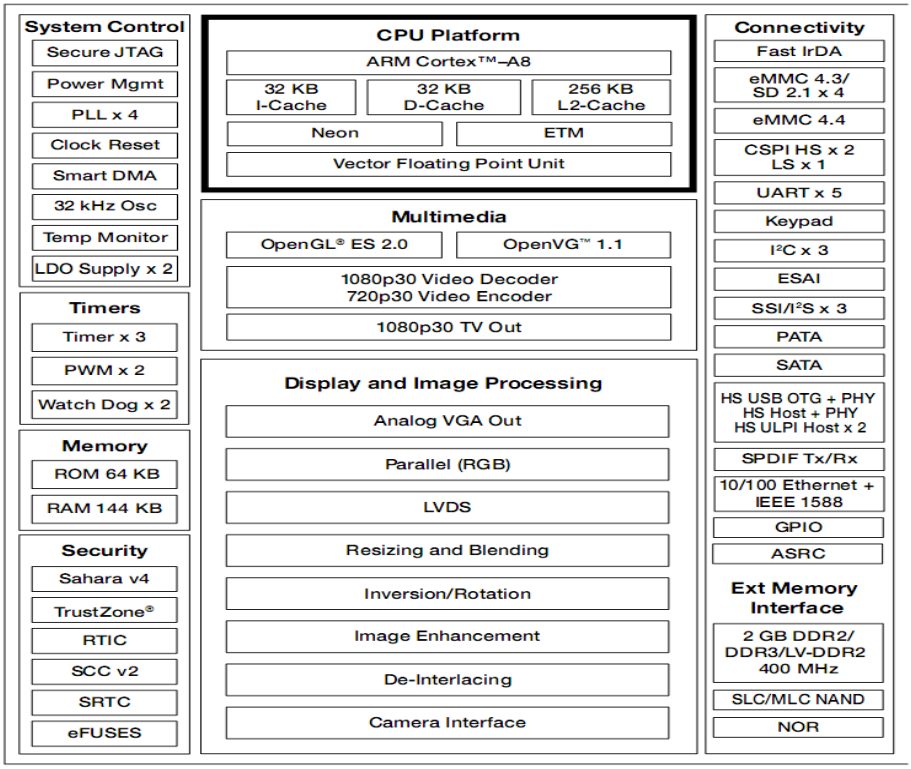
Power Supply

The TX53 accepts an input voltage from various sources:

- 1-cell Li-Ion/Polymer (3.1V to 4.2V)
- 5.0V USB supply or AC wall adapter
- 3.3V

Read more in our TX-Guide:

www.karo-electronics.com/TX-Guide



Ordering Information

Order Number	CPU	SDRAM	Flash	Temp.
TX53/1200/1024S/128F/LVDS	1.2GHz i.MX535	1024MB	128MB	-20°C..70°C
TX53/800/512S/128F/I	800MHz i.MX537	512MB	128MB	-40°C..85°C
TX53/800/512S/128F/LVDS/I	800MHz i.MX537	512MB	128MB	-40°C..85°C

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PINOUT

PIN	Type	Function	i.MX53 Pad Name	Alternate functions	GPIO	Description (refer to i.MX53 manuals for details)
POWER SUPPLY & RESET						
1-4	power	VIN				Module power supply input (3.1V-5.5V)
5-7, 9-12	power	VOUT				3.3V power supply output (up to 1A)
8	3V3	BOOTMODE				Boot mode select H: Boot from NAND / L: Boot from UART/USB
13	power	VBACKUP				DS1339 RTC backup power supply. Supply voltage must be held between 1.3V and 3.7V for proper RTC operation. This pin can be connected to a primary cell such as a lithium button cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used with the trickle charge feature.
14	VIN	PMIC_PWR_BTN			47K-PU to VIN	External Power-On control. (Not available on TX53 version v2) To power down, drive the PWR_ON pin LOW. Refer to LTC3589 datasheet, page 29 for details. LTC3589 IRQ is connected to i.MX53 pad EIM_A25
15	3V3	#RESET_OUT	GPIO_17	ESAI1_TX0 SDMA_EXT_EVENT[0] GPC_PMIC_RDY RTC_CE_RTC_FSV_TRIG SPDIF_OUT1 SNOOP2 SJC_JTAG_ACT	GPIO7[12]	#RESET_OUT may be used to reset peripherals on the carrier board. This signal can be controller by a GPIO function during runtime.
16	VIN	#POR	POR_B		10K-PU to VIN	Power On Reset—Active low input signal. Leave unconnected, if not used.
17	3V3	#RESET_IN	RESET_IN_B	RESET_B	10K-PU to 3V3	Master Reset—External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module, SDRAMC module, and the clock control module) are reset.
18	GND	GND				
Ethernet						
19	analog	ETN_TXN				Transmit Data Negative: 100Base-TX or 10Base-T differential transmit output to magnetics.
20	3V3	#ETN_LED2				Active low - output is driven active when the operating speed is 100Mbps. This LED will go inactive when the operating speed is 10Mbps or during line isolation.
21	analog	ETN_TXP				Transmit Data Positive: 100Base-TX or 10Base-T differential transmit output to magnetics.
22	power	ETN_3V3				+3.3V analog power supply output to magnetics
23	analog	ETN_RXN				Receive Data Negative: 100Base-TX or 10Base-T differential receive input from magnetics.
24	3V3	#ETN_LED1				Active low - output is driven active whenever the device detects a valid link, and blinks indicating activity.
25	analog	ETN_RXP				Receive Data Positive: 100Base-TX or 10Base-T differential receive input from magnetics.
26	GND	GND				
USB-HOST						
27	3V3	USBH_VBUSEN	EIM_D31	WEIM_D[31] UART3_RTS CSI0_D[2] DI0_PIN12 DISP1_DAT[20] USBOH3_USBH1_PWR USBOH3_USBH2_PWR	GPIO3[31]	Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
28	3V3	#USBH_OC	EIM_D30	WEIM_D[30] UART3_CTS CSI0_D[3] DI0_PIN11 DISP1_DAT[21] USBOH3_USBH1_OC USBOH3_USBH2_OC	GPIO3[30] 10K-PU	Active low over-current indicator input connected to a GPIO.
29	analog	USBH_DM	USB_H1_DN			D- pin of the USB cable
30	analog	USBH_VBUS	USB_H1_VBUS			VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.
31	analog	USBH_DP	USB_H1_DP			D+ pin of the USB cable
32	GND	GND				

PIN	Type	Function	i.MX53 Pad Name	Alternate functions	GPIO	Description (refer to i.MX53 manuals for details)
USB-OTG / 2nd CAN						
33	3V3	USBOTG_ID	USB_OTG_ID			ID pin of the USB cable. For an A-Device ID is grounded. For a B-Device ID is floated.
34	3V3	USBOTG_VBUSEN CAN_TX	GPIO_7	ESAI1_TX4_RX1 EPIT1_EPITO CAN1_TXCAN UART2_TXD FIRI_RXD SPDIF_PLOCK CCM_PLL2_BYP	**GPIO1[7]**	Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
35	analog	USBOTG_DM	USB_OTG_DN			D- pin of the USB cable
36	3V3	#USBOTG_OC CAN_RX	GPIO_8	ESAI1_TX5_RX0 EPIT2_EPITO CAN1_RXCAN UART2_RXD FIRI_TXD SPDIF_SRCLK CCM_PLL3_BYP	**GPIO1[8]** 10K-PU	Active low over-current indicator input connected to a GPIO.
37	analog	USBOTG_DP	USB_OTG_DP			D+ pin of the USB cable
38	analog	USBOTG_VBUS	USB_OTG_VBUS			VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.
39	GND	GND				
I2C						
40	3V3	I2C_DATA	GPIO_6	ESAI1_SCKT **I2C3_SDA** CCM_CCM_OUT_0 CSU_INT_DEB OBSRV_INT_OUT1 ESDHC2_LCTL MLBSIG	GPIO1[6]	I2C Data
41	3V3	I2C_CLK	GPIO_3	ESAI1_HCKR **I2C3_SCL** DPLLIP1_TOG_EN CCM_CLKO2 OBSRV_INT_OUT0 USBOH3_USBH1_OC MLBCLK	GPIO1[3]	I2C Clock
PWM						
42	3V3	PWM	GPIO_1	ESAI1_SCKR KPP_ROW[5] CCM_SSI_EXT2_CLK **PWM2_PWMO** WDOG2_WDOG_B ESDHC1_CD TESTER_ACK	GPIO1[1]	PWM Output
1-WIRE						
43	3V3	OWDAT	GPIO_18	ESAI1_TX1 SDMA_EXT_EVENT[1] **OWIRE_LINE** RTC_CE_RTC_ALARM2_TRIG CCM_ASRC_EXT_CLK ESDHC1_LCTL SYSTEM_RST	GPIO7[13]	1-Wire bus. Requires an external pull-up resistor. The recommended resistor is specified by the generic 1-Wire device used in a given system.
CSPI – Configurable Serial Peripheral Interface						
44	3V3	CSPI_SS	EIM_EB2	WEIM_EB[2] CCM_DI1_EXT_CLK SER_DISP1_CS **ECSPI1_SS0** I2C2_SCL	GPIO2[30]	Slave Select (Selectable polarity) signal
45	3V3	CSPI_SS	EIM_D19	WEIM_D[19] DI0_PIN8 DISPB1_SER_RS **ECSPI1_SS1** EPIT1_EPITO UART1_CTS USBOH3_USBH2_OC	GPIO3[19]	Slave Select (Selectable polarity) signal
46	3V3	CSPI_MOSI	EIM_D18	WEIM_D[18] DI0_PIN7 DISPB1_SER_DIO **ECSPI1_MOSI** I2C3_SDA DI1_D0_CS	GPIO3[18]	Master Out/Slave In signal

PIN	Type	Function	i.MX53 Pad Name	Alternate functions	GPIO	Description (refer to i.MX53 manuals for details)
47	3V3	CSPI_MISO	EIM_D17	WEIM_D[17] DI0_PIN6 DISPB1_SER_DIN **ECSPI1_MISO** I2C3_SCL	GPIO3[17]	Master In/Slave Out signal
48	3V3	CSPI_SCLK	EIM_D16	WEIM_D[16] DI0_PIN5 DISPB1_SER_CLK **ECSPI1_SCLK** I2C2_SDA	GPIO3[16]	Serial Clock signal
49	3V3	CSPI_RDY	GPIO_19	KPP_COL[5] CCM_CLKO SPDIF_OUT1 RTC_CE_RTC_EXT_TRIG2 **ECSPI1_RDY** FEC_TDATA[3] INT_BOOT	GPIO4[5]	Serial Data Ready signal
50	GND	GND				
SD – Secure Digital Interface 1						
51	3V3	SD1_CD	EIM_D24	WEIM_D[24] UART3_TXD ECSPI1_SS2 CSPI_SS2 AUD5_RXFS ECSPI2_SS2 UART1_DTR	**GPIO3[24]**	SD Card Detect – connected to a GPIO
52	3V3	SD1_D[0]	SD1_DATA0	**ESDHC1_DAT0** GPT_CAPIN1 CSPI_MISO CCM_PLL3_BYP	GPIO1[16]	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added.
53	3V3	SD1_D[1]	SD1_DATA1	**ESDHC1_DAT1** GPT_CAPIN2 CSPI_SS0 CCM_PLL4_BYP	GPIO1[17]	
54	3V3	SD1_D[2]	SD1_DATA2	**ESDHC1_DAT2** GPT_CMPOUT2 PWM2_PWMO WDOG1_WDOG_B CSPI_SS1 CCM_PLL2_BYP	GPIO1[19]	
55	3V3	SD1_D[3]	SD1_DATA3	**ESDHC1_DAT3** GPT_CMPOUT3 PWM1_PWMO WDOG2_WDOG_B CSPI_SS2 SATA_PHY_DTB[1]	GPIO1[21]	
56	3V3	SD1_CMD	SD1_CMD	**ESDHC1_CMD** GPT_CMPOUT1 CSPI_MOSI CCM_PLL1_BYP	GPIO1[18]	SD Command bidirectional signal
57	3V3	SD1_CLK	SD1_CLK	**ESDHC1_CLK** OSC32K_32K_OUT GPT_CLKIN CSPI_SCLK SATA_PHY_DTB[0]	GPIO1[20]	SD Output Clock.
58	GND	GND				
1st UART						
59	3V3	TXD	PATA_DIOW	PATA_DIOW **UART1_TXD** USBPHY2_DATAOUT[2]	GPIO6[17]	Application UART 1 Transmit Data output signal
60	3V3	RXD	PATA_DMACK	PATA_DMACK **UART1_RXD** USBPHY2_DATAOUT[3]	GPIO6[18]	Application UART 1 Receive Data input signal
61	3V3	RTS	PATA_IORDY	PATA_IORDY ESDHC3_CLK **UART1_RTS** CAN2_RXCAN USBPHY1_DATAOUT[1]	GPIO7[5]	Application UART 1 Request to Send **input** signal
62	3V3	CTS	PATA_RESET_B	PATA_RESET_B ESDHC3_CMD **UART1_CTS** CAN2_TXCAN USBPHY1_DATAOUT[0]	GPIO7[4]	Application UART 1 Clear to Send **output** signal

PIN	Type	Function	i.MX53 Pad Name	Alternate functions	GPIO	Description (refer to i.MX53 manuals for details)
2nd UART						
63	3V3	TXD	PATA_DMARQ	PATA_DMARQ **UART2_TXD** CCM_CCM_OUT_0 USBPHY2_DATAOUT[4]	GPIO7[0]	Application UART 2 Transmit Data output signal
64	3V3	RXD	PATA_BUFFER_EN	PATA_BUFFER_EN **UART2_RXD** CCM_CCM_OUT_1 USBPHY2_DATAOUT[5]	GPIO7[1]	Application UART 2 Receive Data input signal
65	3V3	RTS	PATA_DIOR	PATA_DIOR **UART2_RTS** CAN1_RXCAN USBPHY2_DATAOUT[7]	GPIO7[3]	Application UART 2 Request to Send **input** signal
66	3V3	CTS	PATA_INTRQ	PATA_INTRQ **UART2_CTS** CAN1_TXCAN CCM_CCM_OUT_2 USBPHY2_DATAOUT[6]	GPIO7[2]	Application UART 2 Clear to Send **output** signal
3rd UART						
67	3V3	TXD	PATA_CS_0	PATA_CS_0 **UART3_TXD** USBPHY1_DATAOUT[5]	GPIO7[9]	Application UART 3 Transmit Data output signal
68	3V3	RXD	PATA_CS_1	PATA_CS_1 **UART3_RXD** USBPHY1_DATAOUT[6]	GPIO7[10]	Application UART 3 Receive Data input signal
69	3V3	RTS	PATA_DA_2	PATA_DA_2 ESDHC4_CLK **UART3_RTS** USBPHY1_DATAOUT[4]	GPIO7[8]	Application UART 3 Request to Send **input** signal
70	3V3	CTS	PATA_DA_1	PATA_DA_1 ESDHC4_CMD **UART3_CTS** USBPHY1_DATAOUT[3]	GPIO7[7]	Application UART 3 Clear to Send **output** signal
71	GND	GND				
KEYPAD / 1st CAN						
72	3V3	KP_COL[0]	GPIO_9	ESAI1_FSR **KPP_COL[6]** CCM_REF_EN_B PWM1_PWMO WDOG1_WDOG_B ESDHC1_WP SCC_FAIL_STATE	GPIO1[9]	
73	3V3	KP_COL[1]	GPIO_4	ESAI1_HCKT **KPP_COL[7]** CCM_CCM_OUT_2 CSU_ALARM_AUT[1] OBSRV_INT_OUT3 ESDHC2_CD SCC_SEC_STATE	GPIO1[4]	
74	3V3	KP_COL[2]	KEY_COL2	**KPP_COL[2]** CAN1_TXCAN 32K_256K_CTI_TRIGOUT6 FEC_MDIO ECSPI1_SS1 FEC_RDATA[2] USBPHY1_RXACTIVE	GPIO4[10]	
75	3V3	KP_COL[3]	KEY_COL3	**KPP_COL[3]** USBOH3_H2_DP SPDIF_IN1 I2C2_SCL ECSPI1_SS3 FEC_CRS USBPHY1_SIECLOCK	GPIO4[12]	
76	3V3	TXCAN	KEY_COL4	KPP_COL[4] **CAN2_TXCAN** SISG[4] UART5_RTS USBOH3_USBOTG_OC USBPHY1_LINESTATE[1]	GPIO4[14]	
77	3V3	KP_ROW[0]	GPIO_2	ESAI1_FST **KPP_ROW[6]** CCM_CCM_OUT_1 CSU_ALARM_AUT[0] OBSRV_INT_OUT2 ESDHC2_WP MLBDAT	GPIO1[2]	

PIN	Type	Function	i.MX53 Pad Name	Alternate functions	GPIO	Description (refer to i.MX53 manuals for details)
78	3V3	KP_ROW[1]	GPIO_5	ESAI1_TX2_RX3 **KPP_ROW[7]** CCM_CLKO CSU_ALARM_AUT[2] OBSRV_INT_OUT4 I2C3_SCL CCM_PLL1_BYP	GPIO1[5]	
79	3V3	KP_ROW[2]	KEY_ROW2	**KPP_ROW[2]** CAN1_RXCAN 32K_256K_CTI_TRIGOUT7 FEC_MDC ECSPI1_SS2 FEC_TDATA[2] USBPHY1_RXERROR	GPIO4[11]	
80	3V3	KP_ROW[3]	KEY_ROW3	**KPP_ROW[3]** USBOH3_H2_DM CCM_ASRC_EXT_CLK I2C2_SDA OSC32K_32K_OUT CCM_PLL4_BYP USBPHY1_LINESTATE[0]	GPIO4[13]	
81	3V3	RXCAN	KEY_ROW4	KPP_ROW[4] **CAN2_RXCAN** SISG[5] UART5_CTS USBOH3_USBOTG_PWR USBPHY1_VBUSVALID	GPIO4[15]	
82	GND	GND				
SSI 1 - Serial Audio Port 1						
83	3V3	SSI1_INT	EIM_D26	WEIM_D[26] UART2_TXD FIRI_RXD CSI0_D[1] DI1_PIN11 SISG[2] DISP1_DAT[22]	**GPIO3[26]**	GPIO
84	3V3	SSI1_RXD	KEY_ROW1	KPP_ROW[1] **AUD5_RXD** 32K_256K_CTI_TRIGOUT_ACK7 UART5_RXD ECSPI1_SS0 FEC_COL USBPHY1_RXVALID	GPIO4[9]	Serial Audio Interface serial data line 1
85	3V3	SSI1_TXD	KEY_ROW0	KPP_ROW[0] **AUD5_TXD** 32K_256K_CTI_TRIGIN_ACK7 UART4_RXD ECSPI1_MOSI FEC_TX_ER	GPIO4[7]	Serial Audio Interface serial data line 0
86	3V3	SSI1_CLK	KEY_COL0	KPP_COL[0] **AUD5_TXC** 32K_256K_CTI_TRIGIN7 UART4_TXD ECSPI1_SCLK FEC_RDATA[3] ANY_PU_RST	GPIO4[6]	Serial Audio Interface serial bit clock
87	3V3	SSI1_FS	KEY_COL1	KPP_COL[1] **AUD5_TXFS** 32K_256K_CTI_TRIGOUT_ACK6 UART5_TXD ECSPI1_MISO FEC_RX_CLK USBPHY1_TXREADY	GPIO4[8]	Serial Audio Interface left/right clock
88	GND	GND				
SSI 2 - Serial Audio Port 2						
89	3V3	SSI2_INT	EIM_D27	WEIM_D[27] UART2_RXD FIRI_TXD CSI0_D[0] DI1_PIN13 SISG[3] DISP1_DAT[23]	**GPIO3[27]**	GPIO
90	3V3	SSI2_RXD	CSI0_DAT7	CSI0_D[7] KPP_ROW[6] ECSPI1_SS0 USBOH3_USBH3_DIR **AUD3_RXD**	GPIO5[25]	Serial Audio Interface serial data line 1

PIN	Type	Function	i.MX53 Pad Name	Alternate functions	GPIO	Description (refer to i.MX53 manuals for details)
91	3V3	SSI2_TXD	CSI0_DAT5	CSI0_D[5] KPP_ROW[5] ECSPI1_MOSI USBOH3_USBH3_NXT **AUD3_TXD**	GPIO5[23]	Serial Audio Interface serial data line 0
92	3V3	SSI2_CLK	CSI0_DAT4	CSI0_D[4] KPP_COL[5] ECSPI1_SCLK USBOH3_USBH3_STP **AUD3_TXC**	GPIO5[22]	Serial Audio Interface serial bit clock
93	3V3	SSI2_FS	CSI0_DAT6	CSI0_D[6] KPP_COL[6] ECSPI1_MISO USBOH3_USBH3_CLK **AUD3_TXFS**	GPIO5[24]	Serial Audio Interface left/right clock
94	GND	GND				
Secure Digital Interface 2						
95	3V3	SD2_CD	EIM_D25	WEIM_D[25] UART3_RXD ECSPI1_SS3 CSPI_SS3 AUD5_RXC ECSPI2_SS3 UART1_DSR	GPIO3[25]	SD Card Detect – connected to a GPIO
96	3V3	SD2_D[0]	SD2_DATA0	**ESDHC2_DAT0** KPP_ROW[7] AUD4_RXD CSPI_MISO RTIC_RTIC_DONE_INT	GPIO1[15]	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added.
97	3V3	SD2_D[1]	SD2_DATA1	**ESDHC2_DAT1** KPP_COL[7] AUD4_TXFS CSPI_SS0 RTIC_RTIC_SEC_VIO	GPIO1[14]	
98	3V3	SD2_D[2]	SD2_DATA2	**ESDHC2_DAT2** KPP_ROW[6] AUD4_TXD CSPI_SS1 SJC_FAIL	GPIO1[13]	
99	3V3	SD2_D[3]	SD2_DATA3	**ESDHC2_DAT3** KPP_COL[6] AUD4_TXC CSPI_SS2 SJC_DONE	GPIO1[12]	
100	3V3	SD2_CMD	SD2_CMD	**ESDHC2_CMD** KPP_ROW[5] AUD4_RXC CSPI_MOSI SCC_RANDOM	GPIO1[11]	SD Command bidirectional signal
101	3V3	SD2_CLK	SD2_CLK	**ESDHC2_CLK** KPP_COL[5] AUD4_RXFS CSPI_SCLK SCC_RANDOM_V	GPIO1[10]	SD Output Clock.
102	GND	GND				
CMOS Sensor Interface						
103	3V3	CSI0_DAT12	CSI0_DAT12	**CSI0_D[12]** UART4_TXD USBOH3_USBH3_DATA[0]	GPIO5[30]	
104	3V3	CSI0_DAT13	CSI0_DAT13	**CSI0_D[13]** UART4_RXD USBOH3_USBH3_DATA[1]	GPIO5[31]	
105	3V3	CSI0_DAT14	CSI0_DAT14	**CSI0_D[14]** UART5_TXD USBOH3_USBH3_DATA[2]	GPIO6[0]	
106	3V3	CSI0_DAT15	CSI0_DAT15	**CSI0_D[15]** UART5_RXD USBOH3_USBH3_DATA[3]	GPIO6[1]	
107	3V3	CSI0_DAT16	CSI0_DAT16	**CSI0_D[16]** UART4_RTS USBOH3_USBH3_DATA[4]	GPIO6[2]	

PIN	Type	Function	i.MX53 Pad Name	Alternate functions	GPIO	Description (refer to i.MX53 manuals for details)
108	3V3	CSI0_DAT17	CSI0_DAT17	**CSI0_D[17]** UART4_CTS USBOH3_USBH3_DATA[5]	GPIO6[3]	
109	3V3	CSI0_DAT18	CSI0_DAT18	**CSI0_D[18]** UART5_RTS USBOH3_USBH3_DATA[6]	GPIO6[4]	
110	3V3	CSI0_DAT19	CSI0_DAT19	**CSI0_D[19]** UART5_CTS USBOH3_USBH3_DATA[7] USBPHY2_BISTOK	GPIO6[5]	
111	GND	GND				
112	3V3	CSI0_HSYNC	CSI0_MCLK	**CSI0_HSYNC** CCM_CSI0_MCLK	GPIO5[19]	
113	3V3	CSI0_VSYNC	CSI0_VSYNC	**CSI0_VSYNC**	GPIO5[21]	
114	3V3	CSI0_PIXCLK	CSI0_PIXCLK	**CSI0_PIXCLK**	GPIO5[18]	
115	3V3	CSI0_MCLK	GPIO_0	**CCM_CLKO** KPP_COL[5] CCM_SSI_EXT1_CLK EPIT1_EPITO SRTC_ALARM_DEB USBOH3_USBH1_PWR TD	GPIO1[0]	
116	GND	GND				
LCD Controller and Smart LCD Controller						
117	3V0	LD0	DISP0_DAT0	**DISP0_DAT[0]** CSPI_SCLK USBOH3_USBH2_DATA[0] USBPHY2_TXREADY	GPIO4[21]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_TX2_N	not available		TX53 LVDS version: LVDS display output port 1
118	3V0	LD1	DISP0_DAT1	**DISP0_DAT[1]** CSPI_MOSI USBOH3_USBH2_DATA[1] USBPHY2_RXVALID	GPIO4[22]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_TX1_N	not available		TX53 LVDS version: LVDS display output port 1
119	3V0	LD2	DISP0_DAT2	**DISP0_DAT[2]** CSPI_MISO USBOH3_USBH2_DATA[2] USBPHY2_RXACTIVE	GPIO4[23]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_TX2_P	not available		TX53 LVDS version: LVDS display output port 1
120	3V0	LD3	DISP0_DAT3	**DISP0_DAT[3]** CSPI_SS0 USBOH3_USBH2_DATA[3] USBPHY2_RXERROR	GPIO4[24]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_TX1_P	not available		TX53 LVDS version: LVDS display output port 1
121	3V0	LD4	DISP0_DAT4	**DISP0_DAT[4]** CSPI_SS1 USBOH3_USBH2_DATA[4] USBPHY2_SIECLOCK	GPIO4[25]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_TX3_N	not available		TX53 LVDS version: LVDS display output port 1
122	3V0	LD5	DISP0_DAT5	**DISP0_DAT[5]** CSPI_SS2 USBOH3_USBH2_DATA[5] USBPHY2_LINESTATE[0]	GPIO4[26]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_TX0_N	not available		TX53 LVDS version: LVDS display output port 1
123	3V0	LD6	DISP0_DAT6	**DISP0_DAT[6]** CSPI_SS3 USBOH3_USBH2_DATA[6] USBPHY2_LINESTATE[1]	GPIO4[27]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_TX3_P	not available		TX53 LVDS version: LVDS display output port 1
124	3V0	LD7	DISP0_DAT7	**DISP0_DAT[7]** CSPI_RDY USBOH3_USBH2_DATA[7] USBPHY2_VBUSVALID	GPIO4[28]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_TX0_P	not available		TX53 LVDS version: LVDS display output port 1
125	3V0	LD8	DISP0_DAT8	**DISP0_DAT[8]** PWM1_PWMO WDOG1_WDOG_B USBPHY2_AVALID	GPIO4[29]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_CLK_N	not available		TX53 LVDS version: LVDS display output port 1

PIN	Type	Function	i.MX53 Pad Name	Alternate functions	GPIO	Description (refer to i.MX53 manuals for details)
126	3V0	LD9	DISP0_DAT9	**DISP0_DAT[9]** PWM2_PWMO WDOG2_WDOG_B USBPHY2_VSTATUS[0]	GPIO4[30]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_TX3_P	not available		TX53 LVDS version: LVDS display output port 0
127	3V0	LD10	DISP0_DAT10	**DISP0_DAT[10]** USBOH3_USBH2_STP USBPHY2_VSTATUS[1]	GPIO4[31]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_CLK_P	not available		TX53 LVDS version: LVDS display output port 1
128	3V0	LD11	DISP0_DAT11	**DISP0_DAT[11]** USBOH3_USBH2_NXT USBPHY2_VSTATUS[2]	GPIO5[5]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_TX3_N	not available		TX53 LVDS version: LVDS display output port 0
129	GND	GND				
130	3V0	LD12	DISP0_DAT12	**DISP0_DAT[12]** USBOH3_USBH2_CLK USBPHY2_VSTATUS[3]	GPIO5[6]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_CLK_P	not available		TX53 LVDS version: LVDS display output port 0
131	3V0	LD13	DISP0_DAT13	**DISP0_DAT[13]** AUD5_RXFS USBPHY2_VSTATUS[4]	GPIO5[7]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_TX2_P	not available		TX53 LVDS version: LVDS display output port 0
132	3V0	LD14	DISP0_DAT14	**DISP0_DAT[14]** AUD5_RXC USBPHY2_VSTATUS[5]	GPIO5[8]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_CLK_N	not available		TX53 LVDS version: LVDS display output port 0
133	3V0	LD15	DISP0_DAT15	**DISP0_DAT[15]** ECSPI1_SS1 ECSPI2_SS1 USBPHY2_VSTATUS[6]	GPIO5[9]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_TX2_N	not available		TX53 LVDS version: LVDS display output port 0
134	3V0	LD16	DISP0_DAT16	**DISP0_DAT[16]** ECSPI2_MOSI AUD5_TXC SDMA_EXT_EVENT[0] USBPHY2_VSTATUS[7]	GPIO5[10]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_TX1_P	not available		TX53 LVDS version: LVDS display output port 0
135	3V0	LD17	DISP0_DAT17	**DISP0_DAT[17]** ECSPI2_MISO AUD5_TXD SDMA_EXT_EVENT[1]	GPIO5[11]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_TX0_P	not available		TX53 LVDS version: LVDS display output port 0
136	3V0	LD18	DISP0_DAT18	**DISP0_DAT[18]** ECSPI2_SS0 AUD5_TXFS AUD4_RXFS WEIM_CS[2]	GPIO5[12]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_TX1_N	not available		TX53 LVDS version: LVDS display output port 0
137	3V0	LD19	DISP0_DAT19	**DISP0_DAT[19]** ECSPI2_SCLK AUD5_RXD AUD4_RXC WEIM_CS[3]	GPIO5[13]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_TX0_N	not available		TX53 LVDS version: LVDS display output port 0
138	3V0	LD20	DISP0_DAT20	**DISP0_DAT[20]** ECSPI1_SCLK AUD4_TXC	GPIO5[14]	TX53 standard version: LCD Data Bus
	SATA		SATA_RXM	not available		TX53 LVDS version: SATA port
139	3V0	LD21	DISP0_DAT21	**DISP0_DAT[21]** ECSPI1_MOSI AUD4_TXD	GPIO5[15]	TX53 standard version: LCD Data Bus
	SATA		SATA_TXM	not available		TX53 LVDS version: SATA port

PIN	Type	Function	i.MX53 Pad Name	Alternate functions	GPIO	Description (refer to i.MX53 manuals for details)
140	3V0	LD22	DISP0_DAT22	**DISP0_DAT[22]** ECSPI1_MISO AUD4_TXFS	GPIO5[16]	TX53 standard version: LCD Data Bus
	SATA		SATA_RXP	not available		TX53 LVDS version: SATA port
141	3V0	LD23	DISP0_DAT23	**DISP0_DAT[23]** ECSPI1_SS0 AUD4_RXD	GPIO5[17]	TX53 standard version: LCD Data Bus
	SATA		SATA_TXP	not available		TX53 LVDS version: SATA port
142	GND	GND				
143	3V0	HSYNC	DI0_PIN2	**DI0_PIN2** AUD6_TXD USBPHY1_ENDSESSION	GPIO4[18]	
144	3V0	VSYNC	DI0_PIN3	**DI0_PIN3** AUD6_TXFS USBPHY1_IDDIG	GPIO4[19]	
145	3V0	OE_ACD	DI0_PIN15	**DI0_PIN15** AUD6_TXC USBPHY1_BVALID	GPIO4[17]	
146	3V0	LSCLK	DI0_DISP_CLK	**DI0_DISP_CLK** USBOH3_USBH2_DIR USBPHY1_AVALID	GPIO4[16]	
147	GND	GND				
Module Specific Signals						
148	3V3	CSI1_MCLK	NANDF_CS2	NANDF_CS[2] SISG[0] / ESAI1_TX0 WEIM_CRE CCM_CSI0_MCLK MLBSIG USBPHY1_VSTATUS[6]	GPIO6[15]	
149	3V3	CSI1_PIXCLK	EIM_A16	WEIM_A[16] DI1_DISP_CLK CSI1_PIXCLK BT_CFG1[1]	GPIO2[22]	
150	3V3	CSI1_VSYNC	EIM_D29	WEIM_D[29] UART2_RTS DISPB0_SER_RS CSPI_SS0 / DI1_PIN15 CSI1_VSYNC DI0_PIN14	GPIO3[29]	
151	3V3	CSI1_HSYNC	EIM_EB3	WEIM_EB[3] UART3_RTS UART1_RI / DI1_PIN3 CSI1_HSYNC DI1_PIN16	GPIO2[31]	
152	3V3	CSI1_D[12]	EIM_A17	WEIM_A[17] DISP1_DAT[12] CSI1_D[12] BT_CFG1[2]	GPIO2[21]	
153	3V3	CSI1_D[13]	EIM_A18	WEIM_A[18] DISP1_DAT[13] CSI1_D[13] BT_CFG1[3]	GPIO2[20]	
154	3V3	CSI1_D[14]	EIM_A19	WEIM_A[19] DISP1_DAT[14] CSI1_D[14] BT_CFG1[4]	GPIO2[19]	
155	3V3	CSI1_D[15]	EIM_A20	WEIM_A[20] DISP1_DAT[15] CSI1_D[15] BT_CFG1[5]	GPIO2[18]	
156	3V3	CSI1_D[16]	EIM_A21	WEIM_A[21] DISP1_DAT[16] CSI1_D[16] BT_CFG1[6]	GPIO2[17]	
157	3V3	CSI1_D[17]	EIM_A22	WEIM_A[22] DISP1_DAT[17] CSI1_D[17] BT_CFG1[7]	GPIO2[16]	
158	3V3	CSI1_D[18]	EIM_A23	WEIM_A[23] DISP1_DAT[18] CSI1_D[18] / SISG[3] USBPHY2_ENDSESSION	GPIO6[6]	
159	3V3	CSI1_D[19]	EIM_A24	WEIM_A[24] DISP1_DAT[19] CSI1_D[19] / SISG[2] USBPHY2_BVALID	GPIO5[4]	

PIN	Type	Function	i.MX53 Pad Name	Alternate functions	GPIO	Description (refer to i.MX53 manuals for details)
160	GND	GND				
161	3V3		CSI0_DAT8	CSI0_D[8] / KPP_COL[7] ECSPI2_SCLK USBOH3_USBH3_OC I2C1_SDA	GPIO5[26]	
162	3V3		CSI0_DAT9	CSI0_D[9] / KPP_ROW[7] ECSPI2_MOSI USBOH3_USBH3_PWR I2C1_SCL	GPIO5[27]	
163	3V3		CSI0_DAT10	CSI0_D[10] UART1_TXD ECSPI2_MISO AUD3_RXC	GPIO5[28]	
164	3V3		CSI0_DAT11	CSI0_D[11] UART1_RXD ECSPI2_SS0 AUD3_RXFS	GPIO5[29]	
165	3V3		EIM_D22	WEIM_D[22] DI0_PIN1 DISPB0_SER_DIN CSPI_MISO USBOH3_USBOTG_PWR	GPIO3[22]	
166	3V3		EIM_D23	WEIM_D[23] UART3_CTS UART1_DCD DI0_D0_CS DI1_PIN2 CSI1_DATA_EN DI1_PIN14	GPIO3[23]	
167	3V3	CKIH1	CKIH1			
168	3V3	TVDAC_IOB	TVDAC_IOB			
169	3V3	TVDAC_IOG	TVDAC_IOG			
170	3V3	TVDAC_IOR	TVDAC_IOR			
171	GND	GND				
172	2V8		GPIO_13		GPIO4[3]	Not available on TX53 version v2
173	3V3	EIM_CS0	EIM_CS0	WEIM_CS[0] ECSPI2_SCLK DI1_PIN5	GPIO2[23]	
174	3V3	EIM_CS1	EIM_CS1	WEIM_CS[1] ECSPI2_MOSI DI1_PIN6	GPIO2[24]	
175	3V3	GPIO	CSI0_DATA_EN	CSI0_DATA_EN	GPIO5[20]	EIM_DTACK is used on the TX51, this function is not supported by the TX53
176	3V3	EIM_WAIT	EIM_WAIT	WEIM_WAIT WEIM_DTACK_B	GPIO5[0]	
177	3V3	EIM_EB0	EIM_EB0	WEIM_EB[0] DISP1_DAT[11] CSI1_D[11] GPC_PMIC_RDY BT_CFG2[7]	GPIO2[28]	
178	3V3	EIM_EB1	EIM_EB1	WEIM_EB[1] DISP1_DAT[10] CSI1_D[10] BT_CFG2[6]	GPIO2[29]	
179	3V3	EIM_OE	EIM_OE	WEIM_OE ECSPI2_MISO DI1_PIN7 USBPHY2_IDDIG	GPIO2[25]	
180	3V3	EIM_LBA	EIM_LBA	WEIM_LBA ECSPI2_SS1 DI1_PIN17 BT_CFG1[0]	GPIO2[27]	
181	3V3	EIM_RW	EIM_RW	WEIM_RW ECSPI2_SS0 DI1_PIN8 USBPHY2_ HOSTDISCONNECT	GPIO2[26]	
182	3V3	EIM_BCLK	EIM_BCLK	WEIM_BCLK		
183	GND	GND				
184	3V3	EIM_DA0	EIM_DA0	NAND_WEIM_DA[0]		Fixed function used for NAND flash