# TX6DL

## TX Family Computer On Module

- Processor — Dual ARM® Cortex®-A9 based NXP i.MX6 DualLite, 800MHz
- RAM — 1GB DDR3 SDRAM
- ROM — 128MB SLC NAND Flash / 4GB eMMC
- Power supply — Single 3.1V to 5.5V
- Size — 31mm SO-DIMM
- Grade — Industrial
- Temperature — (-40°C/-25°C to 105°C Tj)


## Key Features

- ARM® Cortex®-A9
- Display support:
  - Full HD LCD controller, 24bpp (Standard version)
  - OpenGL ES 2.0 hardware accelerator
  - Multi-format HD 1080p60 video decoder and 1080p30 encoder hardware engine
  - Dual LVDS display interface (LVDS version)

## Connectivity

- 10/100Mbps Ethernet
- Two High Speed USB 2.0 ports
- Two Camera Interfaces
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - dual, single-precision floating point execute pipeline
- Unified 1MB L2 cache
- Several interfaces:
  3x UART, 2x SDIO, 2x SSI/AC97/I2S,
  I2C, CSPI, Keypad, Ext. Memory I/F
- 3.3V I/O
- 2x Controller Area Network (FlexCAN)
- PCIe 2.0 (1-lane)

## OS Support

- Windows Embedded Compact 7
- Windows Embedded Compact 2013
- Linux
- Android by kernel concepts — www.kernelconcepts.de
- QNX by SITRE — www.sitre.fr

Ka-Ro electronics GmbH - Pascalstr. 22, D-52076 Aachen, Germany - Tel.: +49 2408 1402-0 (FAX -10)
**www.karo-electronics.de**

**Board highlights:**

- Highly integrated
- Standard TX-DIMM pinout
- as small as possible - only 31mm
- 3.3V I/O

The TX6 is a member of the TXCOM module series, specially designed for i.MX multimedia processors. TXCOM modules are complete computers, implemented on a board smaller than a credit card, and ready to be designed into your embedded system. TXCOM modules includes an i.MX processor, SDRAM and Flash memory. The integrated LCD-controller enables direct connection of an LCD screen. The TX6 is specifically targeted at embedded applications where size, high cpu-performance and cost are critical factors.

**Computer on module**

- NXP i.MX6 DualLite, 800 MHz
- 1GByte (64bit) SDRAM DDR3-800
- 128 Mbyte NAND Flash memory
- TXCOM DIMM200-module (67,6mm x 31 mm x 4mm)
- Operating temperature ranges (Processor junction temperature)
  Extended Consumer Grade: -20°C ..105°C
  Industrial Grade: -40°C (eMMC: -25°C) ..105°C
  Automotive Grade: -40°C ..125°C, AEC-Q100 Grade 3

**Processor**

The i.MX 6Dual Lite processors represent NXP Semiconductors' latest achievement in integrated multimedia applications processors. These processors are part of a growing family of multimedia-focused products that offer high performance processing and are optimized for lowest power consumption. The i.MX 6Dual Lite processors feature NXP's advanced implementation of the dual ARM Cortex™-A9 core, which operates at speeds up to 1 GHz. They include 2D and 3D graphics processors, 3D 1080p video processing, and integrated power management. Each processor provides a 64-bit DDR3/LVDDR3/LPDDR2-800 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

**High Performance CPU : Dual ARM® Cortex®-A9**

- Dual ARM® Cortex®-A9, with ARMv7™, Neon, VFPv3 and Trustzone support
- 32K instruction and data L1 caches and 256 KB to 1 MB of L2 cache
- Multi-stream-capable HD video engine delivering 1080p60 decode, 1080p30 encode and 3D video playback in HD in high performance families
- Superior 3D graphics performance with a shader performing up to 50 MT/s. Separate 2D and/or Vertex acceleration engines for an optimal user interface experience
- Stereoscopic image sensor support for 3D imaging

**Standard TXCOM pinout:**

- 4-wire UARTs (x3)
- LCD
- I2C / PWM
- Serial Audio Interfaces (x2)
- 4-wire SD-Card/SDIO

High-Speed communication interfaces incl. onboard Ethernet PHY / on-chip USB PHY allows direct use of connectors/magnetics on the baseboard without the need for additional logic:

- 10/100 Mbps Ethernet
- 480 Mbps USB OTG (Host or Device)
- 480 Mbps USB Host

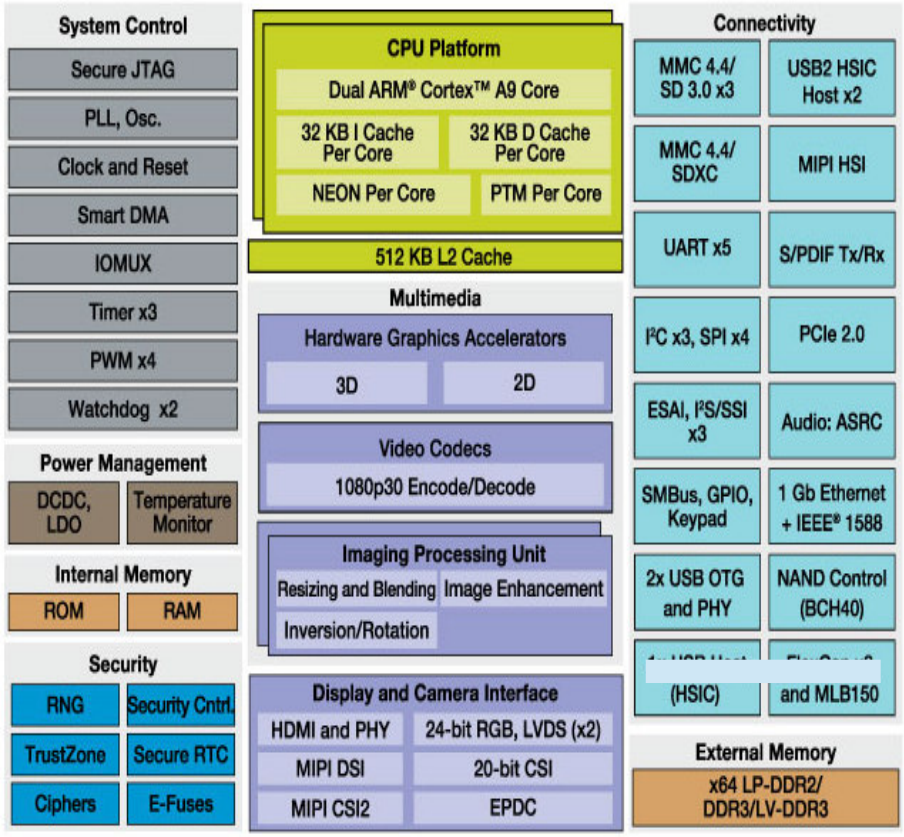
**Power Supply**

The TX6 accepts an input voltage from various sources:

- 1-cell Li-Ion/Polymer (up to 4.2V)
- 5.0V USB supply or AC wall adapter
- 3.3V

**Read more in our TX-Guide:**

www.karo-electronics.com/TX-Guide




Ordering Information

| Order Number | CPU | SDRAM | Flash | RTC | Temp. Grade |
|---|---|---|---|---|---|
| TX6DL/800/1024S/128F/I<br>TX6DL/800/1024S/128F/LVDS/I | 800MHz MCIMX6U7<br>Dual Core Industrial | 1GB | 128MB | DS1339 | industrial<br>-40°C..85°C |
| TX6DL/800/1024S/4GF/E85<br>TX6DL/800/1024S/4GF/LVDS/E85 | 800MHz MCIMX6U7<br>Dual Core Industrial | 1GB | 4GB | i.MX6 | industrial<br>-25°C..85°C |

2019-02-06

## PINOUT

| PIN | Type | Function | i.MX6 Dual Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 Dual manuals for details) |
|---|---|---|---|---|---|---|
| **POWER SUPPLY & RESET** | | | | | | |
| 1-4 | power | VIN | | | | Module power supply input<br>(3.3V-5V, observe DIMM socket contact current rating) |
| 5-7, 9-12 | power | VOUT | | | | 3.3V power supply output.<br>Supplied by RN5T567 LDO2 (max. 300mA) |
| 8 | 3V3 | BOOTMODE | | | 10K-PU | Boot mode select H: Boot from NAND / L: Boot from UART/USB |
| 13 | power | VBACKUP | Version with DS1339 RTC | | | |
| | | | | | | DS1339 RTC backup power supply. Supply voltage must be held between 1.3V and 3.7V for proper RTC operation. This pin can be connected to a primary cell such as a lithium button cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used with the trickle charge feature. |
| | | | Version without DS1339 RTC | | | |
| | | | Connected through a 240 Ohms resistor to VDD_SNVS_IN | | | i.MX6 SNVS backup power supply. Supply voltage must be held between 2.9V and 3.3V if the system requires keeping real time and other data on OFF state. This pin is connected to RN5T567 LDORTC1 (3V/30mA) through an onboard 240R resistor. Leave unconnected if the system does not require keeping real time and other data on OFF state. |
| 14 | VIN | PMIC_PWR_BTN | | | | Connected to RN5T567 PWRON, 10K-PU connected to VIN<br>Leave unconnected, if not used. |
| 15 | 3V3 | #RESET_OUT | GPIO_17 | ESAI_TX0<br>ENET_1588_EVENT3_IN<br>CCM_PMIC_READY<br>SDMA_EXT_EVENT0<br>SPDIF_OUT | GPIO7[12] | #RESET_OUT may be used to reset peripherals on the carrier board. This signal can be controlled by a GPIO function during runtime. |
| 16 | | #POR | POR_B | | 10K-PU | Power On Reset — Active low input signal<br>Leave unconnected, if not used. |
| 17 | | #RESET_IN | POR_B | | | Wire ored to pin 16 |
| 18 | GND | GND | | | | |
| **Ethernet** | | | | | | |
| 19 | analog | ETN_TXN | | | | Transmit Data Negative: 100Base-TX or 10Base-T differential transmit output to magnetics. |
| 20 | 3V3 | #ETN_LED2 | | | | Active low - output is driven active when the operating speed is 100Mbps. This LED will go inactive when the operating speed is 10Mbps or during line isolation. |
| 21 | analog | ETN_TXP | | | | Transmit Data Positive: 100Base-TX or 10Base-T differential transmit output to magnetics. |
| 22 | power | ETN_3V3 | | | | +3.3V analog power supply output to magnetics |
| 23 | analog | ETN_RXN | | | | Receive Data Negative: 100Base-TX or 10Base-T differential receive input from magnetics. |
| 24 | 3V3 | #ETN_LED1 | | | | Active low - output is driven active whenever the device detects a valid link, and blinks indicating activity. |
| 25 | analog | ETN_RXP | | | | Receive Data Positive: 100Base-TX or 10Base-T differential receive input from magnetics. |
| 26 | GND | GND | | | | |
| **USB-HOST** | | | | | | |
| 27 | 3V3 | USBH_VBUSEN | EIM_D31 | EIM_DATA31<br>IPU1_DISP1_DATA20<br>IPU1_DI0_PIN12<br>IPU1_CSI0_DATA02<br>UART3_RTS_B<br>USB_H1_PWR<br>EPDC_SDCLK_P<br>EIM_ACLK_FREERUN | GPIO3[31] | Active high external 5V supply enable. This pin is used to enable the external VBUS power supply. |
| 28 | 3V3 | #USBH_OC | EIM_D30 | EIM_DATA30<br>IPU1_DISP1_DATA21<br>IPU1_DI0_PIN11<br>IPU1_CSI0_DATA03<br>UART3_CTS_B<br>USB_H1_OC<br>EPDC_SDOEZ | GPIO3[30]<br>10K-PU | Active low over-current indicator input connected to a GPIO. |
| 29 | analog | USBH_DM | USB_H1_DN | | | D- pin of the USB cable |
| 30 | analog | USBH_VBUS | USB_H1_VBUS | | | VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs. |
| 31 | analog | USBH_DP | USB_H1_DP | | | D+ pin of the USB cable |
| 32 | GND | GND | | | | |

| PIN | Type | Function | i.MX6 Dual Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 Dual manuals for details) |
|---|---|---|---|---|---|---|
| **USB-OTG / 2nd CAN** | | | | | | |
| 33 | 3V3 | USBOTG_ID | EIM_D23 | EIM_DATA23<br>IPU1_DI0_D0_CS<br>UART3_CTS_B<br>UART1_DCD_B<br>IPU1_CSI1_DATA_EN<br>IPU1_DI1_PIN02<br>IPU1_DI1_PIN14<br>EPDC_DATA11 | **GPIO3[23]** | |
| 34 | 3V3 | USBOTG_VBUSEN<br>CAN_TX | GPIO_7 | ESAI_TX4_RX1<br>EPIT1_OUT<br>FLEXCAN1_TX<br>UART2_TX_DATA<br>SPDIF_LOCK<br>USB_OTG_HOST_MODE<br>I2C4_SCL | **GPIO1[7]** | Active high external 5V supply enable. This pin is used to enable the external VBUS power supply. |
| 35 | analog | USBOTG_DM | USB_OTG_DN | | | D- pin of the USB cable |
| 36 | 3V3 | #USBOTG_OC<br>CAN_RX | GPIO_8 | ESAI_TX5_RX0<br>XTALOSC_REF_CLK_32K<br>EPIT2_OUT<br>FLEXCAN1_RX<br>UART2_RX_DATA<br>SPDIF_SR_CLK<br>USB_OTG_PWR_CTL_WAKE<br>I2C4_SDA | **GPIO1[8]**<br>10K-PU | Active low over-current indicator input connected to a GPIO. |
| 37 | analog | USBOTG_DP | USB_OTG_DP | | | D+ pin of the USB cable |
| 38 | analog | USBOTG_VBUS | USB_OTG_VBUS | | | VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs. |
| 39 | GND | GND | | | | |
| **I2C** | | | | | | |
| 40 | 3V3 | I2C_DATA | GPIO_6 | ESAI_TX_CLK<br>I2C3_SDA<br>SD2_LCTL<br>MLB_SIG | GPIO1[6] | I2C Data |
| 41 | 3V3 | I2C_CLK | GPIO_3 | ESAI_RX_HF_CLK<br>I2C3_SCL<br>XTALOSC_REF_CLK_24M<br>CCM_CLKO2<br>USB_H1_OC<br>MLB_CLK | GPIO1[3] | I2C Clock |
| **PWM** | | | | | | |
| 42 | 3V3 | PWM | GPIO_1 | ESAI_RX_CLK<br>WDOG2_B<br>KEY_ROW5<br>USB_OTG_ID<br>PWM2_OUT<br>SD1_CD_B | GPIO1[1] | PWM Output |
| **1-WIRE** | | | | | | |
| 43 | 3V3 | OWDAT | GPIO_18 | ESAI_TX1<br>ENET_RX_CLK<br>SD3_VSELECT<br>SDMA_EXT_EVENT1<br>ASRC_EXT_CLK<br>SNVS_VIO_5_CTL | GPIO7[13] | 1-Wire bus. Requires an external pull-up resistor. The recommended<br>resistor is specified by the generic 1-Wire device used in a given system. |
| **CSPI – Configurable Serial Peripheral Interface** | | | | | | |
| 44 | 3V3 | CSPI_SS | EIM_EB2 | EIM_EB2<br>ECSPI1_SS0<br>IPU1_CSI1_DATA19<br>HDMI_TX_DDC_SCL<br>I2C2_SCL<br>SRC_BOOT_CFG30<br>EPDC_DATA05 | GPIO2[30] | Slave Select (Selectable polarity) signal |
| 45 | 3V3 | CSPI_SS | EIM_D19 | EIM_DATA19<br>ECSPI1_SS1<br>IPU1_DI0_PIN08<br>IPU1_CSI1_DATA16<br>UART1_CTS_B<br>EPIT1_OUT<br>EPDC_DATA12 | GPIO3[19] | Slave Select (Selectable polarity) signal |
| 46 | 3V3 | CSPI_MOSI | EIM_D18 | EIM_DATA18<br>ECSPI1_MOSI | GPIO3[18] | Master Out/Slave In signal |

| PIN | Type | Function | i.MX6 Dual Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 Dual manuals for details) |
|---|---|---|---|---|---|---|
| | | | | IPU1_DI0_PIN07<br>IPU1_CSI1_DATA17<br>IPU1_DI1_D0_CS<br>I2C3_SDA<br>EPDC_VCOM1 | | |
| 47 | 3V3 | CSPI_MISO | EIM_D17 | EIM_DATA17<br>ECSPI1_MISO<br>IPU1_DI0_PIN06<br>IPU1_CSI1_PIXCLK<br>DCIC1_OUT<br>I2C3_SCL<br>EPDC_VCOM0 | GPIO3[17] | Master In/Slave Out signal |
| 48 | 3V3 | CSPI_SCLK | EIM_D16 | EIM_DATA16<br>ECSPI1_SCLK<br>IPU1_DI0_PIN05<br>IPU1_CSI1_DATA18<br>HDMI_TX_DDC_SDA<br>I2C2_SDA<br>EPDC_DATA10 | GPIO3[16] | Serial Clock signal |
| 49 | 3V3 | CSPI_RDY | GPIO_19 | KEY_COL5<br>ENET_1588_EVENT0_OUT<br>SPDIF_OUT<br>CCM_CLKO1<br>ECSPI1_RDY<br>ENET_TX_ER | GPIO4[5] | Serial Data Ready signal |
| 50 | GND | GND | | | | |
| **SD – Secure Digital Interface 1** | | | | | | |
| 51 | 3V3 | SD1_CD | SD3_CMD | SD3_CMD<br>UART2_CTS_B<br>FLEXCAN1_TX | **GPIO7[2]** | SD Card Detect – connected to a GPIO |
| 52 | 3V3 | SD1_D[0] | SD1_DAT0 | SD1_DATA0<br>GPT_CAPTURE1 | GPIO1[16] | SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added. |
| 53 | 3V3 | SD1_D[1] | SD1_DAT1 | SD1_DATA1<br>PWM3_OUT<br>GPT_CAPTURE2 | GPIO1[17] | |
| 54 | 3V3 | SD1_D[2] | SD1_DAT2 | SD1_DATA2<br>GPT_COMPARE2<br>PWM2_OUT<br>WDOG1_B<br>WDOG1_RESET_B_DEB | GPIO1[19] | |
| 55 | 3V3 | SD1_D[3] | SD1_DAT3 | SD1_DATA3<br>GPT_COMPARE3<br>PWM1_OUT<br>WDOG2_B<br>WDOG2_RESET_B_DEB | GPIO1[21] | |
| 56 | 3V3 | SD1_CMD | SD1_CMD | SD1_CMD<br>PWM4_OUT<br>GPT_COMPARE1 | GPIO1[18] | SD Command bidirectional signal |
| 57 | 3V3 | SD1_CLK | SD1_CLK | SD1_CLK<br>GPT_CLKIN | GPIO1[20] | SD Output Clock. |
| 58 | GND | GND | | | | |
| **1st UART** | | | | | | |
| 59 | 3V3 | TXD | SD3_DAT7 | SD3_DATA7<br>UART1_TX_DATA | GPIO6[17] | Application UART 1 Transmit Data output signal |
| 60 | 3V3 | RXD | SD3_DAT6 | SD3_DATA6<br>UART1_RX_DATA | GPIO6[18] | Application UART 1 Receive Data input signal |
| 61 | 3V3 | RTS | SD3_DAT1 | SD3_DATA1<br>UART1_RTS_B<br>FLEXCAN2_RX | GPIO7[5] | Application UART 1 Request to Send **input** signal |
| 62 | 3V3 | CTS | SD3_DAT0 | SD3_DATA0<br>UART1_CTS_B<br>FLEXCAN2_TX | GPIO7[4] | Application UART 1 Clear to Send **output** signal |
| **2nd UART** | | | | | | |
| 63 | 3V3 | TXD | SD4_DAT7 | SD4_DATA7<br>UART2_TX_DATA | GPIO2[15] | Application UART 2 Transmit Data output signal |
| 64 | 3V3 | RXD | SD4_DAT4 | SD4_DATA4<br>UART2_RX_DATA | GPIO2[12] | Application UART 2 Receive Data input signal |
| 65 | 3V3 | RTS | SD4_DAT5 | SD4_DATA5<br>UART2_RTS_B | GPIO2[13] | Application UART 2 Request to Send **input** signal |
| 66 | 3V3 | CTS | SD4_DAT6 | SD4_DATA6<br>UART2_CTS_B | GPIO2[14] | Application UART 2 Clear to Send **output** signal |
| **3rd UART** | | | | | | |
| 67 | 3V3 | TXD | EIM_D24 | EIM_DATA24<br>ECSPI4_SS2<br>UART3_TX_DATA | GPIO3[24] | Application UART 3 Transmit Data output signal |

| PIN | Type | Function | i.MX6 Dual Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 Dual manuals for details) |
|---|---|---|---|---|---|---|
| | | | | ECSPI1_SS2<br>ECSPI2_SS2<br>AUD5_RXFS<br>UART1_DTR_B<br>EPDC_SDCE7 | | |
| 68 | 3V3 | RXD | EIM_D25 | EIM_DATA25<br>ECSPI4_SS3<br>UART3_RX_DATA<br>ECSPI1_SS3<br>ECSPI2_SS3<br>AUD5_RXC<br>UART1_DSR_B<br>EPDC_SDCE8 | GPIO3[25] | Application UART 3 Receive Data input signal |
| 69 | 3V3 | RTS | SD3_RST | SD3_RESET<br>UART3_RTS_B | GPIO7[8] | Application UART 3 Request to Send **input** signal |
| 70 | 3V3 | CTS | SD3_DAT3 | SD3_DATA3<br>UART3_CTS_B | GPIO7[7] | Application UART 3 Clear to Send **output** signal |
| 71 | GND | GND | | | | |
| **KEYPAD / 1st CAN** | | | | | | |
| 72 | 3V3 | KP_COL[0] | GPIO_9 | ESAI_RX_FS<br>WDOG1_B<br>KEY_COL6<br>CCM_REF_EN_B<br>PWM1_OUT<br>SD1_WP | GPIO1[9] | |
| 73 | 3V3 | KP_COL[1] | GPIO_4 | ESAI_TX_HF_CLK<br>KEY_COL7<br>SD2_CD_B | GPIO1[4] | |
| 74 | 3V3 | KP_COL[2] | KEY_COL2 | ECSPI1_SS1<br>ENET_RX_DATA2<br>FLEXCAN1_TX<br>KEY_COL2<br>ENET_MDC<br>USB_H1_PWR_CTL_WAKE | GPIO4[10] | |
| 75 | 3V3 | KP_COL[3] | KEY_COL3 | ECSPI1_SS3<br>ENET_CRS<br>HDMI_TX_DDC_SCL<br>KEY_COL3<br>I2C2_SCL<br>SPDIF_IN | GPIO4[12] | |
| 76 | 3V3 | TXCAN | KEY_COL4 | FLEXCAN2_TX<br>IPU1_SISG4<br>USB_OTG_OC<br>KEY_COL4<br>UART5_RTS_B | GPIO4[14] | |
| 77 | 3V3 | KP_ROW[0] | GPIO_2 | ESAI_TX_FS<br>KEY_ROW6<br>SD2_WP<br>MLB_DATA | GPIO1[2] | |
| 78 | 3V3 | KP_ROW[1] | GPIO_5 | ESAI_TX2_RX3<br>KEY_ROW7<br>CCM_CLKO1<br>I2C3_SCL<br>ARM_EVENTI | GPIO1[5] | |
| 79 | 3V3 | KP_ROW[2] | KEY_ROW2 | ECSPI1_SS2<br>ENET_TX_DATA2<br>FLEXCAN1_RX<br>KEY_ROW2<br>SD2_VSELECT<br>HDMI_TX_CEC_LINE | GPIO4[11] | |
| 80 | 3V3 | KP_ROW[3] | KEY_ROW3 | ASRC_EXT_CLK<br>HDMI_TX_DDC_SDA<br>KEY_ROW3<br>I2C2_SDA<br>SD1_VSELECT | GPIO4[13] | |
| 81 | 3V3 | RXCAN | KEY_ROW4 | FLEXCAN2_RX<br>IPU1_SISG5<br>USB_OTG_PWR<br>KEY_ROW4<br>UART5_CTS_B | GPIO4[15] | |
| 82 | GND | GND | | | | |
| **SSI 1 - Serial Audio Port 1** | | | | | | |
| 83 | 3V3 | SSI1_INT | EIM_D26 | EIM_DATA26<br>IPU1_DI1_PIN11<br>IPU1_CSI0_DATA01<br>IPU1_CSI1_DATA14<br>UART2_TX_DATA | **GPIO3[26]** | GPIO |

| PIN | Type | Function | i.MX6 Dual Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 Dual manuals for details) |
|---|---|---|---|---|---|---|
| | | | | IPU1_SISG2<br>IPU1_DISP1_DATA22<br>EPDC_SDOED | | |
| 84 | 3V3 | SSI1_RXD | KEY_ROW1 | ECSPI1_SS0<br>ENET_COL<br>AUD5_RXD<br>KEY_ROW1<br>UART5_RX_DATA<br>SD2_VSELECT | GPIO4[9] | Serial Audio Interface serial data line 1 |
| 85 | 3V3 | SSI1_TXD | KEY_ROW0 | ECSPI1_MOSI<br>ENET_TX_DATA3<br>AUD5_TXD<br>KEY_ROW0<br>UART4_RX_DATA<br>DCIC2_OUT | GPIO4[7] | Serial Audio Interface serial data line 0 |
| 86 | 3V3 | SSI1_CLK | KEY_COL0 | ECSPI1_SCLK<br>ENET_RX_DATA3<br>AUD5_TXC<br>KEY_COL0<br>UART4_TX_DATA<br>DCIC1_OUT | GPIO4[6] | Serial Audio Interface serial bit clock |
| 87 | 3V3 | SSI1_FS | KEY_COL1 | ECSPI1_MISO<br>ENET_MDIO<br>AUD5_TXFS<br>KEY_COL1<br>UART5_TX_DATA<br>SD1_VSELECT | GPIO4[8] | Serial Audio Interface left/right clock |
| 88 | GND | GND | | | | |
| **SSI 2 - Serial Audio Port 2** | | | | | | |
| 89 | 3V3 | SSI2_INT | EIM_D27 | EIM_DATA27<br>IPU1_DI1_PIN13<br>IPU1_CSI0_DATA00<br>IPU1_CSI1_DATA13<br>UART2_RX_DATA<br>IPU1_SISG3<br>IPU1_DISP1_DATA23<br>EPDC_SDOE | **GPIO3[27]** | GPIO |
| 90 | 3V3 | SSI2_RXD | CSI0_DAT7 | IPU1_CSI0_DATA07<br>EIM_DATA05<br>ECSPI1_SS0<br>KEY_ROW6<br>AUD3_RXD<br>ARM_TRACE04 | GPIO5[25] | Serial Audio Interface serial data line 1 |
| 91 | 3V3 | SSI2_TXD | CSI0_DAT5 | IPU1_CSI0_DATA05<br>EIM_DATA03<br>ECSPI1_MOSI<br>KEY_ROW5<br>AUD3_TXD<br>ARM_TRACE02 | GPIO5[23] | Serial Audio Interface serial data line 0 |
| 92 | 3V3 | SSI2_CLK | CSI0_DAT4 | IPU1_CSI0_DATA04<br>EIM_DATA02<br>ECSPI1_SCLK<br>KEY_COL5<br>AUD3_TXC<br>ARM_TRACE01 | GPIO5[22] | Serial Audio Interface serial bit clock |
| 93 | 3V3 | SSI2_FS | CSI0_DAT6 | IPU1_CSI0_DATA06<br>EIM_DATA04<br>ECSPI1_MISO<br>KEY_COL6<br>AUD3_TXFS<br>ARM_TRACE03 | GPIO5[24] | Serial Audio Interface left/right clock |
| 94 | GND | GND | | | | |
| **Secure Digital Interface 2** | | | | | | |
| 95 | 3V3 | SD2_CD | SD3_CLK | SD3_CLK<br>UART2_RTS_B<br>FLEXCAN1_RX | GPIO7[3] | SD Card Detect – connected to a GPIO |
| 96 | 3V3 | SD2_D[0] | SD2_DAT0 | SD2_DATA0<br>AUD4_RXD | GPIO1[15] | SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable |

| PIN | Type | Function | i.MX6 Dual Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 Dual manuals for details) |
|---|---|---|---|---|---|---|
| | | | | KEY_ROW7 / DCIC2_OUT | | register, a 50 K–69 K external pull up resistor must be added. |
| 97 | 3V3 | SD2_D[1] | SD2_DAT1 | SD2_DATA1<br>EIM_CS2<br>AUD4_TXFS / KEY_COL7 | GPIO1[14] | |
| 98 | 3V3 | SD2_D[2] | SD2_DAT2 | SD2_DATA2<br>EIM_CS3<br>AUD4_TXD<br>KEY_ROW6 | GPIO1[13] | |
| 99 | 3V3 | SD2_D[3] | SD2_DAT3 | SD2_DATA3<br>KEY_COL6<br>AUD4_TXC | GPIO1[12] | |
| 100 | 3V3 | SD2_CMD | SD2_CMD | SD2_CMD<br>KEY_ROW5<br>AUD4_RXC | GPIO1[11] | SD Command bidirectional signal |
| 101 | 3V3 | SD2_CLK | SD2_CLK | SD2_CLK<br>KEY_COL5<br>AUD4_RXFS | GPIO1[10] | SD Output Clock. |
| 102 | GND | GND | | | | |
| **CMOS Sensor Interface** | | | | | | |
| 103 | 3V3 | CSI0_DAT12 | CSI0_DAT12 | IPU1_CSI0_DATA12<br>EIM_DATA08<br>UART4_TX_DATA<br>ARM_TRACE09 | GPIO5[30] | |
| 104 | 3V3 | CSI0_DAT13 | CSI0_DAT13 | IPU1_CSI0_DATA13<br>EIM_DATA09<br>UART4_RX_DATA<br>ARM_TRACE10 | GPIO5[31] | |
| 105 | 3V3 | CSI0_DAT14 | CSI0_DAT14 | IPU1_CSI0_DATA14<br>EIM_DATA10<br>UART5_TX_DATA<br>ARM_TRACE11 | GPIO6[0] | |
| 106 | 3V3 | CSI0_DAT15 | CSI0_DAT15 | IPU1_CSI0_DATA15<br>EIM_DATA11<br>UART5_RX_DATA<br>ARM_TRACE12 | GPIO6[1] | |
| 107 | 3V3 | CSI0_DAT16 | CSI0_DAT16 | IPU1_CSI0_DATA16<br>EIM_DATA12<br>UART4_RTS_B<br>ARM_TRACE13 | GPIO6[2] | |
| 108 | 3V3 | CSI0_DAT17 | CSI0_DAT17 | IPU1_CSI0_DATA17<br>EIM_DATA13<br>UART4_CTS_B<br>ARM_TRACE14 | GPIO6[3] | |
| 109 | 3V3 | CSI0_DAT18 | CSI0_DAT18 | IPU1_CSI0_DATA18<br>EIM_DATA14<br>UART5_RTS_B<br>ARM_TRACE15 | GPIO6[4] | |
| 110 | 3V3 | CSI0_DAT19 | CSI0_DAT19 | IPU1_CSI0_DATA19<br>EIM_DATA15<br>UART5_CTS_B | GPIO6[5] | |
| 111 | GND | GND | | | | |
| 112 | 3V3 | CSI0_HSYNC | CSI0_MCLK | IPU1_CSI0_HSYNC<br>CCM_CLKO1<br>ARM_TRACE_CTL | GPIO5[19] | |
| 113 | 3V3 | CSI0_VSYNC | CSI0_VSYNC | IPU1_CSI0_VSYNC<br>EIM_DATA01<br>ARM_TRACE00 | GPIO5[21] | |
| 114 | 3V3 | CSI0_PIXCLK | CSI0_PIXCLK | IPU1_CSI0_PIXCLK<br>ARM_EVENTO | GPIO5[18] | |
| 115 | 3V3 | CSI0_MCLK | GPIO_0 | CCM_CLKO1<br>KEY_COL5<br>ASRC_EXT_CLK<br>EPIT1_OUT<br>USB_H1_PWR<br>SNVS_VIO_5 | GPIO1[0] | |
| 116 | GND | GND | | | | |
| **LCD Controller and Smart LCD Controller** | | | | | | |
| 117 | 3V3 | LD0 | **DISP0_DAT0** | IPU1_DISP0_DATA00<br>LCD_DATA00<br>ECSPI3_SCLK | GPIO4[21] | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS1_TX2_N | not available | | TX6DL LVDS version: LVDS display output port 1 |
| 118 | 3V3 | LD1 | **DISP0_DAT1** | IPU1_DISP0_DATA01<br>LCD_DATA01 | GPIO4[22] | TX6DL standard version: LCD Data Bus |

| PIN | Type | Function | i.MX6 Dual Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 Dual manuals for details) |
|---|---|---|---|---|---|---|
| | | | | ECSPI3_MOSI | | |
| | LVDS | | LVDS1_TX1_N | not available | | TX6DL LVDS version: LVDS display output port 1 |
| 119 | 3V3 | LD2 | **DISP0_DAT2** | IPU1_DISP0_DATA02<br>LCD_DATA02<br>ECSPI3_MISO | GPIO4[23] | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS1_TX2_P | not available | | TX6DL LVDS version: LVDS display output port 1 |
| 120 | 3V3 | LD3 | **DISP0_DAT3** | IPU1_DISP0_DATA03<br>LCD_DATA03<br>ECSPI3_SS0 | GPIO4[24] | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS1_TX1_P | not available | | TX6DL LVDS version: LVDS display output port 1 |
| 121 | 3V3 | LD4 | **DISP0_DAT4** | IPU1_DISP0_DATA04<br>LCD_DATA04<br>ECSPI3_SS1 | GPIO4[25] | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS1_TX3_N | not available | | TX6DL LVDS version: LVDS display output port 1 |
| 122 | 3V3 | LD5 | **DISP0_DAT5** | IPU1_DISP0_DATA05<br>LCD_DATA05<br>ECSPI3_SS2<br>AUD6_RXFS | GPIO4[26] | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS1_TX0_N | not available | | TX6DL LVDS version: LVDS display output port 1 |
| 123 | 3V3 | LD6 | **DISP0_DAT6** | IPU1_DISP0_DATA06<br>LCD_DATA06<br>ECSPI3_SS3<br>AUD6_RXC | GPIO4[27] | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS1_TX3_P | not available | | TX6DL LVDS version: LVDS display output port 1 |
| 124 | 3V3 | LD7 | **DISP0_DAT7** | IPU1_DISP0_DATA07<br>LCD_DATA07<br>ECSPI3_RDY | GPIO4[28] | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS1_TX0_P | not available | | TX6DL LVDS version: LVDS display output port 1 |
| 125 | 3V3 | LD8 | **DISP0_DAT8** | IPU1_DISP0_DATA08<br>LCD_DATA08<br>PWM1_OUT<br>WDOG1_B | GPIO4[29] | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS1_CLK_N | not available | | TX6DL LVDS version: LVDS display output port 1 |
| 126 | 3V3 | LD9 | **DISP0_DAT9** | IPU1_DISP0_DATA09<br>LCD_DATA09<br>PWM2_OUT<br>WDOG2_B | GPIO4[30] | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS0_TX3_P | not available | | TX6DL LVDS version: LVDS display output port 0 |
| 127 | 3V3 | LD10 | **DISP0_DAT10** | IPU1_DISP0_DATA10<br>LCD_DATA10 | GPIO4[31] | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS1_CLK_P | not available | | TX6DL LVDS version: LVDS display output port 1 |
| 128 | 3V3 | LD11 | **DISP0_DAT11** | IPU1_DISP0_DATA11<br>LCD_DATA11 | GPIO5[5] | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS0_TX3_N | not available | | TX6DL LVDS version: LVDS display output port 0 |
| 129 | GND | GND | | | | |
| 130 | 3V3 | LD12 | **DISP0_DAT12** | IPU1_DISP0_DATA12<br>LCD_DATA12 | GPIO5[6] | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS0_CLK_P | not available | | TX6DL LVDS version: LVDS display output port 0 |
| 131 | 3V3 | LD13 | **DISP0_DAT13** | IPU1_DISP0_DATA13<br>LCD_DATA13<br>AUD5_RXFS | GPIO5[7] | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS0_TX2_P | not available | | TX6DL LVDS version: LVDS display output port 0 |
| 132 | 3V3 | LD14 | **DISP0_DAT14** | IPU1_DISP0_DATA14<br>LCD_DATA14<br>AUD5_RXC | GPIO5[8] | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS0_CLK_N | not available | | TX6DL LVDS version: LVDS display output port 0 |
| 133 | 3V3 | LD15 | **DISP0_DAT15** | IPU1_DISP0_DATA15<br>LCD_DATA15<br>ECSPI1_SS1<br>ECSPI2_SS1 | GPIO5[9] | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS0_TX2_N | not available | | TX6DL LVDS version: LVDS display output port 0 |
| 134 | 3V3 | LD16 | **DISP0_DAT16** | IPU1_DISP0_DATA16 | GPIO5[10] | |

| PIN | Type | Function | i.MX6 Dual Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 Dual manuals for details) |
|---|---|---|---|---|---|---|
| | | | | LCD_DATA16<br>ECSPI2_MOSI<br>AUD5_TXC<br>SDMA_EXT_EVENT0 | | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS0_TX1_P | not available | | TX6DL LVDS version: LVDS display output port 0 |
| 135 | 3V3 | LD17 | **DISP0_DAT17** | IPU1_DISP0_DATA17<br>LCD_DATA17<br>ECSPI2_MISO<br>AUD5_TXD<br>SDMA_EXT_EVENT1 | GPIO5[11] | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS0_TX0_P | not available | | TX6DL LVDS version: LVDS display output port 0 |
| 136 | 3V3 | LD18 | **DISP0_DAT18** | IPU1_DISP0_DATA18<br>LCD_DATA18<br>ECSPI2_SS0<br>AUD5_TXFS / AUD4_RXFS<br>EIM_CS2 | GPIO5[12] | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS0_TX1_N | not available | | TX6DL LVDS version: LVDS display output port 0 |
| 137 | 3V3 | LD19 | **DISP0_DAT19** | IPU1_DISP0_DATA19<br>LCD_DATA19<br>ECSPI2_SCLK<br>AUD5_RXD / AUD4_RXC<br>EIM_CS3 | GPIO5[13] | TX6DL standard version: LCD Data Bus |
| | LVDS | | LVDS0_TX0_N | not available | | TX6DL LVDS version: LVDS display output port 0 |
| 138 | 3V3 | LD20 | **DISP0_DAT20** | IPU1_DISP0_DATA20<br>LCD_DATA20<br>ECSPI1_SCLK<br>AUD4_TXC | GPIO5[14] | TX6DL standard version: LCD Data Bus |
| | SATA | | | not available | | TX6DL LVDS version: not available |
| 139 | 3V3 | LD21 | **DISP0_DAT21** | IPU1_DISP0_DATA21<br>LCD_DATA21<br>ECSPI1_MOSI<br>AUD4_TXD | GPIO5[15] | TX6DL standard version: LCD Data Bus |
| | SATA | | | not available | | TX6DL LVDS version: not available |
| 140 | 3V3 | LD22 | **DISP0_DAT22** | IPU1_DISP0_DATA22<br>LCD_DATA22<br>ECSPI1_MISO<br>AUD4_TXFS | GPIO5[16] | TX6DL standard version: LCD Data Bus |
| | SATA | | | not available | | TX6DL LVDS version: not available |
| 141 | 3V3 | LD23 | **DISP0_DAT23** | IPU1_DISP0_DATA23<br>LCD_DATA23<br>ECSPI1_SS0<br>AUD4_RXD | GPIO5[17] | TX6DL standard version: LCD Data Bus |
| | SATA | | | not available | | TX6DL LVDS version: not available |
| 142 | GND | GND | | | | |
| 143 | 3V3 | HSYNC | DI0_PIN2 | IPU1_DI0_PIN02<br>LCD_HSYNC<br>AUD6_TXD / LCD_RS | GPIO4[18] | |
| 144 | 3V3 | VSYNC | DI0_PIN3 | IPU1_DI0_PIN03<br>LCD_VSYNC<br>AUD6_TXFS<br>LCD_CS | GPIO4[19] | |
| 145 | 3V3 | OE_ACD | DI0_PIN15 | IPU1_DI0_PIN15<br>LCD_ENABLE<br>AUD6_TXC<br>LCD_RD_E | GPIO4[17] | |
| 146 | 3V3 | LSCLK | DI0_DISP_CLK | IPU1_DI0_DISP_CLK<br>LCD_CLK<br>LCD_WR_RWN | GPIO4[16] | |
| 147 | GND | GND | | | | |
| **Module Specific Signals** | | | | | | |
| 148 | 3V3 | CSI1_MCLK | NANDF_CS2 | NAND_CE2_B<br>IPU1_SISG0<br>ESAI_TX0<br>EIM_CRE<br>CCM_CLKO2 | GPIO6[15] | |
| 149 | 3V3 | CSI1_PIXCLK | EIM_A16 | EIM_ADDR16<br>IPU1_DI1_DISP_CLK<br>IPU1_CSI1_PIXCLK<br>SRC_BOOT_CFG16<br>EPDC_DATA00 | GPIO2[22] | |
| 150 | 3V3 | CSI1_VSYNC | EIM_D29 | EIM_DATA29 | GPIO3[29] | |

| PIN | Type | Function | i.MX6 Dual Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 Dual manuals for details) |
|---|---|---|---|---|---|---|
| | | | | IPU1_DI1_PIN15<br>ECSPI4_SS0<br>UART2_RTS_B<br>IPU1_CSI1_VSYNC<br>IPU1_DI0_PIN14<br>EPDC_PWR_WAKE | | |
| 151 | 3V3 | CSI1_HSYNC | EIM_EB3 | EIM_EB3<br>ECSPI4_RDY<br>UART3_RTS_B<br>UART1_RI_B<br>IPU1_CSI1_HSYNC<br>IPU1_DI1_PIN03<br>SRC_BOOT_CFG31<br>EPDC_SDCE0<br>EIM_ACLK_FREERUN | GPIO2[31] | |
| 152 | 3V3 | CSI1_D[12] | EIM_A17 | EIM_ADDR17<br>IPU1_DISP1_DATA12<br>IPU1_CSI1_DATA12<br>SRC_BOOT_CFG17<br>EPDC_PWR_STAT | GPIO2[21] | |
| 153 | 3V3 | CSI1_D[13] | EIM_A18 | EIM_ADDR18<br>IPU1_DISP1_DATA13<br>IPU1_CSI1_DATA13<br>SRC_BOOT_CFG18<br>EPDC_PWR_CTRL0 | GPIO2[20] | |
| 154 | 3V3 | CSI1_D[14] | EIM_A19 | EIM_ADDR19<br>IPU1_DISP1_DATA14<br>IPU1_CSI1_DATA14<br>SRC_BOOT_CFG19<br>EPDC_PWR_CTRL1 | GPIO2[19] | |
| 155 | 3V3 | CSI1_D[15] | EIM_A20 | EIM_ADDR20<br>IPU1_DISP1_DATA15<br>IPU1_CSI1_DATA15<br>SRC_BOOT_CFG20<br>EPDC_PWR_CTRL2 | GPIO2[18] | |
| 156 | 3V3 | CSI1_D[16] | EIM_A21 | EIM_ADDR21<br>IPU1_DISP1_DATA16<br>IPU1_CSI1_DATA16<br>SRC_BOOT_CFG21<br>EPDC_GDCLK | GPIO2[17] | |
| 157 | 3V3 | CSI1_D[17] | EIM_A22 | EIM_ADDR22<br>IPU1_DISP1_DATA17<br>IPU1_CSI1_DATA17<br>SRC_BOOT_CFG22<br>EPDC_GDSP | GPIO2[16] | |
| 158 | 3V3 | CSI1_D[18] | EIM_A23 | EIM_ADDR23<br>IPU1_DISP1_DATA18<br>IPU1_CSI1_DATA18<br>IPU1_SISG3<br>SRC_BOOT_CFG23<br>EPDC_GDOE | GPIO6[6] | |
| 159 | 3V3 | CSI1_D[19] | EIM_A24 | EIM_ADDR24<br>IPU1_DISP1_DATA19<br>IPU1_CSI1_DATA19<br>IPU1_SISG2<br>SRC_BOOT_CFG24<br>EPDC_GDRL | GPIO5[4] | |
| 160 | GND | GND | | | | |
| 161 | 3V3 | | CSI0_DAT8 | IPU1_CSI0_DATA08<br>EIM_DATA06<br>ECSPI2_SCLK<br>KEY_COL7<br>I2C1_SDA<br>ARM_TRACE05 | GPIO5[26] | |
| 162 | 3V3 | | CSI0_DAT9 | IPU1_CSI0_DATA09<br>EIM_DATA07<br>ECSPI2_MOSI<br>KEY_ROW7<br>I2C1_SCL<br>ARM_TRACE06 | GPIO5[27] | |
| 163 | 3V3 | | CSI0_DAT10 | IPU1_CSI0_DATA10<br>AUD3_RXC<br>ECSPI2_MISO<br>UART1_TX_DATA<br>ARM_TRACE07 | GPIO5[28] | |
| 164 | 3V3 | | CSI0_DAT11 | IPU1_CSI0_DATA11<br>AUD3_RXFS<br>ECSPI2_SS0<br>UART1_RX_DATA<br>ARM_TRACE08 | GPIO5[29] | |

| PIN | Type | Function | i.MX6 Dual Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 Dual manuals for details) |
|---|---|---|---|---|---|---|
| 165 | 3V3 | | EIM_D22 | EIM_DATA22<br>ECSPI4_MISO<br>IPU1_DI0_PIN01<br>IPU1_CSI1_DATA10<br>USB_OTG_PWR<br>SPDIF_OUT<br>EPDC_SDCE6 | GPIO3[22] | |
| 166 | LVDS | | CLK1_N | | | Alternate reference clock for PCIe |
| 167 | LVDS | | PCIE_RXM | | | |
| 168 | LVDS | | CLK1_P | | | Alternate reference clock for PCIe |
| 169 | LVDS | | PCIE_RXP | | | |
| 170 | LVDS | | PCIE_TXM | | | |
| 171 | GND | GND | | | | |
| 172 | LVDS | | PCIE_TXP | | | |
| 173 | 3V3 | EIM_CS0 | EIM_CS0 | EIM_CS0<br>IPU1_DI1_PIN05<br>ECSPI2_SCLK<br>EPDC_DATA06 | GPIO2[23] | |
| 174 | 3V3 | EIM_CS1 | EIM_CS1 | EIM_CS1<br>IPU1_DI1_PIN06<br>ECSPI2_MOSI<br>EPDC_DATA08 | GPIO2[24] | |
| 175 | 3V3 | GPIO | CSI0_DATA_EN | IPU1_CSI0_DATA_EN<br>EIM_DATA00<br>ARM_TRACE_CLK | GPIO5[20] | |
| 176 | 3V3 | EIM_WAIT | EIM_WAIT | EIM_WAIT<br>EIM_DTACK_B<br>SRC_BOOT_CFG25 | GPIO5[0] | |
| 177 | 3V3 | EIM_EB0 | EIM_EB0 | EIM_EB0<br>IPU1_DISP1_DATA11<br>IPU1_CSI1_DATA11<br>CCM_PMIC_READY<br>SRC_BOOT_CFG27<br>EPDC_PWR_COM | GPIO2[28] | |
| 178 | 3V3 | EIM_EB1 | EIM_EB1 | EIM_EB1<br>IPU1_DISP1_DATA10<br>IPU1_CSI1_DATA10<br>SRC_BOOT_CFG28<br>EPDC_SDSHR | GPIO2[29] | |
| 179 | 3V3 | EIM_OE | EIM_OE | EIM_OE<br>IPU1_DI1_PIN07<br>ECSPI2_MISO<br>EPDC_PWR_IRQ | GPIO2[25] | |
| 180 | 3V3 | EIM_LBA | EIM_LBA | EIM_LBA<br>IPU1_DI1_PIN17<br>ECSPI2_SS1<br>SRC_BOOT_CFG26<br>EPDC_DATA04 | GPIO2[27] | |
| 181 | 3V3 | EIM_RW | EIM_RW | EIM_RW<br>IPU1_DI1_PIN08<br>ECSPI2_SS0<br>SRC_BOOT_CFG29<br>EPDC_DATA07 | GPIO2[26] | |
| 182 | 3V3 | EIM_BCLK | EIM_BCLK | EIM_BCLK<br>IPU1_DI1_PIN16<br>EPDC_SDCE9 | GPIO6[31] | |
| 183 | GND | GND | | | | |
| 184 | 3V3 | EIM_DA0 | EIM_DA0 | EIM_AD00<br>IPU1_DISP1_DATA09<br>IPU1_CSI1_DATA09<br>SRC_BOOT_CFG00<br>EPDC_SDCLK_N | GPIO3[0] | |
| 185 | 3V3 | EIM_DA1 | EIM_DA1 | EIM_AD01<br>IPU1_DISP1_DATA08<br>IPU1_CSI1_DATA08<br>SRC_BOOT_CFG01<br>EPDC_SDLE | GPIO3[1] | |
| 186 | 3V3 | EIM_DA2 | EIM_DA2 | EIM_AD02<br>IPU1_DISP1_DATA07<br>IPU1_CSI1_DATA07<br>SRC_BOOT_CFG02<br>EPDC_BDR0 | GPIO3[2] | |
| 187 | 3V3 | EIM_DA3 | EIM_DA3 | EIM_AD03<br>IPU1_DISP1_DATA06 | GPIO3[3] | |