TX6DL

TX Family Computer On Module

- Processor — Dual ARM® Cortex®-A9 based NXP i.MX6 DualLite, 800MHz
- RAM — 1GB DDR3 SDRAM
- ROM — 128MB SLC NAND Flash / 4GB eMMC
- Power supply — Single 3.1V to 5.5V
- Size — 31mm SO-DIMM
- Grade — Industrial
- Temperature — (-40°C/-25°C to 105°C Tj)

Key Features

- ARM® Cortex®-A9
- Display support:
  - Full HD LCD controller, 24bpp (Standard version)
  - OpenGL ES 2.0 hardware accelerator
  - Multi-format HD 1080p60 video decoder and 1080p30 encoder hardware engine
  - Dual LVDS display interface (LVDS version)

Connectivity

- 10/100Mbps Ethernet
- Two High Speed USB 2.0 ports
- Two Camera Interfaces
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - dual, single-precision floating point execute pipeline
- Unified 1MB L2 cache
- Several interfaces:
  3x UART, 2x SDIO, 2x SSI/AC97/I2S,
  I2C, CSPI, Keypad, Ext. Memory I/F
- 3.3V I/O
- 2x Controller Area Network (FlexCAN)
- PCIe 2.0 (1-lane)

OS Support

- Windows Embedded Compact 7
- Windows Embedded Compact 2013
- Linux
- Android by kernel concepts — www.kernelconcepts.de
- QNX by SITRE — www.sitre.fr

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Board highlights:

- Highly integrated
- Standard TX-DIMM pinout
- as small as possible - only 31mm
- 3.3V I/O

The TX6 is a member of the TXCOM module series, specially designed for i.MX multimedia processors. TXCOM modules are complete computers, implemented on a board smaller than a credit card, and ready to be designed into your embedded system. TXCOM modules includes an i.MX processor, SDRAM and Flash memory. The integrated LCD-controller enables direct connection of an LCD screen. The TX6 is specifically targeted at embedded applications where size, high cpu-performance and cost are critical factors.

Computer on module

- NXP i.MX6 DualLite, 800 MHz
- 1GByte (64bit) SDRAM DDR3-800
- 128 Mbyte NAND Flash memory
- TXCOM DIMM200-module (67,6mm x 31 mm x 4mm)
- Operating temperature ranges (Processor junction temperature)
  Extended Consumer Grade: -20°C ..105°C
  Industrial Grade: -40°C (eMMC: -25°C) ..105°C
  Automotive Grade: -40°C ..125°C, AEC-Q100 Grade 3

Processor

The i.MX 6Dual Lite processors represent NXP Semiconductors' latest achievement in integrated multimedia applications processors. These processors are part of a growing family of multimedia-focused products that offer high performance processing and are optimized for lowest power consumption. The i.MX 6Dual Lite processors feature NXP's advanced implementation of the dual ARM Cortex™-A9 core, which operates at speeds up to 1 GHz. They include 2D and 3D graphics processors, 3D 1080p video processing, and integrated power management. Each processor provides a 64-bit DDR3/LVDDR3/LPDDR2-800 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

High Performance CPU : Dual ARM® Cortex®-A9

- Dual ARM® Cortex®-A9, with ARMv7™, Neon, VFPv3 and Trustzone support
- 32K instruction and data L1 caches and 256 KB to 1 MB of L2 cache
- Multi-stream-capable HD video engine delivering 1080p60 decode, 1080p30 encode and 3D video playback in HD in high performance families
- Superior 3D graphics performance with a shader performing up to 50 MT/s. Separate 2D and/or Vertex acceleration engines for an optimal user interface experience
- Stereoscopic image sensor support for 3D imaging

Standard TXCOM pinout:

- 4-wire UARTs (x3)
- LCD
- I2C / PWM
- Serial Audio Interfaces (x2)
- 4-wire SD-Card/SDIO

High-Speed communication interfaces incl. onboard Ethernet PHY / on-chip USB PHY allows direct use of connectors/magnetics on the baseboard without the need for additional logic:

- 10/100 Mbps Ethernet
- 480 Mbps USB OTG (Host or Device)
- 480 Mbps USB Host

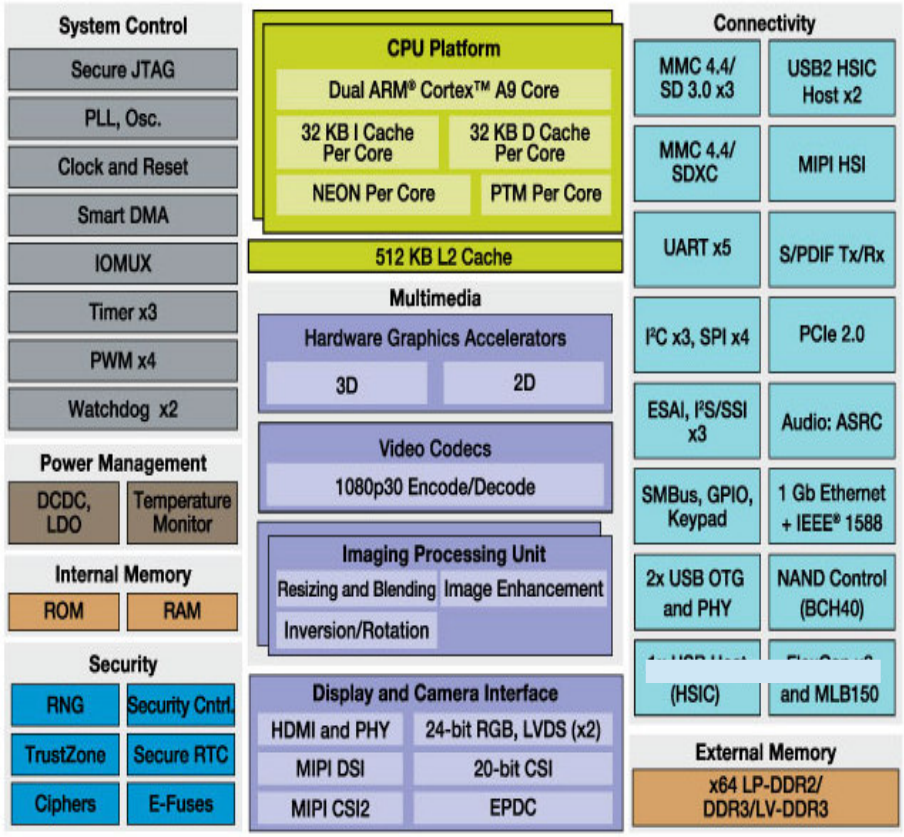
Power Supply

The TX6 accepts an input voltage from various sources:

- 1-cell Li-Ion/Polymer (up to 4.2V)
- 5.0V USB supply or AC wall adapter
- 3.3V

Read more in our TX-Guide:

www.karo-electronics.com/TX-Guide



Ordering Information

Order Number	CPU	SDRAM	Flash	RTC	Temp. Grade
TX6DL/800/1024S/128F/I TX6DL/800/1024S/128F/LVDS/I	800MHz MCIMX6U7 Dual Core Industrial	1GB	128MB	DS1339	industrial -40°C..85°C
TX6DL/800/1024S/4GF/E85 TX6DL/800/1024S/4GF/LVDS/E85	800MHz MCIMX6U7 Dual Core Industrial	1GB	4GB	i.MX6	industrial -25°C..85°C

2019-02-06

PINOUT

PIN	Type	Function	i.MX6 Dual Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
POWER SUPPLY & RESET						
1-4	power	VIN				Module power supply input (3.3V-5V, observe DIMM socket contact current rating)
5-7, 9-12	power	VOUT				3.3V power supply output. Supplied by RN5T567 LDO2 (max. 300mA)
8	3V3	BOOTMODE			10K-PU	Boot mode select H: Boot from NAND / L: Boot from UART/USB
13	power	VBACKUP	Version with DS1339 RTC			
						DS1339 RTC backup power supply. Supply voltage must be held between 1.3V and 3.7V for proper RTC operation. This pin can be connected to a primary cell such as a lithium button cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used with the trickle charge feature.
			Version without DS1339 RTC			
			Connected through a 240 Ohms resistor to VDD_SNVS_IN			i.MX6 SNVS backup power supply. Supply voltage must be held between 2.9V and 3.3V if the system requires keeping real time and other data on OFF state. This pin is connected to RN5T567 LDORTC1 (3V/30mA) through an onboard 240R resistor. Leave unconnected if the system does not require keeping real time and other data on OFF state.
14	VIN	PMIC_PWR_BTN				Connected to RN5T567 PWRON, 10K-PU connected to VIN Leave unconnected, if not used.
15	3V3	#RESET_OUT	GPIO_17	ESAI_TX0 ENET_1588_EVENT3_IN CCM_PMIC_READY SDMA_EXT_EVENT0 SPDIF_OUT	GPIO7[12]	#RESET_OUT may be used to reset peripherals on the carrier board. This signal can be controlled by a GPIO function during runtime.
16		#POR	POR_B		10K-PU	Power On Reset — Active low input signal Leave unconnected, if not used.
17		#RESET_IN	POR_B			Wire ored to pin 16
18	GND	GND				
Ethernet						
19	analog	ETN_TXN				Transmit Data Negative: 100Base-TX or 10Base-T differential transmit output to magnetics.
20	3V3	#ETN_LED2				Active low - output is driven active when the operating speed is 100Mbps. This LED will go inactive when the operating speed is 10Mbps or during line isolation.
21	analog	ETN_TXP				Transmit Data Positive: 100Base-TX or 10Base-T differential transmit output to magnetics.
22	power	ETN_3V3				+3.3V analog power supply output to magnetics
23	analog	ETN_RXN				Receive Data Negative: 100Base-TX or 10Base-T differential receive input from magnetics.
24	3V3	#ETN_LED1				Active low - output is driven active whenever the device detects a valid link, and blinks indicating activity.
25	analog	ETN_RXP				Receive Data Positive: 100Base-TX or 10Base-T differential receive input from magnetics.
26	GND	GND				
USB-HOST						
27	3V3	USBH_VBUSEN	EIM_D31	EIM_DATA31 IPU1_DISP1_DATA20 IPU1_DI0_PIN12 IPU1_CSI0_DATA02 UART3_RTS_B USB_H1_PWR EPDC_SDCLK_P EIM_ACLK_FREERUN	GPIO3[31]	Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
28	3V3	#USBH_OC	EIM_D30	EIM_DATA30 IPU1_DISP1_DATA21 IPU1_DI0_PIN11 IPU1_CSI0_DATA03 UART3_CTS_B USB_H1_OC EPDC_SDOEZ	GPIO3[30] 10K-PU	Active low over-current indicator input connected to a GPIO.
29	analog	USBH_DM	USB_H1_DN			D- pin of the USB cable
30	analog	USBH_VBUS	USB_H1_VBUS			VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.
31	analog	USBH_DP	USB_H1_DP			D+ pin of the USB cable
32	GND	GND				

PIN	Type	Function	i.MX6 Dual Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
USB-OTG / 2nd CAN						
33	3V3	USBOTG_ID	EIM_D23	EIM_DATA23 IPU1_DI0_D0_CS UART3_CTS_B UART1_DCD_B IPU1_CSI1_DATA_EN IPU1_DI1_PIN02 IPU1_DI1_PIN14 EPDC_DATA11	**GPIO3[23]**	
34	3V3	USBOTG_VBUSEN CAN_TX	GPIO_7	ESAI_TX4_RX1 EPIT1_OUT FLEXCAN1_TX UART2_TX_DATA SPDIF_LOCK USB_OTG_HOST_MODE I2C4_SCL	**GPIO1[7]**	Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
35	analog	USBOTG_DM	USB_OTG_DN			D- pin of the USB cable
36	3V3	#USBOTG_OC CAN_RX	GPIO_8	ESAI_TX5_RX0 XTALOSC_REF_CLK_32K EPIT2_OUT FLEXCAN1_RX UART2_RX_DATA SPDIF_SR_CLK USB_OTG_PWR_CTL_WAKE I2C4_SDA	**GPIO1[8]** 10K-PU	Active low over-current indicator input connected to a GPIO.
37	analog	USBOTG_DP	USB_OTG_DP			D+ pin of the USB cable
38	analog	USBOTG_VBUS	USB_OTG_VBUS			VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.
39	GND	GND				
I2C						
40	3V3	I2C_DATA	GPIO_6	ESAI_TX_CLK I2C3_SDA SD2_LCTL MLB_SIG	GPIO1[6]	I2C Data
41	3V3	I2C_CLK	GPIO_3	ESAI_RX_HF_CLK I2C3_SCL XTALOSC_REF_CLK_24M CCM_CLKO2 USB_H1_OC MLB_CLK	GPIO1[3]	I2C Clock
PWM						
42	3V3	PWM	GPIO_1	ESAI_RX_CLK WDOG2_B KEY_ROW5 USB_OTG_ID PWM2_OUT SD1_CD_B	GPIO1[1]	PWM Output
1-WIRE						
43	3V3	OWDAT	GPIO_18	ESAI_TX1 ENET_RX_CLK SD3_VSELECT SDMA_EXT_EVENT1 ASRC_EXT_CLK SNVS_VIO_5_CTL	GPIO7[13]	1-Wire bus. Requires an external pull-up resistor. The recommended resistor is specified by the generic 1-Wire device used in a given system.
CSPI – Configurable Serial Peripheral Interface						
44	3V3	CSPI_SS	EIM_EB2	EIM_EB2 ECSPI1_SS0 IPU1_CSI1_DATA19 HDMI_TX_DDC_SCL I2C2_SCL SRC_BOOT_CFG30 EPDC_DATA05	GPIO2[30]	Slave Select (Selectable polarity) signal
45	3V3	CSPI_SS	EIM_D19	EIM_DATA19 ECSPI1_SS1 IPU1_DI0_PIN08 IPU1_CSI1_DATA16 UART1_CTS_B EPIT1_OUT EPDC_DATA12	GPIO3[19]	Slave Select (Selectable polarity) signal
46	3V3	CSPI_MOSI	EIM_D18	EIM_DATA18 ECSPI1_MOSI	GPIO3[18]	Master Out/Slave In signal

PIN	Type	Function	i.MX6 Dual Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
				IPU1_DI0_PIN07 IPU1_CSI1_DATA17 IPU1_DI1_D0_CS I2C3_SDA EPDC_VCOM1		
47	3V3	CSPI_MISO	EIM_D17	EIM_DATA17 ECSPI1_MISO IPU1_DI0_PIN06 IPU1_CSI1_PIXCLK DCIC1_OUT I2C3_SCL EPDC_VCOM0	GPIO3[17]	Master In/Slave Out signal
48	3V3	CSPI_SCLK	EIM_D16	EIM_DATA16 ECSPI1_SCLK IPU1_DI0_PIN05 IPU1_CSI1_DATA18 HDMI_TX_DDC_SDA I2C2_SDA EPDC_DATA10	GPIO3[16]	Serial Clock signal
49	3V3	CSPI_RDY	GPIO_19	KEY_COL5 ENET_1588_EVENT0_OUT SPDIF_OUT CCM_CLKO1 ECSPI1_RDY ENET_TX_ER	GPIO4[5]	Serial Data Ready signal
50	GND	GND				
SD – Secure Digital Interface 1						
51	3V3	SD1_CD	SD3_CMD	SD3_CMD UART2_CTS_B FLEXCAN1_TX	**GPIO7[2]**	SD Card Detect – connected to a GPIO
52	3V3	SD1_D[0]	SD1_DAT0	SD1_DATA0 GPT_CAPTURE1	GPIO1[16]	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added.
53	3V3	SD1_D[1]	SD1_DAT1	SD1_DATA1 PWM3_OUT GPT_CAPTURE2	GPIO1[17]	
54	3V3	SD1_D[2]	SD1_DAT2	SD1_DATA2 GPT_COMPARE2 PWM2_OUT WDOG1_B WDOG1_RESET_B_DEB	GPIO1[19]	
55	3V3	SD1_D[3]	SD1_DAT3	SD1_DATA3 GPT_COMPARE3 PWM1_OUT WDOG2_B WDOG2_RESET_B_DEB	GPIO1[21]	
56	3V3	SD1_CMD	SD1_CMD	SD1_CMD PWM4_OUT GPT_COMPARE1	GPIO1[18]	SD Command bidirectional signal
57	3V3	SD1_CLK	SD1_CLK	SD1_CLK GPT_CLKIN	GPIO1[20]	SD Output Clock.
58	GND	GND				
1st UART						
59	3V3	TXD	SD3_DAT7	SD3_DATA7 UART1_TX_DATA	GPIO6[17]	Application UART 1 Transmit Data output signal
60	3V3	RXD	SD3_DAT6	SD3_DATA6 UART1_RX_DATA	GPIO6[18]	Application UART 1 Receive Data input signal
61	3V3	RTS	SD3_DAT1	SD3_DATA1 UART1_RTS_B FLEXCAN2_RX	GPIO7[5]	Application UART 1 Request to Send **input** signal
62	3V3	CTS	SD3_DAT0	SD3_DATA0 UART1_CTS_B FLEXCAN2_TX	GPIO7[4]	Application UART 1 Clear to Send **output** signal
2nd UART						
63	3V3	TXD	SD4_DAT7	SD4_DATA7 UART2_TX_DATA	GPIO2[15]	Application UART 2 Transmit Data output signal
64	3V3	RXD	SD4_DAT4	SD4_DATA4 UART2_RX_DATA	GPIO2[12]	Application UART 2 Receive Data input signal
65	3V3	RTS	SD4_DAT5	SD4_DATA5 UART2_RTS_B	GPIO2[13]	Application UART 2 Request to Send **input** signal
66	3V3	CTS	SD4_DAT6	SD4_DATA6 UART2_CTS_B	GPIO2[14]	Application UART 2 Clear to Send **output** signal
3rd UART						
67	3V3	TXD	EIM_D24	EIM_DATA24 ECSPI4_SS2 UART3_TX_DATA	GPIO3[24]	Application UART 3 Transmit Data output signal

PIN	Type	Function	i.MX6 Dual Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
				ECSPI1_SS2 ECSPI2_SS2 AUD5_RXFS UART1_DTR_B EPDC_SDCE7		
68	3V3	RXD	EIM_D25	EIM_DATA25 ECSPI4_SS3 UART3_RX_DATA ECSPI1_SS3 ECSPI2_SS3 AUD5_RXC UART1_DSR_B EPDC_SDCE8	GPIO3[25]	Application UART 3 Receive Data input signal
69	3V3	RTS	SD3_RST	SD3_RESET UART3_RTS_B	GPIO7[8]	Application UART 3 Request to Send **input** signal
70	3V3	CTS	SD3_DAT3	SD3_DATA3 UART3_CTS_B	GPIO7[7]	Application UART 3 Clear to Send **output** signal
71	GND	GND				
KEYPAD / 1st CAN						
72	3V3	KP_COL[0]	GPIO_9	ESAI_RX_FS WDOG1_B KEY_COL6 CCM_REF_EN_B PWM1_OUT SD1_WP	GPIO1[9]	
73	3V3	KP_COL[1]	GPIO_4	ESAI_TX_HF_CLK KEY_COL7 SD2_CD_B	GPIO1[4]	
74	3V3	KP_COL[2]	KEY_COL2	ECSPI1_SS1 ENET_RX_DATA2 FLEXCAN1_TX KEY_COL2 ENET_MDC USB_H1_PWR_CTL_WAKE	GPIO4[10]	
75	3V3	KP_COL[3]	KEY_COL3	ECSPI1_SS3 ENET_CRS HDMI_TX_DDC_SCL KEY_COL3 I2C2_SCL SPDIF_IN	GPIO4[12]	
76	3V3	TXCAN	KEY_COL4	FLEXCAN2_TX IPU1_SISG4 USB_OTG_OC KEY_COL4 UART5_RTS_B	GPIO4[14]	
77	3V3	KP_ROW[0]	GPIO_2	ESAI_TX_FS KEY_ROW6 SD2_WP MLB_DATA	GPIO1[2]	
78	3V3	KP_ROW[1]	GPIO_5	ESAI_TX2_RX3 KEY_ROW7 CCM_CLKO1 I2C3_SCL ARM_EVENTI	GPIO1[5]	
79	3V3	KP_ROW[2]	KEY_ROW2	ECSPI1_SS2 ENET_TX_DATA2 FLEXCAN1_RX KEY_ROW2 SD2_VSELECT HDMI_TX_CEC_LINE	GPIO4[11]	
80	3V3	KP_ROW[3]	KEY_ROW3	ASRC_EXT_CLK HDMI_TX_DDC_SDA KEY_ROW3 I2C2_SDA SD1_VSELECT	GPIO4[13]	
81	3V3	RXCAN	KEY_ROW4	FLEXCAN2_RX IPU1_SISG5 USB_OTG_PWR KEY_ROW4 UART5_CTS_B	GPIO4[15]	
82	GND	GND				
SSI 1 - Serial Audio Port 1						
83	3V3	SSI1_INT	EIM_D26	EIM_DATA26 IPU1_DI1_PIN11 IPU1_CSI0_DATA01 IPU1_CSI1_DATA14 UART2_TX_DATA	**GPIO3[26]**	GPIO

PIN	Type	Function	i.MX6 Dual Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
				IPU1_SISG2 IPU1_DISP1_DATA22 EPDC_SDOED		
84	3V3	SSI1_RXD	KEY_ROW1	ECSPI1_SS0 ENET_COL AUD5_RXD KEY_ROW1 UART5_RX_DATA SD2_VSELECT	GPIO4[9]	Serial Audio Interface serial data line 1
85	3V3	SSI1_TXD	KEY_ROW0	ECSPI1_MOSI ENET_TX_DATA3 AUD5_TXD KEY_ROW0 UART4_RX_DATA DCIC2_OUT	GPIO4[7]	Serial Audio Interface serial data line 0
86	3V3	SSI1_CLK	KEY_COL0	ECSPI1_SCLK ENET_RX_DATA3 AUD5_TXC KEY_COL0 UART4_TX_DATA DCIC1_OUT	GPIO4[6]	Serial Audio Interface serial bit clock
87	3V3	SSI1_FS	KEY_COL1	ECSPI1_MISO ENET_MDIO AUD5_TXFS KEY_COL1 UART5_TX_DATA SD1_VSELECT	GPIO4[8]	Serial Audio Interface left/right clock
88	GND	GND				
SSI 2 - Serial Audio Port 2						
89	3V3	SSI2_INT	EIM_D27	EIM_DATA27 IPU1_DI1_PIN13 IPU1_CSI0_DATA00 IPU1_CSI1_DATA13 UART2_RX_DATA IPU1_SISG3 IPU1_DISP1_DATA23 EPDC_SDOE	**GPIO3[27]**	GPIO
90	3V3	SSI2_RXD	CSI0_DAT7	IPU1_CSI0_DATA07 EIM_DATA05 ECSPI1_SS0 KEY_ROW6 AUD3_RXD ARM_TRACE04	GPIO5[25]	Serial Audio Interface serial data line 1
91	3V3	SSI2_TXD	CSI0_DAT5	IPU1_CSI0_DATA05 EIM_DATA03 ECSPI1_MOSI KEY_ROW5 AUD3_TXD ARM_TRACE02	GPIO5[23]	Serial Audio Interface serial data line 0
92	3V3	SSI2_CLK	CSI0_DAT4	IPU1_CSI0_DATA04 EIM_DATA02 ECSPI1_SCLK KEY_COL5 AUD3_TXC ARM_TRACE01	GPIO5[22]	Serial Audio Interface serial bit clock
93	3V3	SSI2_FS	CSI0_DAT6	IPU1_CSI0_DATA06 EIM_DATA04 ECSPI1_MISO KEY_COL6 AUD3_TXFS ARM_TRACE03	GPIO5[24]	Serial Audio Interface left/right clock
94	GND	GND				
Secure Digital Interface 2						
95	3V3	SD2_CD	SD3_CLK	SD3_CLK UART2_RTS_B FLEXCAN1_RX	GPIO7[3]	SD Card Detect – connected to a GPIO
96	3V3	SD2_D[0]	SD2_DAT0	SD2_DATA0 AUD4_RXD	GPIO1[15]	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable

PIN	Type	Function	i.MX6 Dual Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
				KEY_ROW7 / DCIC2_OUT		register, a 50 K–69 K external pull up resistor must be added.
97	3V3	SD2_D[1]	SD2_DAT1	SD2_DATA1 EIM_CS2 AUD4_TXFS / KEY_COL7	GPIO1[14]	
98	3V3	SD2_D[2]	SD2_DAT2	SD2_DATA2 EIM_CS3 AUD4_TXD KEY_ROW6	GPIO1[13]	
99	3V3	SD2_D[3]	SD2_DAT3	SD2_DATA3 KEY_COL6 AUD4_TXC	GPIO1[12]	
100	3V3	SD2_CMD	SD2_CMD	SD2_CMD KEY_ROW5 AUD4_RXC	GPIO1[11]	SD Command bidirectional signal
101	3V3	SD2_CLK	SD2_CLK	SD2_CLK KEY_COL5 AUD4_RXFS	GPIO1[10]	SD Output Clock.
102	GND	GND				
CMOS Sensor Interface						
103	3V3	CSI0_DAT12	CSI0_DAT12	IPU1_CSI0_DATA12 EIM_DATA08 UART4_TX_DATA ARM_TRACE09	GPIO5[30]	
104	3V3	CSI0_DAT13	CSI0_DAT13	IPU1_CSI0_DATA13 EIM_DATA09 UART4_RX_DATA ARM_TRACE10	GPIO5[31]	
105	3V3	CSI0_DAT14	CSI0_DAT14	IPU1_CSI0_DATA14 EIM_DATA10 UART5_TX_DATA ARM_TRACE11	GPIO6[0]	
106	3V3	CSI0_DAT15	CSI0_DAT15	IPU1_CSI0_DATA15 EIM_DATA11 UART5_RX_DATA ARM_TRACE12	GPIO6[1]	
107	3V3	CSI0_DAT16	CSI0_DAT16	IPU1_CSI0_DATA16 EIM_DATA12 UART4_RTS_B ARM_TRACE13	GPIO6[2]	
108	3V3	CSI0_DAT17	CSI0_DAT17	IPU1_CSI0_DATA17 EIM_DATA13 UART4_CTS_B ARM_TRACE14	GPIO6[3]	
109	3V3	CSI0_DAT18	CSI0_DAT18	IPU1_CSI0_DATA18 EIM_DATA14 UART5_RTS_B ARM_TRACE15	GPIO6[4]	
110	3V3	CSI0_DAT19	CSI0_DAT19	IPU1_CSI0_DATA19 EIM_DATA15 UART5_CTS_B	GPIO6[5]	
111	GND	GND				
112	3V3	CSI0_HSYNC	CSI0_MCLK	IPU1_CSI0_HSYNC CCM_CLKO1 ARM_TRACE_CTL	GPIO5[19]	
113	3V3	CSI0_VSYNC	CSI0_VSYNC	IPU1_CSI0_VSYNC EIM_DATA01 ARM_TRACE00	GPIO5[21]	
114	3V3	CSI0_PIXCLK	CSI0_PIXCLK	IPU1_CSI0_PIXCLK ARM_EVENTO	GPIO5[18]	
115	3V3	CSI0_MCLK	GPIO_0	CCM_CLKO1 KEY_COL5 ASRC_EXT_CLK EPIT1_OUT USB_H1_PWR SNVS_VIO_5	GPIO1[0]	
116	GND	GND				
LCD Controller and Smart LCD Controller						
117	3V3	LD0	**DISP0_DAT0**	IPU1_DISP0_DATA00 LCD_DATA00 ECSPI3_SCLK	GPIO4[21]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_TX2_N	not available		TX6DL LVDS version: LVDS display output port 1
118	3V3	LD1	**DISP0_DAT1**	IPU1_DISP0_DATA01 LCD_DATA01	GPIO4[22]	TX6DL standard version: LCD Data Bus

PIN	Type	Function	i.MX6 Dual Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
				ECSPI3_MOSI		
	LVDS		LVDS1_TX1_N	not available		TX6DL LVDS version: LVDS display output port 1
119	3V3	LD2	**DISP0_DAT2**	IPU1_DISP0_DATA02 LCD_DATA02 ECSPI3_MISO	GPIO4[23]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_TX2_P	not available		TX6DL LVDS version: LVDS display output port 1
120	3V3	LD3	**DISP0_DAT3**	IPU1_DISP0_DATA03 LCD_DATA03 ECSPI3_SS0	GPIO4[24]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_TX1_P	not available		TX6DL LVDS version: LVDS display output port 1
121	3V3	LD4	**DISP0_DAT4**	IPU1_DISP0_DATA04 LCD_DATA04 ECSPI3_SS1	GPIO4[25]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_TX3_N	not available		TX6DL LVDS version: LVDS display output port 1
122	3V3	LD5	**DISP0_DAT5**	IPU1_DISP0_DATA05 LCD_DATA05 ECSPI3_SS2 AUD6_RXFS	GPIO4[26]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_TX0_N	not available		TX6DL LVDS version: LVDS display output port 1
123	3V3	LD6	**DISP0_DAT6**	IPU1_DISP0_DATA06 LCD_DATA06 ECSPI3_SS3 AUD6_RXC	GPIO4[27]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_TX3_P	not available		TX6DL LVDS version: LVDS display output port 1
124	3V3	LD7	**DISP0_DAT7**	IPU1_DISP0_DATA07 LCD_DATA07 ECSPI3_RDY	GPIO4[28]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_TX0_P	not available		TX6DL LVDS version: LVDS display output port 1
125	3V3	LD8	**DISP0_DAT8**	IPU1_DISP0_DATA08 LCD_DATA08 PWM1_OUT WDOG1_B	GPIO4[29]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_CLK_N	not available		TX6DL LVDS version: LVDS display output port 1
126	3V3	LD9	**DISP0_DAT9**	IPU1_DISP0_DATA09 LCD_DATA09 PWM2_OUT WDOG2_B	GPIO4[30]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_TX3_P	not available		TX6DL LVDS version: LVDS display output port 0
127	3V3	LD10	**DISP0_DAT10**	IPU1_DISP0_DATA10 LCD_DATA10	GPIO4[31]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_CLK_P	not available		TX6DL LVDS version: LVDS display output port 1
128	3V3	LD11	**DISP0_DAT11**	IPU1_DISP0_DATA11 LCD_DATA11	GPIO5[5]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_TX3_N	not available		TX6DL LVDS version: LVDS display output port 0
129	GND	GND				
130	3V3	LD12	**DISP0_DAT12**	IPU1_DISP0_DATA12 LCD_DATA12	GPIO5[6]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_CLK_P	not available		TX6DL LVDS version: LVDS display output port 0
131	3V3	LD13	**DISP0_DAT13**	IPU1_DISP0_DATA13 LCD_DATA13 AUD5_RXFS	GPIO5[7]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_TX2_P	not available		TX6DL LVDS version: LVDS display output port 0
132	3V3	LD14	**DISP0_DAT14**	IPU1_DISP0_DATA14 LCD_DATA14 AUD5_RXC	GPIO5[8]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_CLK_N	not available		TX6DL LVDS version: LVDS display output port 0
133	3V3	LD15	**DISP0_DAT15**	IPU1_DISP0_DATA15 LCD_DATA15 ECSPI1_SS1 ECSPI2_SS1	GPIO5[9]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_TX2_N	not available		TX6DL LVDS version: LVDS display output port 0
134	3V3	LD16	**DISP0_DAT16**	IPU1_DISP0_DATA16	GPIO5[10]	

PIN	Type	Function	i.MX6 Dual Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
				LCD_DATA16 ECSPI2_MOSI AUD5_TXC SDMA_EXT_EVENT0		TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_TX1_P	not available		TX6DL LVDS version: LVDS display output port 0
135	3V3	LD17	**DISP0_DAT17**	IPU1_DISP0_DATA17 LCD_DATA17 ECSPI2_MISO AUD5_TXD SDMA_EXT_EVENT1	GPIO5[11]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_TX0_P	not available		TX6DL LVDS version: LVDS display output port 0
136	3V3	LD18	**DISP0_DAT18**	IPU1_DISP0_DATA18 LCD_DATA18 ECSPI2_SS0 AUD5_TXFS / AUD4_RXFS EIM_CS2	GPIO5[12]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_TX1_N	not available		TX6DL LVDS version: LVDS display output port 0
137	3V3	LD19	**DISP0_DAT19**	IPU1_DISP0_DATA19 LCD_DATA19 ECSPI2_SCLK AUD5_RXD / AUD4_RXC EIM_CS3	GPIO5[13]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_TX0_N	not available		TX6DL LVDS version: LVDS display output port 0
138	3V3	LD20	**DISP0_DAT20**	IPU1_DISP0_DATA20 LCD_DATA20 ECSPI1_SCLK AUD4_TXC	GPIO5[14]	TX6DL standard version: LCD Data Bus
	SATA			not available		TX6DL LVDS version: not available
139	3V3	LD21	**DISP0_DAT21**	IPU1_DISP0_DATA21 LCD_DATA21 ECSPI1_MOSI AUD4_TXD	GPIO5[15]	TX6DL standard version: LCD Data Bus
	SATA			not available		TX6DL LVDS version: not available
140	3V3	LD22	**DISP0_DAT22**	IPU1_DISP0_DATA22 LCD_DATA22 ECSPI1_MISO AUD4_TXFS	GPIO5[16]	TX6DL standard version: LCD Data Bus
	SATA			not available		TX6DL LVDS version: not available
141	3V3	LD23	**DISP0_DAT23**	IPU1_DISP0_DATA23 LCD_DATA23 ECSPI1_SS0 AUD4_RXD	GPIO5[17]	TX6DL standard version: LCD Data Bus
	SATA			not available		TX6DL LVDS version: not available
142	GND	GND				
143	3V3	HSYNC	DI0_PIN2	IPU1_DI0_PIN02 LCD_HSYNC AUD6_TXD / LCD_RS	GPIO4[18]	
144	3V3	VSYNC	DI0_PIN3	IPU1_DI0_PIN03 LCD_VSYNC AUD6_TXFS LCD_CS	GPIO4[19]	
145	3V3	OE_ACD	DI0_PIN15	IPU1_DI0_PIN15 LCD_ENABLE AUD6_TXC LCD_RD_E	GPIO4[17]	
146	3V3	LSCLK	DI0_DISP_CLK	IPU1_DI0_DISP_CLK LCD_CLK LCD_WR_RWN	GPIO4[16]	
147	GND	GND				
Module Specific Signals						
148	3V3	CSI1_MCLK	NANDF_CS2	NAND_CE2_B IPU1_SISG0 ESAI_TX0 EIM_CRE CCM_CLKO2	GPIO6[15]	
149	3V3	CSI1_PIXCLK	EIM_A16	EIM_ADDR16 IPU1_DI1_DISP_CLK IPU1_CSI1_PIXCLK SRC_BOOT_CFG16 EPDC_DATA00	GPIO2[22]	
150	3V3	CSI1_VSYNC	EIM_D29	EIM_DATA29	GPIO3[29]	

PIN	Type	Function	i.MX6 Dual Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
				IPU1_DI1_PIN15 ECSPI4_SS0 UART2_RTS_B IPU1_CSI1_VSYNC IPU1_DI0_PIN14 EPDC_PWR_WAKE		
151	3V3	CSI1_HSYNC	EIM_EB3	EIM_EB3 ECSPI4_RDY UART3_RTS_B UART1_RI_B IPU1_CSI1_HSYNC IPU1_DI1_PIN03 SRC_BOOT_CFG31 EPDC_SDCE0 EIM_ACLK_FREERUN	GPIO2[31]	
152	3V3	CSI1_D[12]	EIM_A17	EIM_ADDR17 IPU1_DISP1_DATA12 IPU1_CSI1_DATA12 SRC_BOOT_CFG17 EPDC_PWR_STAT	GPIO2[21]	
153	3V3	CSI1_D[13]	EIM_A18	EIM_ADDR18 IPU1_DISP1_DATA13 IPU1_CSI1_DATA13 SRC_BOOT_CFG18 EPDC_PWR_CTRL0	GPIO2[20]	
154	3V3	CSI1_D[14]	EIM_A19	EIM_ADDR19 IPU1_DISP1_DATA14 IPU1_CSI1_DATA14 SRC_BOOT_CFG19 EPDC_PWR_CTRL1	GPIO2[19]	
155	3V3	CSI1_D[15]	EIM_A20	EIM_ADDR20 IPU1_DISP1_DATA15 IPU1_CSI1_DATA15 SRC_BOOT_CFG20 EPDC_PWR_CTRL2	GPIO2[18]	
156	3V3	CSI1_D[16]	EIM_A21	EIM_ADDR21 IPU1_DISP1_DATA16 IPU1_CSI1_DATA16 SRC_BOOT_CFG21 EPDC_GDCLK	GPIO2[17]	
157	3V3	CSI1_D[17]	EIM_A22	EIM_ADDR22 IPU1_DISP1_DATA17 IPU1_CSI1_DATA17 SRC_BOOT_CFG22 EPDC_GDSP	GPIO2[16]	
158	3V3	CSI1_D[18]	EIM_A23	EIM_ADDR23 IPU1_DISP1_DATA18 IPU1_CSI1_DATA18 IPU1_SISG3 SRC_BOOT_CFG23 EPDC_GDOE	GPIO6[6]	
159	3V3	CSI1_D[19]	EIM_A24	EIM_ADDR24 IPU1_DISP1_DATA19 IPU1_CSI1_DATA19 IPU1_SISG2 SRC_BOOT_CFG24 EPDC_GDRL	GPIO5[4]	
160	GND	GND				
161	3V3		CSI0_DAT8	IPU1_CSI0_DATA08 EIM_DATA06 ECSPI2_SCLK KEY_COL7 I2C1_SDA ARM_TRACE05	GPIO5[26]	
162	3V3		CSI0_DAT9	IPU1_CSI0_DATA09 EIM_DATA07 ECSPI2_MOSI KEY_ROW7 I2C1_SCL ARM_TRACE06	GPIO5[27]	
163	3V3		CSI0_DAT10	IPU1_CSI0_DATA10 AUD3_RXC ECSPI2_MISO UART1_TX_DATA ARM_TRACE07	GPIO5[28]	
164	3V3		CSI0_DAT11	IPU1_CSI0_DATA11 AUD3_RXFS ECSPI2_SS0 UART1_RX_DATA ARM_TRACE08	GPIO5[29]	

PIN	Type	Function	i.MX6 Dual Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
165	3V3		EIM_D22	EIM_DATA22 ECSPI4_MISO IPU1_DI0_PIN01 IPU1_CSI1_DATA10 USB_OTG_PWR SPDIF_OUT EPDC_SDCE6	GPIO3[22]	
166	LVDS		CLK1_N			Alternate reference clock for PCIe
167	LVDS		PCIE_RXM			
168	LVDS		CLK1_P			Alternate reference clock for PCIe
169	LVDS		PCIE_RXP			
170	LVDS		PCIE_TXM			
171	GND	GND				
172	LVDS		PCIE_TXP			
173	3V3	EIM_CS0	EIM_CS0	EIM_CS0 IPU1_DI1_PIN05 ECSPI2_SCLK EPDC_DATA06	GPIO2[23]	
174	3V3	EIM_CS1	EIM_CS1	EIM_CS1 IPU1_DI1_PIN06 ECSPI2_MOSI EPDC_DATA08	GPIO2[24]	
175	3V3	GPIO	CSI0_DATA_EN	IPU1_CSI0_DATA_EN EIM_DATA00 ARM_TRACE_CLK	GPIO5[20]	
176	3V3	EIM_WAIT	EIM_WAIT	EIM_WAIT EIM_DTACK_B SRC_BOOT_CFG25	GPIO5[0]	
177	3V3	EIM_EB0	EIM_EB0	EIM_EB0 IPU1_DISP1_DATA11 IPU1_CSI1_DATA11 CCM_PMIC_READY SRC_BOOT_CFG27 EPDC_PWR_COM	GPIO2[28]	
178	3V3	EIM_EB1	EIM_EB1	EIM_EB1 IPU1_DISP1_DATA10 IPU1_CSI1_DATA10 SRC_BOOT_CFG28 EPDC_SDSHR	GPIO2[29]	
179	3V3	EIM_OE	EIM_OE	EIM_OE IPU1_DI1_PIN07 ECSPI2_MISO EPDC_PWR_IRQ	GPIO2[25]	
180	3V3	EIM_LBA	EIM_LBA	EIM_LBA IPU1_DI1_PIN17 ECSPI2_SS1 SRC_BOOT_CFG26 EPDC_DATA04	GPIO2[27]	
181	3V3	EIM_RW	EIM_RW	EIM_RW IPU1_DI1_PIN08 ECSPI2_SS0 SRC_BOOT_CFG29 EPDC_DATA07	GPIO2[26]	
182	3V3	EIM_BCLK	EIM_BCLK	EIM_BCLK IPU1_DI1_PIN16 EPDC_SDCE9	GPIO6[31]	
183	GND	GND				
184	3V3	EIM_DA0	EIM_DA0	EIM_AD00 IPU1_DISP1_DATA09 IPU1_CSI1_DATA09 SRC_BOOT_CFG00 EPDC_SDCLK_N	GPIO3[0]	
185	3V3	EIM_DA1	EIM_DA1	EIM_AD01 IPU1_DISP1_DATA08 IPU1_CSI1_DATA08 SRC_BOOT_CFG01 EPDC_SDLE	GPIO3[1]	
186	3V3	EIM_DA2	EIM_DA2	EIM_AD02 IPU1_DISP1_DATA07 IPU1_CSI1_DATA07 SRC_BOOT_CFG02 EPDC_BDR0	GPIO3[2]	
187	3V3	EIM_DA3	EIM_DA3	EIM_AD03 IPU1_DISP1_DATA06	GPIO3[3]	