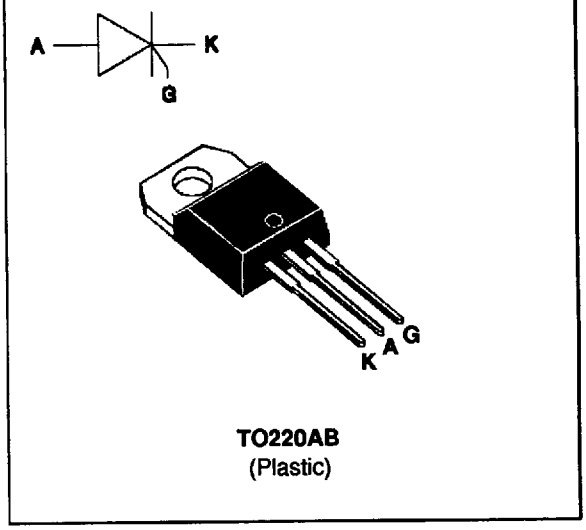
SGS-THOMSON MICROELECTRONICS

TYN 225 ---> TYN 1225

SCR

FEATURES

- HIGH SURGE CAPABILITY
- HIGH ON-STATE CURRENT
- HIGH STABILITY AND RELIABILITY



TO220AB
(Plastic)

DESCRIPTION

The TYN 225 ---> TYN 1025 Family Silicon Controlled Rectifiers are high performance glass passivated chips technology.
This general purpose Family Silicon Controlled Rectifiers is designed for power supply up to 400Hz on resistive or inductive load.

ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
$I_{T(RMS)}$	RMS on-state current (180° conduction angle)	Tc = 95 °C	25	A
$I_{T(AV)}$	Average on-state current (180° conduction angle, single phase circuit)	Tc = 95 °C	16	A
I_{TSM}	Non repetitive surge peak on-state current (Tj initial = 25°C)	tp = 8.3 ms	260	A
		tp = 10 ms	250	
I^2t	I^2t value	tp = 10 ms	310	A^2s
dI/dt	Critical rate of rise of on-state current Gate supply : I_G = 100 mA di_G/dt = 1 A/µs		100	A/µs
Tstg Tj	Storage and operating junction temperature range		- 40 to + 150 - 40 to + 125	°C °C
Tl	Maximum lead temperature for soldering during 10 s at 4.5 mm from case		260	°C

Symbol	Parameter	TYN						Unit
		225	425	625	825	1025	1225	
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Tj = 125 °C	200	400	600	800	1000	1200	V

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
Rth (j-a)	Junction to ambient	60	°C/W
Rth (j-c) DC	Junction to case for DC	1.3	°C/W

GATE CHARACTERISTICS (maximum values)

$P_{G\ (AV)}$ = 1W P_{GM} = 10W (tp = 20 µs) I_{FGM} = 4A (tp = 20 µs) V_{RGM} = 5 V.

ELECTRICAL CHARACTERISTICS

Symbol	Test Conditions			Value	Unit
I_{GT}	V_D=12V (DC) R_L=33Ω	Tj=25°C	MAX	40	mA
V_{GT}	V_D=12V (DC) R_L=33Ω	Tj=25°C	MAX	1.5	V
V_{GD}	V_D=V_{DRM} R_L=3.3kΩ	Tj= 125°C	MIN	0.2	V
tgt	V_D=V_{DRM} I_G = 200mA dI_G/dt = 1.5A/µs	Tj=25°C	TYP	2	µs
I_L	I_G= 1.2 I_{GT}	Tj=25°C	TYP	80	mA
I_H	I_T= 100mA gate open	Tj=25°C	MAX	50	mA
V_{TM}	ITM= 50A tp= 380µs	Tj=25°C	MAX	1.6	V
I_{DRM} I_{RRM}	V_{DRM} Rated V_{RRM} Rated	Tj=25°C	MAX	0.01	mA
		Tj= 125°C		4	
dV/dt	Linear slope up to V_D=67%V_{DRM} gate open	Tj= 125°C	MIN	500	V/µs
tq	V_D=67%V_{DRM} I_{TM}= 50A V_R= 25V dI_{TM}/dt=30 A/µs dV_D/dt= 50V/µs	Tj= 125°C	TYP	70	µs

Fig.1 : Maximum average power dissipation versus average on-state current.

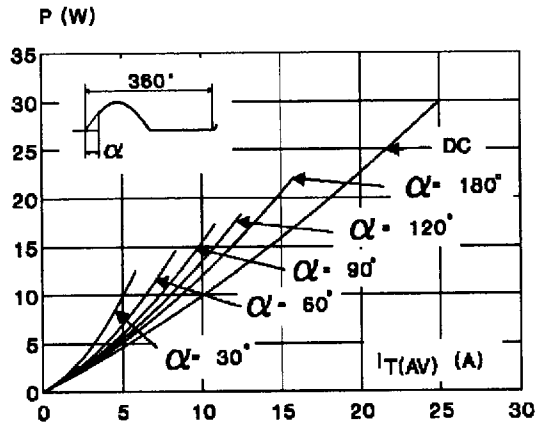


Fig.2 : Correlation between maximum average power dissipation and maximum allowable temperatures (T_{amb} and T_{case}) for different thermal resistances heatsink + contact.

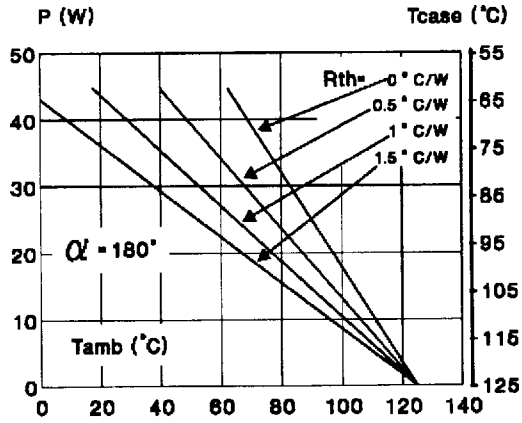


Fig.3 : Average on-state current versus case temperature.

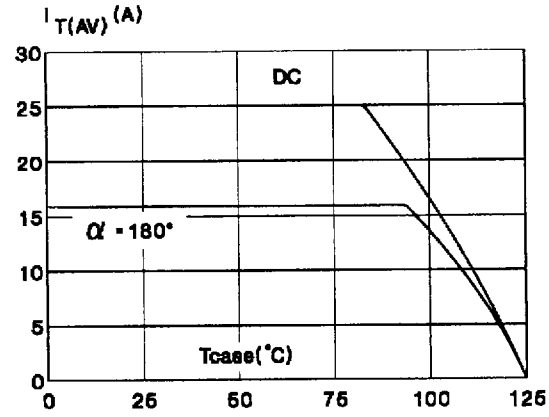


Fig.4 : Relative variation of thermal impedance versus pulse duration.

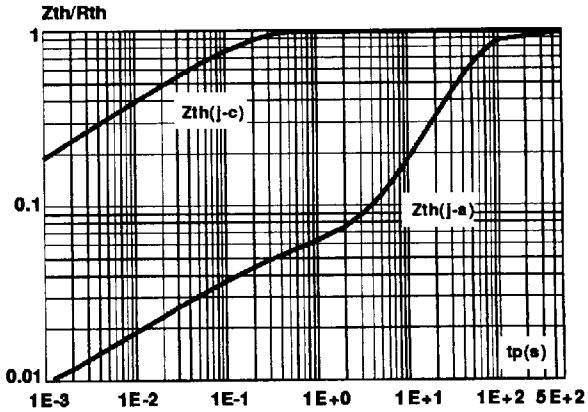


Fig.5 : Relative variation of gate trigger current versus junction temperature.

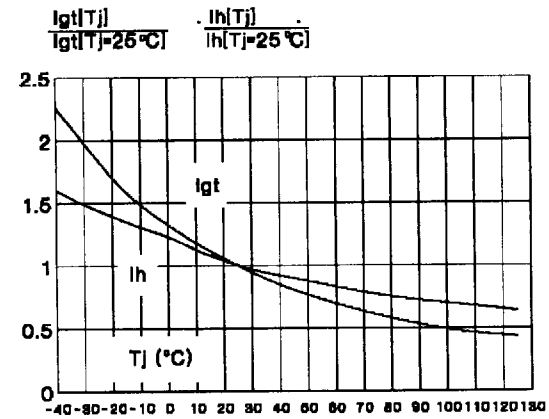


Fig.6 : Non repetitive surge peak on-state current versus number of cycles.