UATM30M2C Datasheet

CENTELLAX

0.04 - 30GHz Broadband MMIC Low-Noise Amplifier

Application

The UATM30M2C Broadband MMIC Low-Noise Amplifier is designed for low-noise and broadband flat-gain applications in RF and microwave communications, test equipment and military systems. By using specific external components, the bandwidth of operation can be extended below 40MHz.

Description

The UATM30M2C is an eight stage traveling wave amplifier. The amplifier has been designed for low noise, flat gain, and good return loss to 30GHz. The amplifier typically has 2.5dB NF and 18dB gain from 6-20GHz, and 16dB gain from 0.04-30GHz.

Features

The UATM30M2C has >30dB dynamic gain control, and includes a temperature-referenced power detector output.

Device Highlights

- Low noise, ultra-flat gain 6-20GHz:
  - 2.5dB NF, 18 ± 0.3dB gain
- Excellent 1.5-20GHz performance:
  - Very flat gain (18 ± 0.6dB)
  - High P_{sat} at 20GHz (20dBm)
  - High P_{-1dB} at 20GHz (17dBm)
- Wideband operation: 0.04-30GHz
- Good input / output return loss
- High isolation
- >30dB dynamic gain control
- Integrated power detector
- 100% DC, RF, and visually tested
- Size: 2390x920um (94.1x36.2mil)

Key Specifications

Vdd=5.0V, Idd=150mA, Zo=50Ω   Specifications pertain to wafer measurements with RF probes and DC bias cards @ 25°C

		6 - 20GHz			1.5 - 20GHz			0.04 - 30GHz		
Parameter	Description	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
S21 (dB)	Small Signal Gain	16.5	18		16.5	18		14.5	16	
Flatness (±dB)	Gain Flatness		0.3	0.6		0.6	1.0		1.5	2.0
S11 (dB)	Input Match		-16	-13		-16	-13		-10	-8
S22 (dB)	Output Match		-18	-15		-18	-15		-18	-15
S12 (dB)	Reverse Isolation		-35	-30		-35	-30		-30	-25
P_{-1dB} (dBm)	1dB Compressed Output Power	16	17		16	17		12	13.5	
P_{sat} (dBm)	Saturated Output Power	19	20		19	20		14	16.5	
P_{out} @16dB (dBm)	Output Power at 16dB Gain	17	18.5		17	18.5				
NF (dB)	Noise Figure		2.5			5			5.5	
RF_{det} (mV/mW)	RF Detector Sensitivity		0.5			0.5			0.5	

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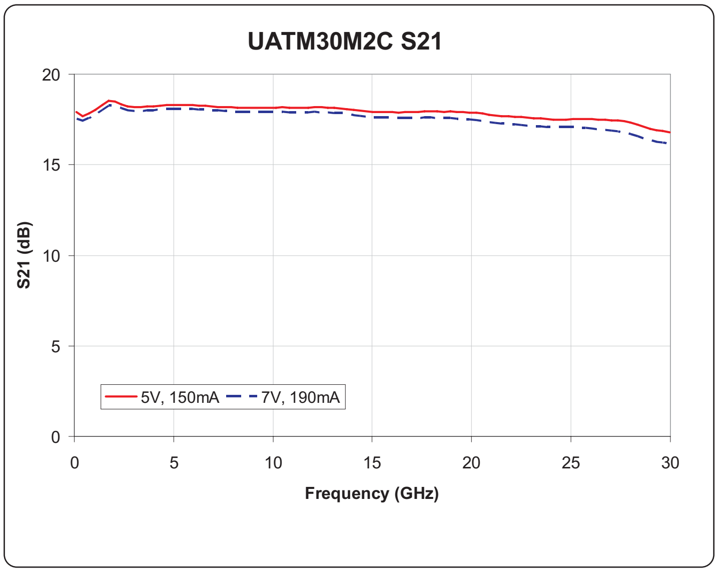
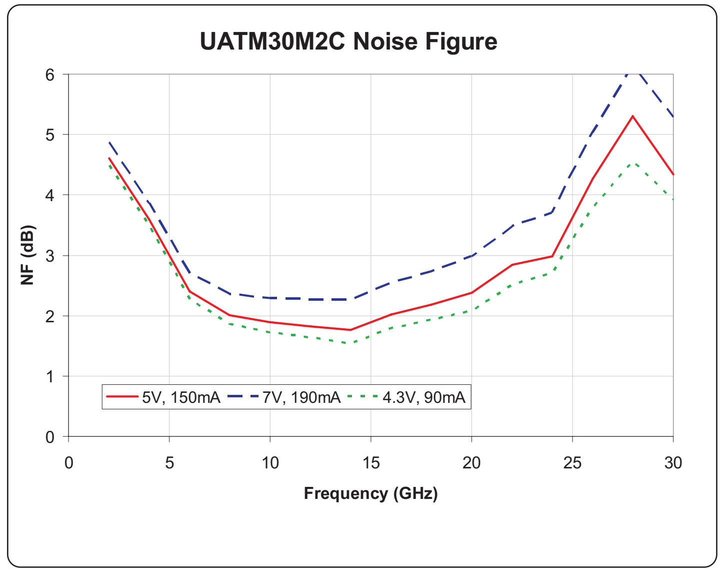
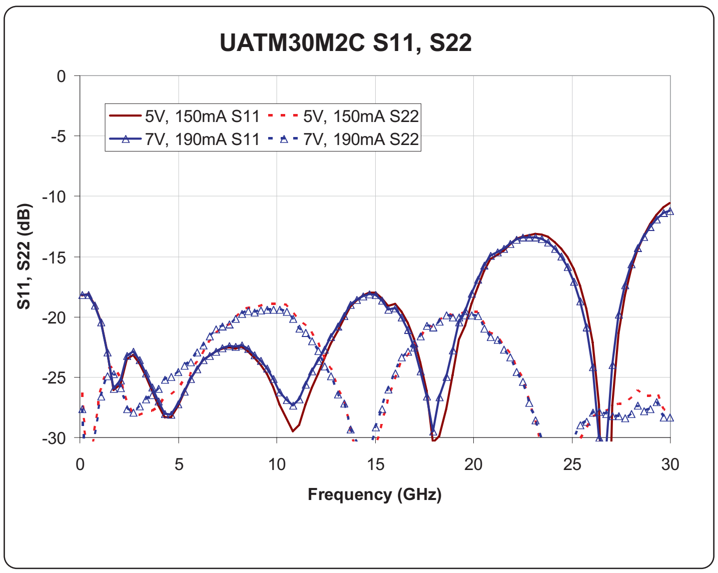


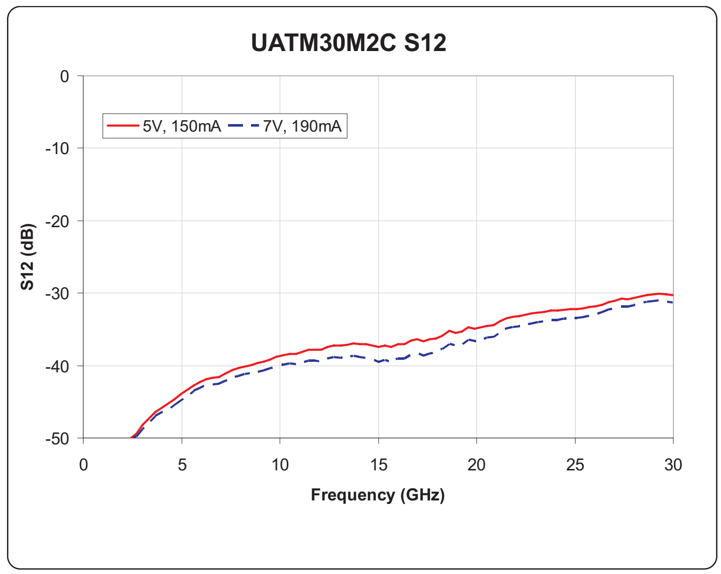
Typical IC performance measured on-wafer



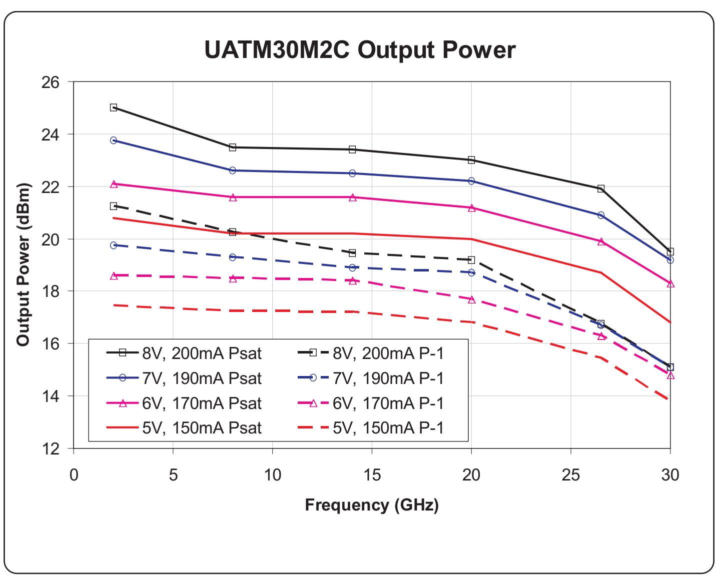
Typical IC performance with package de-embedded



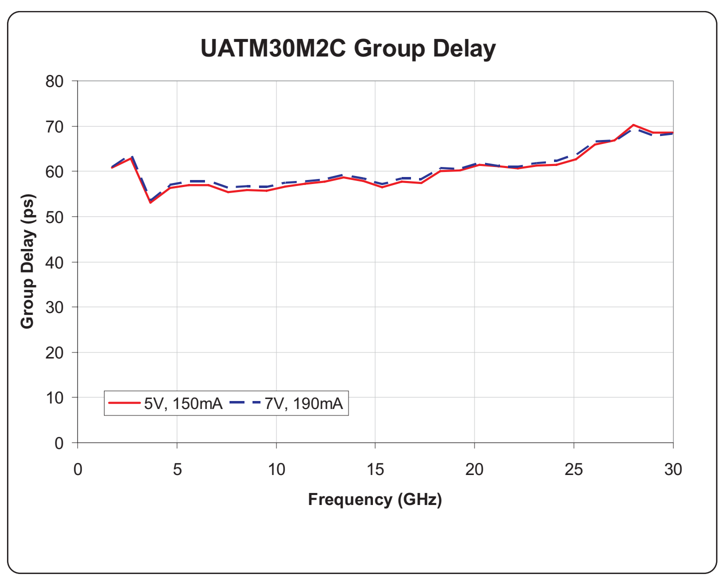
Typical IC performance measured on-wafer



Typical IC performance measured on-wafer



Typical IC performance measured on-wafer



Typical IC performance measured on-wafer

Typical measurement data is available upon request. Email support@centellax.com for more information.

Supplemental Specifications

Parameter	Description	Min	Typ	Max
Vdd	Drain Bias Voltage	3V	5V	8V
Idd	Drain Bias Current	—	150mA	250mA
Vg1	1st Gate Bias Voltage	-4V	—	0V
Vg2	2nd Gate Bias Voltage	Vdd-Vg2<7V	N/C	+4V
P_{in}	Input Power (CW)			20dBm
P_{dc}	Power Dissipation		0.75W	
T_{ch}	Channel Temperature			150°C
Θ_{ch}	Thermal Resistance (T_{case}=85°C)		18°C/W	

DC Bias

The UATM30M2C is biased by applying a positive voltage to the drain (Vdd), then setting the drain current (Idd) using a negative voltage on the gate (Vg1).

When zero volts is applied to the gate, the drain to source channel is open; this results in high Idd. When Vg1 is biased negatively, the channel is pinched off and Idd decreases.

The nominal bias is Vdd=5.0V, Idd=150mA. Improved noise or power performance can be achieved with application-specific biasing.

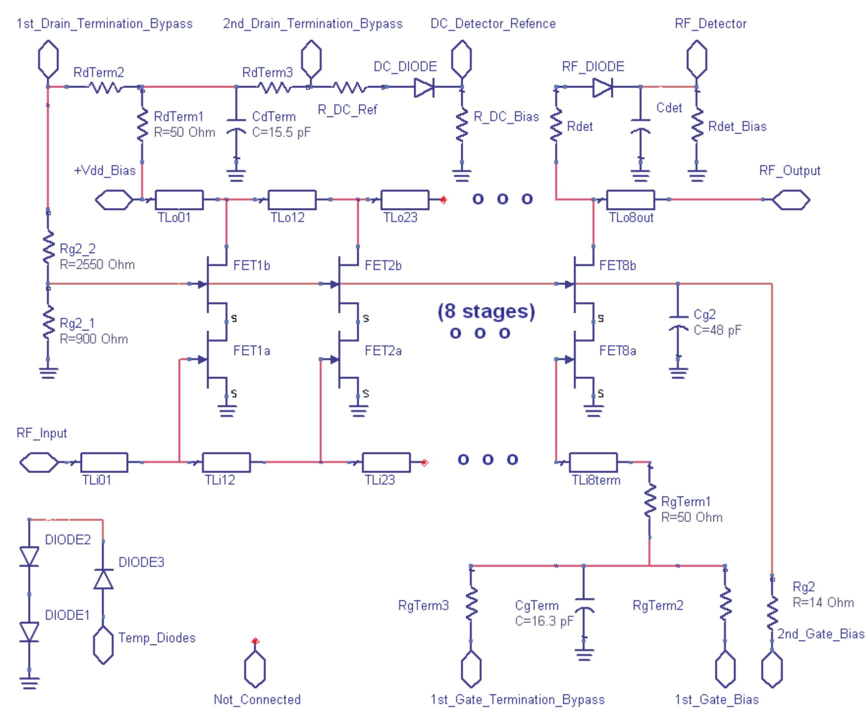
Gain Control

Dynamic gain control is available when operating the amplifier in the linear gain region. Negative voltage applied to the second gate (Vg2) reduces amplifier gain.

RF Power Detection

RF output power can be calculated from the difference between the RF detector voltage and the DC detector voltage, minus a DC offset. Please consult the power detector application note available from the Centellax webpage.

Simplified Circuit Schematic



Low-Frequency Use

The UATM30M2C has been designed so that the bandwidth can be extended to low frequencies. The low end corner frequency of the device is primarily determined by the external biasing and AC coupling circuitry.

Matching

The amplifier incorporates on-chip termination resistors on the RF input and output. These resistors are RF grounded through on-chip capacitors, which are small and become open circuits at frequencies below 1GHz.

A pair of gate and drain termination bypass pads are provided for connecting external capacitors required for the low frequency extension network. These capacitors should be 10x the value of the DC blocking capacitors.

DC Blocks

The amplifier is DC coupled to the RF input and output pads; DC voltage on these pads must be isolated from external circuitry.

For operation above 2GHz, a series DC-blocking capacitor with minimum value of 20pF is recommended; operation above 40MHz requires a minimum of 120pF.

Inductor Bias

DC bias applied to the drain (Vdd) must be decoupled with an off-chip RF choke inductor. The amount of bias inductance will determine the low frequency operating point. Inductive biasing can also be applied to the chip through the RF output.

For many applications above 2GHz, a bondwire from the Vdd pad will suffice as the biasing inductor. Ensure the correct bond length as shown in the assembly diagrams.