UC3844B, UC3845B, UC2844B, UC2845B

High Performance Current Mode Controllers

The UC3844B, UC3845B series are high performance fixed frequency current mode controllers. They are specifically designed for Off−Line and dc−dc converter applications offering the designer a cost−effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

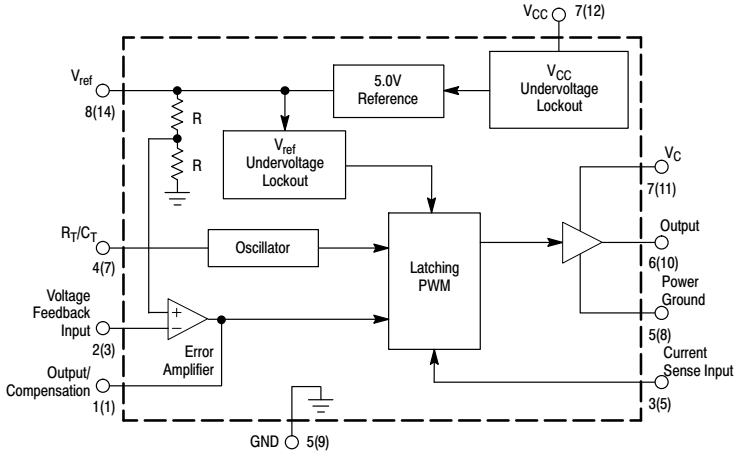
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle−by−cycle current limiting, a latch for single pulse metering, and a flip−flop which blanks the output off every other oscillator cycle, allowing output deadtimes to be programmed from 50% to 70%.

These devices are available in an 8−pin dual−in−line and surface mount (SOIC−8) plastic package as well as the 14−pin plastic surface mount (SOIC−14). The SOIC−14 package has separate power and ground pins for the totem pole output stage.

The UCX844B has UVLO thresholds of 16V (on) and 10V (off), ideally suited for off−line converters. The UCX845B is tailored for lower voltage applications having UVLO thresholds of 8.5V (on) and 7.6V (off).

Features

- Trimmed Oscillator for Precise Frequency Control
- Oscillator Frequency Guaranteed at 250 kHz
- Current Mode Operation to 500 kHz Output Switching Frequency
- Output Deadtime Adjustable from 50% to 70%
- Automatic Feed Forward Compensation
- Latching PWM for Cycle−By−Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current
- These Devices are Pb−Free and are RoHS Compliant
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable



Pin numbers in parenthesis are for the D suffix SOIC−14 package.

Figure 1. Simplified Block Diagram

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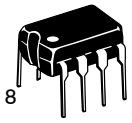
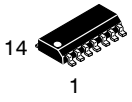


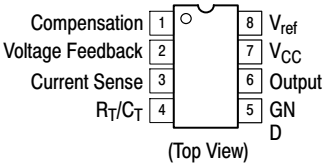
PDIP−8
N SUFFIX
CASE 626



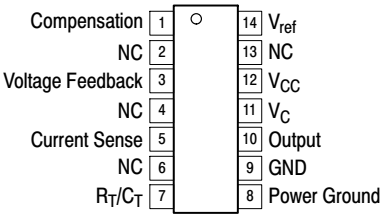
SOIC−14
D SUFFIX
CASE 751A

SOIC−8
D1 SUFFIX
CASE 751

PIN CONNECTIONS



(Top View)



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 16 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Bias and Driver Voltages (Zero Series Impedance, see also Total Device spec) (Note 1)	V_{CC}, V_C	36	V
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 2)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	− 0.3 to + 5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics			
D Suffix, Plastic Package, SOIC−14 Case 751A			
Maximum Power Dissipation @ T_A = 25°C	P_D	862	mW
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	145	°C/W
D1 Suffix, Plastic Package, SOIC−8 Case 751			
Maximum Power Dissipation @ T_A = 25°C	P_D	702	mW
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	178	°C/W
N Suffix, Plastic Package, Case 626			
Maximum Power Dissipation @ T_A = 25°C	P_D	1.25	W
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature UC3844B, UC3845B	T_A	0 to +70	°C
UC2844B, UC2845B		−25 to +85	
UC3844BV, UC3845BV		−40 to +105	
Storage Temperature Range	T_{stg}	− 65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The voltage is clamped by a zener diode (see page 9 Under Voltage Lockout section). Therefore this voltage may be exceeded as long as the total power supply and zener current is not exceeded.
2. Maximum package power dissipation limits must be observed.
3. This device series contains ESD protection and exceeds the following tests: Human Body Model 4000 V per JEDEC Standard JESD22-A114B, Machine Model Method 200 V per JEDEC Standard JESD22-A115-A
4. This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78

ELECTRICAL CHARACTERISTICS

(V_{CC} = 15 V [Note 5], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 6], unless otherwise noted.)

Characteristic	Symbol	UC284xB Min	UC284xB Typ	UC284xB Max	UC384xB, xBV, NCV384xBV Min	UC384xB, xBV, NCV384xBV Typ	UC384xB, xBV, NCV384xBV Max	Unit
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	−	2.0	20	−	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	−	3.0	25	−	3.0	25	mV
Temperature Stability	T_S	−	0.2	−	−	0.2	−	mV/°C
Total Output Variation over Line, Load, & Temperature	V_{ref}	4.9	−	5.1	4.82	−	5.18	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	−	50	−	−	50	−	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	−	5.0	−	−	5.0	−	mV
Output Short Circuit Current	I_{SC}	− 30	− 85	−180	− 30	− 85	−180	mA
OSCILLATOR SECTION								
Frequency T_J = 25°C	f_{OSC}	49	52	55	49	52	55	kHz
$T_A = T_{low}$ to T_{high}		48	−	56	48	−	56	
T_J = 25°C (R_T = 6.2 k, C_T = 1.0 nF)		225	250	275	225	250	275	
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{OSC}/\Delta V$	−	0.2	1.0	−	0.2	1.0	%
Frequency Change w/ Temperature ($T_A = T_{low}$ to T_{high})	$\Delta f_{OSC}/\Delta T$	−	1.0	−	−	0.5	−	%
Oscillator Voltage Swing (Peak−to−Peak)	V_{OSC}	−	1.6	−	−	1.6	−	V

5. Adjust V_{CC} above the Startup threshold before setting to 15 V.
6. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
   T_{low} = 0°C for UC3844B, UC3845B; T_{high} = + 70°C for UC3844B, UC3845B
   = − 25°C for UC2844B, UC2845B; = + 85°C for UC2844B, UC2845B
   = − 40°C for UC384xBV, NCV384xBV; =+105°C for UC3844BV, UC3845BV
   = +125°C for NCV384xBV

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 7], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 8], unless otherwise noted.)

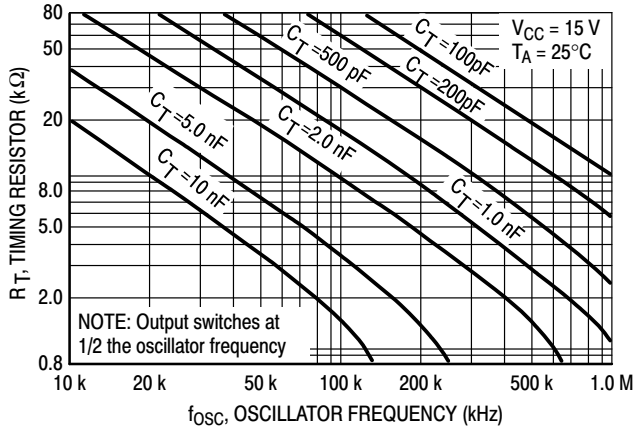
Characteristic	Symbol	UC284xB Min	UC284xB Typ	UC284xB Max	UC384xB, xBV, NCV384xBV Min	UC384xB, xBV, NCV384xBV Typ	UC384xB, xBV, NCV384xBV Max	Unit
OSCILLATOR SECTION								
Discharge Current (V_{OSC} = 2.0 V) T_J = 25°C	I_{dischg}	7.8	8.3	8.8	7.8	8.3	8.8	mA
$T_A = T_{low}$ to T_{high} (UC284XB, UC384XB)		7.5	–	8.8	7.6	–	8.8	
(UC384XBV)		–	–	–	7.2	–	8.8	
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	–	– 0.1	–1.0	–	– 0.1	– 2.0	μA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	–	65	90	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	–	60	70	–	dB
Output Current – Sink (V_O = 1.1 V, V_{FB} = 2.7 V)	I_{Sink}	2.0	12	–	2.0	12	–	mA
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}	– 0.5	–1.0	–	– 0.5	–1.0	–	
Output Voltage Swing								V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	–	5.0	6.2	–	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}							
(UC284XB, UC384XB)		–	0.8	1.1	–	0.8	1.1	
(UC384XBV)		–	–	–	–	0.8	1.2	
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 9 & 10)	A_V							V/V
(UC284XB, UC384XB)		2.85	3.0	3.15	2.85	3.0	3.15	
(UC384XBV)		–	–	–	2.85	3.0	3.25	
Maximum Current Sense Input Threshold (Note 9)	V_{th}							V
(UC284XB, UC384XB)		0.9	1.0	1.1	0.9	1.0	1.1	
(UC384XBV)		–	–	–	0.85	1.0	1.1	
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V) (Note 9)	PSRR	–	70	–	–	70	–	dB
Input Bias Current	I_{IB}	–	– 2.0	–10	–	– 2.0	–10	μA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(In/Out)}$	–	150	300	–	150	300	ns
OUTPUT SECTION								
Output Voltage								V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.1	0.4	–	0.1	0.4	
(I_{Sink} = 200 mA, UC284XB, UC384XB)		–	1.6	2.2	–	1.6	2.2	
(I_{Sink} = 200 mA, UC384XBV)		–	–	–	–	1.6	2.3	
High State (I_{Source} = 20 mA, UC284XB, UC384XB)	V_{OH}	13	13.5	–	13	13.5	–	
(I_{Source} = 20 mA, UC384XBV)		–	–	–	12.9	–	–	
(I_{Source} = 200 mA)		12	13.4	–	12	13.4	–	
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	–	0.1	1.1	–	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	50	150	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	150	–	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Startup Threshold UCX844B, BV	V_{th}	15	16	17	14.5	16	17.5	V
UCX845B, BV		7.8	8.4	9.0	7.8	8.4	9.0	
Minimum Operating Voltage After Turn–On UCX844B, BV	$V_{CC(min)}$	9.0	10	11	8.5	10	11.5	V
UCX845B, BV		7.0	7.6	8.2	7.0	7.6	8.2	

7. Adjust V_{CC} above the Startup threshold before setting to 15 V.
8. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
   T_{low} = 0°C for UC3844B, UC3845B; T_{high} = + 70°C for UC3844B, UC3845B
   = – 25°C for UC2844B, UC2845B; = + 85°C for UC2844B, UC2845B
   = – 40°C for UC384xBV, NCV384xBV; = +105°C for UC3844BV, UC3845BV
   = +125°C for NCV384xBV
9. This parameter is measured at the latch trip point with V_{FB} = 0 V.
10. Comparator gain is defined as: $A_V = \frac{\Delta V \text{ Output/Compensation}}{\Delta V \text{ Current Sense Input}}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 11], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 12], unless otherwise noted.)

Characteristic	Symbol	UC284xB			UC384xB, xBV, NCV384xBV			Unit
		Min	Typ	Max	Min	Typ	Max	
PWM SECTION								
Duty Cycle								%
Maximum (UC284XB, UC384XB)	$DC_{(max)}$	47	48	50	47	48	50	
(UC384XBV)		–	–	–	46	48	50	
Minimum	$DC_{(min)}$	–	–	0	–	–	0	
TOTAL DEVICE								
Power Supply Current	I_{CC}							mA
Startup (V_{CC} = 6.5 V for UCX845B, 14 V for UCX844B, BV)		–	0.3	0.5	–	0.3	0.5	
Operating (Note 11)		–	12	17	–	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	–	30	36	–	V

11. Adjust V_{CC} above the Startup threshold before setting to 15 V.
12. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
    T_{low} = 0°C for UC3844B, UC3845B; = – 25°C for UC2844B, UC2845B; = – 40°C for UC384xBV, NCV384xBV
    T_{high} = + 70°C for UC3844B, UC3845B; = + 85°C for UC2844B, UC2845B; = +105°C for UC3844BV, UC3845BV; =+125°C for NCV384xBV



$$\text{For } R_T > 5\text{ Kf} \sim \frac{1.72}{R_T C_T}$$

Figure 2. Timing Resistor versus Oscillator Frequency

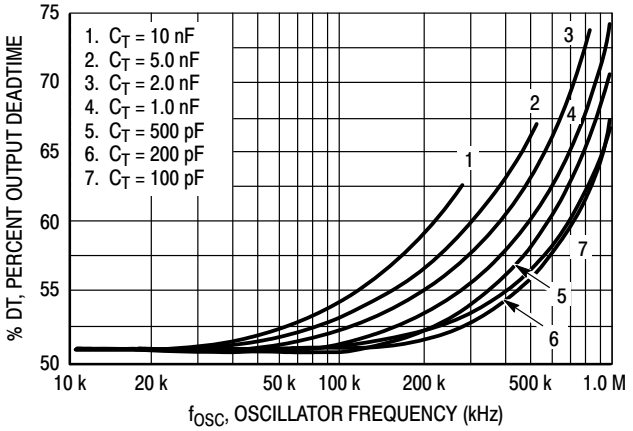


Figure 3. Output Deadtime versus Oscillator Frequency

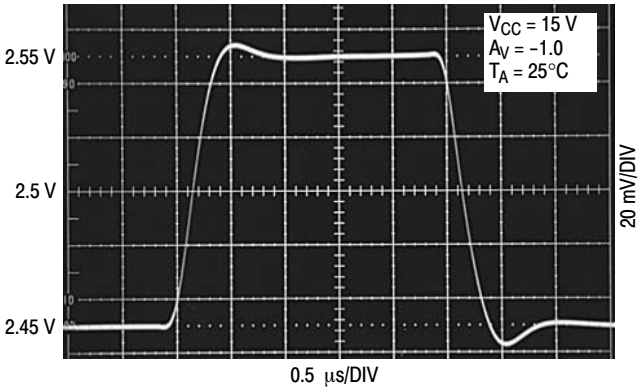


Figure 4. Error Amp Small Signal Transient Response

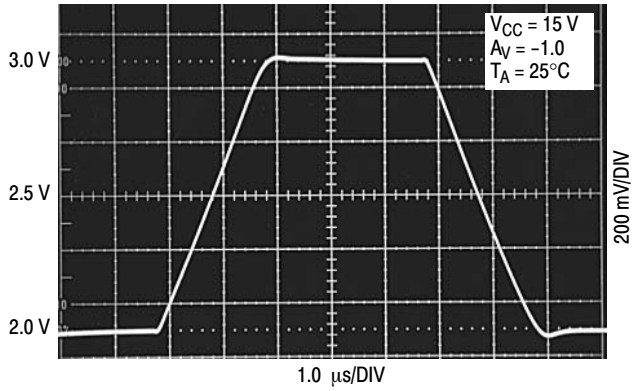


Figure 5. Error Amp Large Signal Transient Response

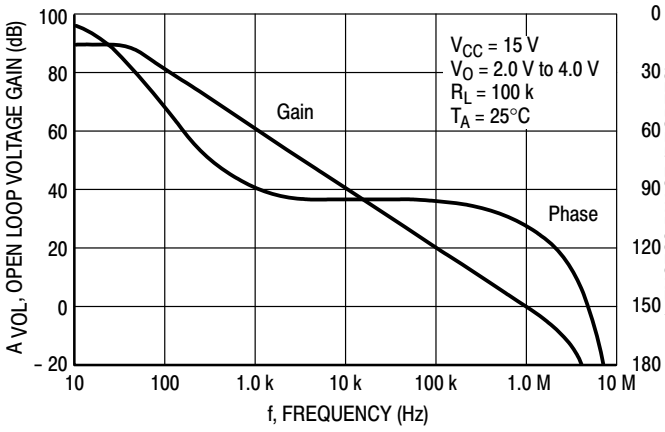


Figure 6. Error Amp Open Loop Gain and Phase versus Frequency

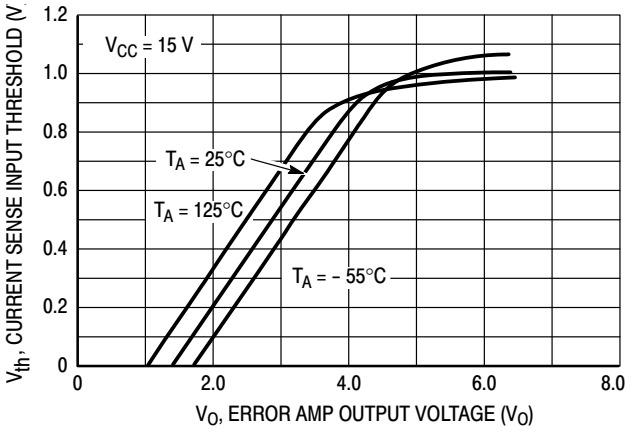


Figure 7. Current Sense Input Threshold versus Error Amp Output Voltage

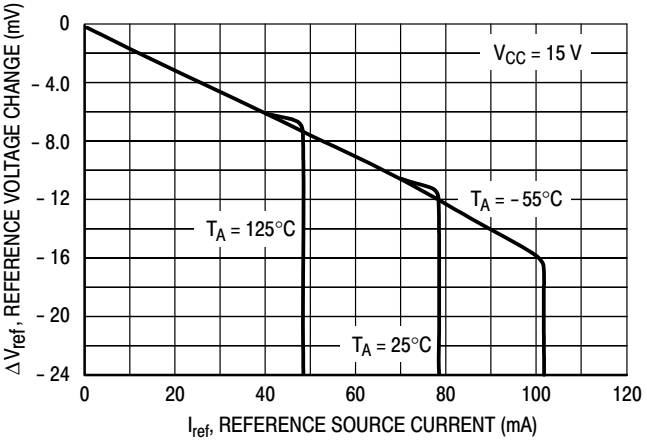


Figure 8. Reference Voltage Change versus Source Current

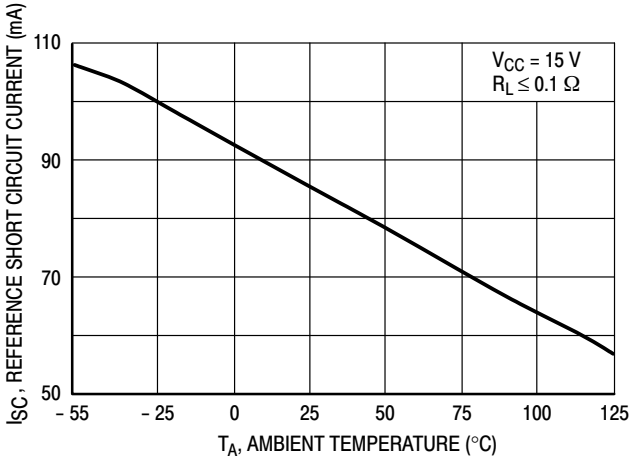


Figure 9. Reference Short Circuit Current versus Temperature

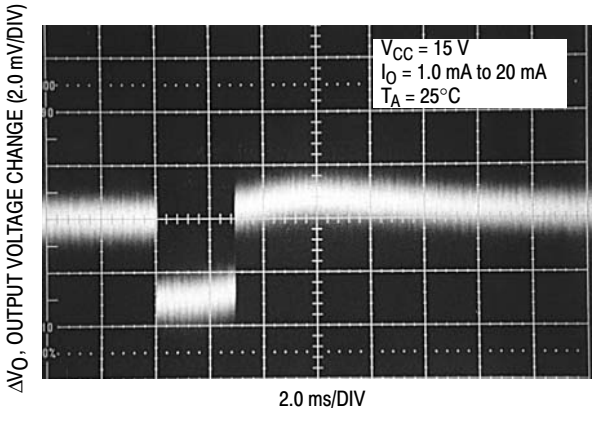


Figure 10. Reference Load Regulation

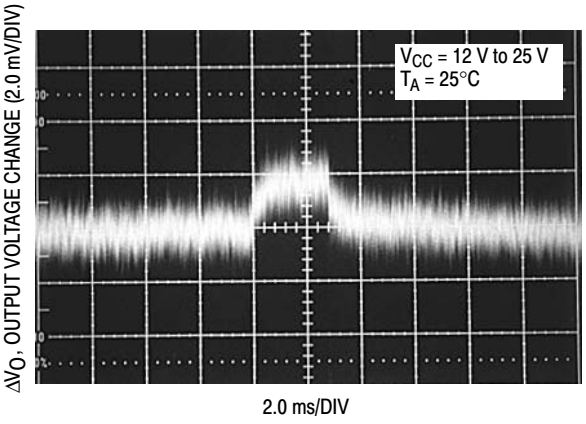


Figure 11. Reference Line Regulation

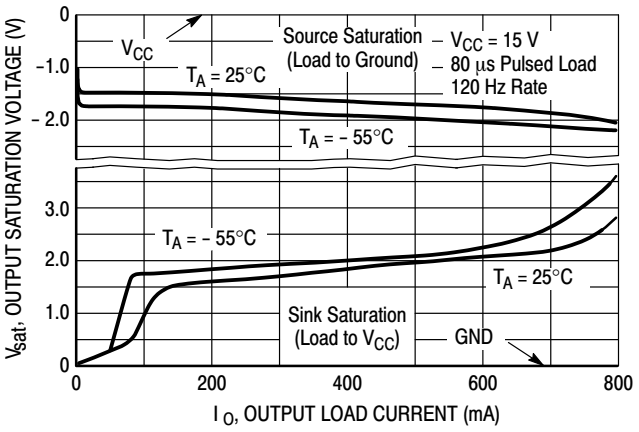


Figure 12. Output Saturation Voltage versus Load Current

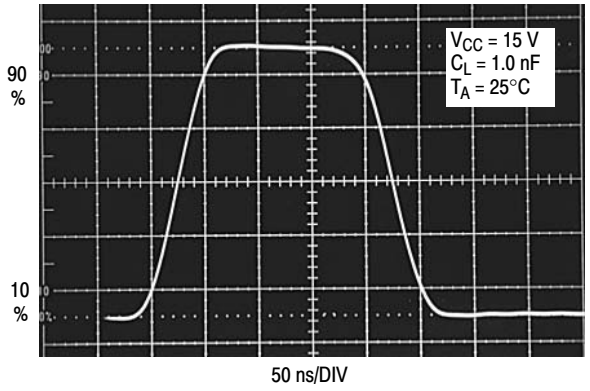


Figure 13. Output Waveform

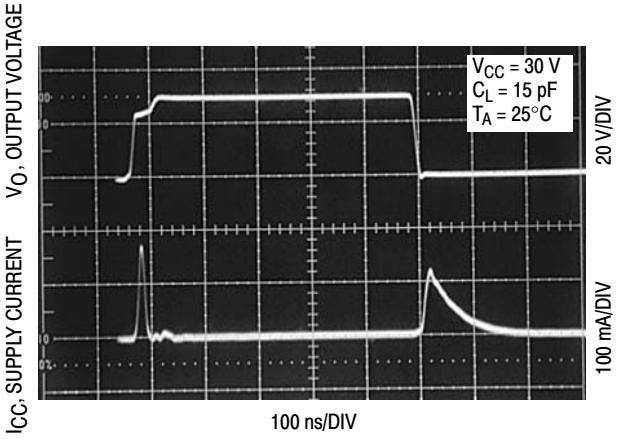


Figure 14. Output Cross Conduction

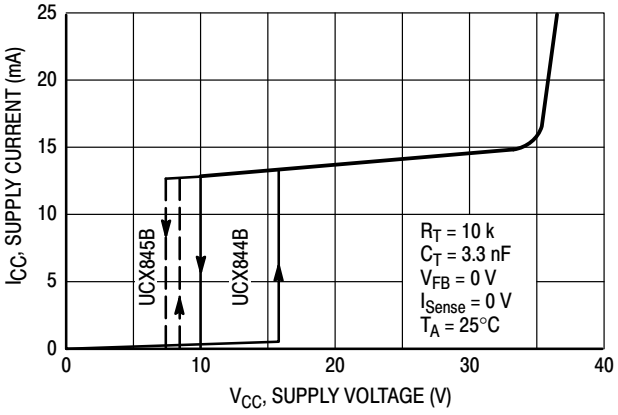


Figure 15. Supply Current versus Supply Voltage

PIN FUNCTION DESCRIPTION

Pin		Function	Description
8−Pin	14−Pin		
1	1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Oscillator operation to 1.0 kHz is possible.
5		GND	This pin is the combined control circuitry and power ground.
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin. The output switches at one−half the oscillator frequency.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
	8	Power Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
	9	GND	This pin is the control circuitry ground return and is connected back to the powersource ground.
	2,4,6,13	NC	No connection. These pins are not internally connected.

OPERATING DESCRIPTION

The UC3844B, UC3845B series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off−Line and DC−DC converter applications offering the designer a cost−effective solution with minimal external components. A representative block diagram is shown in Figure 16.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. An internal flip−flop has been incorporated in the UCX844/5B which blanks the output off every other clock cycle by holding one of the inputs of the NOR gate high. This in combination with the C_T discharge period yields output deadtimes programmable from 50% to 70%. Figure 2 shows R_T versus Oscillator Frequency and Figure 3, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated to within ±6% at 50 kHz. Also, because of industry trends moving the UC384X into higher and higher frequency applications, the UC384XB is guaranteed to within ±10% at 250 kHz.

In many noise−sensitive applications it may be desirable to frequency−lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 18. For reliable locking, the free−running oscillator frequency should be set about 10% less than the clock frequency. A method for multi−unit synchronization is shown in Figure 19. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved to realize output deadtimes of greater than 70%.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 6). The non−inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is −2.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 29). The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when Pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft−start interval (Figures 21, 22). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The UC3844B, UC3845B operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle−by−cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground−referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 1 where:

$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 20. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability (refer to Figure 24).

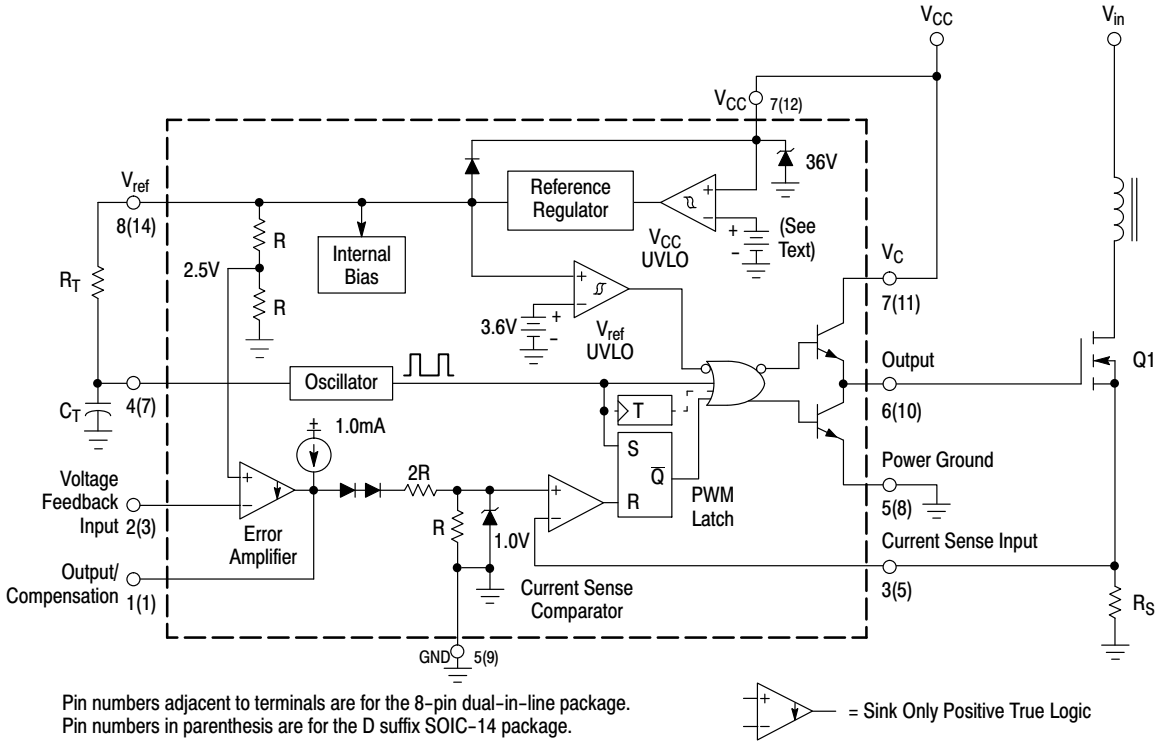


Figure 16. Representative Block Diagram

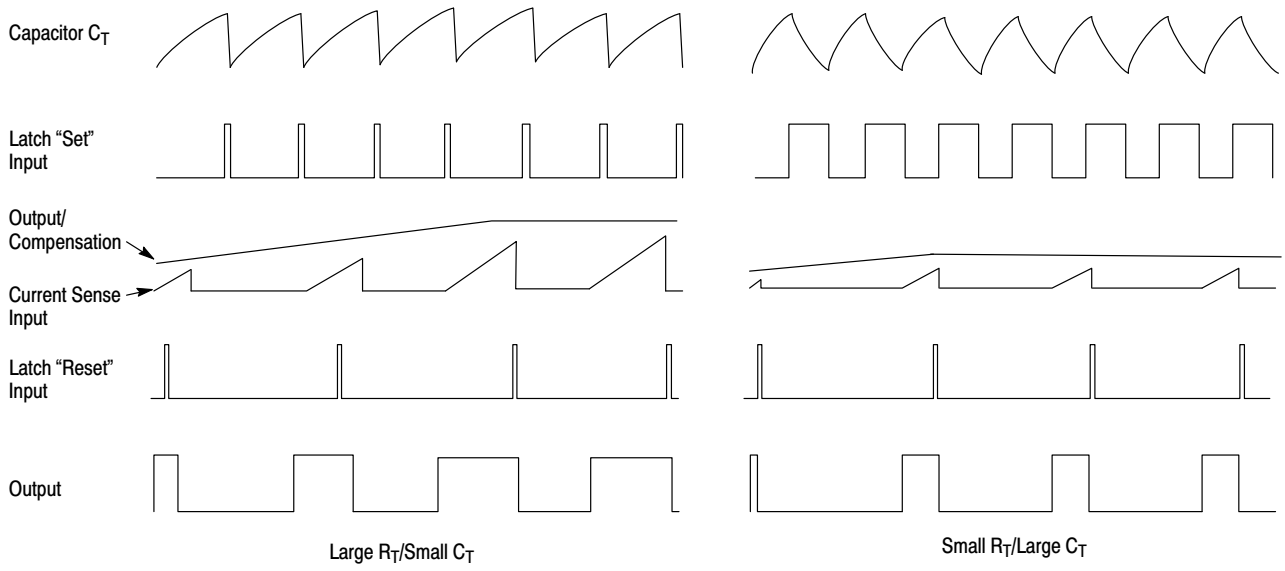


Figure 17. Timing Diagram

Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built−in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX844B, and 8.4 V/7.6 V for the UCX845B. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V. The large hysteresis and low startup current of the UCX844B makes it ideally suited in off−line converter applications where efficient bootstrap startup techniques are required (Figure 30). The UCX845B is intended for lower voltage dc−dc converter applications. A 36 V Zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage for the UCX844B is 11 V and 8.2 V for the UCX845B.

Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pulldown resistor.

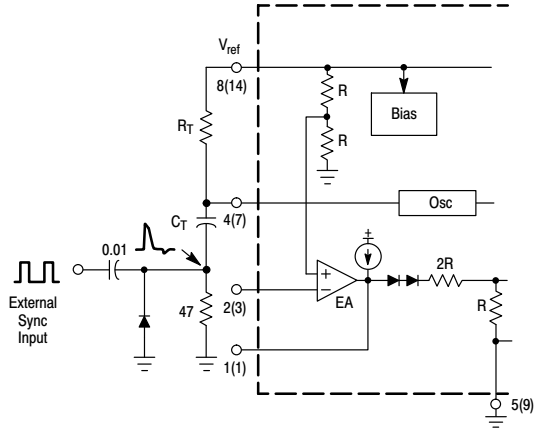
The SOIC−14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A Zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V. Figure 23 shows proper power and control ground connections in a current−sensing power MOSFET application.

Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at T_J = 25°C on the UC284XB, and ±2.0% on the UC384XB. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short−circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

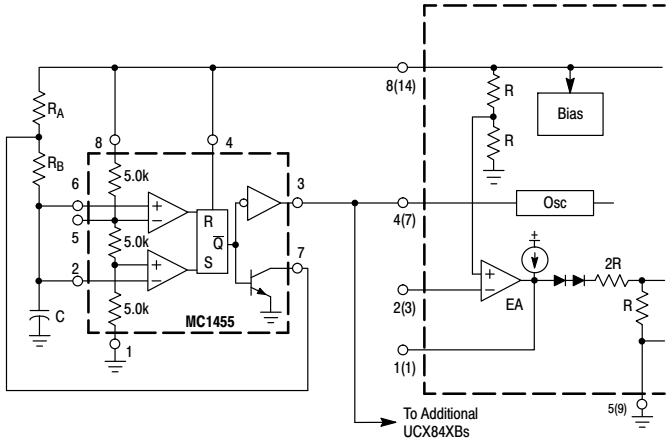
Design Considerations

Do not attempt to construct the converter on wire−wrap or plug−in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse−width jitter. This is usually caused by excessive noise pick−up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low−current signal and high−current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise−generating components.



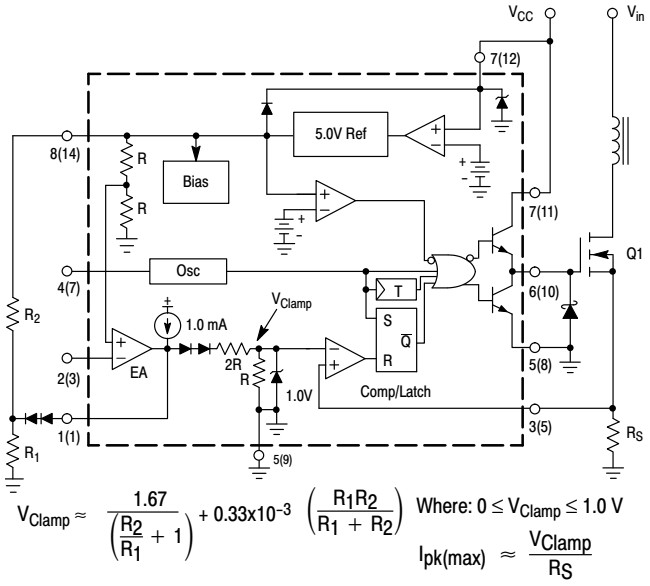
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

Figure 18. External Clock Synchronization



$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{(max)} = \frac{R_A}{R_A + 2R_B}$$

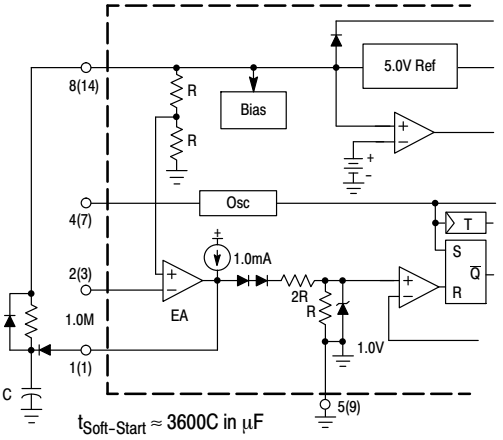
Figure 19. External Duty Cycle Clamp and Multi−Unit Synchronization



$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} + 0.33x10^{-3}\left(\frac{R_1R_2}{R_1 + R_2}\right) \quad \text{Where: } 0 \le V_{Clamp} \le 1.0\ V$$

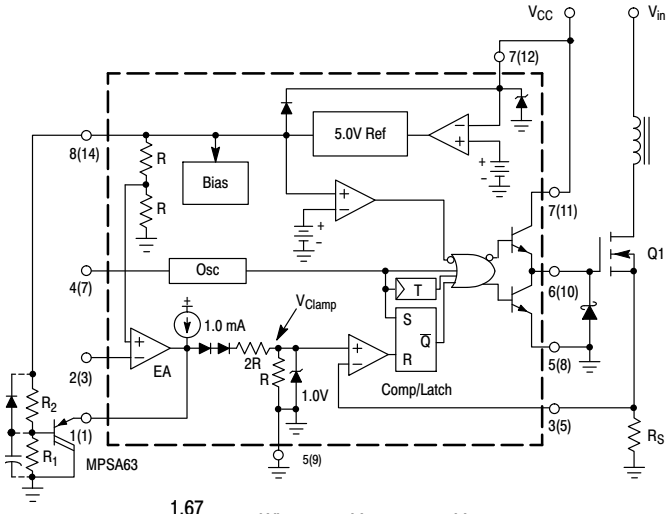
$$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Figure 20. Adjustable Reduction of Clamp Level



$$t_{Soft\text{-}Start} \approx 3600C \text{ in } \mu F$$

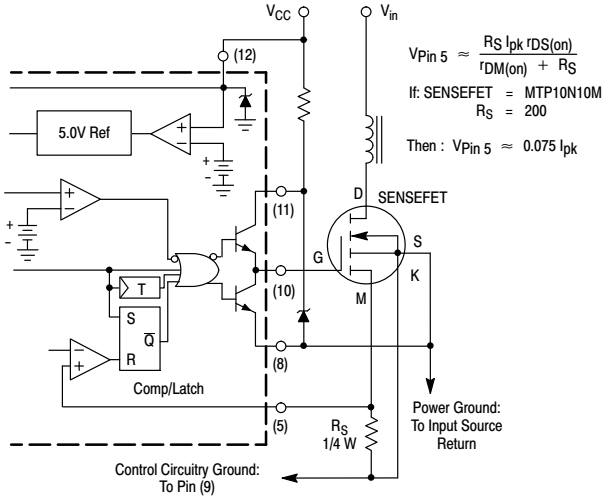
Figure 21. Soft−Start Circuit



$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} \quad \text{Where: } 0 \le V_{Clamp} \le 1.0\ V$$

$$t_{Soft\text{-}Start} = -\ln\left[1 - \frac{V_C}{3V_{Clamp}}\right] C\frac{R_1 R_2}{R_1 + R_2} \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Figure 22. Adjustable Buffered Reduction of Clamp Level with Soft−Start



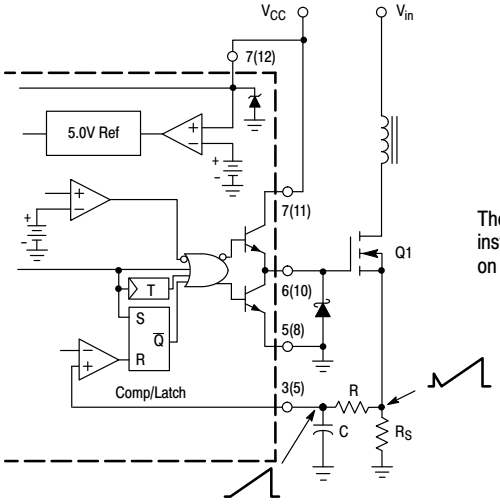
$$V_{Pin\ 5} \approx \frac{R_S\, I_{pk}\, r_{DS(on)}}{r_{DM(on)} + R_S}$$

If: SENSEFET = MTP10N10M
R_S = 200

Then : $V_{Pin\ 5} \approx 0.075\ I_{pk}$

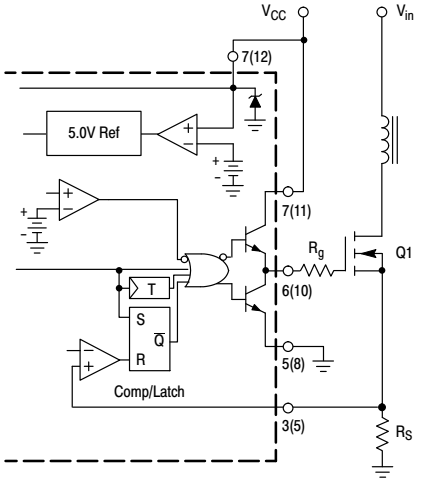
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET™ power switch. For proper operation during over−current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 20 and 22.

Figure 23. Current Sensing Power MOSFET



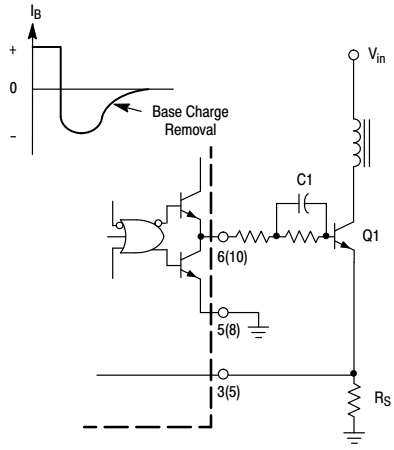
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 24. Current Waveform Spike Suppression



Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate−source circuit.

Figure 25. MOSFET Parasitic Oscillations



The totem pole output can furnish negative base current for enhanced transistor turn−off, with the addition of capacitor C_1.

Figure 26. Bipolar Transistor Drive

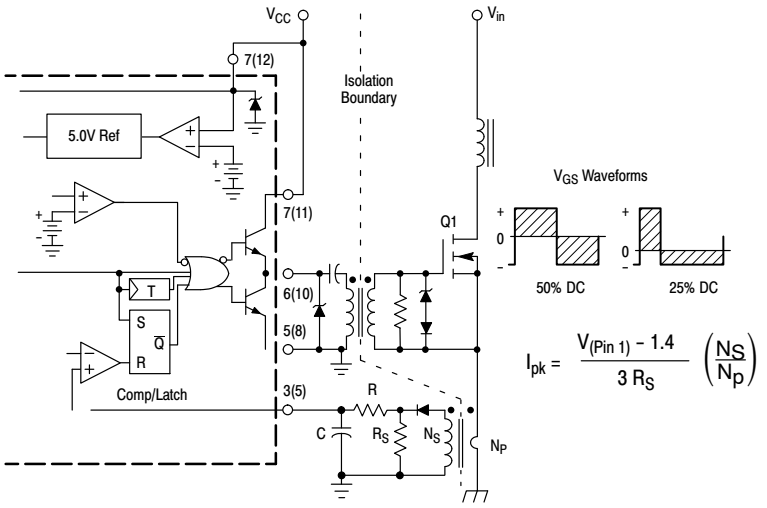
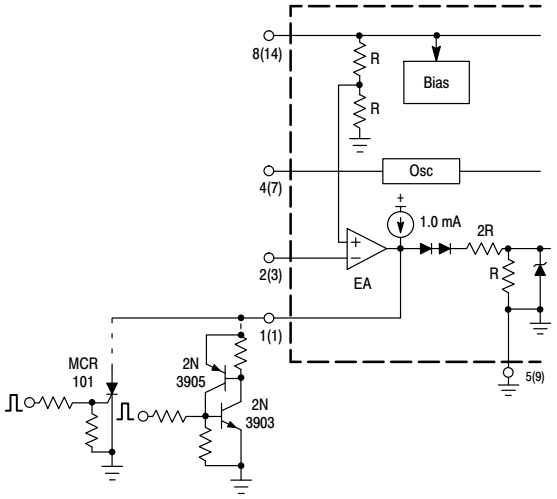
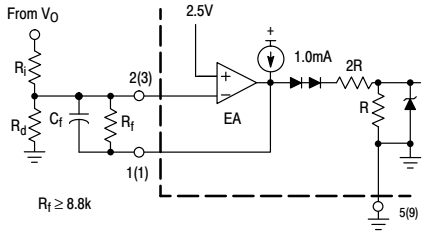


Figure 27. Isolated MOSFET Drive

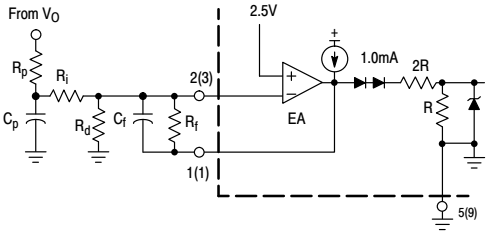


The MCR101 SCR must be selected for a holding of < 0.5 mA @ $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

Figure 28. Latched Shutdown

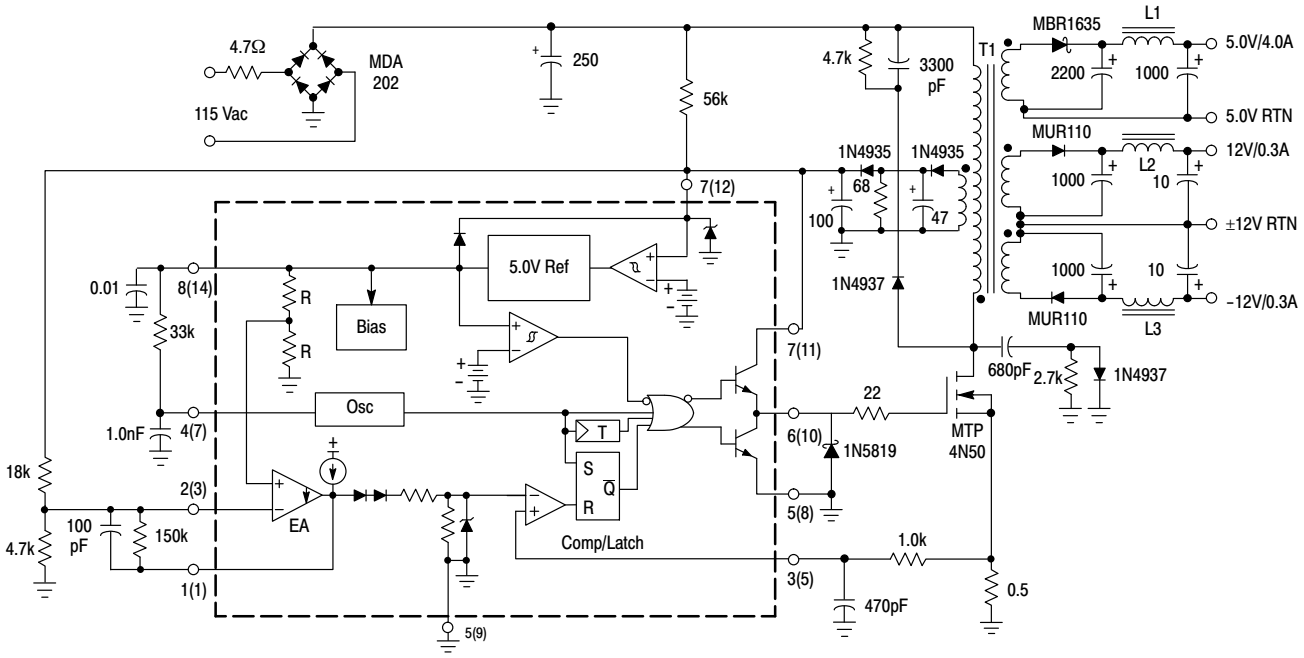


Error Amp compensation circuit for stabilizing any current mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current mode boost and flyback topologies operating with continuous inductor current.

Figure 29. Error Amplifier Compensation



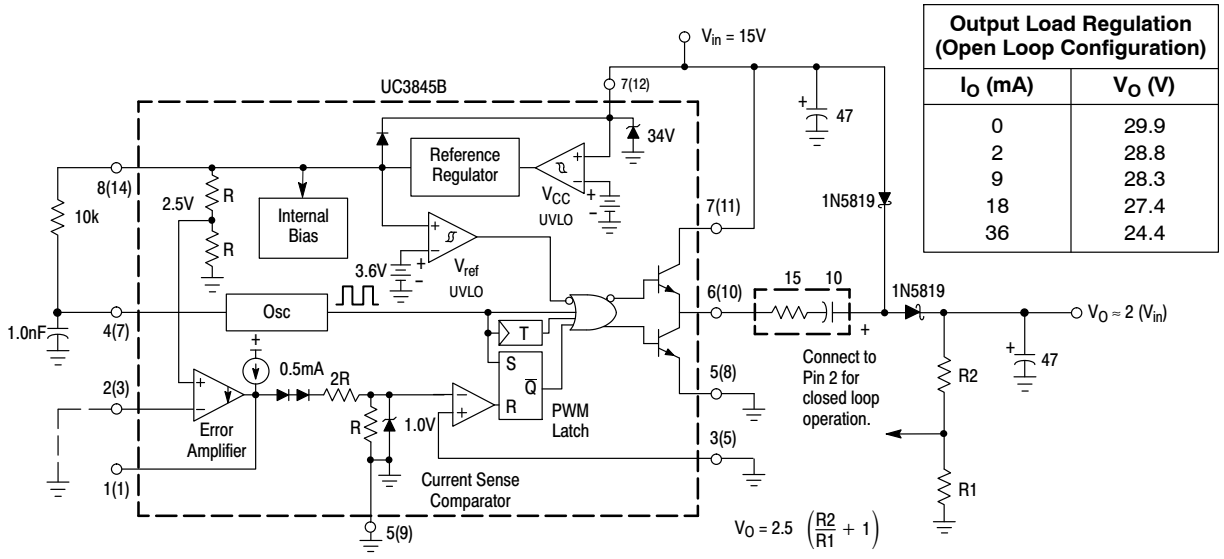
T1 - Primary: 45 Turns #26 AWG
Secondary ±12 V: 9 Turns #30 AWG (2 Strands) Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands) #26 Hexfiliar Wound
Secondary Feedback: 10 Turns #30 AWG (2 strands) Bifiliar Wound
Core: Ferroxcube EC35−3C8
Bobbin: Ferroxcube EC35PCB1
Gap: ≈ 0.10" for a primary inductance of 1.0 mH

L1 - 15 μH at 5.0 A, Coilcraft Z7156
L2, L3 - 25 μH at 5.0 A, Coilcraft Z7157

Figure 30. 7 W Off−Line Flyback Regulator

Test		Conditions	Results
Line Regulation:	5.0 V ±12 V	V_{in} = 95 Vac to 130 Vac	Δ = 50 mV or ±0.5% Δ = 24 mV or ±0.1%
Load Regulation:	5.0 V ±12 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 300 mV or ±3.0% Δ = 60 mV or ±0.25%
Output Ripple:	5.0 V ±12 V	V_{in} = 115 Vac	40 mV_{pp} 80 mV_{pp}
Efficiency		V_{in} = 115 Vac	70%

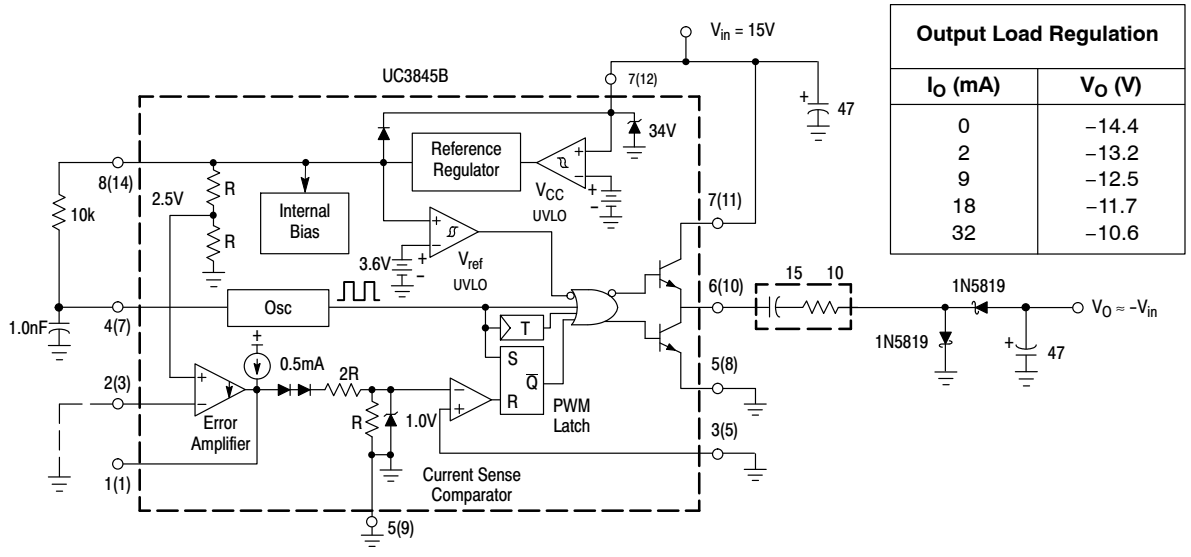
All outputs are at nominal load currents unless otherwise noted.



Output Load Regulation (Open Loop Configuration)	
I_O (mA)	V_O (V)
0	29.9
2	28.8
9	28.3
18	27.4
36	24.4

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A. An additional series resistor may be required when using tantalum or other low ESR capacitors. The converter's output can provide excellent line and load regulation by connecting the R2/R1 resistor divider as shown.

Figure 31. Step−Up Charge Pump Converter



Output Load Regulation	
I_O (mA)	V_O (V)
0	−14.4
2	−13.2
9	−12.5
18	−11.7
32	−10.6

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A.
An additional series resistor may be required when using tantalum or other low ESR capacitors.

Figure 32. Voltage−Inverting Charge Pump Converter

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping†
UC384xBDG	T_A = 0° to +70°C	SOIC−14 (Pb−Free)	55 Units/Rail
UC384xBDR2G		SOIC−14 (Pb−Free)	2500 Tape & Reel
UC384xBD1G		SOIC−8 (Pb−Free)	98 Units/Rail
UC384xBD1R2G		SOIC−8 (Pb−Free)	2500 Tape & Reel
UC384xBNG		PDIP−8 (Pb−Free)	50 Units/Rail
UC284xBDG	T_A = −25° to +85°C	SOIC−14 (Pb−Free)	55 Units/Rail
UC284xBDR2G		SOIC−14 (Pb−Free)	2500 Tape & Reel
UC284xBD1G		SOIC−8 (Pb−Free)	98 Units/Rail
UC284xBD1R2G		SOIC−8 (Pb−Free)	2500 Tape & Reel
UC284xBNG		PDIP−8 (Pb−Free)	50 Units/Rail
UC384xBVDG	T_A = −40° to +105°C	SOIC−14 (Pb−Free)	55 Units/Rail
UC384xBVDR2G		SOIC−14 (Pb−Free)	2500 Tape & Reel
UC384xBVD1G		SOIC−8 (Pb−Free)	98 Units/Rail
UC384xBVD1R2G		SOIC−8 (Pb−Free)	2500 Tape & Reel
UC384xBVNG		PDIP−8 (Pb−Free)	50 Units/Rail
NCV3845BVD1R2G*	T_A = −40° to +125°C	SOIC−8 (Pb−Free)	2500 Tape & Reel

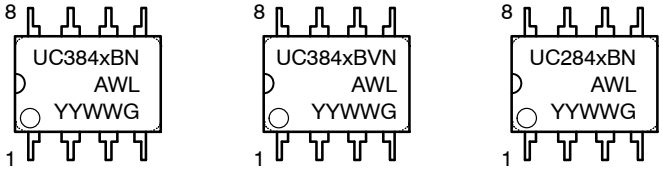
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

x indicates either a 4 or 5 to define specific device part numbers.

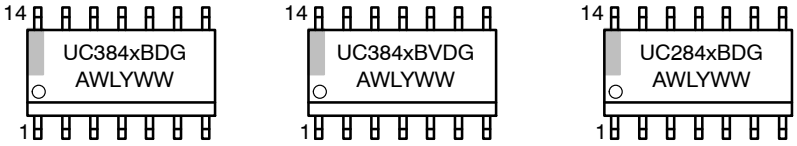
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MARKING DIAGRAMS

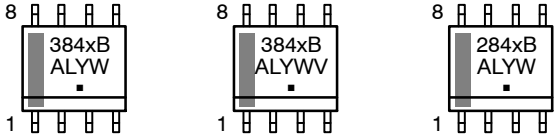
PDIP−8
N SUFFIX
CASE 626



SOIC−14
D SUFFIX
CASE 751A



SOIC−8
D1 SUFFIX
CASE 751



x = 4 or 5
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

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SCALE 1:1

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CASE 626–05
ISSUE P

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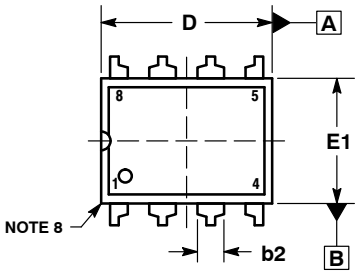
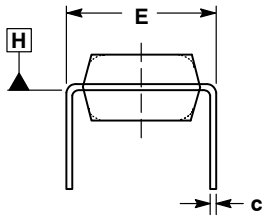
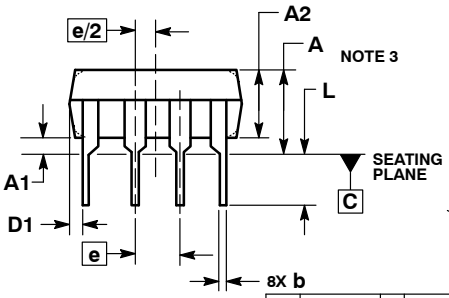


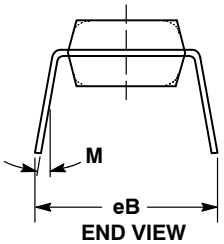
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



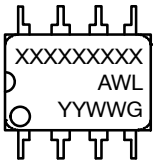
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

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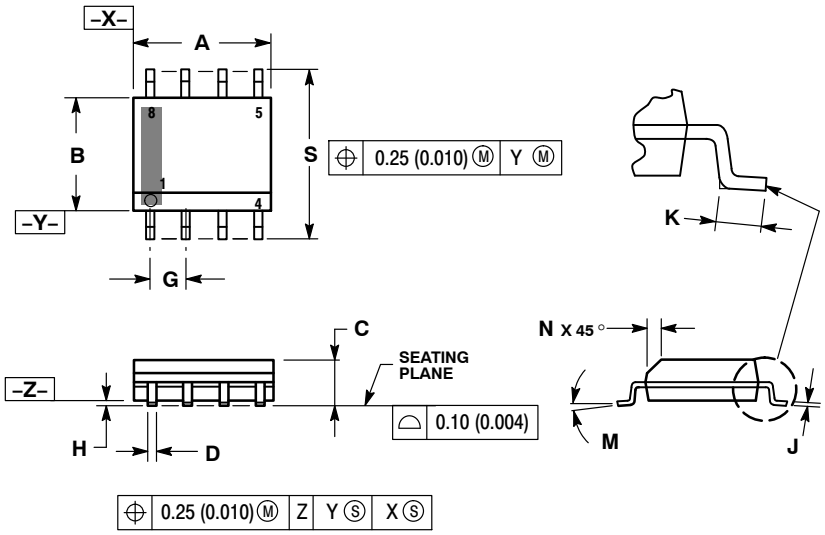
ISSUE AK

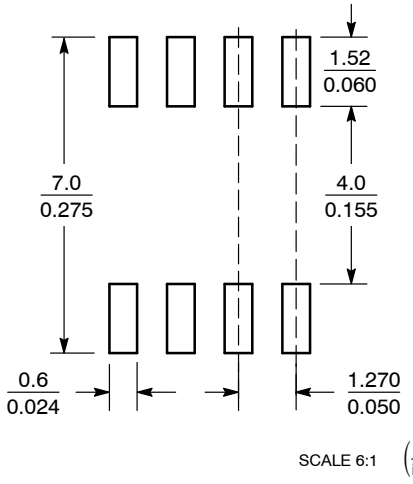
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

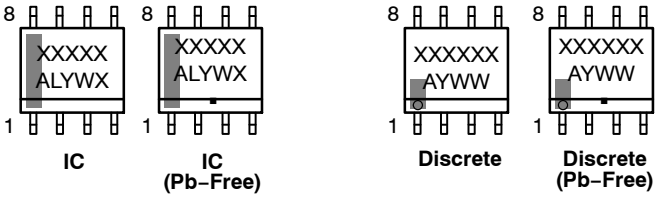
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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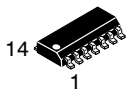
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

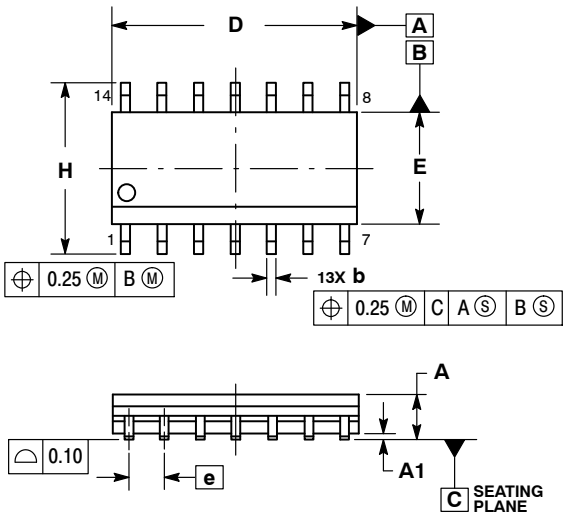
ON Semiconductor®

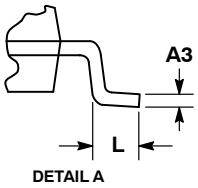


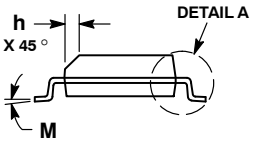
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



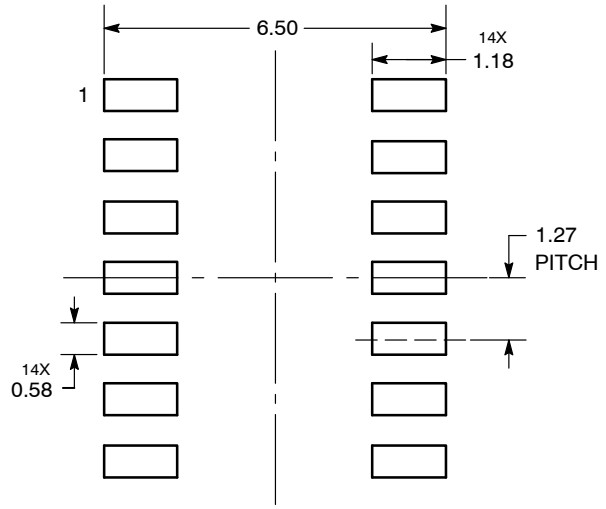




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

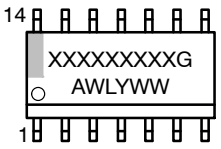
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	SOIC−14 NB		PAGE 1 OF 2

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE