Description

The µClamp™ series of TVS arrays are designed to protect sensitive electronics from damage or latch-up due to ESD. It is designed to replace multilayer varistors (MLVs) in portable applications such as cell phones, notebook computers, and PDA's. It features large cross-sectional area junctions for conducting high transient currents. It offers superior electrical characteristics such as lower clamping voltage and no device degradation when compared to MLVs. They offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

The µclamp™0501H is in a ultra-small SOD-523 package ideal for use in portable electronics such as cell phones, PDA's, notebook computers, and digital cameras. It will protect one unidirectional line operating at 5 volts. It gives the designer the flexibility to protect one line in applications where arrays are not practical. Additionally, it may be "sprinkled" around the board in applications where board space is at a premium.

This device may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (15kV air, 8kV contact discharge).

Features

- Transient protection for data lines to
  IEC 61000-4-2 (ESD) 15kV (air), 8kV (contact)
  IEC 61000-4-4 (EFT) 40A (tp = 5/50ns)
  Cable Discharge Event (CDE)
- Ultra-small SOD-523 package (1.7 x 0.9 x 0.7mm)
- Protects one I/O or power line
- Low clamping voltage
- Working voltage: 5V
- Low leakage current
- Solid-state silicon-avalanche technology

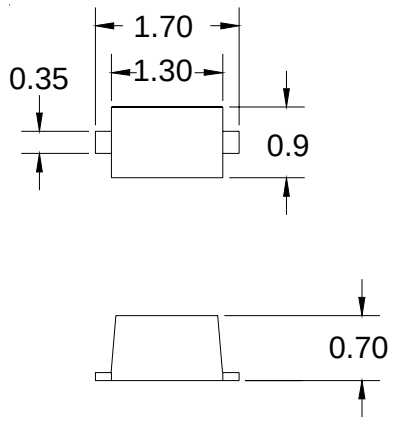
Mechanical Characteristics

- EIAJ SOD-523 package
- Molding compound flammability rating: UL 94V-0
- Marking : Marking code, cathode band
- Packaging : Tape and Reel per EIA 481
- Lead Finish: Matte tin

Applications

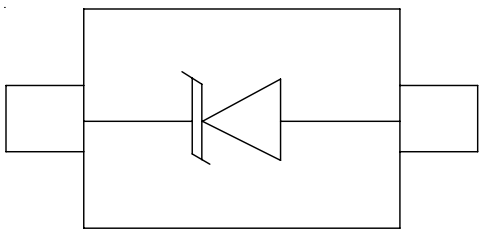
- Cellular Handsets & Accessories
- Cordless Phones
- Personal Digital Assistants (PDA's)
- Notebooks & Handhelds
- Portable Instrumentation
- Digital Cameras
- Peripherals
- MP3 Players

Dimensions



Maximum Dimensions (mm)

Schematic & PIN Configuration



SOD-523 (Top View)

Absolute Maximum Rating

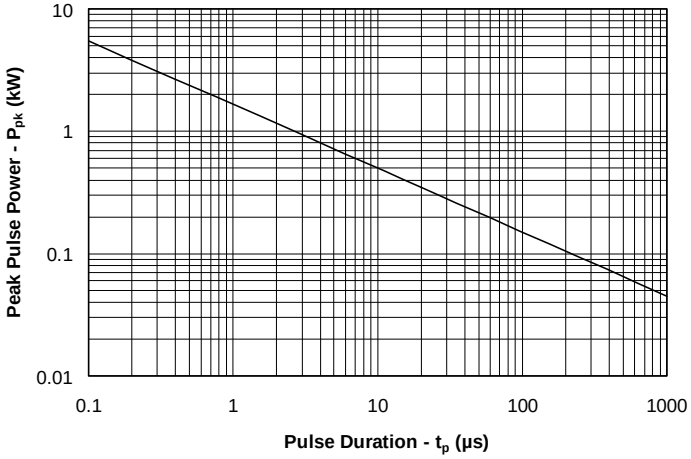
Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{pk}	240	Watts
Maximum Peak Pulse Current (tp = 8/20µs)	I_{pp}	16	Amps
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{PP}	+/- 20 +/- 15	kV
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C)

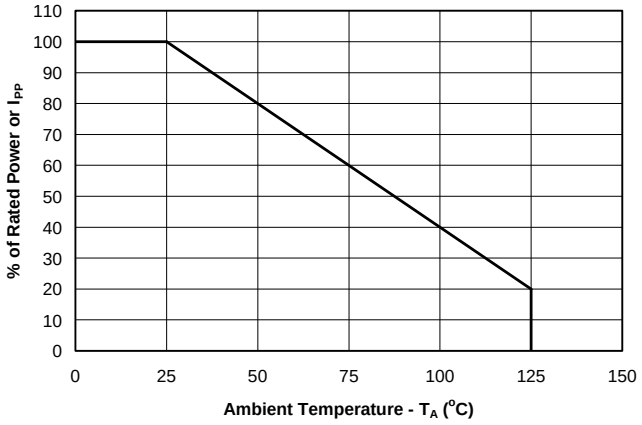
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	6			V
Reverse Leakage Current	I_R	V_{RWM} = 5V, T=25°C			5	µA
Forward Voltage	V_F	I_F = 10mA		0.80		V
Clamping Voltage	V_C	I_{PP} = 5A, t_p = 8/20µs			9.8	V
Clamping Voltage	V_C	I_{PP} = 16A, t_p = 8/20µs			12.5	V
Junction Capacitance	C_j	V_R = 0V, f = 1MHz			160	pF

Typical Characteristics

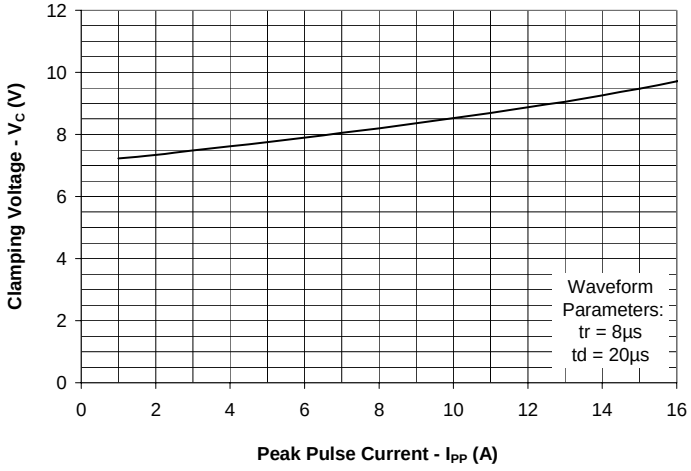
Non-Repetitive Peak Pulse Power vs. Pulse Time



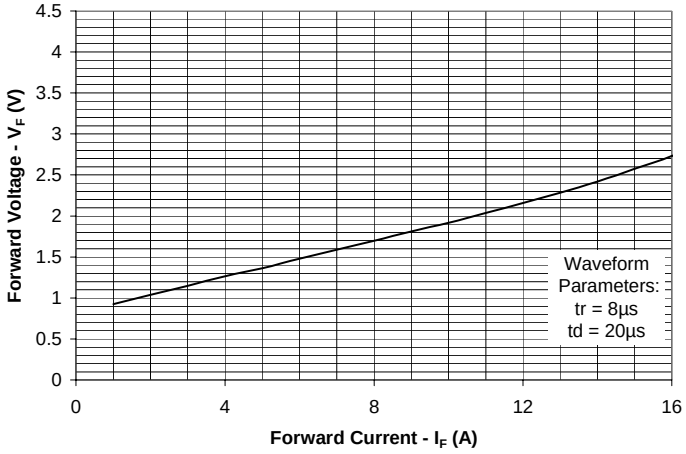
Power Derating Curve



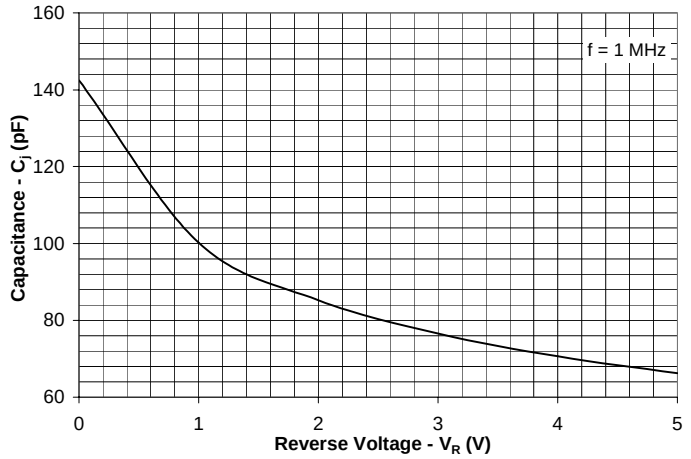
Clamping Voltage vs. Peak Pulse Current



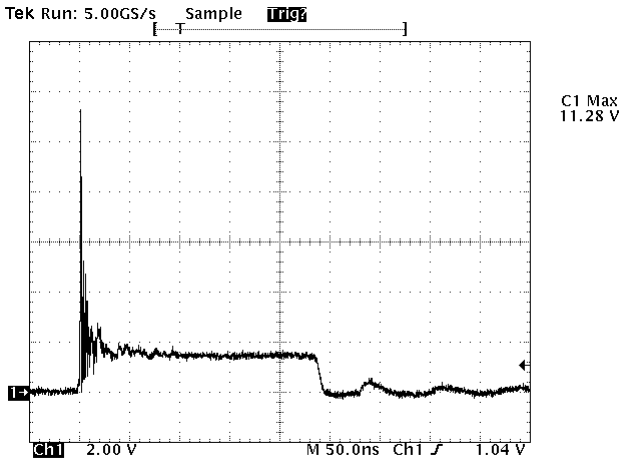
Forward Voltage vs. Forward Current



Junction Capacitance vs. Reverse Voltage



ESD Clamping (8kV Contact per IEC 61000-4-2)



Applications Information

Device Connection Options

These TVS diodes are designed to protect one data, I/O, or power supply line. The device is unidirectional and may be used on lines where the signal polarity is above ground. The cathode band should be placed towards the line that is to be protected.

Circuit Board Layout Recommendations for Suppression of ESD.

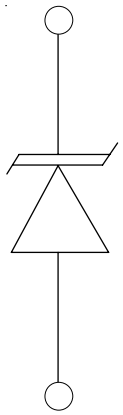
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

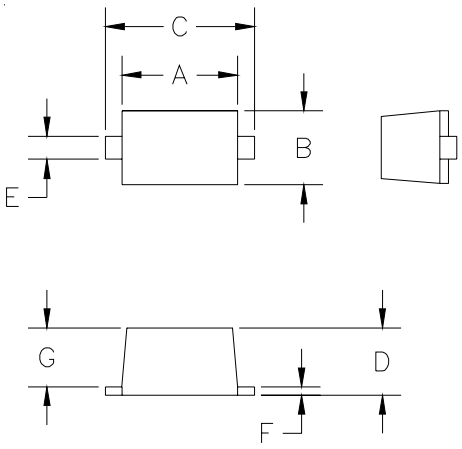
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

Circuit Diagram



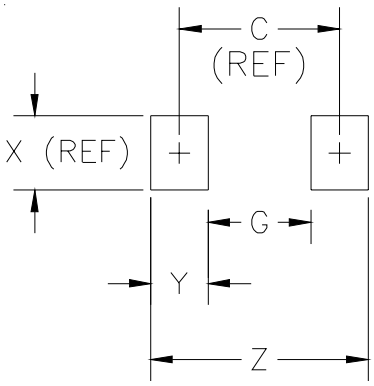
Outline Drawing



DIMENSIONS					
DIM	INCHES		MM [1]		NOTE
	MIN	MAX	MIN	MAX	
A	.043	.051	1.10	1.30	–
B	.028	.035	0.70	0.90	–
C	.059	.067	1.50	1.70	–
D	.020	.028	0.50	0.70	–
E	.010	.014	0.25	0.35	–
F	.004	.008	0.10	0.20	–
G	.020	.028	0.50	0.70	–

[1] CONTROLLING DIMENSION: MILLIMETERS

Land Pattern



DIMENSIONS					
DIM	INCHES		MM [1]		NOTE
	MIN	MAX	MIN	MAX	
C	–	.067	–	1.70	REF
G	–	.043	–	1.10	–
X	–	.031	–	0.80	REF
Y	–	.024	–	0.60	–
Z	–	.091	–	2.30	–

[1] CONTROLLING DIMENSION: MILLIMETERS