

# μClamp0511Z Ultra Small µClamp® 1 Line, 5V ESD Protection

### PROTECTION PRODUCTS

## Description

μClamp® TVS diodes are designed to protect sensitive electronics from damage or latch-up due to ESD. They features large cross-sectional area junctions for conducting high transient currents. These devices offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

The µClamp®0511Z is in a 2-pin SLP0603P2X3 package. It measures 0.6 x 0.3 mm with a nominal height of only 0.25mm. The leads are finished with lead-free NiAu. Each device will protect one line operating at 5 volts. It gives the designer the flexibility to protect single lines in applications where arrays are not practical. The combination of small size and high ESD surge capability makes them ideal for use in portable applications such as cellular phones, digital cameras, and tablet PC's.

#### **Features**

- High ESD withstand Voltage: +/-15kV (Air) and +/-8kV (contact) per IEC 61000-4-2
- Able to withstand over 1000 ESD strikes per IEC61000-4-2 Level 4
- Ultra-small 0201 package
- Protects one data line or power line
- Low leakage current: <10nA (V<sub>p</sub>=5V)
- Working voltage: +/-5V
- Low dynamic resistance: 0.64  $\Omega$  (typ)
- Solid-state silicon-avalanche technology

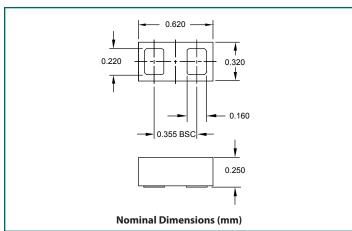
### **Mechanical Characteristics**

- SLP0603P2X3 package
- Pb-Free, Halogen Free, RoHS/WEEE compliant
- Nominal Dimensions: 0.6 x 0.3 x 0.25 mm
- Lead Finish: NiAu
- Marking: Marking code + dot matrix date code
- Packaging: Tape and Reel

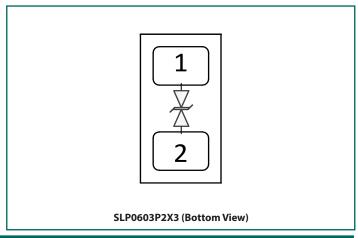
## **Applications**

- Cellular Handsets & Accessories
- Keypads, Side Keys, Audio Ports
- Portable Instrumentation
- **Digital Lines**
- **MP3 Players**

# **Package Dimension**



## **Schematic & Pin Configuration**



# **Absolute Maximum Rating**

Rating	Symbol	Value	Units
ESD per IEC 61000-4-2 (Air) <sup>(2)</sup> ESD per IEC 61000-4-2 (Contact) <sup>(2)</sup>	V <sub>ESD</sub>	±15 ±8	kV
Operating Temperature	T <sub>J</sub>	-55 to +125	∘C
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C

# **Electrical Characteristics (T=25°C unless otherwise specified)**

Parameter	Symbol	Conditions		Min.	Тур.	Max.	Units
Reverse Stand-Off Voltage	V <sub>RWM</sub>	Pin1 to 2 or 2 to 1				5	٧
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>t</sub> = 1mA, Pin 1 to 2 or 2 to 1		6	8.2	9.5	V
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 5V, Pin 1 to 2 or 2 to 1			3	50	nA
Clamping Voltage	V <sub>C</sub>	I <sub>pp</sub> =1A, tp = 8/20μs, Pin1 to 2 or 2 to 1				15	V
FCD Clause in a Valta ma?	2 4 0 2 4 0 0	h 0.2/100m	$I_{pp} = 4A$		11.2		
ESD Clamping Voltage <sup>2</sup> $V_c$ $t_p = 0.2/100$ ns	$t_{p} = 0.2/100$ ns	I <sub>PP</sub> = 16A		19.4		V	
Dynamic Resistance <sup>2,3</sup>	R <sub>DYN</sub>	$t_p = 0.2/100$ ns			0.64		Ω
Junction Capacitance	C <sub>J</sub>	$V_R = 0V, f = 1MHz$	T = 25°C		4	7	рF

#### Notes

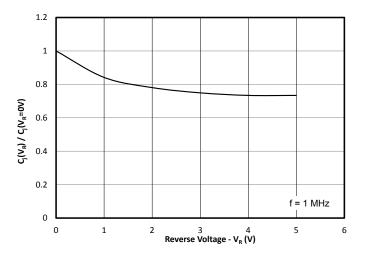
<sup>1)</sup> Measured with a 20dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to ESD ground plane.

<sup>2)</sup> Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns,  $I_{TLP}$  and  $V_{TLP}$  averaging window: t1 = 70ns to t2 = 90ns.

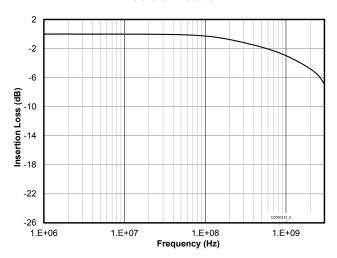
<sup>3)</sup> Dynamic resistance calculated from  $I_{\text{TLP}} = 4A$  to  $I_{\text{TLP}} = 16A$ 

# **Typical Characteristics**

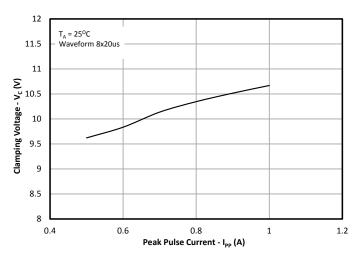
### Normalized Junction Capacitance vs. Reverse Voltage



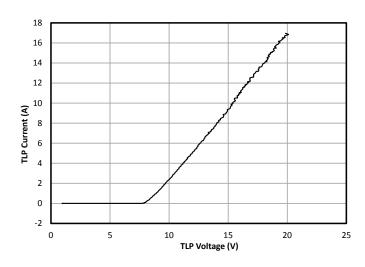
#### **Insertion Loss-S21**



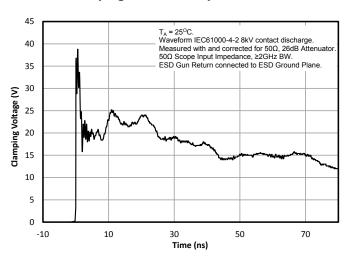
### Clamping Voltage vs. Peak Pulse Current (tp=8/20 µs)



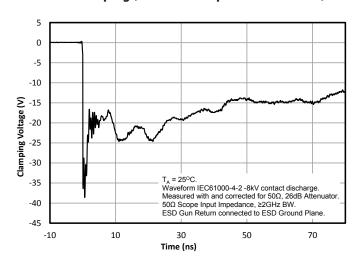
**TLP Characteristic (Positive Pulse)** 



### ESD Clamping (8kV Contact per IEC 61000-4-2)



ESD Clamping (-8kV Contact per IEC 61000-4-2)



## **Application Information**

### **Assembly Guidelines**

The small size of this device means that some care must be taken during the mounting process to insure reliable-solder joints. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing-parameters will require some experimentation to get the desired solder application. Semtech's recommendedmounting pattern is based on the following design guidelines:

#### **Land Pattern**

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

#### **Solder Stencil**

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. An area

ratio of 0.70 – 0.75 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

Area Ratio = (L \* W) / (2 \* (L + W) \* T)

Where:

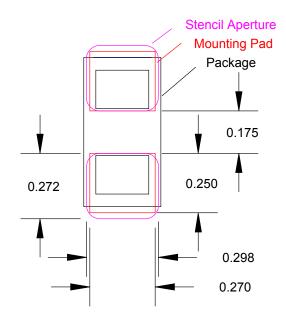
L = Aperture Length

W = Aperture Width

T = Stencil Thickness

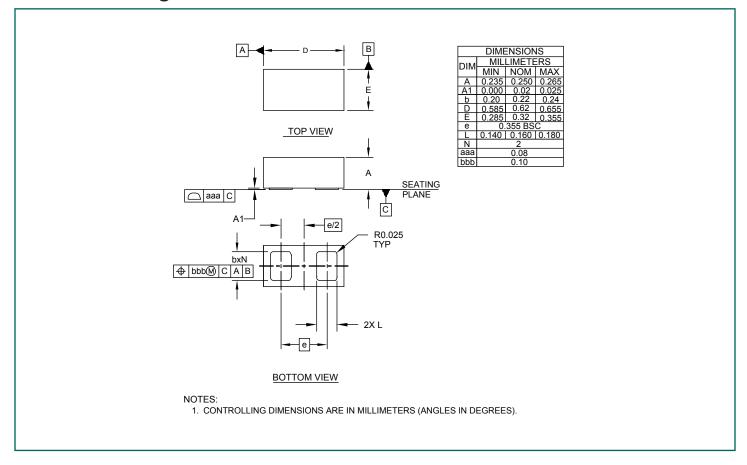
Semtech recommends a stencil thickness of 0.100mm for this device. The stencil should be laser cut with electropolishedfinish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. For small pitch components, Semtech recommends a square aperture with rounded corners for consistent solder release. Due to the small aperture size, a solder paste with Type 4 or smaller particles are recommended.

### **Recommended Mounting Pattern**

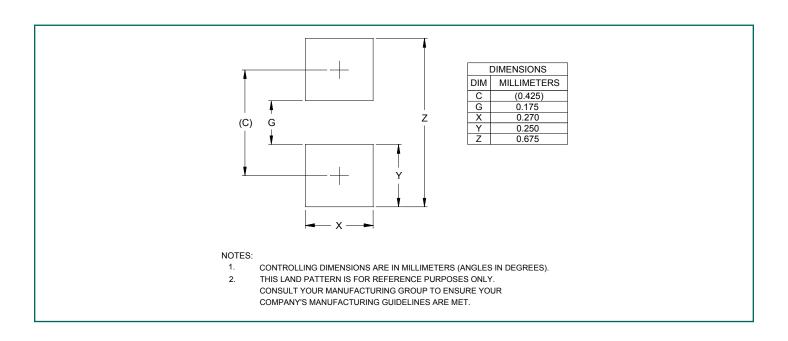


Assembly Parameter	Recommendation		
Solder Stencil Design	Laser cut, Electro-polished		
Aperture shape	Rectangular with rounded corners		
Solder Stencil Thickness	0.100 mm (0.004")		
Solder Paste Type	Type 4 size sphere or smaller		
Solder Reflow Profile	Per JEDEC J-STD-020		
PCB Solder Pad Design	Non-Solder mask defined		
PCB Pad Finish	OSP OR NiAu		

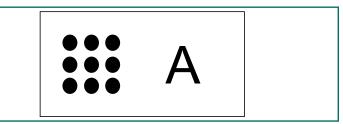
# **Outline Drawing - SLP0603P2X3**



## Land Pattern - SLP0603P2X3

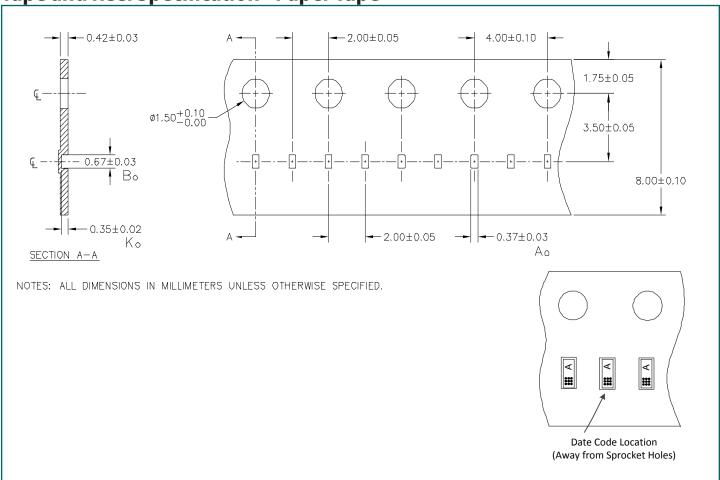


# **Marking Code**

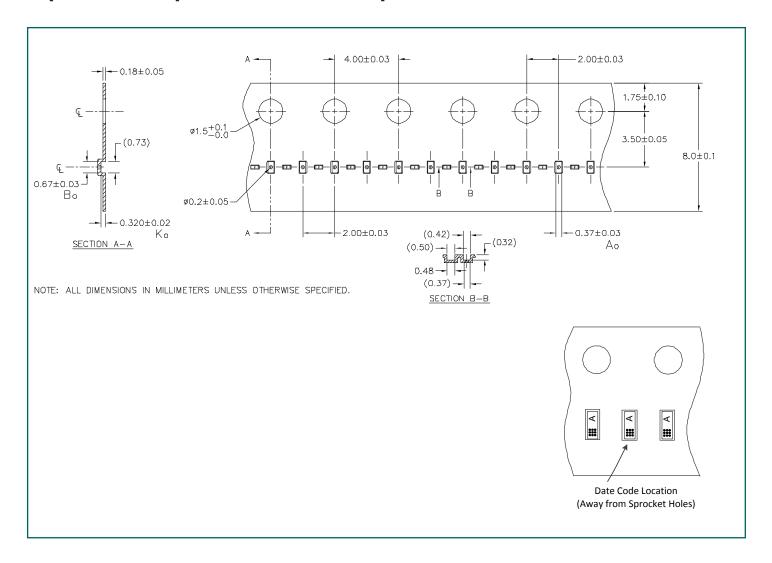


Note: Dots represent date code matrix

**Tape and Reel Specification - Paper Tape** 



# **Tape and Reel Specification-Plastic Tape**



**Ordering Information** 

Part Number	Qty per Reel	Carrier Tape	Reel Size
μClamp0511Z.TFT	15,000	Paper	7"
μClamp0511Z.TNT	10,000	Plastic	7"