uClamp3304A
µClamp™
4-Line ESD protection Array

PROTECTION PRODUCTS - MicroClamp™

Description

The µClamp™ series of TVS arrays are designed to protect sensitive electronics from damage or latch-up due to ESD. They are designed for use in applications where board space is at a premium. Each device requires less than 2.9mm^2 of PCB area and will protect up to four lines. They are unidirectional devices and may be used on lines with positive signal polarities.

The µclamp™3304A is constructed using Semtech's proprietary EPD process technology. The EPD process provides low standoff voltages with significant reductions in leakage currents and capacitance over silicon-avalanche diode processes. They feature a true operating voltage of 3.3 volts for superior protection when compared to traditional pn junction devices.

These devices may be used to meet the immunity requirements of IEC 61000-4-2, level 4. They offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation. The small SC89 package makes them ideal for use in portable electronics such as cell phones, PDAs, notebook computers, and digital cameras.

Features

- Transient protection for data lines to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
- Protects four unidirectional I/O lines
- Ultra-small SC-89 package (**1.7 x 1.7 x 0.6mm**) requires less than 2.9mm^2 of PCB area
- Working voltage: 3.3V
- Low leakage current
- Low operating and clamping voltages
- Solid-state silicon-avalanche technology

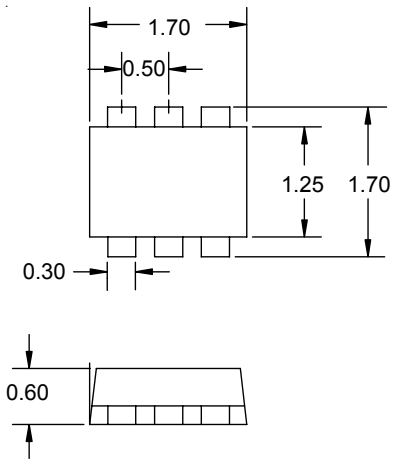
Mechanical Characteristics

- SC-89 (SOT-666) package
- Molding compound flammability rating: UL 94V-0
- Marking: Marking Code
- Lead Finish: Matte Tin
- RoHS Compliant
- Weight: 2.9mg (typical)
- Packaging: Tape and Reel per EIA 481

Applications

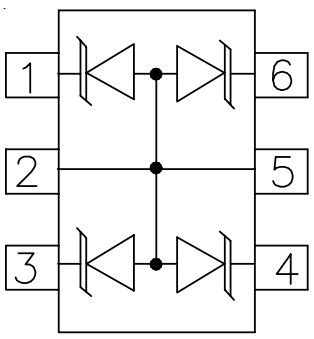
- Cellular Handsets and Accessories
- Cordless Phones
- Notebooks and Handhelds
- Portable Instrumentation
- Digital Cameras
- Peripherals
- MP3 Players

Dimensions



Maximum Dimensions (mm)

Schematic & PIN Configuration



SC-89 (Top View)

Absolute Maximum Rating

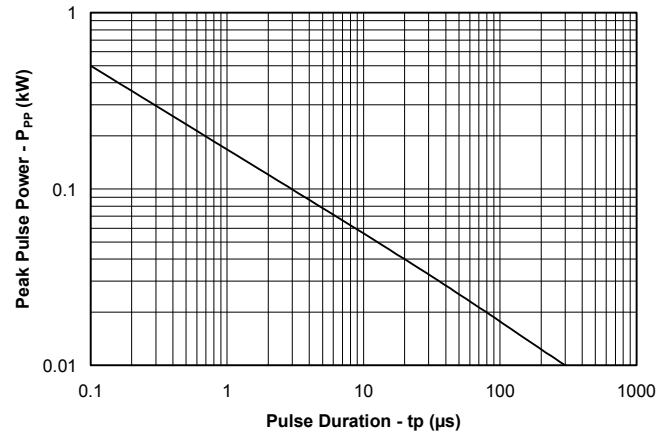
Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P_{pk}	40	Watts
Maximum Peak Pulse Current (tp = 8/20μs)	I_{pp}	5	Amps
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{PP}	+/- 20 +/- 15	kV
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C)

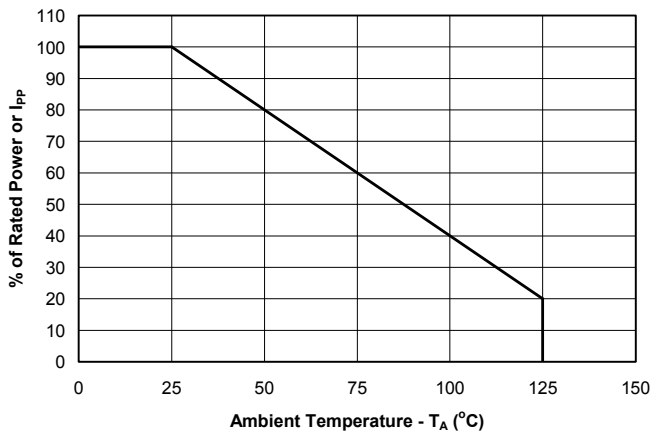
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				3.3	V
Punch-Through Voltage	V_{PT}	I_{PT} = 2μA	3.5			V
Snap-Back Voltage	V_{SB}	I_{SB} = 50mA	2.8			V
Reverse Leakage Current	I_R	V_{RWM} = 3.3V		0.05	0.5	μA
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20μs			5.5	V
Clamping Voltage	V_C	I_{PP} = 5A, tp = 8/20μs			8.0	V
Reverse Clamping Voltage	V_{CR}	I_{PP} = 1A, tp = 8/20μs			2.4	V
Junction Capacitance	C_j	I/O pin to Gnd V_R = 0V, f = 1MHz		22	30	pF
		I/O pin to Gnd V_R = 3.3V, f = 1MHz		14		pF

Typical Characteristics

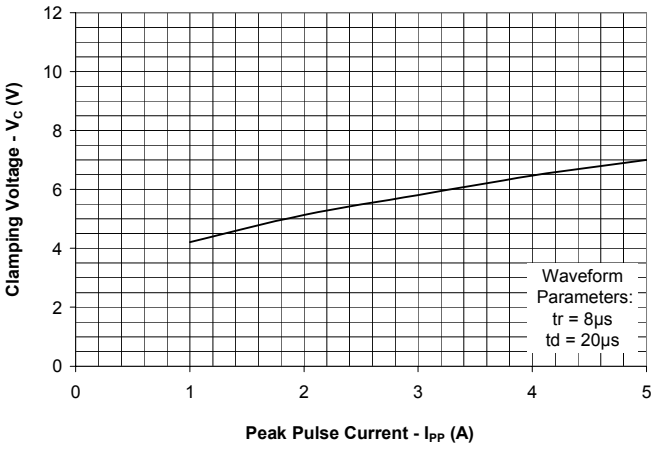
Non-Repetitive Peak Pulse Power vs. Pulse Time



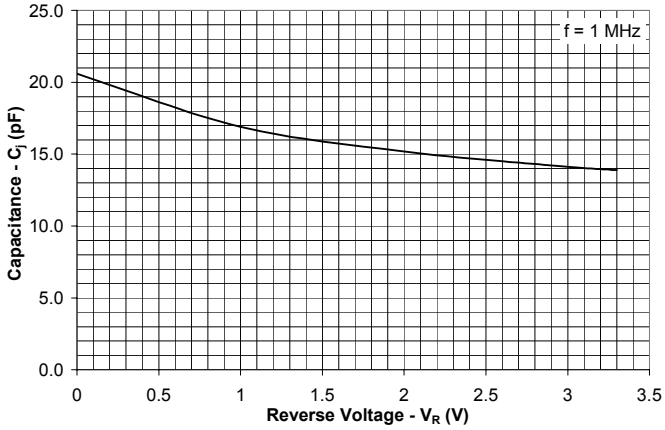
Power Derating Curve



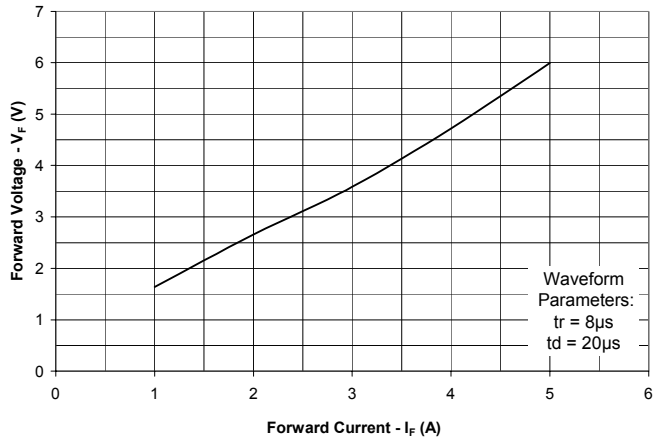
Clamping Voltage vs. Peak Pulse Current



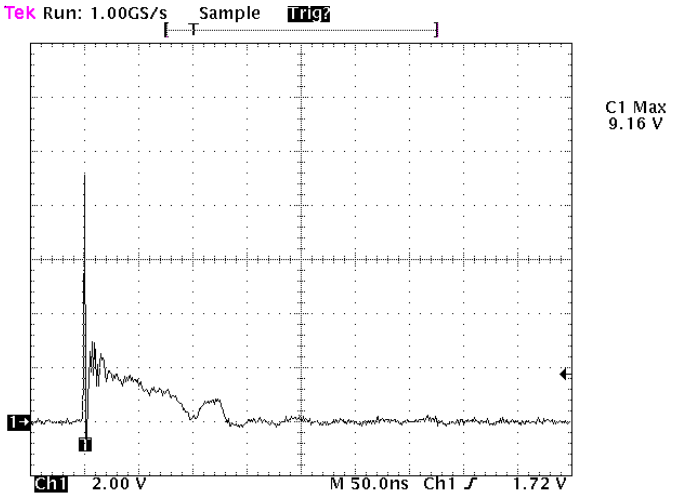
Junction Capacitance vs. Reverse Voltage



Forward Voltage vs Forward Current



ESD Clamping (8kV Contact per IEC 61000-4-2)



Applications Information

Device Connection for Protection of Four Data Lines

These devices are designed to protect up to four unidirectional data lines. The device is connected as follows:

1. Unidirectional protection of four I/O lines is achieved by connecting pins 1, 3, 4, and 6 to the data lines. Pins 2 and 5 are connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.

Circuit Board Layout Recommendations for Suppression of ESD.

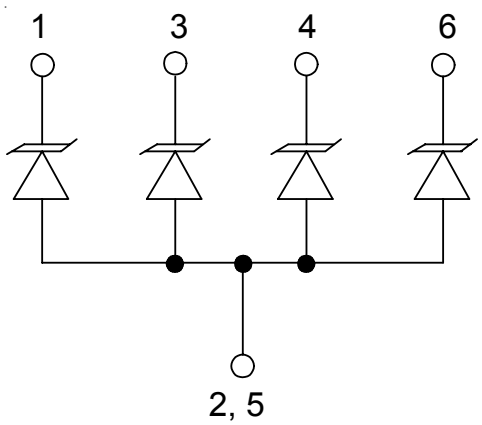
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

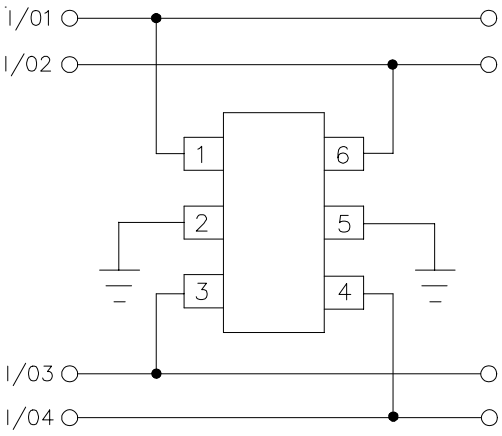
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

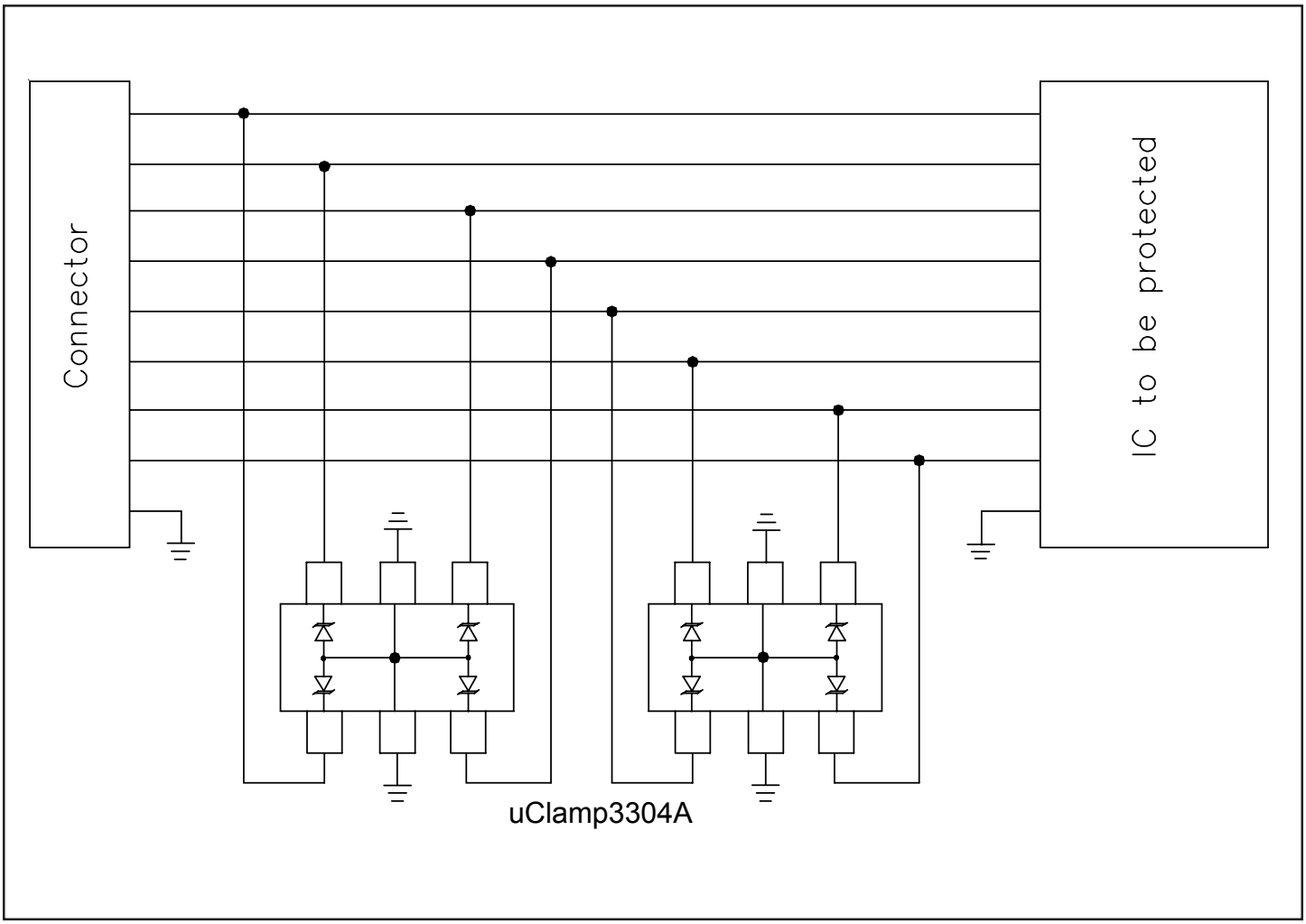
Circuit Diagram



Protection of Four Unidirectional Lines



Typical Applications



Applications Information - Spice Model

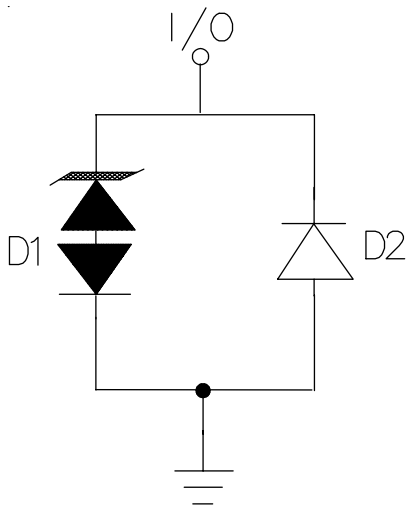
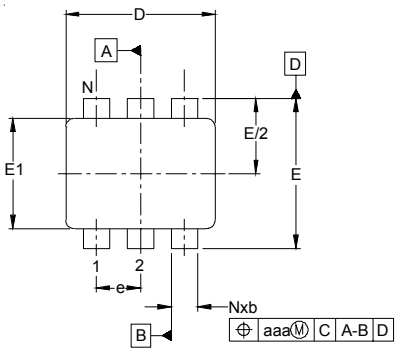


Figure 1 - µClamp3304A Spice Model

Table 1 - µClamp3304A Spice Parameters

Parameter	Unit	D1 (TVS)	D2 (LCRD)
IS	Amp	1.00E-20	1.00E-20
BV	Volt	3.47	8
VJ	Volt	14	0.70
RS	Ohm	0.737	0.795
IBV	Amp	1.0E-3	1.0E-3
CJO	Farad	14.53E-12	6E-12
TT	sec	2.541E-9	2.541E-9
M	--	0.152	0.152
N	--	1.1	1.1
EG	eV	1.11	1.11

Outline Drawing - SC-89 (SOT-666)

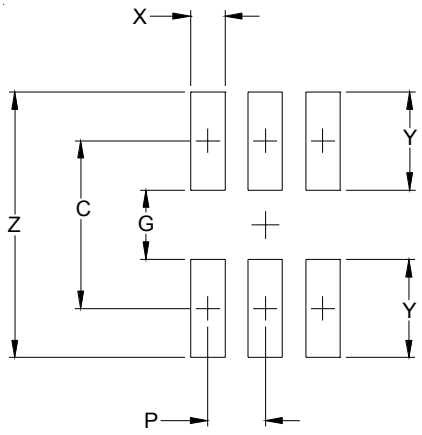


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.019	-	.024	0.50	-	0.60
b	.005	-	.012	0.15	-	0.30
c	.003	-	.007	0.10	-	0.18
D	.059	.063	.067	1.50	1.60	1.70
E	.061	.063	.067	1.55	1.60	1.70
E1	.043	.047	.049	1.10	1.20	1.25
e	.020 BSC			0.50 BSC		
L	.003	.008	.012	0.10	0.20	0.30
L1	.003	.006	.008	0.10	0.15	0.20
N	6			6		
aaa	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Land Pattern - SC-89 (SOT-666)



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.057)	(1.45)
P	.020	0.50
G	.024	0.60
X	.012	0.30
Y	.033	0.85
Z	.090	2.30

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.