uClamp3312T
Low Voltage µClamp® for Gigabit Ethernet

Description

The µClamp®3312T TVS diode is specifically designed to meet the performance requirements of Gigabit Ethernet interfaces. They are designed to protect sensitive PHY chips from damage or upset due to electrostatic discharge (ESD), lightning, electrical fast transients (EFT), and cable discharge events (CDE).

The µClamp3312T is constructed using Semtech's low voltage EPD process technology. The EPD process provides low operating voltages with significant reductions in leakage current and capacitance over silicon-avalanche diode processes. The device features low variation in capacitance over bias for stable operation on GbE lines. This means the µClamp3312T will introduce zero traffic frame errors on GbE interfaces up to a PHY temperature of 120ºC (100M Cat 5/5e Cable). The µClamp3312T also features high surge capability and is designed to be placed between the magnetics and the PHY chip. In this configuration, the device can withstand intra-building lightning surges per Telcordia GR-1089.

The µClamp3312T is in a 8-pin SLP2010N8T package. It measures 2.0 x 1.0 x 0.4mm. The leads are spaced at a pitch of 0.5mm and are finished with lead-free NiPdAu. Each device will protect two line pairs operating at 3.3 volts. It gives the designer the flexibility to protect multiple lines in applications where space is at a premium. The small size and easy layout of the uClamp3312T make it ideal for use in RJ-45 connectors with integrated magnetics.

Features

- High ESD withstand Voltage: **+/-30kV** (Contact/Air) per **IEC 61000-4-2**
- Able to withstand over 1000 ESD strikes per IEC 61000-4-2 Level 4
- Flow-through design simplifies layout
- Protects two line pairs
- Low reverse current: 10nA typical (VR=3.3V)
- Low variation in capacitance vs. bias voltage: **1.3pF** Typical (VR = 0 to 3.3V)
- Working voltage: 3.3V
- Solid-state silicon-avalanche technology

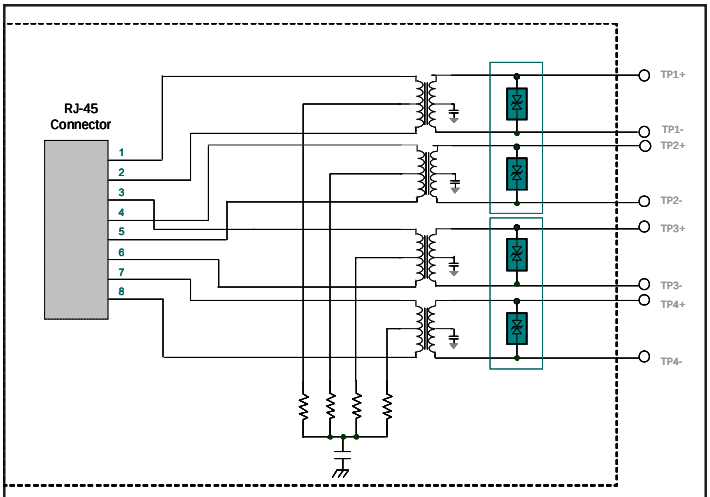
Mechanical Characteristics

- SLP2010N8T package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Nominal Dimensions: 2.0 x 1.0 x 0.4 mm
- Lead Finish: NiPdAu
- Molding compound flammability rating: UL 94V-0
- Marking: Marking code
- Packaging: Tape and Reel

Applications

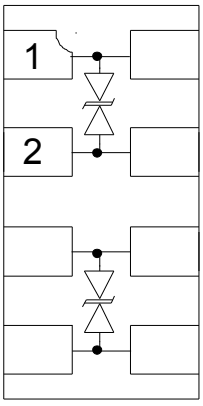
- 10/100/1000 Ethernet
- Integrated magnetics/RJ-45 connectors
- LAN/WAN Equipment
- Security Cameras
- Industrial Controls
- Notebooks & Desktop Computers

Typical Application



GBE Integrated Magnetics Module

Schematic & PIN Configuration



SLP2010N8T

Absolute Maximum Rating

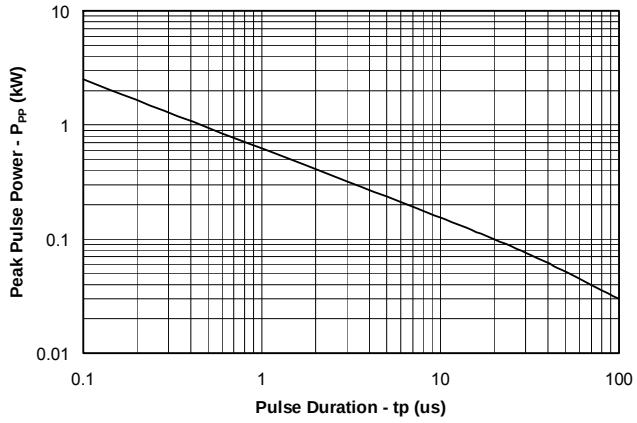
Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{pk}	100	Watts
Maximum Peak Pulse Current (tp = 8/20µs)	I_{pp}	10	Amps
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	+/- 30 +/- 30	kV
Operating Temperature	T_J	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C)

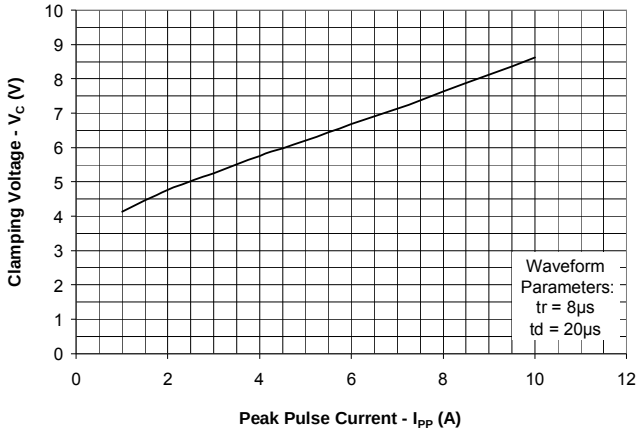
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				3.3	V
Punch-Through Voltage	V_{PT}	I_{PT} = 2µA	3.5	3.8	4.3	V
Snap-Back Voltage	V_{SB}	I_{SB} = 50mA	2.8			V
Reverse Leakage Current	I_R	V_{RWM} = 3.3V		0.01	0.05	µA
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20µs			5.6	V
Clamping Voltage	V_C	I_{PP} = 10A, tp = 8/20µs			11	V
Variation in capacitance with reverse bias [1]		Pins 1, 8 to 2, 7 and pins 3, 6 to 4, 5 VR = 0 to 2.5V f = 1MHz Pins 1, 8 to 2, 7 and pins 3, 6 to 4, 5 VR = 2.5V, f = 1MHz		1.3		pF
Junction Capacitance	C_j	I/O pin to Gnd V_R = 0V, f = 1MHz		4.5	6	pF

Notes:
1) This parameter guaranteed by design and characterization and is not production tested

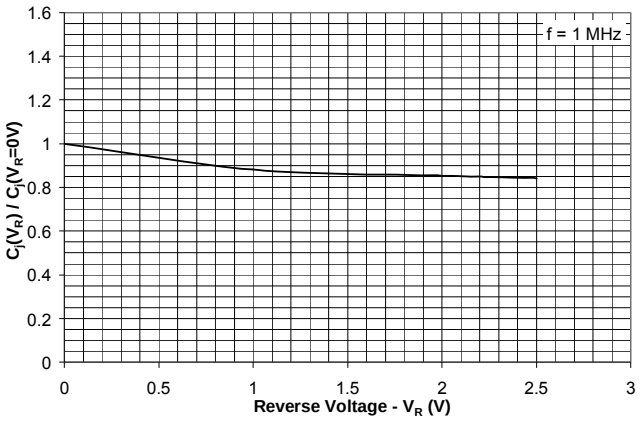
Non-Repetitive Peak Pulse Power vs. Pulse Time



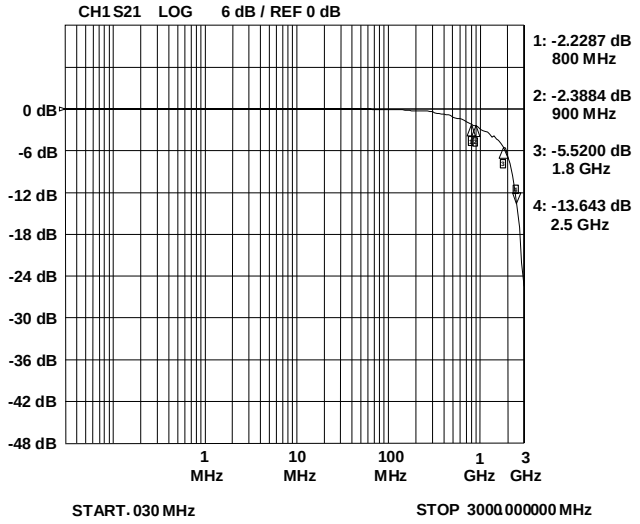
Clamping Voltage vs. Peak Pulse Current



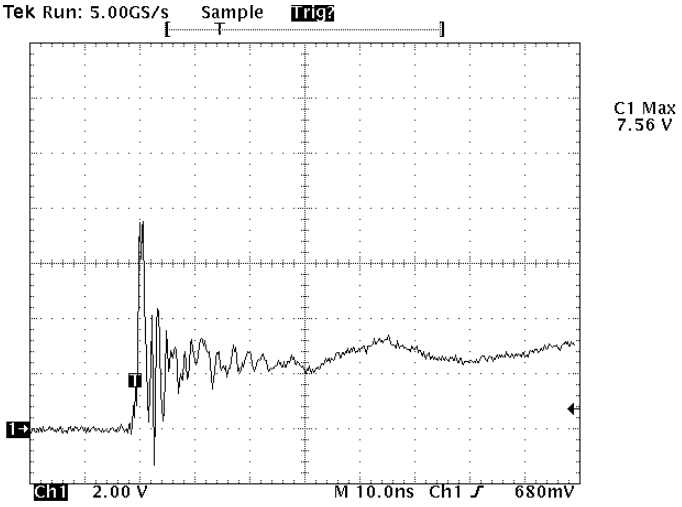
Normalized Junction Capacitance vs. Reverse Voltage



Typical Insertion Loss (S21)

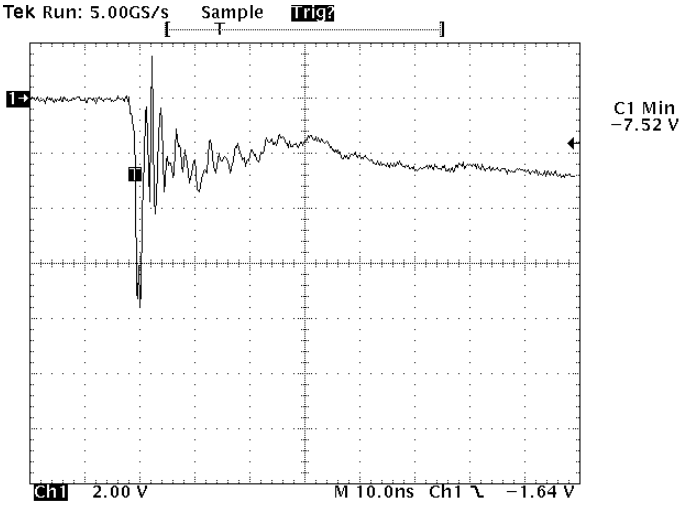


ESD Clamping (Pin 1 to 2 and 2 to 1) (8kV Contact per IEC 61000-4-2)



Note: Data is taken with a 10x attenuator

ESD Clamping (Pin 1 to 2 and 2 to 1) (-8kV Contact per IEC 61000-4-2)



Note: Data is taken with a 10x attenuator

Applications Information

Gigabit Ethernet Protection Solutions

Ethernet systems with connections external to the building are subject to high-level transient threats. This type of equipment may even be required to meet the surge immunity requirements of Telcordia GR-1089. Reliable protection of the Ethernet transceiver requires a device that can absorb the expected transient energy, clamp the incoming surge to a safe level, and yet remain transparent to the system under normal operation. The uClamp3312T has been designed to meet these demanding requirements. Typical IEEE 802.3 template test results for a GbE circuit with uClamp3312T are shown in Figure 2.

Transient Protection

When designing Ethernet protection, the entire system must be considered. An Ethernet port includes interface magnetics in the form of transformers and common mode chokes. Transformers and chokes can be discrete components, but integrated solutions that include the RJ-45 connector, resistors, capacitors, and protection are also available. In either case, the transformer will provide a high level of common mode isolation to external voltages, but no protection for metallic (line-to-line) surges. During a metallic transient event, current will flow into one line, through the transformer and back to the source. As the current flows, it charges the windings of the transformer on the line side. Once the surge is removed, the windings on the line side will stop charging and will transfer its stored energy to the IC side where the PHY IC is located. The magnitude and duration of the surge is attenuated by the inductance of the magnetics. The amount of attenuation will vary by vendor and configuration of the magnetics. It is this transferred energy that must be clamped by the protection circuitry.

A typical protection scheme which utilizes the uClamp3312T is shown in Figure 1. One device is placed across two line pairs and is located on the PHY side of the transformer as close to the magnetics as possible. This is done to minimize parasitic inductance and improve clamping performance. In this design, the isolation voltage of the transformer is relied upon to suppress common mode lightning surges. High voltage capacitors and resistors are commonly utilized from the center tap to ground to aid in transient protection. Metallic surges will be transferred in some form to the PHY side and clamped by the uClamp3312T. The uClamp3312T will turn on when the voltage across it exceeds the punch-through voltage of the device. Low voltage turn on is important since many PHY chips have integrated ESD protection structures. These structures are for protection of the device during manufacture and are not designed to handle large amounts of energy. Should they turn on before the external protection, they can be damaged resulting in failure of the PHY chip.

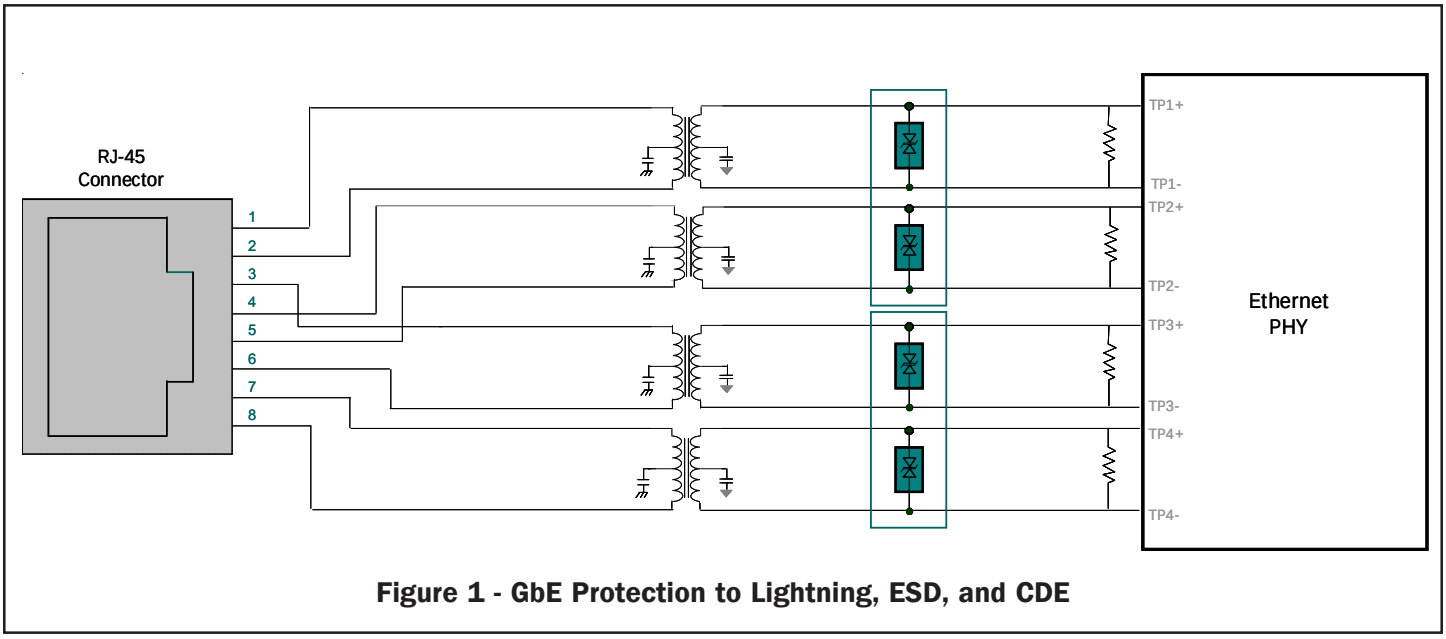


Figure 1 - GbE Protection to Lightning, ESD, and CDE

Point A

Point B

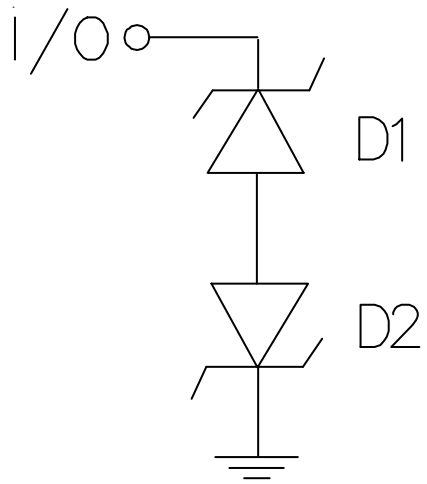
Point C

Point D

Point F

Point H

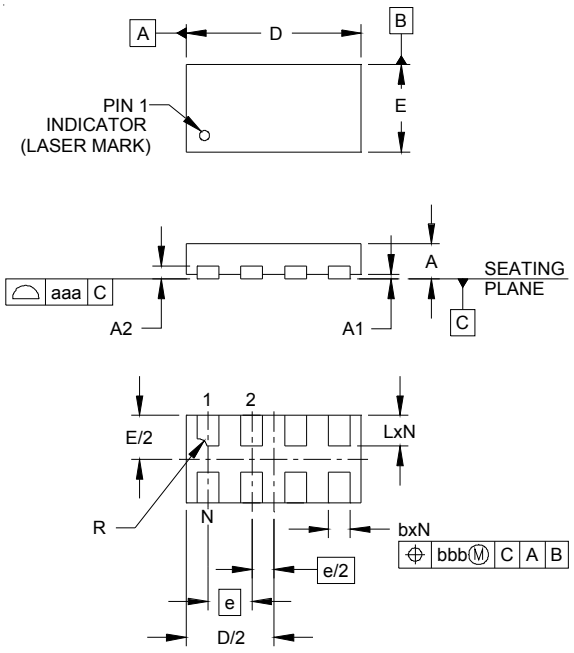
Figure 2 - Typical IEEE 802.3 Template Test Results (With uClamp3312T)



Spice Model

uClamp3312T Spice Parameters			
Parameter	**Unit**	**D1 (TVS)**	**D2 (TVS)**
IS	Amp	1E-20	1E-20
BV	Volt	2.8	2.8
VJ	Volt	0.7	0.7
RS	Ohm	0.2	0.2
IBV	Amp	1E-3	1E-3
CJO	Farad	10E-12	1E-12
TT	sec	2.541E-9	2.541E-9
M	--	0.05	0.05
N	--	1.1	1.1
EG	eV	1.11	1.11

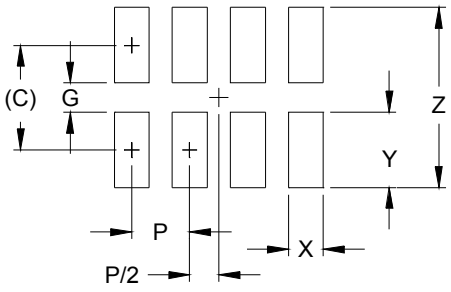
Outline Drawing - SLP2010N8T



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.37	0.40	0.43
A1	0.00	0.02	0.05
A2		(0.13)	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
E	0.90	1.00	1.10
e		0.50 BSC	
L	0.30	0.35	0.40
R	0.05	0.10	0.15
N		8	
aaa		0.08	
bbb		0.10	

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Land Pattern - SLP2010N8T



DIMENSIONS	
DIM	MILLIMETERS
C	(0.90)
G	0.25
P	0.50
X	0.30
Y	0.65
Z	1.55

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.